UNIVERSITI SAINS MALAYSIA

Second Semester Examination
Academic Session 2007/2008

April 2008

EEE 510 – ANALOG CIRCUIT DESIGN

Duration: 3 hours

Please check that this examination paper consists of SIX pages of printed material before you begin the examination.

This paper contains SIX questions.

Instructions: Answer **FIVE (5)** questions.

Answer to any question must start on a new page.

Distribution of marks for each question is given accordingly

All questions must be answered in English.

...2/-

1. Given a MOS transistor in a configuration as shown in Figure 1. Draw the small signal model of the transistor. Assume $V_{sb} = V_{ds} = 0$. g_{mb}, r_o, C_{sb} and C_{db} are ignored. Prove that

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gb} + C_{gd}}$$

Compare the above expression with the unity gain frequency expression for the BJT.

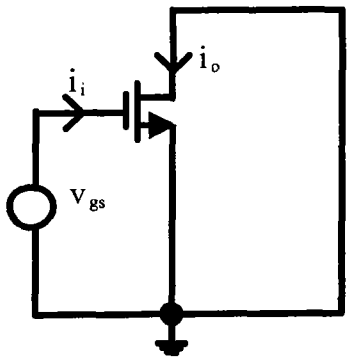

Figure 1

(20 marks)

2. Determine the voltage gain of the transistor amplifier circuit shown in Figure 2. Assume $\beta_{ac} = \beta_{dc} = 100$. $V_T = 26\,mV$ and $V_{BE} = 0.7\,V$. Neglect all parasitic elements in the small-signal equivalent circuit of the BJT in this amplifier circuit. Neglect the base charging capacitance and the collector-base resistances. Assume that r_o is very large.

(20 marks)

...3/-

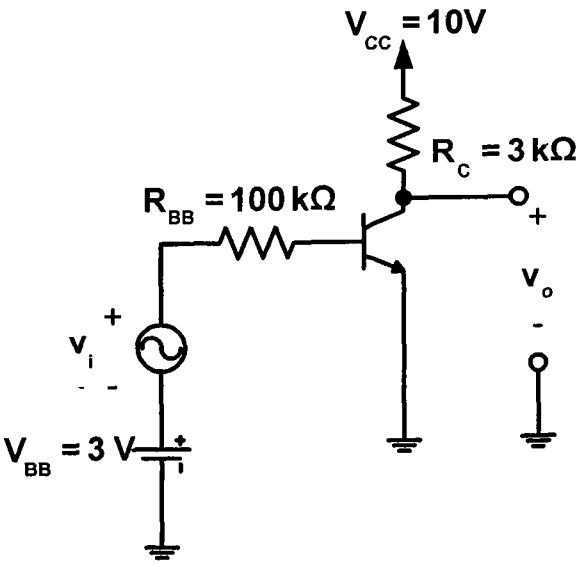

Figure 2

3. Consider the BiCMOS amplifier shown in Figure 3. The BJT has $V_{BE} = 0.7\,V$ and $\beta = 200$. The NMOS transistor has a threshold voltage $V_t = 1\,V$ and $k'\,W/L = 2\,mA/V^2$. Consider the DC bias circuit for this amplifier. Neglect the base current of Q_2 in determining the current in Q_1. Find the DC bias currents in Q_1 and Q_2, and show that they are approximately $100\,\mu A$ and 1 mA respectively.

...4/-

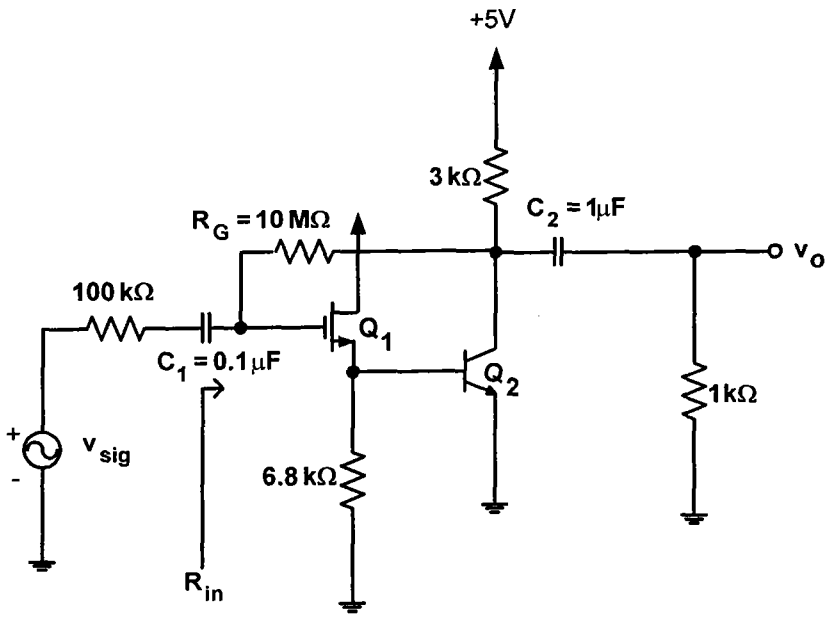

Figure 3

(20 marks)

4. Figure 4 shows a non-inverting configuration of an operational amplifier.

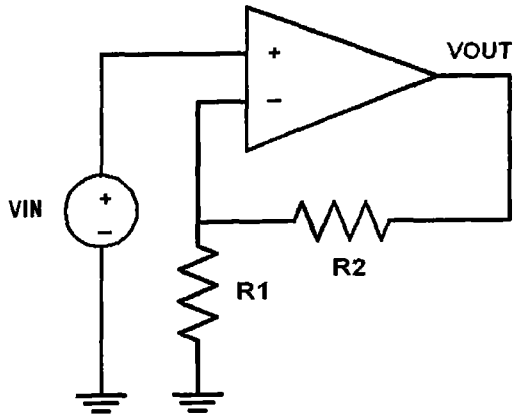

Figure 4

...5/-

(a) Identify the type of feedback in this circuit. (5 marks)

(b) Find the expression of the loop gain. (5 marks)

(c) Find the expression of the closed loop gain. (10 marks)

5. Circuit in Figure 5 has a GBW of 200 MHz. If VDD is 2.5 V and $\mu_n C_{OX} = 100\mu\frac{A}{V^2}$, $\mu_p C_{OX} = 50\mu\frac{A}{V^2}$, $V_{thn} = |V_{thp}| = 0.5V$ and CL is 1 pF

Find :

(a) gm. (10 marks)

(b) W/L of MN1 (10 marks)

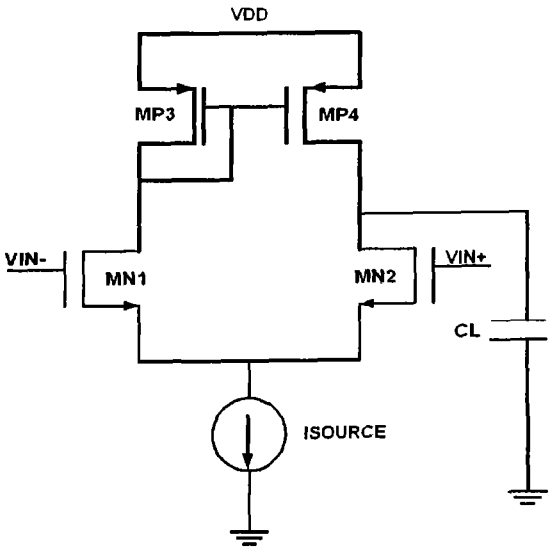

Figure 5

6. Based on Figure 6, draw IX versus VIN (20 marks)

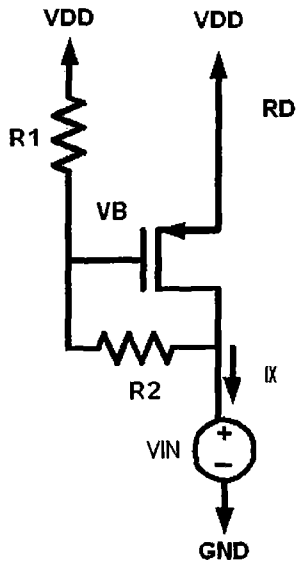

Figure 6

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