CARBON DOPED SILICON DIOXIDE LOW K DIELECTRIC MATERIAL

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CARBON DOPED SILICON DIOXIDE LOW K DIELECTRIC MATERIAL

by

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ABSTRACT

The objective of this research is to study the effectiveness of doping carbon content compounds onto SiO_2 to form a low k dielectric material. This carbon doped dielectric material, which serves as an important interlayer dielectric in modern microelectronic devices, is expected to have k constant as low as 2.4.

This study is divided into 3 parts. Firstly, a new approach is introduced to use the methanol as a source of dopant on SiO_2 to form low k dielectric material. Secondly, different alkyl oxygenated alcohols (ethanol & propanol compared to methanol) are used as the dopant to compare the effectiveness of the doping. Thirdly, carbon monoxide is used to dope. A discovery is made in growing a dielectric material where the dielectric constant of a material can be controlled by using carbon monoxide. A RC simulation study using an inverter is carried out to determine the delay time improved by using the lower dielectric constant material.

In the first and second part, all the silicon samples are dip in the alkyl liquids as mention respectively before sending for CVD. SEM-EDS results show there is carbon in the doped SiO_2 and the FTIR scan result confirms that $Si-CH_3$ bond is formed. The methyl doped SiO_2 has dielectric constant as low as 3.11 compared to an untreated SiO_2 with dielectric constant value of 3.90. Similarly, the ethyl and proply doped SiO_2 provide even lower dielectric constant value of 2.85 and 2.76 respectively.

The dielectric constant of carbon monoxide doped SiO_2 found could be controlled through the amount of carbon monoxide (CO) being exposed onto the sample. The result shows the forming of carbon silicon bond and the dielectric constant can decrease to 2.60 as the carbon content increased from 0 to 9.2%, which is equivalent to 1.5hrs of CO exposure. Similarly, the simulation result show that the lower the dielectric constant, the shorter the delay time. It can improve as much as 17% with dielectric constant decrease to 2.60.

These results are promising and this indicates that there is great potential of achieving an even lower dielectric constant for a carbon doped SiO_2.

SILIKON DIOKSIDA TERDOP KARBON BAHAN DIELEKTRIK K RENDAH

ABSTRAK

Objektif kajian ini adalah untuk mengkaji keberkesanan mendopkan sebatian karbon keatas SiO_2 untuk menghasilkan bahan dielektrik k rendah. Bahan dielektrik ini yang didopkan dengan karbon diramalkan mempunyai nilai malar k serendah 2.4 dimana ini merupakan sifat lapisan antara yang sangat penting bagi dielektrik pada litar mikroelektrik.

Hasil kerja ini dibahagikan kepada tiga bahagian. Pertama, satu pendekatan baru diperkenalkan iaitu dengan menggunakan metanol sebagai sumber untuk mendopkan karbon ke dalam SiO_2 untuk menghasilkan material dielektrik yang mempunyai nilai k yang rendah. Kedua, pelbagai jenis alkohol teroksigen alkyl (etanol, propanol) digunakan untuk sebagai pendop untuk melihat keberkesanan process pendopan. Ketiga, karbon monoksida digunakan untuk mendop. Suatu kaedah penumbuhan bahan dielektrik telah diperolehi dimana pemalar dielektrik bahan dapat dikawal dengan menggunakan gas karbon monoksida. Satu kajian simulasi RC menggunakan penyongsang dijalankan bagi menentukan penambah baik masa tangguh dengan menggunakan bahan dielektrik yang lebih rendah.

Di bahagian pertama dan kedua, semua sampel silikon direndam di dalam cecair alkyl sebagaumana yang telah dinyatakan sebelum di hantar ke CVD. Keputusan SEM-EDS menunjukkan bahawa wujudnya karbon dalam SiO_2 terdop manakala skan FTIR telah membuktikan ikatan Si-CH_3 telah dibentukkan. SiO_2 terdop metil mempunyai

nilai pemalar dielektrik serendah 3.11 berbandingkan SiO_2 yang asalnya mempunyai nilai pemalar dielektrik 3.90. Begitu juga, SiO_2 terdop etil dan propil memberi nilai pemalar dielektrik lebih rendah 2.85 dan 2.76 masing-masing.

Nilai pemalar dielektrik bagi SiO_2 yang terdop karbon monoksida boleh dikawal melalui kawalan kandungan karbon monoksida (CO) yang telah didedahkan kepada sampel SiO_2. Keputusan yang didapati telah menunjukkan bahawa ikatan silikon karbon terbentuk dan ia telah menurunkan nilai pemalar dielektrik kepada 2.60 apabila kandungan karbon bertambah dari 0% kepada 9.2% yang bersepadan dengan pendedahan CO selama 1.5 jam. Seperti itu juga, kajian simulasi menunjukkan bahawa lagi rendah nilai pemalar dielektrik maka lagi pendek nilai masa tunda. Ia boleh jadi sebaik 17% sekiranya nilai pemalar dielektrik menyusut ke nilai 2.6.

Keputusan ini amat merangsangkan dan ini menunjukkan bahawa ada kemungkinan besar untuk mencapai pemalar dielektrik yang lebih rendah bagi SiO_2 terdop karbon.

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION TO LOW K DIELECTRIC/INTERCONNECT TECHNOLOGY

The semiconductor industry is entering a new millennium where scientists and engineers are continuing to search for the ideal dielectric material for future chip fabrication. The metal widths and line spacings are now getting smaller. The main barriers for chips to operate at higher speeds will be the delay within the metal interconnects and the increases in capacitance between adjacent conducting lines that can potentially lead to cross-talk between the lines. (Sermon et al, 1999)

Achieving lower dielectric constants of materials will be the goal driven by the semiconductor industries to solve the delay problem which can be done by introducing new interconnect technology that exploits copper instead of standard metal components such as aluminum and tungsten and the capacitance problem will be addressed by reducing the dielectric constant of the inter metal dielectric materials that isolates conducting lines from each other.

The new dielectric materials must have a dielectric constant k that is less than 3.9 of the standard silicon dioxide dielectrics that are currently in use. This will allow metal lines to be put closer together, offering the possibility of producing faster and more efficient semiconductor devices.

1.2 THE IDEAL DIELECTRIC MATERIAL

A dielectric material is defined as a substance that is a poor conductor of electricity, but an efficient supporter of electrostatic field. If the flow of current between opposite electric charge poles is kept to a minimum while the electrostatic lines of flux are not impeded or interrupted, an electrostatic field can store energy. An important property of a dielectric is its ability to support an electrostatic field while dissipating minimal energy in the form of heat. The lower the dielectric loss (the proportion of energy lost as heat), the more effective is a dielectric material. (Neves, 1996)

Before we discuss about the ideal characteristic of dielectric material, it will be beneficial to understand what dielectric constant means. Dielectric constant is the property of a material that determines the relative speed that an electrical signal will travel in the material. A low dielectric constant material will result in high signal propagation and a high dielectric constant material will result in much slower signal propagation speed. A good analogy is to imagine one running along the beach with feet 6 inches in the water. The dielectric constant is analogous to viscosity of the water. If the tide goes out, then one can run faster (lower dielectric constant).

Materials that have low dielectric values are not necessarily an ideal dielectric materials. This is because in the fabrication process, there are others factors we need to take into account where a dielectric material is suitable for the process or are manufacturable.

Basically in general, the ideal dielectric material should have the following characteristics. Of course there is always no material 100% meeting the characteristics but nearest to the requirement. i.e. there is material that has high mechanical strength but poor thermal stability. Besides this, selecting right dielectric material to be used is also depends ion the process equipment and the needs.

Below is a list of the characteristics an ideal dielectric material should have (Bremmer, 2001):

- Have low dielectric constant
- High breakdown field strength
- Low leakage, even under electric fields close to the breakdown field strength
- No moisture absorption or permeability to moisture should occur
- Should exhibit low stress
- Good adhesions to the layer above and below
- Stable up at high temperatures
- No incorporated electrical charge or dipoles
- Contains no metallic impurities
- After process of introduction the dielectric, it does not produce reentrant angles
- Good thickness uniformity across the wafer and from wafer to wafer
- Low defect density (pinholes and particles)
- Contain no residual constituents that outgas during later processing to the degree that they degrade the properties of other layers of the interconnect system.

1.3 MOTIVATION & OBJECTIVE OF THESIS

As mention in 1.1, the feature size in integrated circuits has continued to shrink down to deep sub micro meter regions. As a consequence of shrinking, both the metal line widths and the spacing between them has become smaller is an increase in propagation delay, cross talk noise, and power dissipation caused by resistance-capacitance coupling (RC). An effective method to make the reduction of the RC delay is to decrease the parasitic capacitance by employing a low dielectric constant material.

According to the International Technology Roadmap for Semiconductor 2001 Updates, the dielectric constant will decrease from <2.7 to <2.1 by year 2007. The RC delay with 1mm line will increase from 86ps to 324ps while the line length where RC delay will decrease from 174um to 58um. For long term prediction, it says that the dielectric constant requirement will reach <1.6 at year 2016 and the manufacturable solutions are not known yet.

This has brought the motivation to study the low constant k dielectric material. In this project, carbon doped silicon dioxide is studied as a dielectric material. Traditionally, silicon dioxide is used as the inter metal dielectric material in making both simple and complex semiconductor devices. If films are grown correctly using a high purity low defect silicon substrate it can be an excellent dielectric (insulating) thin film with dielectric constant k of 3.9. When carbon is doped onto the silicon dioxide, the dielectric constant will decrease due to the inclusion of carbon bond bound to the silicon atom within the oxide lattice and lowers the electronic contribution which is related to the number of bonds per unit volume.

The objective of this project is to develop a new method to study the effectiveness of the carbon doped SiO_2 to form low k dielectric constant material as well as to determine a feasible fabrication process to build this layer of dielectric constant material. Basically, the study is divided into 3 parts of experimental studies and ended with a simulation study.

Firstly, a new carbon content material is identified as a dopant material on SiO_2. In industry, methyl gases commonly used are tetramethylsilane, trimethylsilane and etc. Here, methanol (CH_3OH) is used as a source of dopant on SiO_2 to form low k dielectric material. To the best of our knowledge, there has been no experimental work found in the literature using this approach to study the methyl doped SiO_2 compound. First, the study is to carry out to understand if methyl is bound to the oxide layer. Several techniques to introduce methanol to silicon dioxide are then in place for the experiment to identify the best condition for the fabrication process. Next is characterization work like FTIR scans and SEM-EDS investigations to be carried out to ensure methyl is incorporated into SiO_2 and has lower dielectric constant.

Secondly, different alkyl oxygenated alcohols which refers to ethanol (C_2H_5OH) and propanol (C_3H_7OH)) are used as the dopant to compare the effectiveness of the doping to methanol (CH_3OH). Ethanol and propanol have higher carbon content which is 52.1 and 60 atomic percentage respectively and are believe to form more carbon bond with SiO_2 under a similar condition and hence, results in a reduced dielectric constant value. With this, investigation is carried out to understand the effectiveness of the doping with respect to different levels of carbon content alcohol. Of course, the condition for the fabrication used for methanol is being restudied to understand if it is suitable when ethanol and propanol is used.

In the third part of this project, the dielectric material formed should have a characteristic whereby the dielectric constant of the material can be controlled through the doping level. It should be low cost and easy to be produced. A suitable fabrication process, which is simple and straightforward, needs to be defined as well. Then, once the material is built, characterization work is carried out to study the effectiveness of the doping with respect to the doping level of this material and to ensure the material formed is a dielectric controllable material. In this part, carbon monoxide is likely to be the candidate. This idea is original and considered a break through, as carbon monoxide as dopant to silicon dioxide is never been used in industry or done in any research study.

Here, a low cost method to produce carbon monoxide from carbon dioxide need to be developed and the best fabrication environment using this gas need has to be defined. In this research work, carbon monoxide using UV light generator has been adopted. The depth in knowledge in equipment setup needs to be demonstrated in order to achieve the goal of this project. The setup will be discussed in Chapter 4.

At the end, a simulation study is carried out by simulating the RC delay with the empirical data collected throughout the projects. An inverter circuit is created and is simulated to understand the RC delay value with different dielectric constant value or capacitance value measured. It is expected that the lower the dielectric constant, the lower the RC delay.

1.4 THESIS OVERVIEW

The thesis is divided into 7 chapters. The first chapter is a brief introduction to the low k dielectric/interconnects technology. The motivation and objective of this project are stated. Chapter 2 is the literature review. This chapter discussed the technical challenges and issues on low dielectric as well as the history of introducing carbon to silicon dioxide to form low k dielectric material. Several techniques available in industry to produce low k dielectric constant material are included.

In Chapter 3, the discussion is on the theory involved in this project. To study the dielectric constant of a material, understanding on what is RCA cleaning process, deposition process to grow dielectric layer, thickness and reflective index measurement, FTIR measurement and SEM-EDS measurement are required. The last part of this chapter includes the theory on how a dielectric constant of a material can be calculated by performing the measurement on C_{ox} of the dielectric layer. Fundamental on how a RC delay simulation is going to carry out will be discussed in the last part of this chapter.

Chapter 4 is the experimental setup where type and brand of equipment set used in this project will be stated. The specification of the equipment setup and the key attributes of the equipment system used are included.

Next, Chapter 5 will discuss the methodology used. In this project, 3 experiments are defined to achieve the objective. The experimental flow will be helpful to provide an overview picture of the project. In this chapter, the discussion will also emphasize on how a simulation study is carried out. Here, circuitry design and simulation software will be introduced. Chapter 6 is the results and discussion of the project and finally, the conclusion and the future work of this research are presented in Chapter 7.

CHAPTER 2

LITERATURE REVIEW

2.1 REVIEW OF TECHNOLOGY CHALLENGES AND ISSUES ON LOW K DIELECTRIC MATERIAL

The main challenge facing the development of low k films is that altering the composition or density of silicon dioxide also changes its physical and chemical properties. These changes can lead to problems with integrating the new material into standard manufacturing processes. For example, films containing high levels of carbon are susceptible to damage from O_2 plasmas during future processing steps such as photoresist removal. There are many problems that need to be addressed when developing new low k materials. Favorable compromises need to be made between film properties, compatibility with subsequent processing steps and production costs. (Beekman et al, 2000)

The use of low k materials brings new issues, some of which have no solutions at present. To overcome these issues requires carefully controlled engineering of the process flow in the fabrication, i.e., an integration solution. A partial list of examples include low adhesion, low mechanical strength, DUV photo resist poisoning, porous low-k voiding and damage due to etch, ash or cleans processes. Furthermore, the effective k value of an integrated dielectric stack is determined by all the materials in the stack, i.e., the hard mask, CMP cap and etch stop layers increase the effectiveness k value. Consequently, selection of material of these layers must consider their k value and layer thickness should be minimized.

Reliability is also another main concern. Not all issues show up during the fabrication process and some are only evident after reliability stress testing or package assessment, and require alteration of the fabrication process flow. Consequently, integration engineering must include reliability and package test. There is always limit data when new dielectric material is introduced.

The situation becomes more challenge when the industries are moving on using Cu. Integration between copper and dielectric material will be another challenges. So, assume that low k material were completely impervious to copper, it is unlikely that barrier films could be eliminated. Copper can diffuse through the low k material itself and along the interfaces between materials. The latter can cause leakage or charge storage effects in interconnect, which could prove to be bigger issues that the poisoning of transistors by copper.

As a summary, there is lot of challenges in low k dielectric material development. Even if we can get material with low dielectric constants like gas, which has possible value for the dielectric constant 1, there will be issues that still need to be solved like the mechanical stability of the structure, as well as problems associated with the poor thermal conductivity of the ‘gas’. There is always pro and con and the developer need to have the right judgments and final goal in its mind for the technology to be achieved.

In this research project, the scoped is narrowed down to identify a new method to introduce carbon to silicon dioxide to form a low k dielectric constant material. A suitable fabrication process will be defined to provide the best environment to build the material. Several characterization works will be carried out to understand how low the dielectric constant can achieve.

2.2 COMPARISON OF LOW K DIELECTRIC MATERIAL AVAILABLE

The semiconductor industry has long relied on insulating layers of silicon dioxide so it is not surprising that some of the first attempts at producing low k materials have been doped versions of standard silicon dioxide films. The main dopants used to date are fluorine and carbon in the form of alkyl groups such as CH_3. These are generally incorporated into the films by replacing a standard precursor like silane (SiH_4) with SiH_2F_2 or CH_3SiH_3 (Sermon et al, 1999).

Fluorine has the effect of lowering the ionic contribution, which minimizes the response of atoms within the film to an applied electric field while doping a film with alkyl groups terminates some of the silicon bonds within the oxide lattice and lowers the electronic contribution which is related to the number of bonds per unit volume. This leads to a reduction in film density.

Density is an important parameter because low-density materials have low k values. Although doping with carbon and fluorine forms the main focus of low k research, but there is still research being carried out incorporate larger longer chain hydrocarbon groups or new families of materials like organo-fluorides. Example of this material will be discussed later.

Reducing the density of the material is an idea that is taken to an extreme with the development of nanoporous films. These materials consist of fine cage-like skeletal structures with more than 90% of their volume being occupied by air.

The Table 2.1 shows the properties of promising dielectric materials which are used in the industry.

Dielectric	Dielectric Constant (k)	Refractive index	Water adsorption (%)	Stress (MPa)	Gap fill (um)	Cure temperature (°C)
FSG (silicon oxyflouride, F_ySiO_y)	3.4-4.1	1.42	<1.5	-130	<0.35	-
HSQ (hydrogen silsesquioxane)	2.9	1.37	<0.5	70-80	<0.10	350-450
Nanoporous silica	1.3-2.5	1.15	TBD	0	<0.25	300
Fluorinated Silica	2.6-2.9	TBD	1.5	2	<0.5	350
Poly(arylene) ether	2.6-2.8	1.67	<0.4	60	<0.15	375-425
Parylene AF4 (aliphatic tetraflourinated poly-p-xylylene)	2.5	1.59	TBD	100	0.18	420-450
PTFE (polytetraflouroethylene)	1.9	1.34	<0.01	25-27	<0.30	360-390
DVS-BCB (divinyl siloxane bis-benzocyclobutene)	2.65	1.56	<0.2	30-35	<0.22	300
Aromatic hydrocarbon	2.65	1.63	<0.25	55-60	<0.05	400-450
Hybrid- silsesquioxanes	<3.0	1.58	0	30-40	<0.1	450

Table 2.1 Low-k Dielectric Material for ULSI interconnect

CVD of fluorinated oxide (FSG) is material was among the early dielectric material used in industry. It can be produced using spin on technology. FSG, a silicon oxyfluoride (F_xSiO_y), yields k of about 3.5. The high electro negatively of fluorite reduces the polarizability of the film and hence decreasing its dielectric constant.

Besides, FSG, hydrogen silseunoxane (HSQ) is another dielectric material candidates. The early interest in using HSQ was for process simplification. HSQ was used initially only between metal wiring lines (where it was needed most), and giving dielectric constant range of 3.1-3.6 depending on the dielectric type and thickness developed.

Another leading inorganic dielectric material with dielectric constant 1.3-2.5 is nanoporous silica. It is claimed that by using the Cu/Nanoglass devices provided a 36% reduction in capacitance for lines of equal resistance and a 46% reduction for interconnects of equal capacitance (The Information Network, 2003). It has a tunable dielectric constant that relies on pore density. This material has also demonstrated high thermal stability and process simplicity.

From the table, spin on polymer has also shown promising low k value. Organics polymer such as poly(arylene)ethers, Parylene AF4 (aliphatic tetraflourinated poly-p-xylylene), DVS-BCB (divinyl siloxane bis-benzocyclobutene) and aromatic hydrocarbon are giving dielectric constant range from 2.5 to 3.0.

Lastly is the PTFE dielectric material which is chemically and electrically different from the form used in wafer carrier, high purity piping and wet benches. This material has k value of 1.9.

2.3 HISTORY OF INTRODUCING CARBON TO SILICON DIOXIDE TO FORM LOW K DIELECTRIC MATERIAL

Silicon dioxide (SiO_2), the established insulating material that the semiconductor industry has relied upon for years, is beginning to reach limitations in addressing today’s leading-edge device demands. Moving onwards, carbon doped silicon dioxide as dielectric material is being pursued as it has dielectric constant less then 3. The primary driver for this transition can be attributed to the disrupting noise that arises between different signal lines, commonly referred to as cross-talk. As line widths become narrower and those lines, more closely packed together, the adverse signal distortion effects of cross-talk have become an area of increasing concern among chip designers (and source for design alterations). Today's low-k materials are able to reduce cross-talk on the order of 40% to 50% (Ried et al, 2001).

The first type of low k dielectric used was fluorine doped silicon dioxide. The dielectric constant of a typical fluorine silicate glass (FSG) film is between 3.4 and 3.6. When the film has a dielectric constant in this range, there is little to no impact on fabrication performance. Many fabrication using aluminum interconnect in adopt FSG material. It is basically fluorine doping of the silicon dioxide. FSG on aluminum interconnect has been used by some chipmakers at the 0.35 and 0.25 micron nodes (Ried et al, 2001).

Later, researcher found that carbon could bring the dielectric constant even lower compare to fluorine doped silicon dioxide. The low k material that is being integrated in advanced devices is carbon-doped oxide (CDO). This also is a chemical vapor deposited (CVD) film with dielectric constant results between 2.4 and 2.8. The amount of carbon in the film has been known to change the density and hence reduce the dielectric constant. The reduction of the ionic contribution due to the carbon doped oxide lattice was the predominant factor leading to a decreasing the overall dielectric constant (Kim, 2001). Besides using CVD, spin on low k polymer type carbon doped dielectric material is being introduced as well. In general, spin on low k films have a lower dielectric constant than CVD low k films but at the same time, they are more difficult to integrate into interconnect schemes. This will be discussed in Chapter 3.

2.4 DIFFERENT TECHNIQUES IN PRODUCING LOW K CARBON DOPED SILICON DIOXIDE

Silicon dioxide films that are doped with carbon have also been studied extensively and have yielded many promising results. There are several techniques developed to produce carbon doped silicon dioxide. The common techniques used in industry are spin-on-glass, chemical vapor deposition (CVD) and plasma-enhanced CVD. Sometimes, high-frequency plasma techniques can also be used to deposit silicon dioxide dielectrics that are doped with carbon. These methods create lower density films, not only due to the carbon incorporation, but also because operating at the higher frequency that reduces the energy of the ion species that are generated during deposition. The ion energy is directly proportional to the calculation of dielectric constant.

As for example, carbon doped SiO_2 low k thin film can be prepared by radio frequency plasma-enhance CVD at 400C from polymerization of tetramethysilane (4MS) and copolymerization tetramethylsilane and silane (SiH_4) precursor, with nitrous oxide as the oxidant gas. The physical properties are investigated for dielectric constant, refractive index, and thermal stability measurements. The films prepared show excellent thermal stability at temperatures as high as 400˚C and a dielectric constant of about 3, which indicates that it has potential as low k dielectric for advance interconnect application. (Han et al, 2001).

Besides, film with k of about 3 can be formed using a low k Flowfill CVD® process developed by Trikon Technologies. The process reacts methylsilane (CH_30SiH_3) with H_2O_2 to form nonsilicic acid, which condenses on cool water and it converted into an amorphous methylsilane oxide. Beyond methylsilane studies show a possible k of 2.75 using dimethylsilane in the Flowfill CVD® process. It forms high quality dielectric layers and is unique because it can fill gaps and planarize simultaneously, eliminating the need for CMP on some devices. This method is capable of filling very small gaps and it leaves very little moisture content in the film after final treatment and allows for low moisture reabsorbance.

Trikon Technology Ltd (Beekmaan et al, 2000) also published that the methyl doped low k Flowfill® oxide films have k constant range from 2.4 till 3.1. The films deposited in room temperature can provide a stable low k material which in turn can be integrated into 0.18 micron process. By adjusting the process condition such as pressure, temperature and oxidant flow the physical properties of the films can be modified. In another word, the k constant is controllable.

Another characterization work carried out (HouCui et al, 2001) shows that methyl doped SiO_2 films can be doped using CVD. Result shows that the peak of $Si-CH_3$ is detectable through FTIR scan, high thermal stability with annealing in N_2 ambient for ½ hour at different temperature and hardness at about 2.4Gpa comparing to 12.3 Gpa of SiO_2. Besides, the study also shows that the films has low leakage current and breakdown field >3MV/cm.

It is suggested that the properties of low-k SiCOH film can be deposited by plasma enhance chemical vapor deposition using trimethylsilane (Narayanan et al, 2002). The results show the deposition rate decrease with increase in deposition temperature. The -OH related bonds were not detected in films even when the deposition is done at 200˚C. All deposition conditions studies resulted in films with dielectric constant less than 3 and the lowest being ~2.7 when deposited at 200˚C.

Study was carried out also on SiH_4- based PECVD low k carbon doped silicon dioxide with comparison of the carbon doped silicon films which were deposited using organosilicon precursor $(CH_3)_xSiH_{4-x}$ (Yang et al, 2000). The results shows that the SiOC films growth has similar gross physical and electrical characteristic to those of $(CH_3)_xSIH_{4-x}$ based SiOC. The dielectric constant ranges from 2.8 to 3.2. It also stated that the deposition at 400˚C results in higher dielectric constant of 3.1 but the post anneal process is not necessary. It also demonstrated good adhesion, etching and CMP properties.

Besides carbon doped silicon dioxide as mention above, there is study shows that carbon doped SiOF films has even lower k constant compare to fluorine doped SiO_2 (Lubguan, et al, 1999). The carbon doped SiO_2:F films were deposited by adding CH_4 gas into $SiH_4/O_2/CF_4$ gas mixture using a PECVD. The films growth has a dielectric constant range of 3.1-3.6. The dielectric constant is dependant on the carbon density. It was shown that there was a close correlation between a decrease in dielectric constant and an increase in Si-CH_3 bond density.

Another report has supported the study on the carbon doped SiO_2:F (Ding et al, 2000). In this technique, tetraethoxysilane (TOES), C_4F_8 and Ar are used to produce the low dielectric by using plasma enhanced chemical vapor deposition (PECVD). The measurement of C-V characteristics of the films indicates that the dielectric constant of the deposited film decreased with increasing C_4H_8 flow rate which is in accord with the increase in the frequency of Si-O stretching mode. When the flow rate ratio of C_4H_8 to TOES is equal to 1.8, the dielectric constant of the film is 2.35.

2.5 TECHNIQUE ADOPTED

In this project, oxygenated alcohol and carbon monoxide are selected as the dopant for the silicon dioxide to form low k dielectric material. These materials are easier to obtain and less dangerous compared to the gases (ie trimetylsilane) used in industry. Silicon samples are treated in these dopants either before or during the oxide growth process. Here, atmosphere pressure chemical vapor deposition process (APCVD) is used. In this study, we are using this technique, as this is the traditional method to grow a silicon dioxide layer on the wafer. This is the best way to study the dielectric constant of a doped silicon dioxide compared to undope silicon dioxide. In a typical CVD process, reactant gases (i.e., carbon monoxide) at room temperature enter the reaction chamber. The gas mixture is heated as it approaches the deposition surface, heated radioactively or placed upon a heated substrate. Depending on the process and operating conditions, the reactant gases may undergo homogeneous chemical reactions in the vapor phase before striking the surface.

The detail of the experiment methodology, setup will be discussed in Chapter 5. In this research, the oxygenated alcohol used like methanol, ethanol and propanol are expected to produce material with dielectric constant of 2.7-3.2. On another hand, carbon monoxide doped silicon dioxide will have even lower dielectric constant, which is depending on the amount of carbon doped to silicon dioxide. From the experiment, it can go as low as 2.6. The technique adopted in the project is highly recommended and compatible to be introduced.

CHAPTER 3

THEORY

3.1 THE IMPORTANT OF LOW K DIELECTRIC CONSTANT MATERIALS

As the dimension of a device shrinks, the transistor switching speed itself no longer limits the logic delay or access time of the IC. The scaling of the interconnect line widths does not bring about a corresponding decrease in the propagation delay time through the interconnect lines. This is even worst when the die sizes increases, the interconnect path lengths will also increase, and in fact the most of the large integrated circuits will have higher interconnect propagation delay time.

The propagation delay exhibited by integrated circuits is therefore almost always limited by the large RC delay of the interconnect line. As example, is a polysilicon line having a 20-ohm/sq-sheet resistance is used to connect one corner of a 0.7x0.7cm chip to the diagonal corner, it is predicted that the propagation delay will be 1.4us. Even is Al is used as interconnect layer, the delay caused by 1cm long interconnection lines will limit the circuits speed once device dimension fall below~2um (Keyes, 1981).

In order for circuit to better performance at higher speed, two goals must be met. First, the material used for transmitting signal over long distance must have the lowest possible resistance values. Here, it refers to the conductive layer or trace. Second, is the internal dielectric material used. The lower the dielectric constant a material has, the lower the RC value achieved. The RC value here is directly proportional to the propagation delay. Of course, in design perspective, the length of interconnect lines on a chip must be make as short as possible. (Wolf, 1990)

The formula below shows the relationship of dielectric constant to the propagation delay. That is,

$$R = (\rho l)/(wt_m)$$
$$C = \varepsilon wl / t_{ox}$$

And therefore

$$RC = \frac{\varepsilon \rho l^2}{t_m t_{ox}}$$

where ρ is the resistively, l is the interconnect lines length, w is the line width, ε is the permittivity, t_m is the thickness of the metal and t_{ox} is the thickness of the oxide. From the *RC* equation here, it show that the *RC* delay is directly proportional to the square of the length of the interconnect line.

In short, in order for a circuitry to perform at maximum speed with minimum delay time, a low constant k dielectric material is needed and this constant is the function of the delay time.

3.2 SILICON DIOXIDE AS INTERCONNECT DIELECTRIC MATERIAL

3.2.1 OXIDATION GROWTH RATE

The basic mechanism for the formation of SiO_2 from Si is well understood. Deal and Grove developed a mathematical model which accurately describes the growth kinetics of oxide films with thicknesses >300A. They proposed that oxidation proceed by the diffusion of an oxidant (molecular H_2O or O_2) through the existing oxide to the Si/SiO_2 interface, where the molecules react with Si to form SiO_2. The oxidation reaction occurs at the Si/SiO_2 interface. Therefore, as the oxide grows, silicon is consumed and the interface moves into the silicon. Based on the relative densities and molecular weights of Si and SiO_2 it is found that the amount of silicon consumed is ~45% of the final oxide thickness. Thus if 1000A of oxide is grown, ~450A of the Si will be consumed. This relationship is important for calculation step heights that form in the silicon as a result of varying oxidation rates at different locations of the silicon surface.

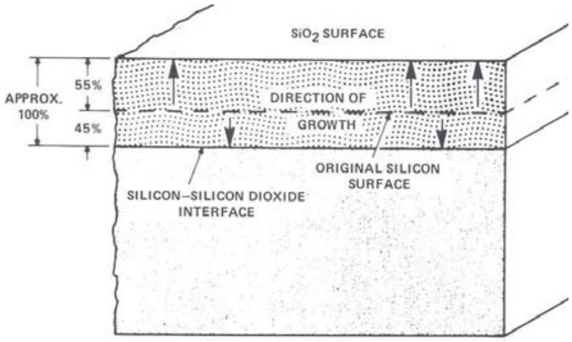

Figure 3.1 SiO_2 surface growths on silicon (Schulz et al, 1990)

When silicon is exposed to an oxidizing atmosphere, such as oxygen, the reaction:

Si (solid) +O_2 (vapor) → SiO_2 (solid) Dry oxidation

Si (solid) +H_2O(vapor) → SiO_2(solid) +2H(gas) Wet oxidation

At room temperature in air, a silicon dioxide (SiO_2) layer develops in a matter of second. However, the oxide layer formed is sufficiently dense that more oxygen atoms are unable to diffuse through the layer to continue the oxidation, and the native oxide formed is limited to a thickness of about 10 to 20 angstroms (Bowman et al, 1990).

When the temperature is raised to more that 600°C at atmospheric pressure, the diffusion of oxygen through the oxide proceeds at a predictable rate and thicker oxides can be grown. The growth rates are a function of time, temperature, furnace ambient, and pressure. The oxidation process reacts oxygen from an external source with the silicon surface to generate SiO_2. Therefore, silicon is consumed during the chemical reaction (Wolf et al, 1986).

The oxide layers thus grown are essentially amorphous quarts, which is a good dielectric. When properly grown under sufficiently clean conditions, these quartz layers – even when only a few-hundred angstroms thick – have strong adherence to the silicon substrate and exhibit excellent dielectric and density properties.

3.3 DEPOSITION PROCESS

Dielectric film deposition has been used extensively in ICs since the device planarization technique was developed. Dielectric films including silicon dioxide are used as the isolation, mask and passivation layers. There are many deposition techniques for the material formations. These methods can be classified into 2 main mechanisms:

1. chemical vapor deposition
2. physical vapor deposition

3.3.1 CHEMICAL VAPOR DEPOSITION

Chemical vapor deposition is defined as the formation of a nonvolatile solid film on a substrate by the reaction of vapor-phase chemicals (reactants) that contain the required constituents. It is most often used for semiconductor processing. It is material synthesis process whereby the constituents of the vapor phases react chemically near or on a substrate surface to form a solid product. (Cheng, 1996)

Several step must occurs in every CVD reaction:

1. Transport of reacting gaseous species to the substrate surface
2. Absorption, or chemisorption, of the species on the substrate surface
3. Heterogeneous surface reaction catalyzed by the substrate surface
4. Desorption of gaseous reaction products
5. Transport of reaction products away from the substrate surface

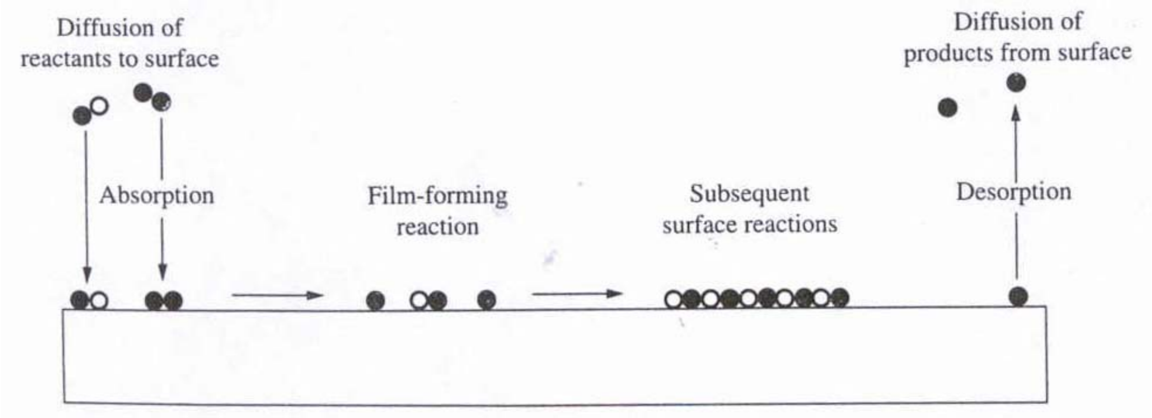

Figure 3.3 Sequence of reaction step in CVD (Cheng, 1996)

In practice, the chemical reactions of the reactant gases leading to the formation of a solid material will take place not only on (or very close to) the surface (heterogeneous reaction) but also in the gas phase (homogeneous reaction). Heterogeneous reaction are much more desirable, because such reactions occur selectively only on the heated surfaces and produce good-quality films. Homogeneous reactions, on the other hand, are undesirable, because such they form gas phase clusters of the depositing material, resulting in poorly adhering, low-density films with defects. In addition, such reaction also consumes the reactants and can cause a decrease in deposition rates. Thus, one important issue of a chemical reaction for CVD application is the degree to which heterogeneous reactions are favored over gas phase reaction.

The most common deposition methods are atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD) and plasma-enhanced CVD (PECVD). The Table 3.1 shows the differences in characteristic and application of CVD processes.

Process	Advantages	Disadvantages	Application
APCVD	Simple reactor, fast deposition, low temperature	Poor step coverage, particle contamination, low throughput	Low temperature oxides (both doped and undoped)
LPCVD	Excellent purity and uniformity, conformal step coverage, large wafer capacity, high throughput	High temperature, low deposition rate	High temperature oxides (both doped and undoped), silicon nitride, poly-Si, W, WSi2
PECVD	Low temperature, fast deposition, good step coverage	Chemical and particle contamination	Low temperature insulators over metals, passivation (nitride)

Table 3.1: Characteristic and application of CVD processes (Adams, 1983)

3.3.2 PHYSICAL VAPOR DEPOSITION

Physical vapor depositions are different from CVD in the deposition mechanism. The deposition rate for CVD will be proportional to the deposition temperature. However, the deposition rate for PVD will generally decrease with increasing deposition temperature. The PVD technologies usually used are described as follows.

Evaporation technology

This is not of the oldest techniques used for depositioning thin films. A vapor is first generated, by evaporating a source material in a vacuum chamber, then transported from the source to the substrate and condensed to a solid film on the substrate surface.