Optical, Mechanical, and Electronic Properties of Etched Silicon Nanopillars

Thesis by

Sameer S. Walavalkar

In Partial Fulfillment of the Requirements

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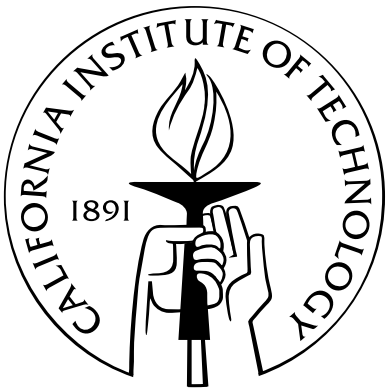
Doctor of Philosophy



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To my family: Mom, Dad, Smita. You are the glue that holds together the gears of my life.

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Abstract

This work focuses on the fabrication, characterization and applications of silicon nanopillars. We explain the techniques involved in creating sub 50 nm diameter pillars with aspect ratios of 60:1. Original work encompassed the use of a novel etch mask made of reactive ion sputtered aluminum oxide, 'pseudo-Bosch' inductively coupled reactive ion etching (ICP-RIE) to etch structures on the nanoscale. These methods demonstrate a unique approach to the largely 'bottom-up' technology used in nanowire fabrication.

We also explored the self-terminating oxidation behavior of convex, two-dimension silicon structures. It was found that during the oxidation process, strain built up at the moving Si-SiO_2 interface eventually led to a cessation of oxidation. This was used to predictably reduce the diameter of these pillars to 2 nm, making 'nanowhiskers.' We were able to characterize the results of this oxidation non-destructively by utilizing reflection mode transmission electron microscopy (R-TEM).

Using spun-on PMMA and an electron beam to constrict it and bend the pillars, we were able to incorporate as much as 25% strain. More interestingly this deformation appeared to be elastic, as the pillars, once freed from the polymer, would snap back to their upright poisition.

A consequence of the creation of silicon nanowhiskers was that silicon, a normally poor light emittier due to its indirect bandgap, became photoluminescent. As we reduced the diameter we noticed that the bandgap became direct and the emission peak was blue-shifted. We were able to utilize a tight-binding model (TBM) that was modified by the oxidation induced strain. This modified model predicted the blue-shift in peak emission wavelength with decreasing pillar diameter. The strain induced in the pillar during the oxidation played a significant role in the peak emission wavelength and shape of the bandstructure. By corrugating the pillars with an oscillating etch technique we were able to turn our nanopillars into quantum dots which also proved to photoluminesce.

Finally we look at the possibilities of creating a silicon light emitting diode. By creating a double-gated structure it is possible to overcome the difficulties encountered with sub 5 nm diameter pillars. A possible fabrication process, and the current work done to implement it, is presented as well as a simulation explaining the behavior of this device in the future.

Published Work

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Chapter 1

Motivation

Silicon forms the backbone of modern integrated circuit (IC) technology. Almost all computer chips are fabricated out of or on wafers of silicon. Over the past 50 years silicon processing technology has improved in both repeatability and fidelity. The payoff for this improvement has been the ability to pack ever increasing numbers of transistors or circuit elements of smaller and smaller sizes onto computer chips. The rapid pace of the rise in transistor density was quantified by Gordon Moore in 1965 and has come to be known as "Moore's Law". The law, stated simply, is that the on-chip transistor density doubles every two years [12]. Figure 1.1 shows a plot of the increase in transistor density on a log plot over the last 40 years.

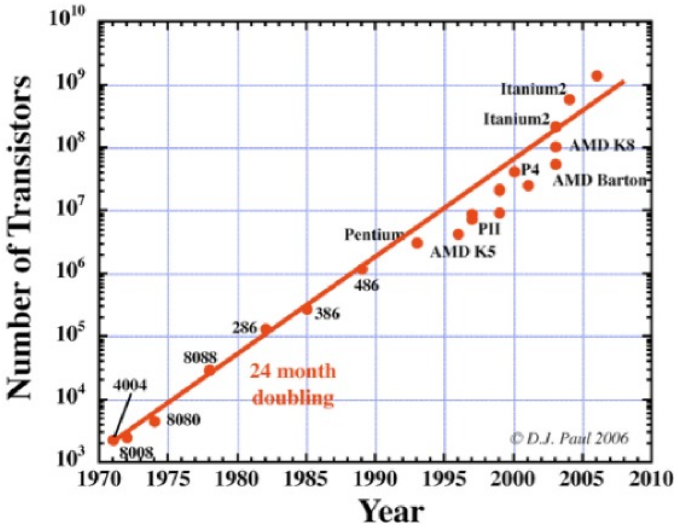


Figure 1.1: Plot of the scaling of Moore's Law showing the doubling of transistors per chip every 24 months.

The technology developed to make silicon, and other semiconductor, devices as small as possible has spawned numerous areas of study. Decreasing the size of silicon components to the micron-scale created the field of micro-electromechanical systems (MEMS). These devices, now ubiquitous, are

used in everyday products from airbags to the Texas Instruments DLP projector. The ability to decrease the size of silicon elements has also allowed the incorporation of optical waveguides onto chips. This spawned the field of silicon 'photonics', which meshes optics and electronics for studying and exploiting interesting light-matter interactions. As the drive towards miniaturization began to approach the atomic limit, the field of nanotechnology was born. The fascinating feature of materials at the nanometer size scale is that they can behave completely differently than bulk quantities of the same material. Stiff materials can become flexible, dark materials can begin to emit light and good conductors can stop passing electrical current.

This thesis is meant to elucidate some recent work into the techniques and science of manipulating silicon at the nanometer length scale. We will initially focus on methods of fabricating silicon nanopillars (Chapter 2). This will be followed by methods used to shrink these devices from diameters of tens of nanometers down to diameters as small as two nanometers, and to characterize them (Chapter 3). Then we will investigate three main areas of interest regarding silicon at the nanometer length scale: mechanics, optics, and electronics. The rest of this chapter will focus on setting up the motivation for the work in this field.

Why silicon?

As mentioned before, silicon is the most common material used in semiconductor fabrication. It is plentiful, as it is the second most abundant element found in the Earth's crust, and easy to purify, making it an inexpensive material to work with. For reference, the price of a pound of silicon currently sits between \$1–2, a bargain considering that a pound of silicon could be used to make tens of thousands of computer chips. Silicon is purified from silicon-dioxide, found as sand, by heating it in the presence of carbon. The carbon acts as a getter for the oxygen in the silicon dioxide and leaves behind roughly 98% pure, or metallurgical grade, silicon. This can be further purified by a variety of methods and be melted and re-formed into single crystal boules of silicon by what's known as the Czochralski (CZ) method. These cylinders of silicon are diced with a diamond tipped saw and polished to a mirror finish before they are sent to be processed in fabrication foundries. Examples of the boules resulting from the CZ process and the final, diced wafers are shown in figure 1.2.

By itself silicon is not conductive, however it can be induced to pass current by the addition of impurities from groups III and V from the periodic table, such as boron and phosphorus. By selectively diffusing or implanting these dopants into certain areas, it is possible to create pockets of hole or electron rich material. Most of the diode and transistor technology stems from the nature of the junction between electron (n-type) and hole (p-type) regions.

Furthermore, silicon's native oxide, SiO_2, is basically the glass that is ubiquitous in our lives. Aside from being insulating and resistant to most chemicals, this oxide layer is bio-compatible. It

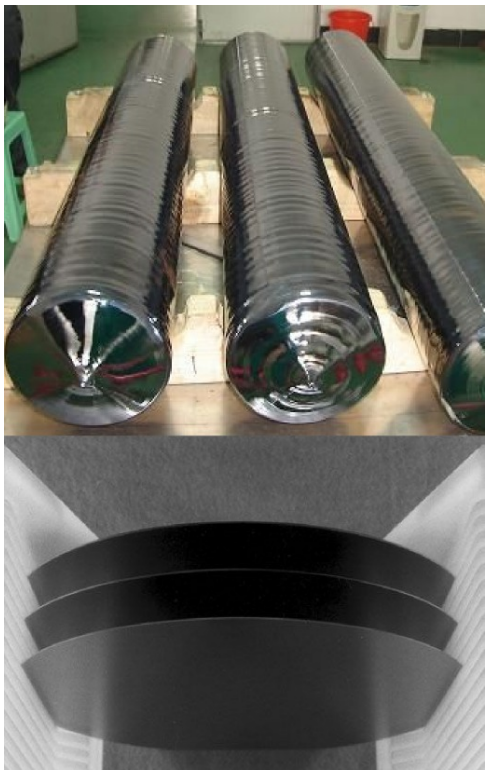


Figure 1.2: (Top) Single crystal silicon boules pulled from a melt in CZ growth. (Bottom) Diced and polished 6 inch diameter wafers

can be used to passivate and protect the surface of a silicon chip and remains solid up to 1400 ^{o}C, past the melting point of silicon itself. The oxide can be deposited through a variety of techniques or can be thermally grown on the surface of a silicon wafer by heating it in a furnace in the presence of oxygen or water vapor.

The technology to shape and process silicon has been developed at universities and companies over the last 50 years. Silicon can be wet etched isotropically with a nitric/hydrofluoric acid mixture or anisotropically along <111> crystal planes with potassium hydroxide or tetramethyl-ammonium hydroxide. Silicon can be dry etched with either a fluorine or chlorine etch chemistry; for deep micron scale features it can be etched with an SF_6 'cryo-etch' and for nanometer scale features it can be etched with a mixed mode, SF_6/C_4F_8 'pseudo-bosch' etch.

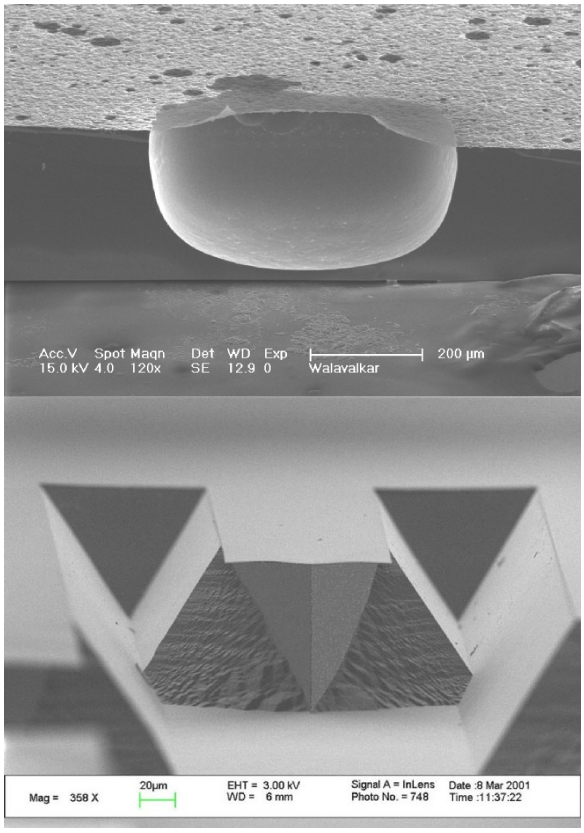


Figure 1.3: (Top) Isotropic silicon etching done with XeF_2 gas. (Bottom) Anisotropic etch done with KOH. Note that the angled sidewalls are <111> planes.

Silicon can be bonded to itself, glass, and even III-V compounds like InP to expand its role beyond simply an electronic material. The first few chapters of this thesis will focus on applying variations of these developed techniques to create and characterize silicon nanostructures.

Why small?

Why has there been such a drive towards miniaturization? The easiest answer is so that we can make more of something in a given area. If we can pack more devices into a smaller region then we can consume less real-estate on a chip or waste fewer resources in its fabrication. However, the drive for numbers is only a part of the advantage in the development of nanotechnology. Frequently materials will exhibit different mechanical, optical or electronic characteristics when they are formed or shaped into nanostructures than they would in their bulk forms.

Mechanics

Silicon, in its bulk, single crystal form is a stiff, brittle ceramic prone to shattering along its crystal planes; as seen in figure 1.4. In other words if one attempted to bend a rod of silicon it would snap like a dinner plate. However, if we were to take this same rod, retain the aspect ratio, and scale the dimensions down to nanometer length scales, it is possible to bend this rod like a stiff tube of rubber. Chapter 4 examines how a force-mediating polymer is used to tunably deform silicon nanopillars in order to incorporate large amounts of strain into the silicon lattice, modifying the electronic and optical properties of the material.

Optics

In most zinc-blend semiconductors the valence band edge is composed of a mixture of p-orbitals, while the conduction band edge is a mixture of spherical s-orbitals. This allows these two band edges to align in momentum space creating a 'direct' band gap semiconductor. In silicon, however, the conduction band contains some mixed portion of the p-orbitals, splitting the normally spherically symmetric band edge at the zero momentum point into six degenerate band minima that are misaligned in momentum space, creating an 'indirect' band gap. The indirect gap is shown on the left hand frame of figure 1.5. This misalignment forces electrons to borrow momentum from lattice vibrations (phonons) in order to conserve momentum while de-exciting from the conduction to the valence band during light emission. Since optical emission in silicon is now a second-order process involving both charge carriers and phonons, the rate of light emission in silicon is much lower than the rate of carrier relaxation through non-radiative means, making silicon a very inefficient light emitter. However, by shrinking the spatial dimensions of silicon through nanofabrication and thermal oxidation, it is possible to confine electrons sufficiently in real space such that they are smeared out in momentum space by the uncertainty principle, making a direct, phonon-unassisted transition more likely. The band-structure of such a spatially confined silicon nanopillar, with a diameter of 2.5 nm, is shown on the right-hand side of 1.5, with a vertical and horizontal ball and stick model of the structure. Furthermore, spatially restricting the electrons blue-shifts the photon emission energy

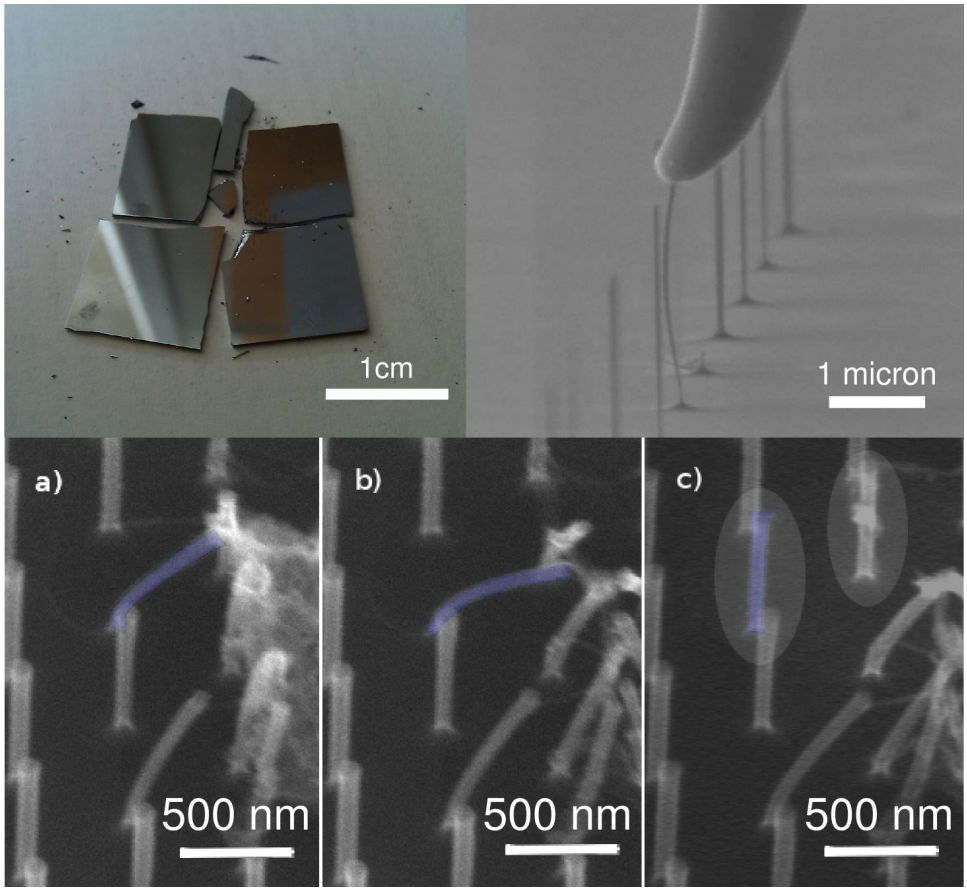


Figure 1.4: Flexibility of silicon at macroscopic (top left frame) and micro/nanoscopic dimensions (top right and bottom frames). In the bottom frame a silicon pillar that is bent completely over is highlighted in blue.

through a quantum confinement effect allowing silicon, which normally emits at 1100 nm, to emit at wavelengths as short as 400 nm. Figure 1.6 shows the emission spectra for various diameter silicon nanopillars and a TEM of the thin silicon cores that are able to emit light. In chapters 5 and 6 we examine the optical emission properties of silicon structures with diameters as small as 2 nm and how the size and strain found in these nanoscopic structures allow silicon to efficiently emit light.

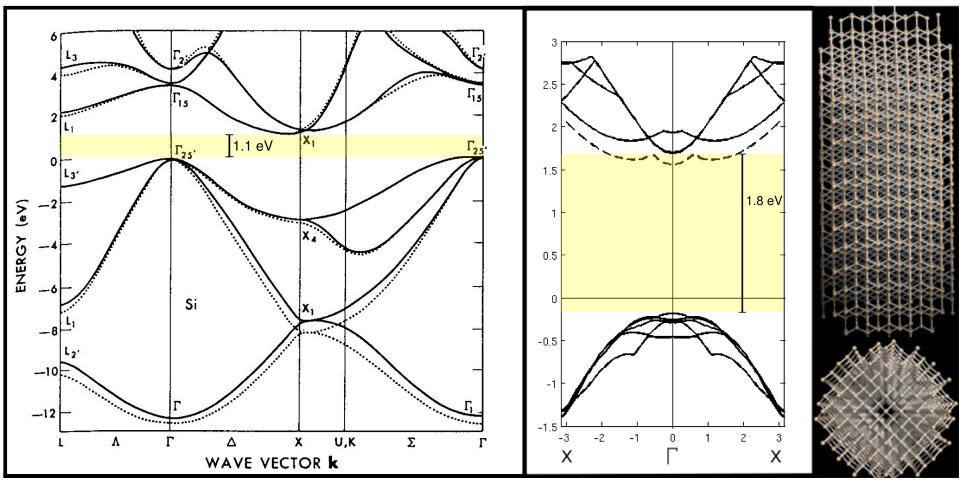


Figure 1.5: Bandstructure of bulk (left hand side) and nanopillar (right hand side) silicon; the right hand side inset shows the structure of the nanopillar.

Electronics

There are a host of interesting electronic quantum effects that become relevant when silicon devices are scaled down to sub-10nm sizes. It is possible to see phenomena such as coulomb blockade, where the electron-electron repulsion prevents current flow, or ballistic carrier transport in transistors, where the gate length of a device is much smaller than the diffusion length so carriers can travel between electrodes without scattering. When the silicon pillars investigated in this work are scaled down to sub-10nm diameters we begin to lose the ability to dope them and thus they become insulating. However, by introducing a wraparound gate structure it is possible to electrostatically dope the pillars and create switchable, ambipolar diodes or transistors. A FIB cross-section of a dual gated diode structure is seen in figure 1.7. Since the doping and thus device characteristics could be changed on the fly, such devices could prove to be quite useful in creating in-situ reprogrammable logic. Chapter 7 describes the fabrication, testing and theory behind such structures.

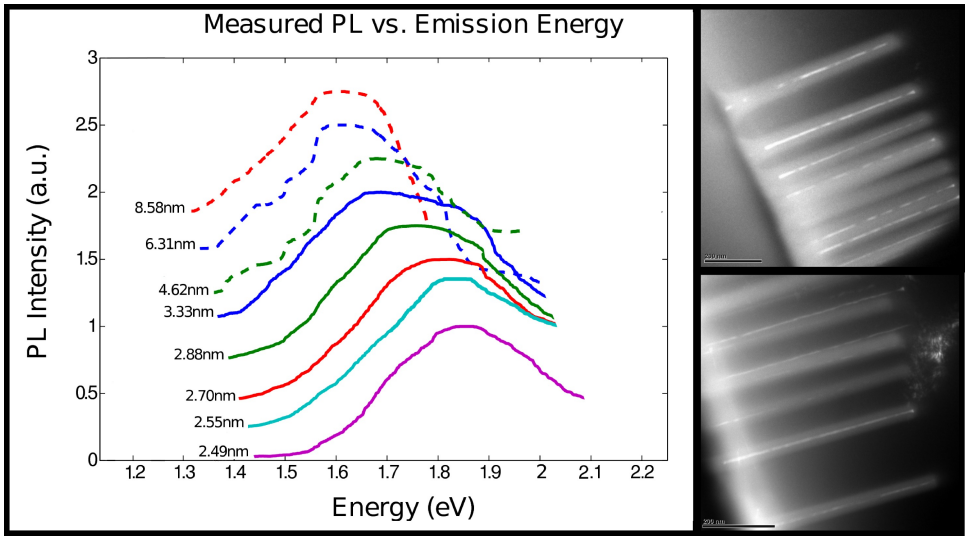


Figure 1.6: Photoluminescence spectra for silicon nanopillars of various diameters. The TEM image is of a pad of oxidation thinned nanopillars with sub 10 nm diameter single crystal silicon whiskers running up the middle (shown in white under diffraction contrast).

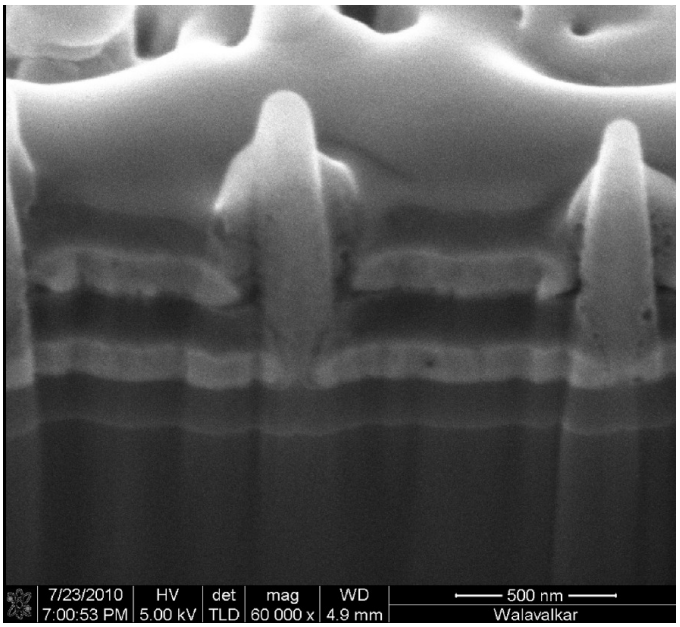


Figure 1.7: FIB cross-section of an ambipolar silicon LED. The light gray stacked layers are copper gates while the dark layers are silicon dioxide and silicon nitride insulating layers. The 3 nm diameter pillar is surrounded by an insulating sheath of silicon dioxide.

Why top-down?

A very interesting avenue towards the construction of nanoscale devices is through self-assembly or 'bottom-up' growth. Such devices rely on the energetics of the atomic or molecular assembly of materials to create larger, well-ordered structures. While these devices may represent the cutting edge of nanotechnology it remains to be seen whether or not they could be useful for anything but serial fabrication for scientific investigation. It is currently difficult to pattern or predict ahead of time how such structures will form over a large area or over multiple chips, even with identical processing conditions. Methods such as vapor-liquid-solid (VLS) growth of silicon nanowires have been successful at making dense arrays of nanowires; making electronic contact to them is still difficult as it usually involves knocking the wires over and hunting around in an SEM or optical microscope to find an isolated wire and then patterning contacts.

The work presented here focuses on 'top-down' or etched silicon nanopillars. The advantage in this case is the ability to accurately and repeatably set the size and location of these structures with electron beam lithography. Although electron beam lithography is a serial process the size of features defined through this process could be replicated with industrial photolithography techniques and thus these structures would retain the ability to be fabricated through cost-effective parallel processing. Electron beam lithography was used in this work since we were not interested in creating millions of identical chips but rather rapidly prototyping and testing numerous chips with slightly different designs. The ability to define where these devices are located allows for easy contacting using optical lithography utilizing alignment marks patterned on the same layer as the nanopillars. Thus it has been possible to address multiple instances of single nanopillars or even multiple instances of large pads of nanopillars in parallel without having to search around for them on a chip. Furthermore the use of lithographic techniques does not require the use of metals or materials that are normally not found in a silicon fabrication foundry thus simplifying the transfer of this technology to mass production.

Chapter 2

Fabrication

This chapter will focus on the materials and methods used in fabricating top-down silicon nanostructures. It will cover the selection of silicon, the electron beam patterning process, the sputtering process, the lift-off process and the etching process. A summary of this fabrication method is given in *Henry et al.* [13]. Figure 2.1 shows an outline of the fabrication process used to make vertical silicon nanopillars. These and variations of these structures are used as the basis for nanostructuring silicon.

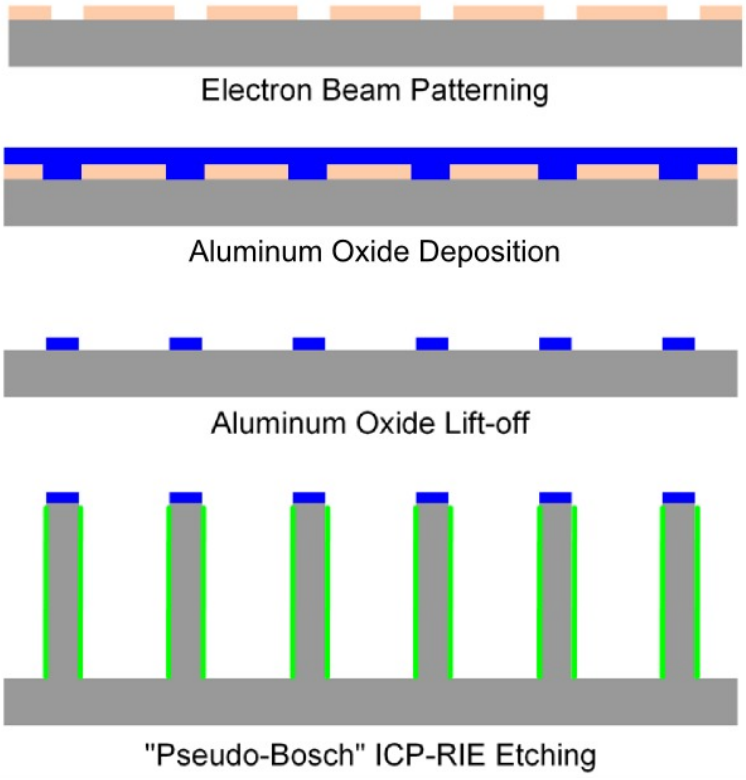


Figure 2.1: Schematic of silicon nanopillar fabrication

2.1 Silicon and wafer preparation

All the fabrication in this work was done on CZ grown, [100] , single-side polished silicon. Depending on the intended application of the devices, wafers of a given doping polarity as well as doping density were chosen. For an optical application such as a photoluminescence measurement wafers doped in the 1-10 $\Omega \cdot cm$ range were selected in order to reduce the amount of ionized impurity scattering and extend the life-time of excited carriers, while the requirement for a current path through the wafer necessitated the use of highly doped (.001 $\Omega \cdot cm$) wafers.

2.2 Electron beam patterning

Prior to application of an electron beam (e-beam) sensitive resist the wafer was rinsed (in order) with acetone, isopropyl alcohol (IPA), dichloro-methane, and IPA again, then blown dry with nitrogen. This process removed organics contaminants on the surface; the fabrication process was not sensitive to native oxide or metal contamination and thus a more extensive clean was not needed.

The electron beam resist used in this work is poly(methyl methacrylate) (PMMA), a well characterized and robust resist. In order to define features as small as 25 nm, a 100 nm thick layer of PMMA was applied to the wafer. Microchem PMMA 950 A3 was spun on at 4000 RPM for 1 minute and soft baked at 180 ^{o}C to drive off solvents. To verify the thickness of the resist, a broad band interference measurement was done in an optical microscope using a Filmetrics F40 and the thickness was calculated by fitting to a material model of PMMA 950.

The wafer was patterned in a Leica EBPG 5000+ beam writer. In order to define nanopillars, circular areas were exposed in the PMMA with diameters that could range from 25 to 500 nm depending on the application. The dose used for the 100 nm thickness of PMMA was 1275 $\mu C/cm^2$. When the pattern was repeated in a 1 cm center to center grid sixteen complete samples could be written on a two inch wafer; when the period was 0.5 cm up to 49 samples could be written on one two inch wafer in approximately 1.5 hours. Patterns were always written with two beams, a small beam ($\sim$1.5 nA) to define the nanopillars and a large beam ($\sim$175 nA) to define micron sized alignment marks, used to locate the pattern. The two scales of fabrication can be seen in figure 2.2, where the red patterns are the alignment marks and the inset shows the circular areas to be exposed on the PMMA.

The wafer was developed by dipping in a 1:3 solution of methyl isobutyl ketone (MIBK) to IPA for 25 seconds. After removal from the bath the wafer was immediately rinsed with DI water and blown dry with nitrogen.

Figure 2.3 shows an array of 200 nm holes developed in PMMA. These holes are large compared to those typically used to fabricate useful nanopillars; they are shown here as an example.

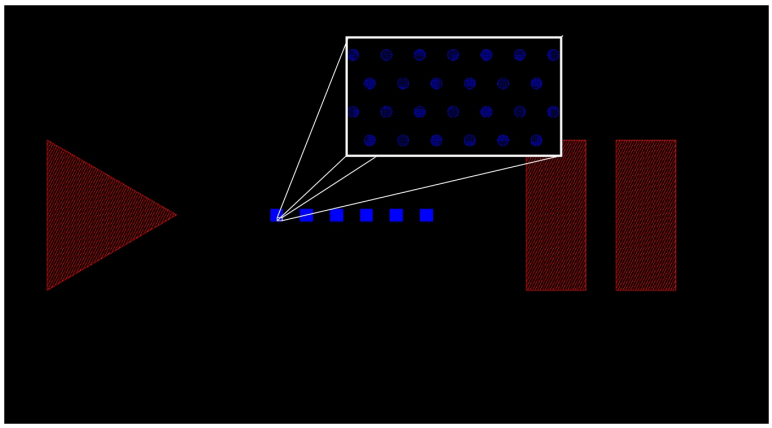


Figure 2.2: Sample electron beam pattern layout. The red areas are the alignment marks and the blue are the disks that define the nanopillars.

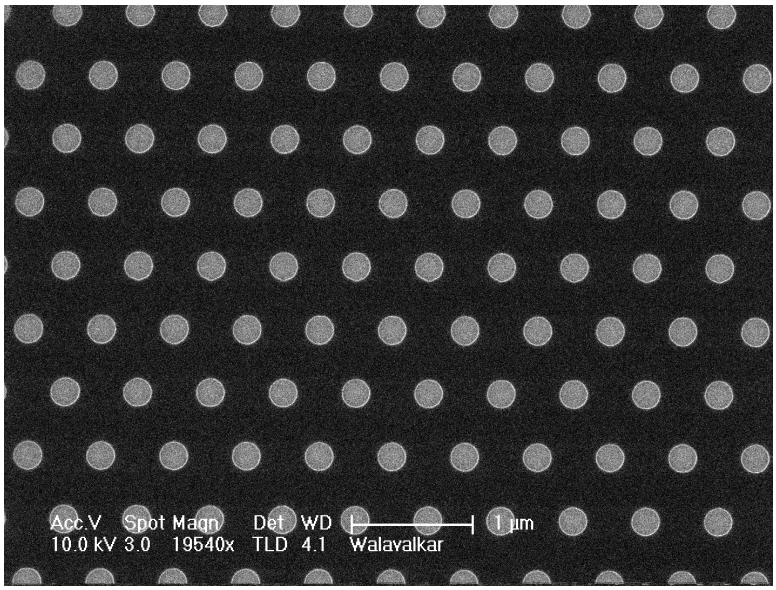


Figure 2.3: Developed pattern of 200 nm diameter holes in PMMA.

2.3 Aluminum oxide deposition and patterning

As explained in *Henry et al.*[13] aluminum oxide (Al_2O_3) was chosen as an etch mask for both its resistance to chemical etching by fluorine and its resistance to physical milling. Specifically, aluminum fluoride is formed on the surface of the mask during the etch, passivating the surface of the alumina. This layer of aluminum fluoride is not volatile at the temperature of the etch[1] so it remains on the surface of the mask, protecting it from further degradation. A plot of the volatility of aluminum fluoride is given in 2.4, since the etch was done at room temperature and the aluminum fluoride becomes volatile at temperatures greater than 1300^o C the passivated mask does not sublime to any appreciable degree. The alumina was deposited using a reactive sputtering process; DC reactive sputtering was chosen as the deposition method over other techniques to ensure stoichiometric deposition of alumina at reasonable deposition rates. Another popular method is to sputter an alumina target in only argon with an RF sputtering setup using the reversal of the bias to send electrons to the target to negate the charging effects of the positive accelerated ions. Unfortunately this method tends to have a slow ($< 2 - 3nm/min$) deposition rate and does not necessarily produce stoichiometric alumina[14]. The sputtering was done with an aluminum target

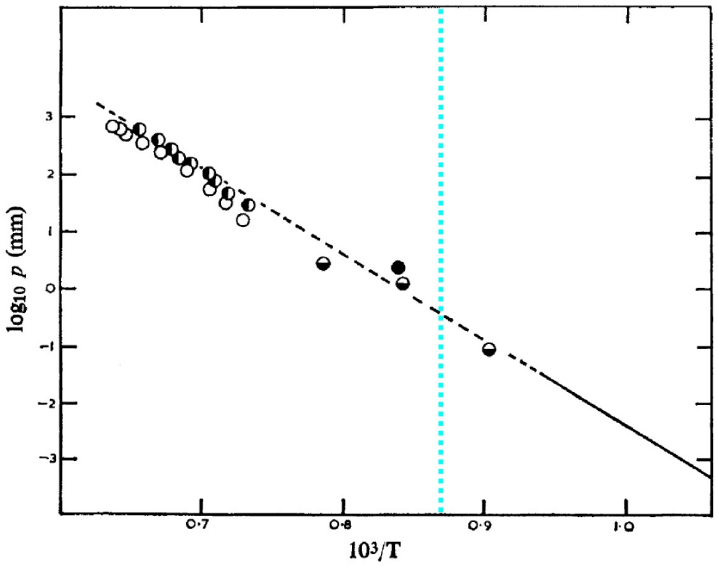


Figure 2.4: Plot from *Witt et al.*[1] showing the vapor pressure of aluminum fluoride vs. temperature. Blue dotted line placed by the author of this text to show the temperature value at which AlF_3 begins to become volatile.

at 10 mTorr with a gas ratio of 5:1 Ar:O_2. Tuning the gas ratio correctly is critical as too much oxygen will grow a dielectric on the surface of the target, which when bombarded with argon ions will impart a positive charge to the dielectric. Once the target becomes charged the argon ions needed to sputter the alumina are deflected by the surface and no material is sputtered; in this case

the target is considered "poisoned". If the gas ratio is oxygen deficient the deposition results in a soft, aluminum rich, metallic mask, which does not hold up to the physical component of the etching process. Figure 2.5 shows the variation in the accelerating voltage drop between the plasma and the sputtering target. As the oxygen partial pressure passes a certain point the accelerating voltage and thus the sputtering rate drops. In order to get stoichiometric alumina with deposition rates of > 25

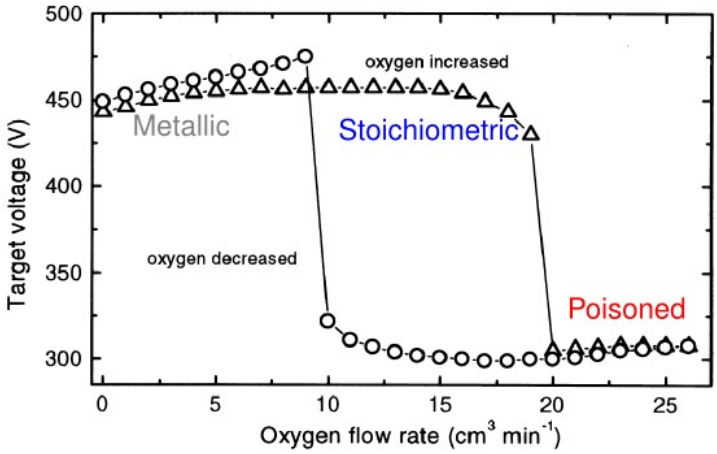


Figure 2.5: Plot from *Koski et al.*[2] showing the hysteretic variation in the accelerating voltage as a function of oxygen flow rate. Labels are added by the author

nm/minute the sputtering must be done at a partial pressure of oxygen that corresponds to roughly 15 cm^3/min in figure 2.5[14, 2, 15]. In our case we pushed the oxygen partial pressure above this point, but still below the inflection point, in order to drop the accelerating voltage to reduce the deposition rate and ensure that the mask was stoichiometric.

The 5:1 Ar:O_2 with 100 sccm flow rate for argon and 20 sccm flow rate for oxygen was found to work well with a 400 W DC plasma. The deposition rate was 10 nm/minute and the typical deposited mask thickness was 30 nm. When the correct gas ratio and power is achieved the plasma switches from a dark purple color to a deep cobalt blue, as seen in figure 2.6

The stoichiometry of the deposited material was measured using an energy-dispersive X-ray spectroscopy (EDS/EDAX) system attached to an FEI Sirion scanning electron microscope (SEM). The composition of deposited material was found to have a ratio of Al:O of 0.65 which is within 2% of the correct stoichiometric ratio. This can be seen in figure 2.7.

The sputtered alumina was patterned via a liftoff process. Initially the sample was placed in an acetone bath, which swelled the PMMA and cracked the alumina layer. The PMMA was then dissolved in dichloromethane leaving the alumina disks that were deposited into the holes in the PMMA layer. The alumina has exceptional adhesion to silicon and lift-off can be done with sonication or scrubbing via q-tip without worry of scraping off the mask. A set of 150 nm diameter

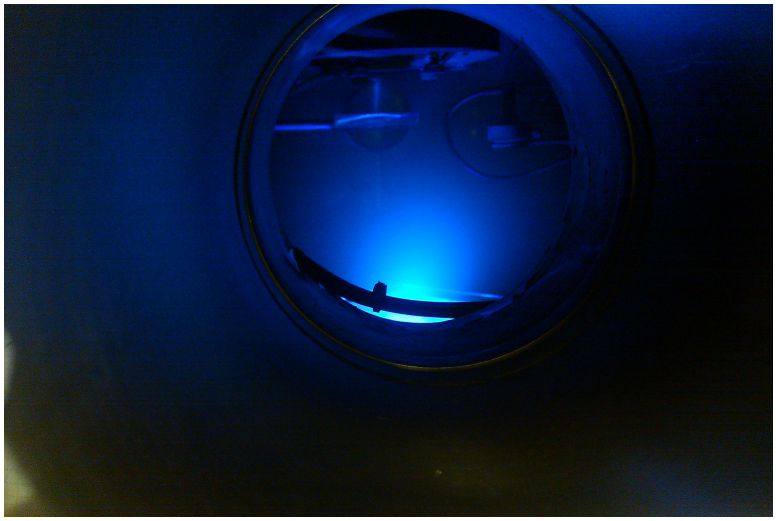


Figure 2.6: Picture of sputtering chamber during aluminum oxide deposition. The deep blue color of the plasma is correlated with the deposition of stiochiometric alumina.

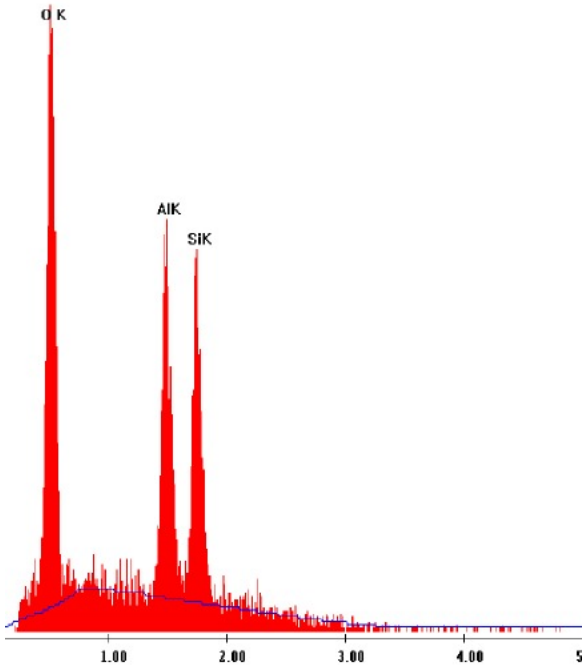


Figure 2.7: EDAX spectra for deposited reactive sputtered alumina on silicon. Note the relative signal intensity of the aluminum to the oxygen matches the 2:3 stoichiometric ratio.

alumina disks is shown in figure 2.8.

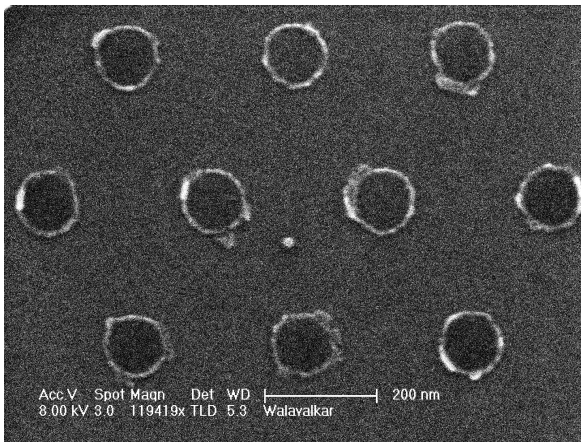


Figure 2.8: SEM image of 150 nm diameter alumina disks left after lift-off. The non-uniformity of the disks comes from the polycrystaline nature of the alumina.

2.4 Etching

Samples were etched in an Oxford Plasmalab 380 ICP-RIE. Figure 2.9 shows a schematic view of the inside of two types of etching chambers. In a standard RIE (frame (a) in 2.9) a plasma is created between an anode (usually the chamber walls) and a cathode (the plate on which the sample sits). The anode is grounded and the cathode has a capacitor to store charges. When a plasma is struck by the RF field electrons are torn from the gas and are swept alternatively towards the anode and cathode, and are stored in the capacitor on the cathode. Ions, being several times more massive, are not moved by the rapidly oscillating field (usually at 13.56 MHz) and are attracted by the DC field set up by the stored electrons on the capacitor in the cathode. These ionized gas species get accelerated towards the sample and the energy given to these ions is known as the 'forward power' of the etch. These ions can serve to both physically and chemically etch the sample. The power delivered to the plasma determines the amount of ionization as well as the DC bias voltage between the plasma and the cathode (sample). Furthermore, the amount of ionization governs the number of available ions for etching, the greater the ionization the greater number of ions are flung at the sample. The DC bias voltage is the potential used to accelerate the ions towards the sample; more power delivered to the plasma means more kinetic energy given to the etching ions (forward power). Therefore if one wanted to increase the number of ions delivered to the sample one would be required to increase the forward power as well, since the two characteristics are linked. In an ICP-RIE (frame (b) in 2.9) an inductor is wrapped around the chamber to create a magnetic field to deliver power directly to the plasma; this power increases the amount of ionization in the plasma without requiring

an increase in forward power. Therefore, with an ICP-RIE one has independent control over both the number ions delivered to the sample as well as the kinetic energy imparted to the ion.

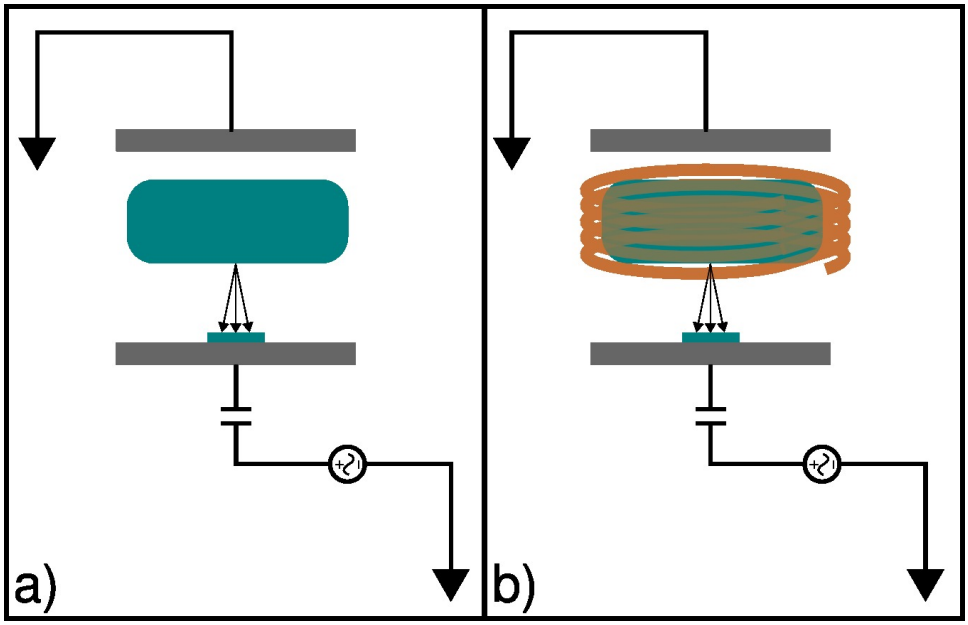


Figure 2.9: Schematic of an RIE (a) and an ICP-RIE (b) etching chamber.

In order to etch silicon nanopillars we utilized an SF_6 and C_4F_8 gas chemistry for etching and passivation, respectively. The etching gas in this case is the SF_6 which, when ionized, reacts with silicon to produce the volatile gas SiF_4 which diffuses away from the sample. This dual gas process has been termed a 'pseudo-Bosch' etch, since it is a variation of the original Bosch deep RIE etch. In the inductively coupled plasma the extra power delivered by the magnetic field is used to tear apart C_4F_8 into chains of fluorinated carbon, which are deposited uniformly on the sample. Simultaneously the fluorine from the SF_6 is accelerated towards the sample by the bias between the plasma and the sample. Since these ions are primarily directed in the downward direction they mill the fluorinated carbon coating on horizontal surfaces away and begin to etch the underlying areas of silicon that are not masked, while leaving the coating on vertical surfaces virtually untouched. This sidewall passivation is the key element that allows us to etch pillars with aspect ratios as large as 60 and with diameters as small as 25 nm; it is represented in figures 2.1 and 2.10 in light green. An example of this etch can be seen in figure 2.11; note the vertical side walls and uniformity in size of pillars. These pillars have an aspect ratio of 20; for comparison, the Washington Monument has an aspect ratio of 10. Figure 2.12 shows the density that can be achieved with patterned pillars. Figure 2.13 shows the ability to repeatedly write specific patterns of pillars at well defined distances from alignment marks so that future processing steps could be done solely with optical lithography.

The pillars fabricated by this method are the simplest manifestations of our silicon nanostructur-

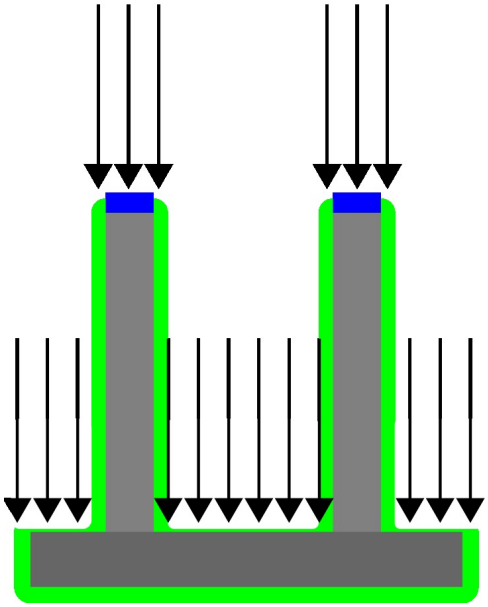


Figure 2.10: Location of C_4F_8 passivation removal by vertically directed SF_6 plasma species.

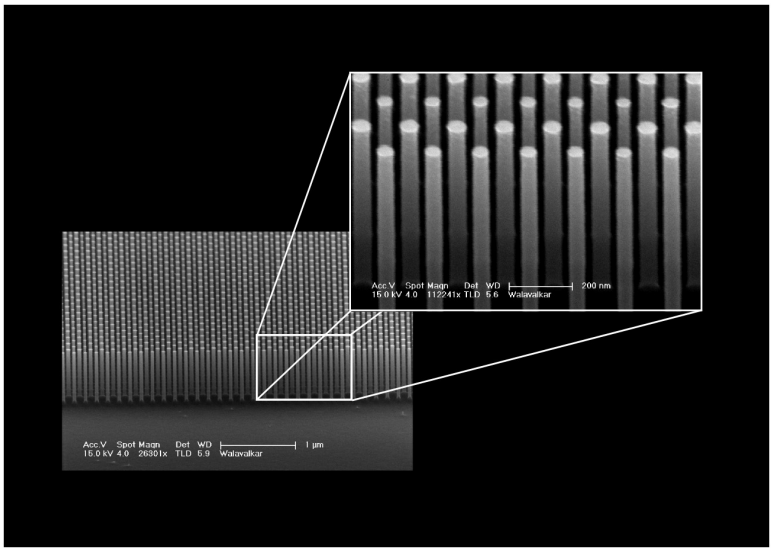


Figure 2.11: SEM images of 50 nm diameter pillars etched to a height of 1 micron.

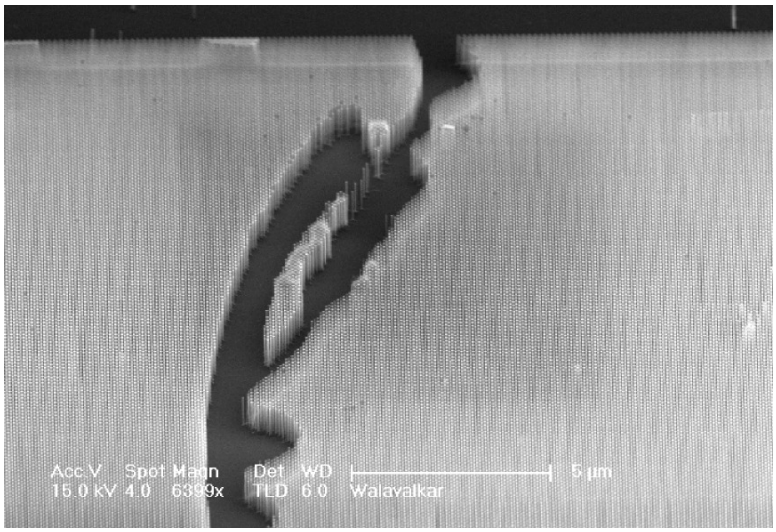


Figure 2.12: SEM images of a 50 nm diameter pillar array. Note the possible density and uniformity of pillars. The large 'feature' in the middle is an errant tweezer mark.

ing. Variations and modifications to this fabrication, to be covered in the following chapters, allow for the exploration of interesting mechanical, optical, and electronic properties of nanometer scaled silicon structures.

2.5 Failure modes

It is important to note that while fabrication yield eventually approached 100% there were some failure modes that had to be overcome in the beginning. Initially the PMMA for e-beam patterning was a 75 nm thick layer of A2 950. This thin layer had problems during the lift-off stage as the conformal coating of alumina as well as the narrow resist layer made it difficult for the solvent to dissolve the PMMA. An example of an incomplete lift-off is shown in frame (a) of figure 2.14. When such a sample is etched the alumina layer that remains between the pillars masks the etch resulting in a solid block of silicon instead of silicon pillars (figure 2.14 (b)). This problem was solved by increasing the PMMA layer thickness to 100 nm as well as using a more aggressive lift-off procedure utilizing q-tips and sonication; the adhesion of the alumina to the silicon allowed for such techniques to be used. Care had to be taken to ensure that flakes of aluminum oxide that had been removed did not re-deposit onto the sample. A combination of poor lift-off and re-deposition is seen in figure 2.15. Sonication, scrubbing with a q-tip, and constant flushing of solvent were required to prevent the re-deposition of alumina flakes.

When the aluminum sputter target became depleted or contaminated it would result in the deposition of a weaker, metal-rich, alumina mask. Figure 2.16 shows a pad of pillars after etching

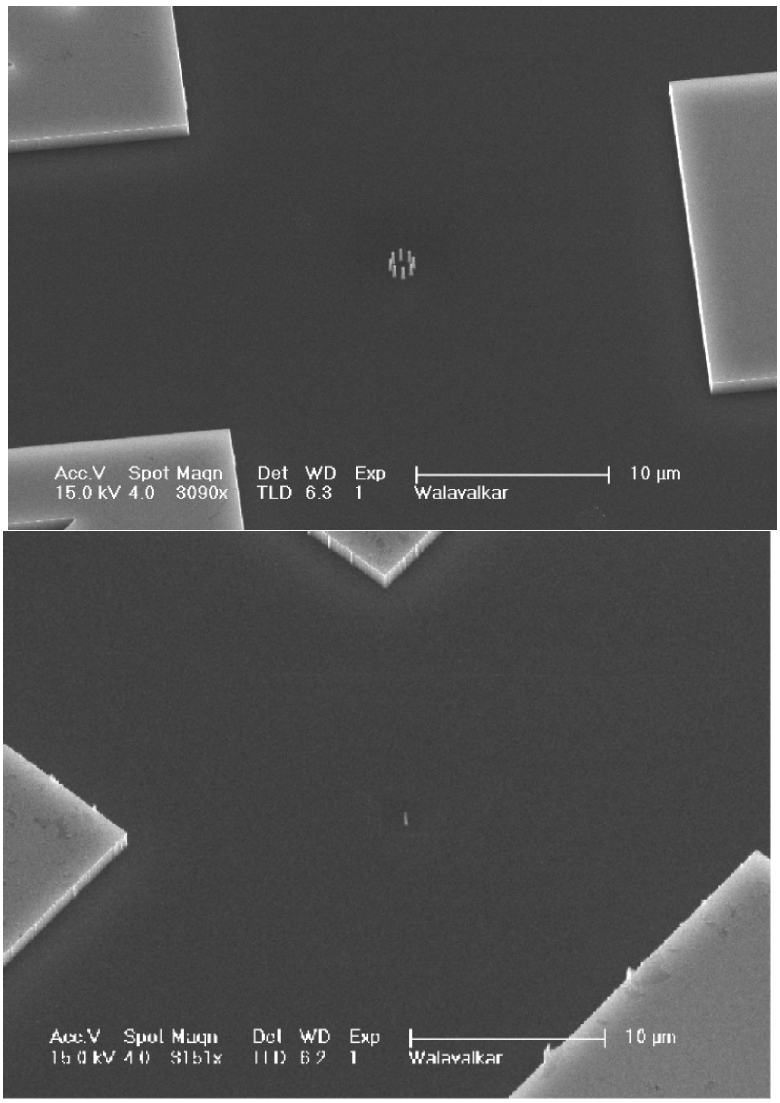


Figure 2.13: SEM images of a precisely placed single pillar and ring of pillars. These images show the benefit of utilizing electron beam lithography as it allows for the patterning of specific structures in specific locations. Large structures are alignment marks for the optical lithography used to contact these structures.

using a sub-standard alumina mask. The relative heights and shapes of the pillars can give insight into how fast and in what manner the mask eroded. For example a squat cylindrical pillar would indicate that the mask failed uniformly after etching to the height of the pillar and then the etch continued down uniformly. A pillar with a spire would indicate that while most of the mask eroded a flake of alumina managed to continue to mask the etch.

Since the condition of the machines used to develop the etch for these nanopillars was in a constant state of flux due to their recent installation occasionally the recipe had to be tweaked to take into account the chamber condition. Figure 2.17 shows a set of pillars that were undercut due to under-passivation. The corrugation appears due to the lateral etching allowed by the stochastic breakdown of the side-wall passivation. The pseudo-bosch etch was sensitive to the coating and conditions of the chamber walls; typically before an etch the chamber should have been conditioned to stablize the state of the system. Figure 2.18 shows an etch that was done in an unconditioned chamber; the change in diameter as the etch proceeded downward was due to the change in chamber conditions during the etch.

It will be shown in future chapters that these silicon nanopillars are incredibly flexible, however when bent by the meniscus force of drying water they can easily snap at the base. Figure 2.19 shows a pad of pillars after etching and processing with water; the pillars are bent together by the drying water and remain stuck due to Van der Waals forces. Figure 2.20 shows the remnants of an array of pillars after they were snapped due to the cohesive force of water. This problem could be solved by using a critical point dryer to remove the water without causing stiction or by increasing the rigidity of the nanopillars by thermally growing a layer of silicon dioxide.

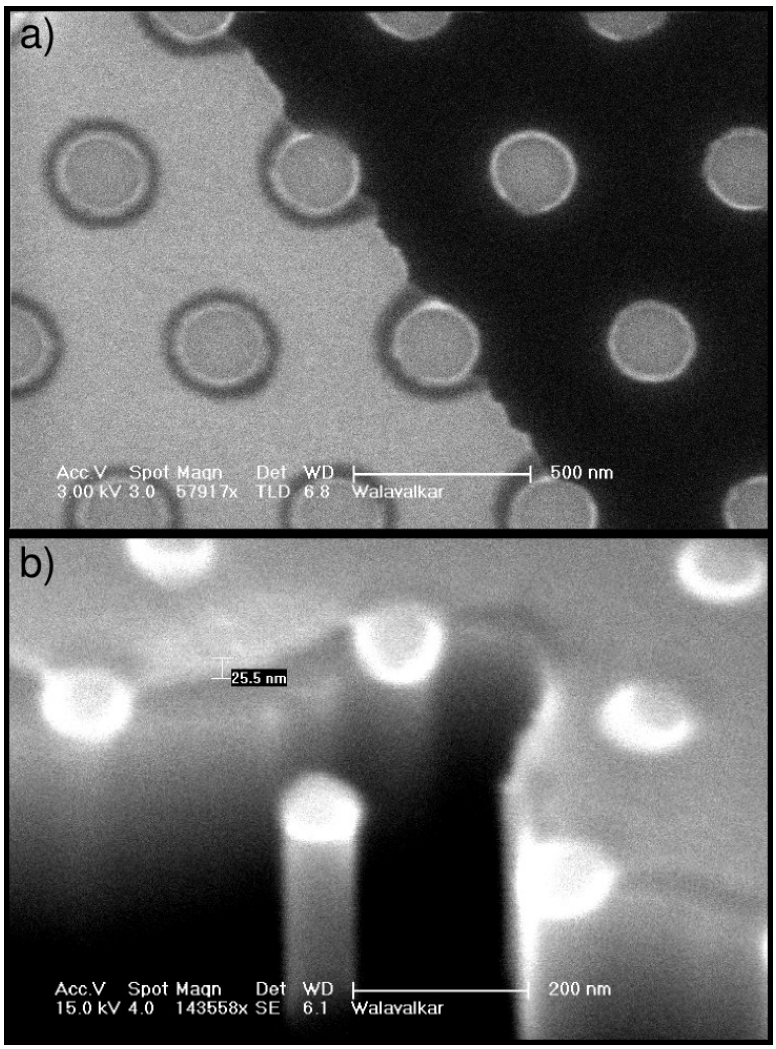


Figure 2.14: a) Incomplete lift-off of alumina due to thin PMMA b) Resulting etch of structure showing the alumina masking unintended regions

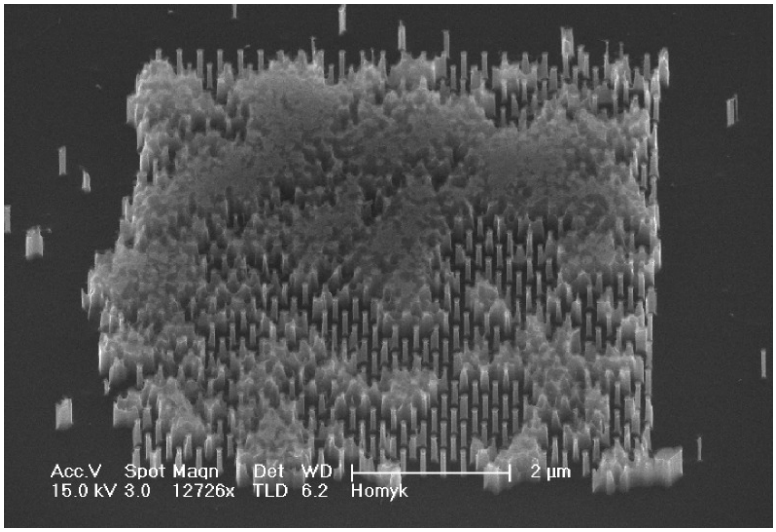


Figure 2.15: Incomplete lift-off of alumina results in clumps and islands instead of pillars. This was remedied by using a thicker e-beam resist and sonicating the sample in dichloromethane.

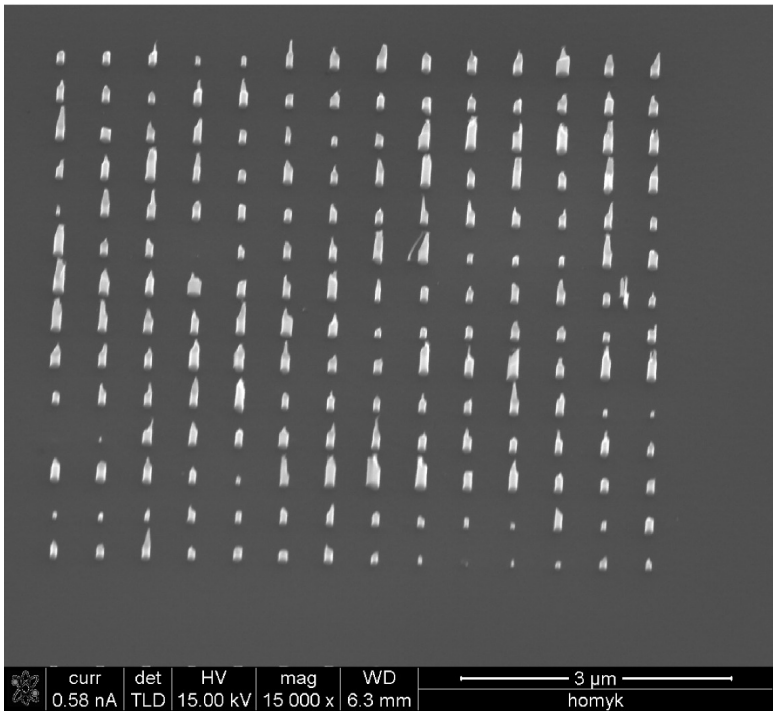


Figure 2.16: Pad of pillars imaged after mask failure during the etch. The relative heights and shapes of the pillars can give insight into how fast and in what manner the mask eroded.

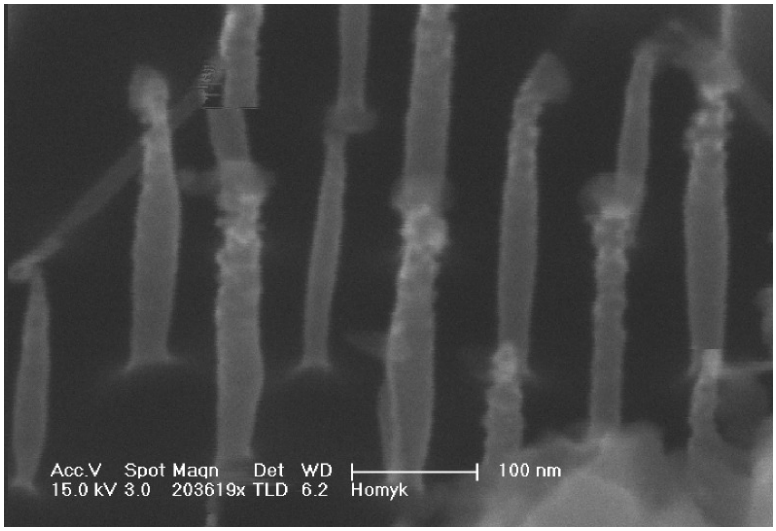


Figure 2.17: Undercut sample due to under-passivation. The roughness comes from the stochastic breakdown of the side-wall passivation.

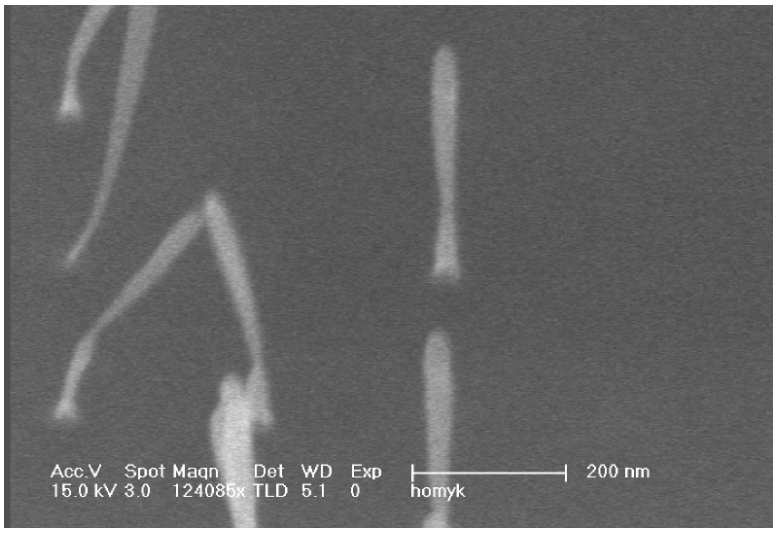


Figure 2.18: Example of an etch performed in an unconditioned chamber. The diameter variation with pillar height shows how the chamber conditions changed during processing and affected the properties of the etch.

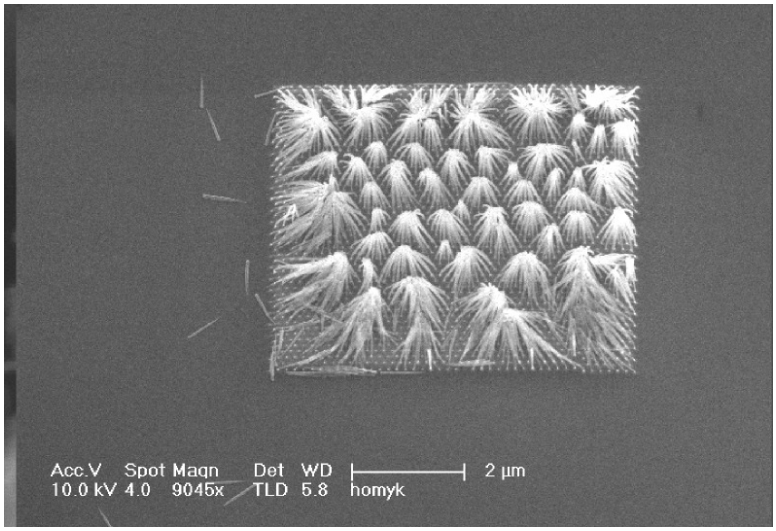


Figure 2.19: Pad of pillars after wet processing with water. The meniscus force pulled sets of pillars together and they are held in place by Van der Waals forces.

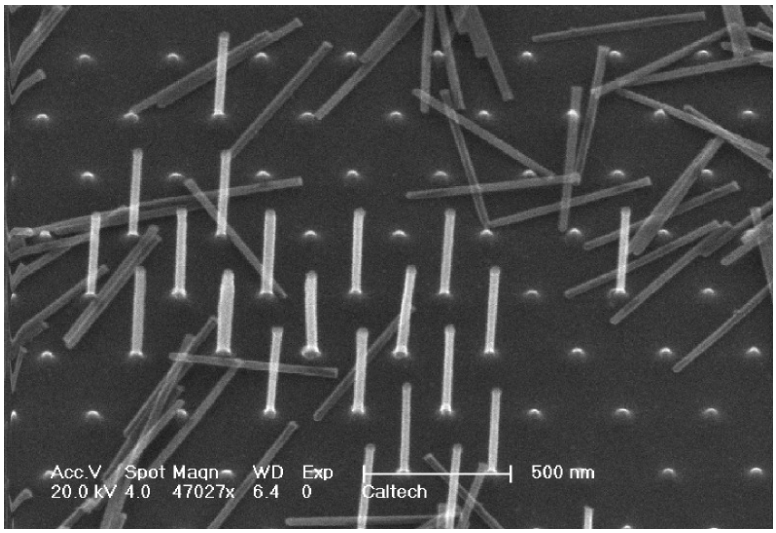


Figure 2.20: Remnants of an array of pillars after wet processing. Note that the pillars break consistently at their contact points with the substrate; this is where the maximum strain is found.

Chapter 3

Oxidation and characterization

Silicon thermal oxidation is a field that has been studied in great depth. Most studies have been done with respect to planar oxidation, which plays a critical role in growing gate and field oxides for MOSFETs. When we began to study the oxidation of the three dimensional structures fabricated in this work, we found an interesting feature not seen in planar oxidation. When convex silicon structures are oxidized the strain created from forcing more oxygen atoms into the lattice actually builds to a point that the oxidation self-terminates. We exploited this feature to controllably thin down our etched pillars to diameters as small as 2 nm; in most cases we did not bother to remove the oxide as it provided structural support for the silicon whisker held inside. In order to characterize the oxidation behavior we relied on a non-destructive, reflection mode TEM measurement to see the silicon core inside the oxide sheath. This section will cover our characterization methods, self-terminating oxidation, and our successful attempts to reduce the width of nanopillars to the order of the electron deBroglie wavelength.

3.1 Reflection mode TEM

Typically TEM measurements of nanowires or nanopillars are conducted by snapping the wires off the substrate and then casting them onto a TEM grid[4]. This method, while effective, is destructive to the sample and randomizes the orientations and positions of the nanowires. We chose, instead, to perform our TEM analysis non-destructively while the pillars were still on the original sample, using reflection mode TEM (RTEM).

The standard setup for a TEM measurement has the beam of electrons pass through a grid, containing samples, that is mounted perpendicular to the beam path. In RTEM the sample is mounted parallel to the beam path such that the features on the surface protrude into the path of electrons (figure 3.1). For clarity figure 3.2 shows the view from the detector of the sample and holder. Using this technique we were able to view and measure samples before and after oxidation to characterize the oxidation process.

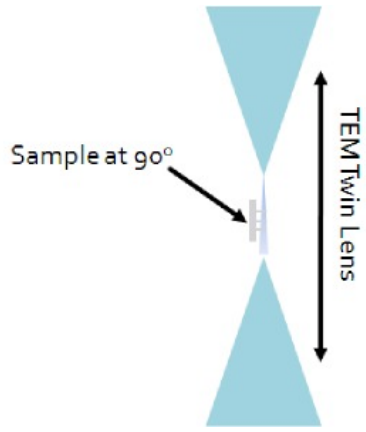


Figure 3.1: Schematic of RTEM sample setup

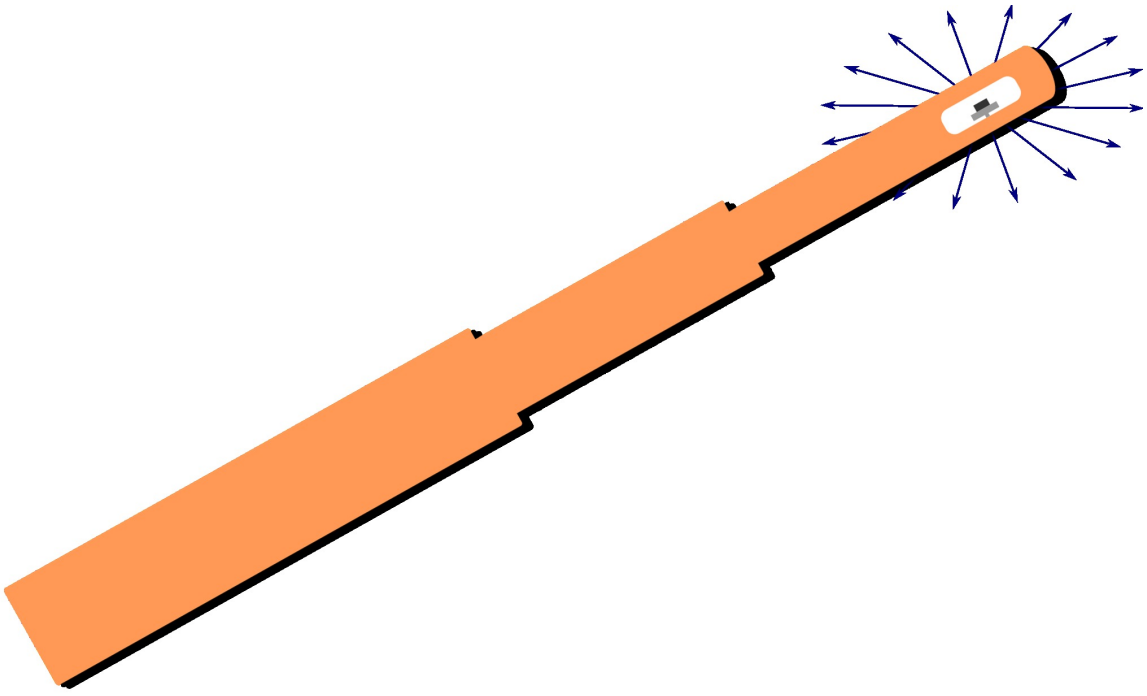


Figure 3.2: Point of view from the detector of the sample and TEM holder.

So that the electron beam has a relatively unhindered path through the pillars and to the detector the sample is mounted such that the beam traverses the pad of pillars at a 45^o angle. The path of the beam is represented in the top frame of figure 3.3 as a blue arrow. The resulting RTEM image is shown in the bottom frame of figure 3.3. Note that the ringed, brightness variations are from the lattice of the single crystal silicon diffracting the electrons.

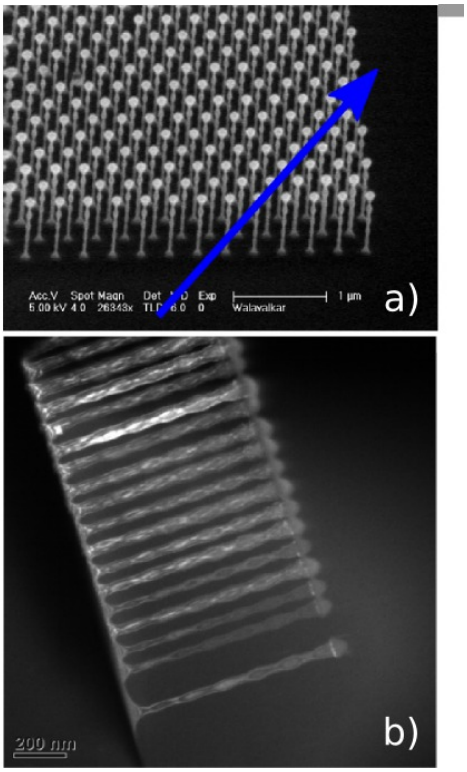


Figure 3.3: a) SEM view of a pad of corrugated nanopillars. The blue arrow represents the intended path of the electron beam in the TEM. b) RTEM image of the same pad of pillars.

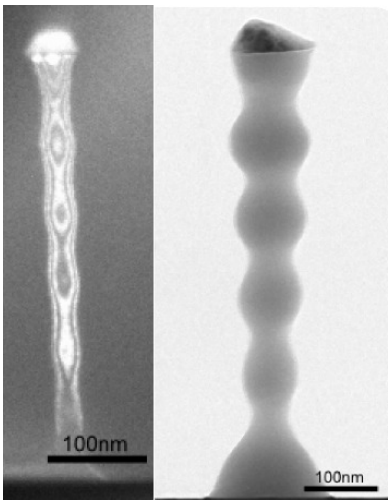


Figure 3.4: RTEM image of corrugated pillars before and after oxidation. Note that in the pre-oxidation image it is possible to see the electron diffraction from the single crystal silicon as bright fringes; in the post oxidation image the fringes disappear as the silicon dioxide is amorphous.

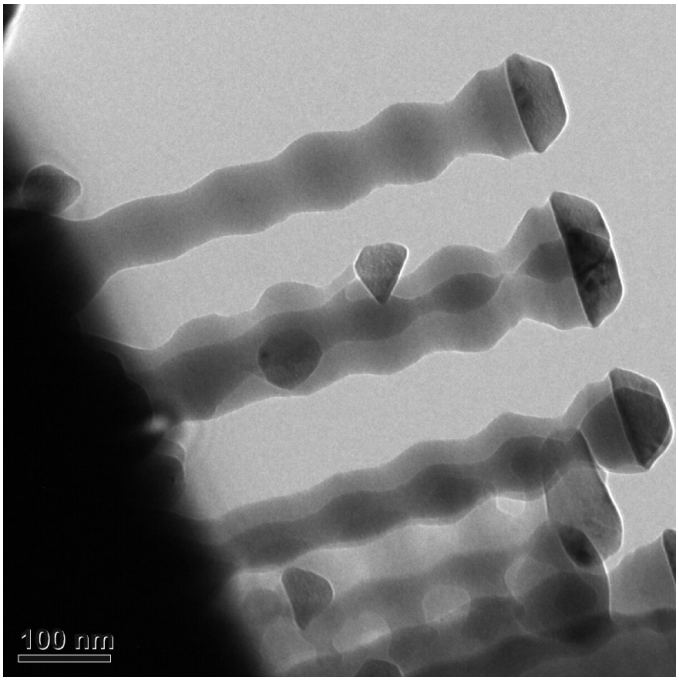


Figure 3.5: RTEM image of an array of corrugated pillars after oxidation.

An example of a dark-field RTEM image is shown in figure 3.6. This image was taken along a corner of a close-packed array – making the pillars appear to stand in distinct rows. In order to measure the crystaline cores of the nanowires after an oxidation step we utilized diffraction contrast to light up the single crystal silicon while leaving the oxide relatively dim. This effect is shown in figure 3.7 as the contrast between the cores and cladding of the pillars.

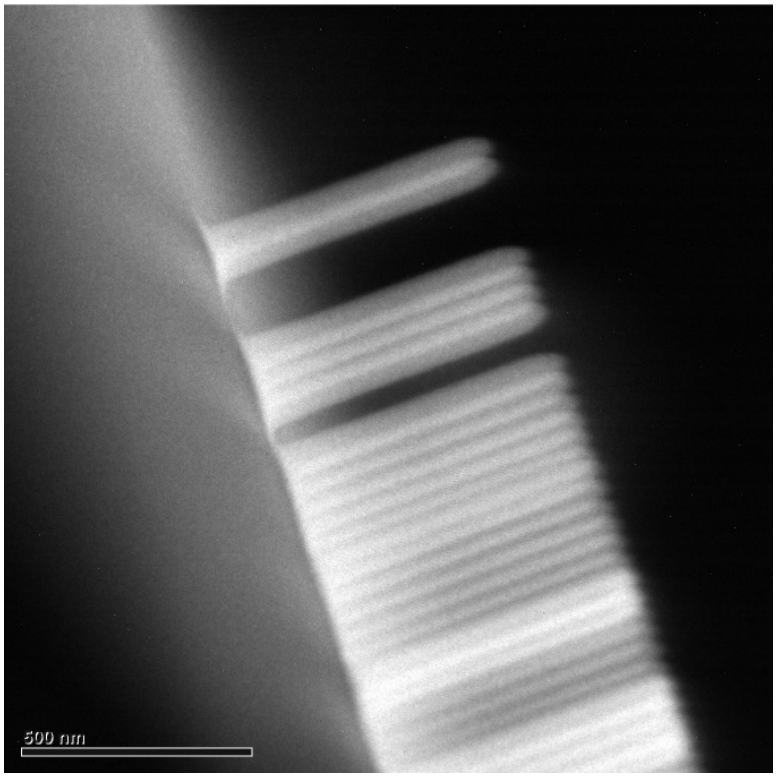


Figure 3.6: Dark-field RTEM image of an array of oxidized silicon pillars.

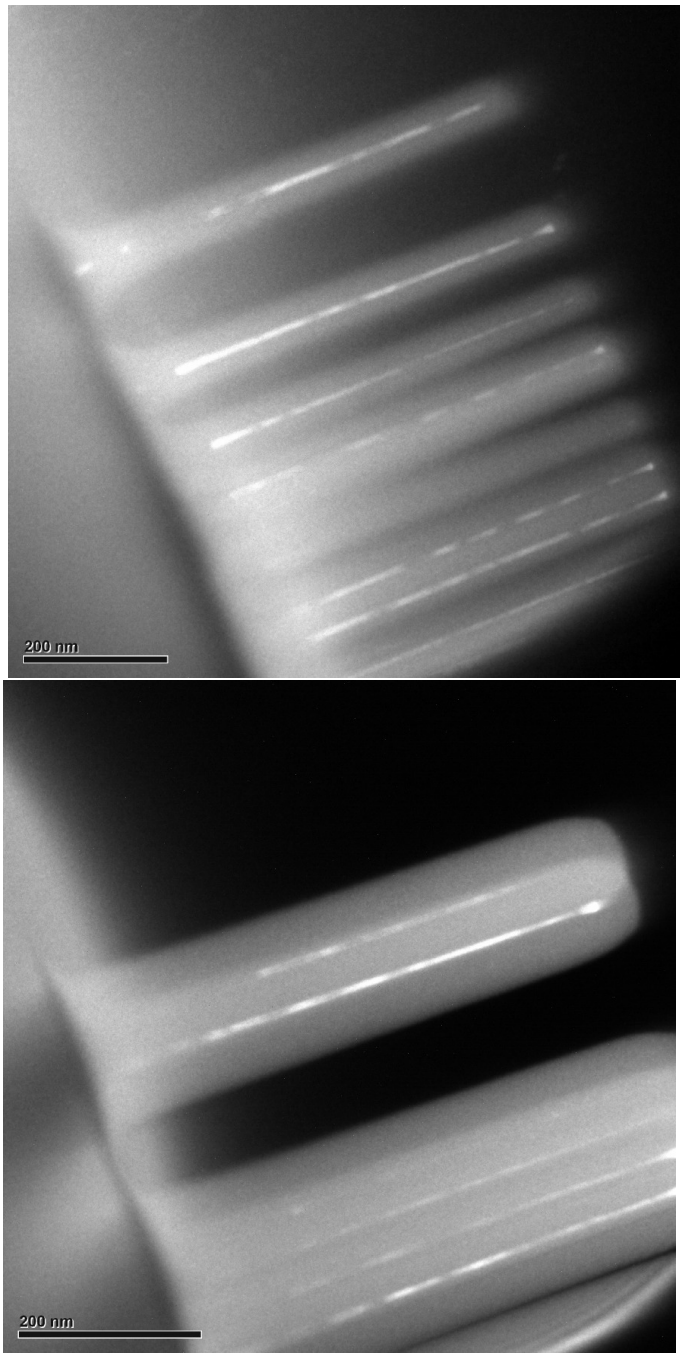


Figure 3.7: RTEM image of an array of oxidized silicon pillars with the crystaline silicon in white and the oxide sheath in dull grey.

3.2 Two-dimensional oxidation

3.2.1 Planar oxidation

The planar, one-dimensional model of silicon thermal oxidation was originally presented by Deal and Grove in 1965[16]. The model was based on the physical picture of oxidants diffusing through the existing oxide to grow new layers of oxide at the Si-SiO_2 interface. Therefore there were three critical parameters that determined the oxidation rate: the diffusivity of oxidants in the oxide D, the solid solubility of oxidants in the oxide C^*, and the surface reaction coefficient k_s[17]. For convenience the symbols and diagrams will be defined as found in *Kao et al. and Deal et al.*[17, 16] as the derivations follow those presented in those papers.

The planar model proposed by Deal and Grove is shown in figure 3.8; in steady state the three labeled fluxes are equal. Specifically, the flux from the gas to the oxide is equal to the flux through the oxide; this in turn is equal to the rate at which the oxidants are converted to silicon dioxide. Fick's law gives the flux of oxidants across the grown oxide:

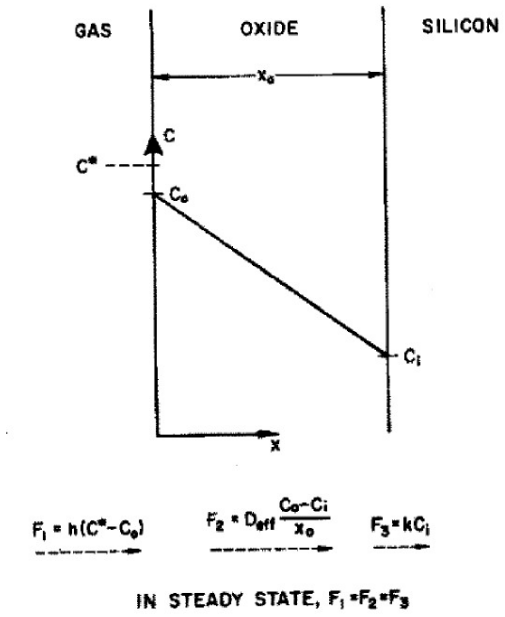


Figure 3.8: Steady-state, planar oxidation schematic proposed by Deal and Grove

$$F_2 = -D\frac{dC}{dx}, \tag{3.1}$$

where D is the diffusivity and dC/dx is concentration gradient of oxidants in the grown oxide between the gas interface to the silicon interface. From the steady state assumption F_2 must be constant across the oxide and therefore the concentration gradient must be linear; from the diagram we can

write:

$$F_2 = D\frac{(C_o - C_i)}{x_o}, \tag{3.2}$$

with the labels corresponding to figure 3.8. In steady state we make one further assumption; the diffusivity is small compared to the gas phase transport coefficient (h) and the oxidation rate (k_s). In this case, the concentration of oxidants at the Si-SiO_2 drops to zero and the concentration of oxidants in the gas phase is equal to the concentration of the oxidants at the gas/oxide interface. In this 'diffusion controlled' regime it is possible to write the flux as:

$$F_1 = F_2 = F_3 = \frac{kC^*}{1 + k/h + kx_o/D}. \tag{3.3}$$

This flux can be re-cast as a differential equation that determines the 'velocity' of the oxidation front. For N oxidants incorporated per unit volume of oxide:

$$\frac{dx_o}{dt} = \frac{F}{N} = \frac{C^*/N}{1/k + 1/h + x_o/D}. \tag{3.4}$$

It is from this equation that Deal and Grove formulated their linear/parabolic oxidation model. In the regime of a thin oxide $x_o \sim 0$ the growth of the oxide front is depends linearly on the rate constants. Once a thick oxide has been grown ($kx_o/D \gg k/h$) the oxidation is determined by the rate of oxidant diffusion, transitioning to a parabolic rate.

3.2.2 Oxidation of convex silicon structures

The oxidation of a convex, two-dimensional silicon structure can be modeled in a similar way. For this model the oxidation is based only on geometry and not crystal orientation, i.e. the oxidation rate k_s is considered to be constant and not vary with crystal orientation. The schematic can be seen in figure 3.9; as, with the planar model, the oxidation is at steady state. We can cast Fick's

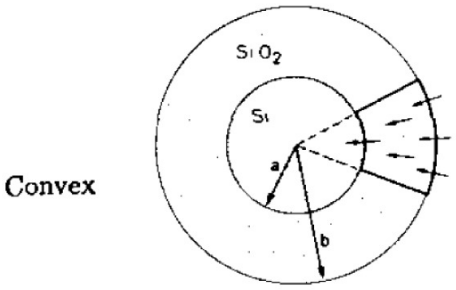


Figure 3.9: Cylindrical oxidation schematic of a convex silicon structure proposed by Kao et al.

second law in cylindrical coordinates, noting the steady state condition:

$$\frac{\partial C}{\partial t} = D\nabla^2 C = D\frac{1}{r}\frac{\partial}{\partial r}(r\frac{\partial C}{\partial r}) = 0. \tag{3.5}$$

Assuming symmetry around the circumferential direction and no variation in the z direction due to a 'long' cylinder, the solution to the Laplace equation in cylindrical coordinates is of the form:

$$C(r) = A + B\ln r, \tag{3.6}$$

where the coefficients are determined by the flux at the gas/oxide and oxide/silicon interfaces. The flux at the gas/oxide interface is:

$$D\frac{\partial C}{\partial r} = h(C^* - C). \tag{3.7}$$

The flux at the Si-SiO_2 interface is:

$$D\frac{\partial C}{\partial r} = k_s C. \tag{3.8}$$

Using a to represent the radius of the silicon core and b to represent the radius of the grown oxide the full solution is:

$$C(r) = \frac{C^* abhk_s}{abhk_s \ln(b/a) + Dhb + Dk_s a} \cdot \left(\frac{D}{ak_s} + \ln\frac{r}{a}\right) \tag{3.9}$$

To determine the 'velocity' of the oxidation front we find C(a) i.e. the concentration of oxidants at the Si-SiO_2 interface. As with equation 3.4 we can write the oxidation rate as:

$$\frac{dx_o}{dt} = \frac{1}{N}k_s C(a) = \frac{C^*/N}{1/k_s + (1/h)(a/b) + (1/D)a\ln(b/a)} \tag{3.10}$$

where $x_o = b - a$. When we compare the rates in figures 3.4 and 3.10 we can see that at the outset of oxidation, where x_o is small, that both the Deal-Grove and the cylindrical oxidation revert to a reaction rate (k_s) limited regime. As the oxidation progresses we must consider the contribution of the coefficient of the diffusivity term. In 3.4 this term scales linearly with x_o and in 3.10 this term scales as $a\ln(\frac{b}{a}) = a\ln(1 + \frac{x_o}{a})$. For a given silicon core radius a, the coefficient of the diffusion term in 3.10 scales sub-linearly with increasing oxide thickness, implying that the oxidation of a convex structure remains dominated by the surface reaction rate. Since a convex surface supplies more oxidants than a planar surface [17], simply considering the theoretical oxidation rate, convex structures should oxidize faster and maintain a faster oxidation rate than a planar sample. For short time-scales of oxidation this holds true, however, as the oxidation time increases it is found that the oxidation of a silicon pillar proceeds *slower* than planar oxidation.

Figure 3.10 (a)[18] shows a plot measuring the oxide thickness vs. oxidation time of etched

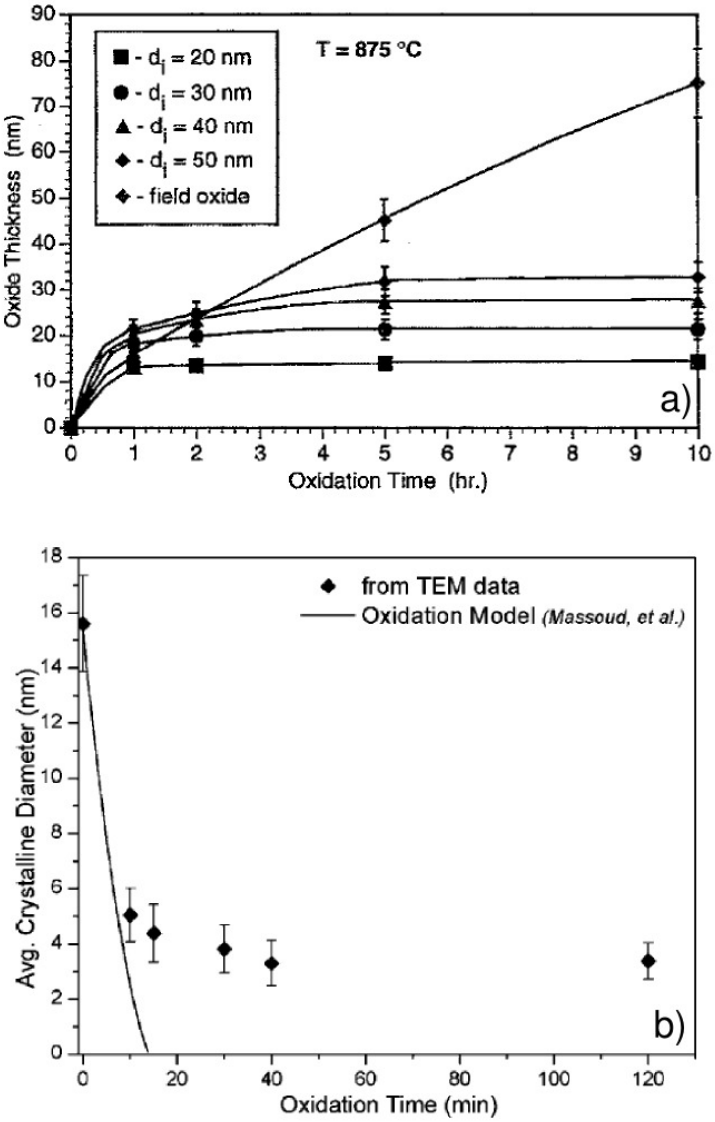


Figure 3.10: a) Oxidation thickness vs. time from *Liu et al.* Note that the oxidation rate is faster for the convex samples for the first hour and then slows and saturates as the oxidation time progresses. b) Remaining core diameter vs. oxidation time from *Guichard et al.* Note that this oxidation was done at 950 ^{o}C hence the decrease in core size saturated quickly as compared to the oxidation at 875 ^{o}C in frame a).

silicon nanopillars at 875 ^{o}C. From the data it is seen that the oxidation of the convex structures proceeds faster for the first 1-2 hours than the planar oxidation; after that time the oxidation slows and saturates, remaining unchanged between 5-10 hours. Similarly, figure 3.10 (b)[19] shows the shrinking of the silicon core diameter vs. oxidation time in grown silicon nanopillars. This oxidation was performed at 950 ^{o}C and the theoretical planar oxidation out-paces the convex oxidation within 20 minutes.

Published data[18, 20] has shown a few key characteristics of the self-terminating oxidation. The final diameter of the silicon core in the oxidized nanopillar depends on both the initial pillar diameter and the temperature of the oxidation. The fact that no self-terminating behavior was seen above 960 ^{o}C and pillars were completely oxidized indicates that the limiting behavior may have to do with the viscoelastic flow of glass. At temperatures greater than 960 ^{o}C glass can flow to abate the strain incorporated into thermal oxide due to the volumetric expansion between the Si and SiO_2. Below 960 ^{o}C the strain due to the incorporation of oxygen into the silicon lattice continues to build and build. Several mechanisms have been proposed to explain the self-limiting oxidation behavior of silicon nanopillars; the two most viable both focus on the impact of the interfacial stress at the Si-SiO_2 boundary. *Liu et al.* explain the strain as being kinetically limited[18] such that it is no longer energetically favorable to continue to oxidize against strain at the interface. This explanation runs into trouble when estimates of the energy cost of turning Si into SiO_2 are more than two orders of magnitude smaller than the 9 eV gained in the exothermic oxidation[18, 21]. *Cui et al.* proposed that the large strain concentrated at the Si-SiO_2 interface creates a thin, dense layer of oxide which prevents oxygen diffusion to the oxidation front. Their claim, backed by molecular dynamics simulations[22], is that a 1 nm thick layer of amorphous SiO_2, with a maximal density of 2.7g/cm^3, provides an Arrhenius type energy barrier ($D \simeq D_o \exp E_b/kT$) to oxygen diffusion that increases based on the ratio of b/a (oxide to silicon diameter). Consequently, as the strain energy increases the 'velocity' of the oxidation front (3.10) drops off exponentially[21]. While the exact mechanism of the self-terminating oxidation has not been determined the effect is well characterized and easily tunable.

3.3 Oxidation for this work

Oxidation for this work was carried out in a Thermco 'Black Max,' three-zone, 4 inch, tube furnace. The furnace was calibrated with a five foot long, tungsten thermocouple to ensure flat and accurate temperature control over the three zones. Oxidation was carried out in a pure, dry, oxygen ambient using ultra high purity (UHP) oxygen. When anneals were required they were performed either in the same furnace during the cool down portion of the run or in a separate Thermco 'Mini Brute', 4 inch, tube furnace; these anneals could be done in a nitrogen or forming gas (5% H_2/95% N_2)

atmosphere. Specific details concerning the oxidation in each project will be found in the chapters describing the project. Figure 3.11 shows two examples of self-terminating oxidation; one of etched pillars and one of etched corrugated pillars, terminating in a quantum dot.

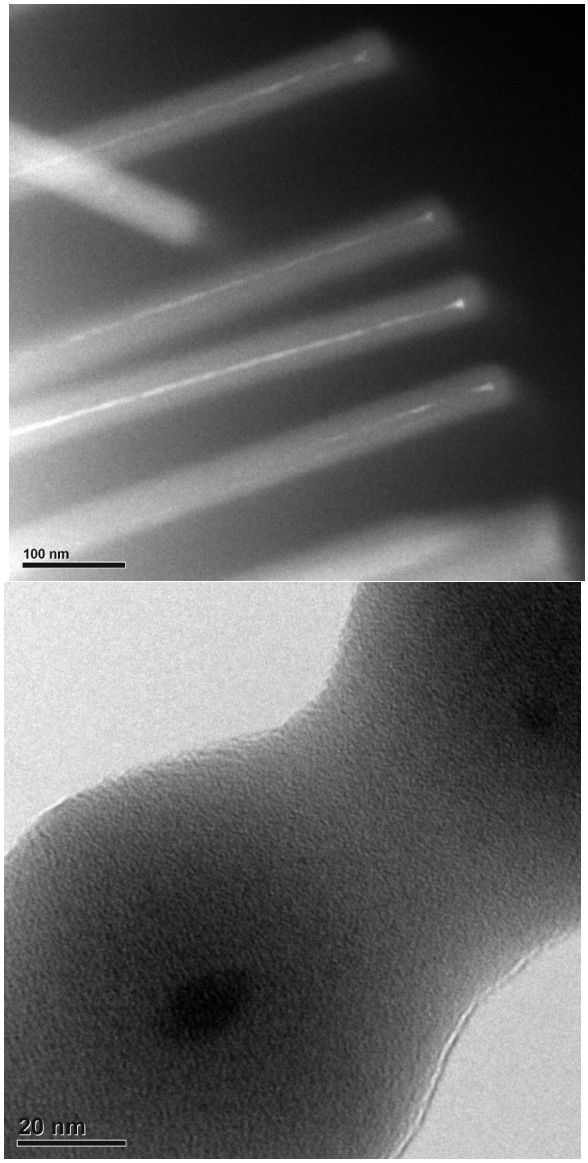


Figure 3.11: REM images of self-terminating oxidation of etched pillars(top) and quantum dots(bottom).

Chapter 4

Mechanics

Fabricated silicon nanostructures demonstrate mechanical properties unlike their macroscopic counterparts. Here we use a force mediating polymer to controllably and reversibly deform silicon nanowires. This technique is demonstrated on multiple nanowire configurations, which undergo deformation without noticeable macroscopic damage after the polymer is removed. Calculations estimate a maximum of nearly 24% strain induced in 30 nm diameter pillars. The use of an electron activated polymer allows retention of the strained configuration without any external input. As a further illustration of this technique, we demonstrate nanoscale tweezing by capturing 300 nm alumina beads using circular arrays of these silicon nanowires.

4.1 Nanopillar deformation

The physical manipulation of objects at the nanoscale has been a huge area of inquiry. There have been several attempts to scale successful MEMS technology down to nanometer length scales and directly apply it to manipulate nanostructures. Some of these methods include electrostatic actuation, magnetic actuation, and thermal (bimorph) actuation. Unfortunately these techniques run into a host of problems when they are scaled down in size. Addressing individual nanostructures is difficult as it requires precise alignment and even with precise electron beam lithography, accuracy to within 30 nm is prohibitive. Forces used to actuate structures also scale with decreasing size. For example, the force on a magnetic structure by a fixed field is[23]:

$$F_m = V_m \Delta\chi \nabla(\frac{\mathbf{B}^2}{2\mu_o}). \tag{4.1}$$

Where $\Delta\chi, \mathbf{B}, V_m$ are relative differences of the succpetability, the fixed magnetic field, and the volume of the magnetic structure, respectively. If, for simplicity, we assume this structure is a sphere then for every decrease in the order of magnitude of the radius there is a corresponding decrease of a factor of 1000 in the force. Similarly it is difficult to obtain more than 1-2^o deflection for a

bimorph actuator with a width of about 300 nm and an aspect ratio as large as 60[24]. Mechanical manipulation using electro-static actuation[25, 26] requires power to be continuously supplied to the device to maintain deformation.

Aside from the simple manipulation of objects at the nanoscale, mechanical deformation can serve as a way to incorporate strain into nanostructures. Static deformation methods—such as pseudomorphic growth—lack the ability to reversibly tune the amount of strain in the material once it has been patterned, and cannot achieve strain $> 2-3\%$[27, 28]. Given its influence on electronic as well as optical properties[29, 30, 28], methods to accurately control strain are becoming increasingly important in modern devices.

Finally, previous work has shown that nano-scale structures experience deformation differently than their bulk counterparts[31, 32, 33, 34, 35]. Specifically silicon nanowires can demonstrate yield strength as well as total strain much greater than bulk silicon[36, 37]. In two notable studies [38, 37] grown silicon nanowires were shown to have an elongation ratio of 125% and a maximum strain of 21.5% without failure. Furthermore previous efforts have utlized the length contraction of polymerization to apply significant forces to induce elongation, buckling and bending of silicon nanowires and carbon nanotubes[38, 37, 39]. However, common limitations shared by these approaches are the use of grown nanowires or nanotubes resulting in stochastically distributed structures [37, 39] as well as the permanence of the deformed position achieved by the nanowire or nanotube.

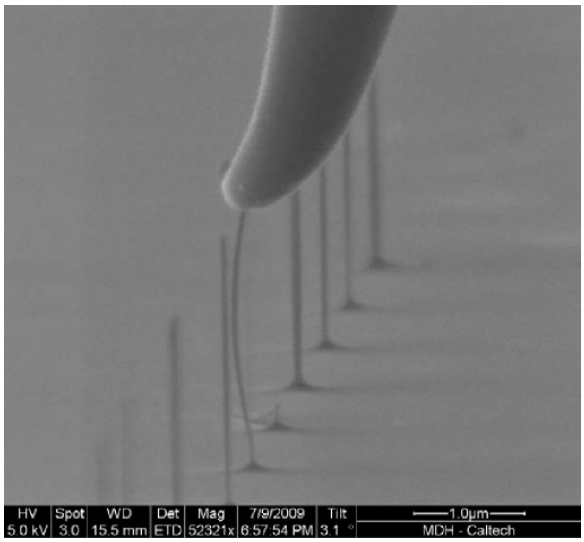


Figure 4.1: SEM image of an etched nanopillar deforming under a load applied with a probe tip. The pillar is 45 nm in diameter and 2.5 microns tall. (Photo courtesy of M. D. Henry)

4.2 Polymer-mediated deformation

We passively manipulated etched silicon nanowires using polymethylmethacrylate (PMMA) as a force mediating polymer. The force exerted by the PMMA on the nanowires may be tuned by varying the electron beam exposure, heating, and selective polymer removal, permitting controllable, as well as fully reversible, bending and straining of structures. Due to the stability of PMMA at room temperature, the nanowire configuration remains fixed, enabling further electrical or mechanical tests to be performed on the sample while under strain.

4.2.1 Application of polymer

The first step was to pattern the wafer with whatever structure we wanted to manipulate. We then spun on PMMA to slightly thicker than the desired thickness and baked at 180 ^{o}C for 5 minutes. The samples were then placed in an barrel asher, oxygen plasma for 1 minute at 100 W forward power to clean the PMMA off the sides of the pillars and ensure that the PMMA was planar. The thickness of the PMMA was measured with a Filmetrics F40 interference thickness measurement system. The pillars were not deformed by the application of the PMMA or during the baking process; PMMA reflows above 120 ^{o}C, thus relieving any strain applied during the spin process.

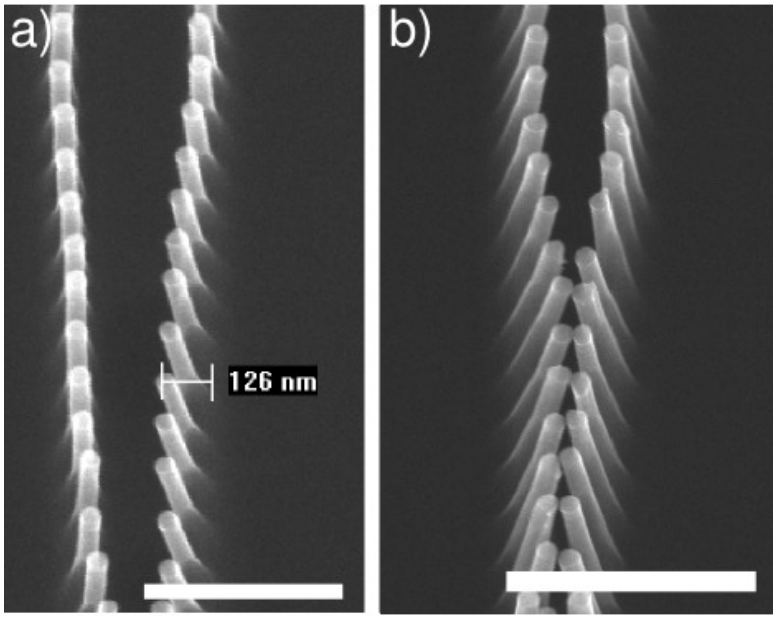


Figure 4.2: SEM images of rows of pillars protruding from planarized PMMA during actuation. Scale bar is 500 nm in a) and 1 micron in b).

4.2.2 Manipulation of polymer

PMMA has been widely used as a positive tone electron beam resist. The high-energy electrons used to pattern the resist remove a carbonyl group from the side of the main polymer back-bone, resulting in scission of the main polymer chain[40]. These shorter segments are more soluble in an appropriate solvent (such as 1:3 solution of methyl isobutyl ketone to IPA) and therefore develop away leaving the unexposed regions. In parallel to this process is a process of polymerization that produces a hard insoluble material. At low electron beam doses the scission process is dominant, however at high doses the polymerization process outpaces the scission allowing PMMA to be used as a negative resist[40].

This transition to a negative tone resist happens at about 10 times the dose used in electron beam lithography, roughly 10,000 $\mu C/cm^2$[41, 42]. Along with this change in resist tone, the cross-linking causes a volumetric contraction of the resist. By strategically exposing areas of PMMA covered chips it is possible to use this contraction to deform silicon structures. We utilize this contraction to selectively deform pillars; directional control is achieved using asymmetric electron beam exposure. An example of this can be seen in frame (b) of 4.2; the middle of the columns of pillars has been exposed, dragging the two rows together.

4.2.3 Deformation of silicon nanopillars

This section will highlight several examples of this actuation method.

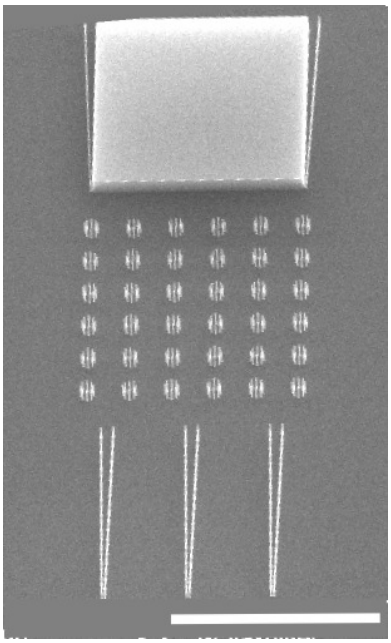


Figure 4.3: SEM images etched test pattern. This array was used to characterize the deformation caused by over-exposure of PMMA.

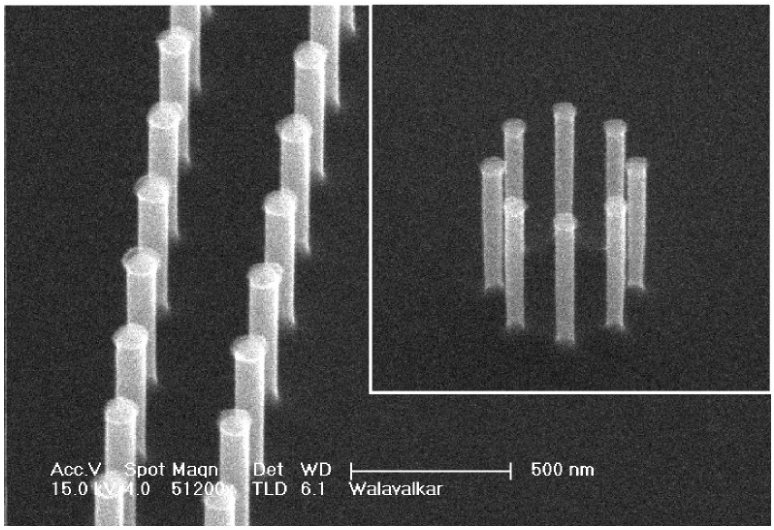


Figure 4.4: Magnified image of as-etched test pattern. The main image is that of the 'zipper' of pillars and the inset is a circular array of pillars. The scale bar is 500 nm for both.

Figures 4.3 and 4.4 show the structures that were used to characterize the properties of the polymer deformation. Several sets of these pillars with diameters from 30 nm to 150 nm were fabricated on the same chip.

Figure 4.5 shows two sets of 75 nm diameter nanowires emerging from a 300 nm-thick PMMA film. By exposing only the right hand set of pillars, cross-linking in this area pulls these pillars inwards while neighboring strips remain undeformed. The inset shows the comparison in more detail. We note that the bottom few pillars of both the right and left patterns have been brought together from the exposure of taking this picture. The length of exposure dictates the electron dose and hence the amount of contraction between pillars. Since this exposure is done in an SEM, we could view the progress of the deformation in real time, freeze exposures, take measurements and continue until a desired exposure was obtained. Using this process, it should be possible to obtain SEM resolution limited precision in the final deformation of the pillars. In a second experiment, we arranged rings of eight nanowires 75 nm in diameter and 800 nm tall (4.6). The rings were initially 500 nm in diameter with 230 nm circumferential spacing between the pillars. The central region of the ring was exposed in an SEM, yielding a uniform radial deformation. Contraction terminated when the pillars were flush, with a final diameter of 184 nm after exposure. As shown in 4.7, we also exposed the inner region of a ring of 50nm diameter pillars that were 1μm tall. The ring started at 500 nm in diameter and contracted until the pillars were fully touching, giving a deformation distance at the tip of approximately 250 nm. By measuring the beam current and exposure time, we determined that a dose of approximately 10,000 μC/cm^2 is required to achieve full contraction of the pillars. This dose matches other results for that required to fully cross-link PMMA[42]. An

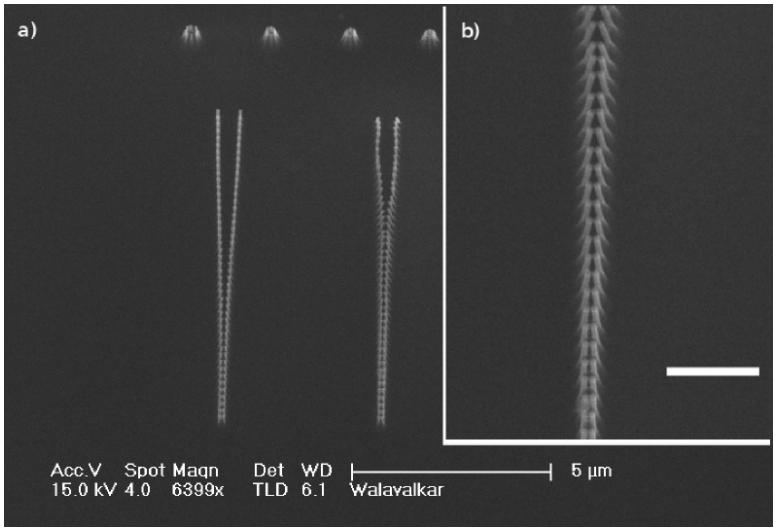


Figure 4.5: a) SEM of deformed strip next to an undeformed strip. b) Close up of lower section of deformed strip of pillars. Note the increased bend angle for the pillars that were originally further apart. Scale bar in inset is one micron.

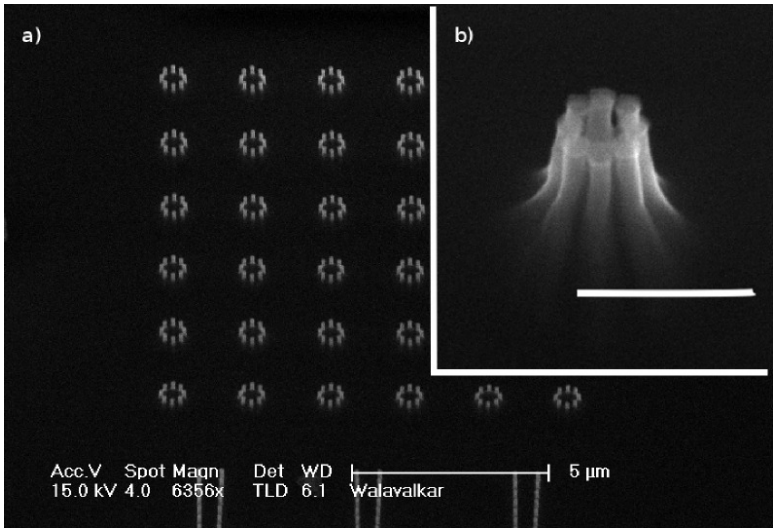


Figure 4.6: a) Array of 75 nm pillars in circular patterns with 500 nm diameter spacing. b) Contraction of pillars after the exposure of the central region. Scale bar is 500 nm.

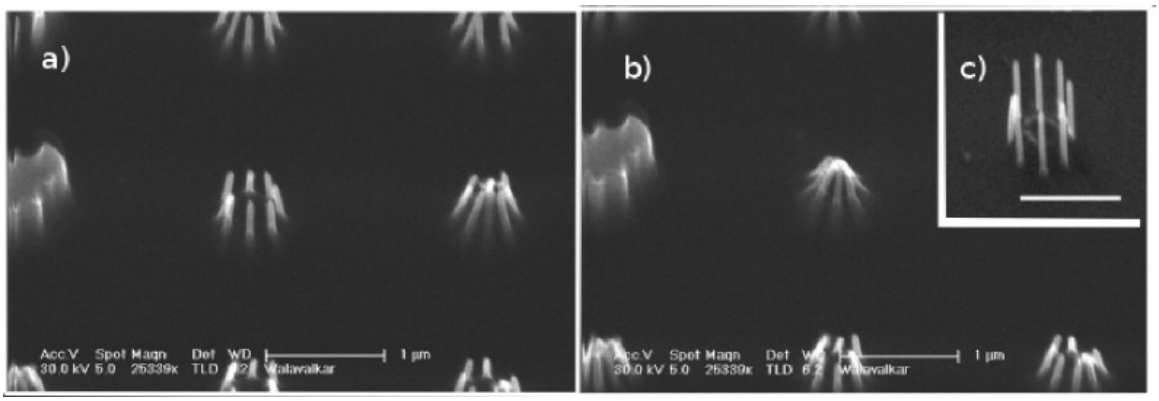


Figure 4.7: a) 500 nm wide circle of 50 nm diameter pillars. b) Same array after deformation. c) Same array after oxygen plasma release. Scale bar in picture is 1 micron.

interesting consequence of overexposing the resist is its resilience to dissolution by acetone[42, 41]. Once the area of interest had been exposed, we dipped the sample in acetone to remove the non-overexposed portions of resist, leaving the intended pillars locked in place while freeing the rest of the chip from PMMA. This permits further processing steps to be performed on the chip. Pillars can be relaxed by heating the chip, causing the PMMA to reflow, or by removing the PMMA with an oxygen plasma (inset, 4.7). After a plasma clean it was possible to repeat the process of straining and unstraining the pillars. This cyclic loading without fracture has been previously demonstrated in amorphous silicon samples[43]. For illustration of the extent of possible bending, a clump of

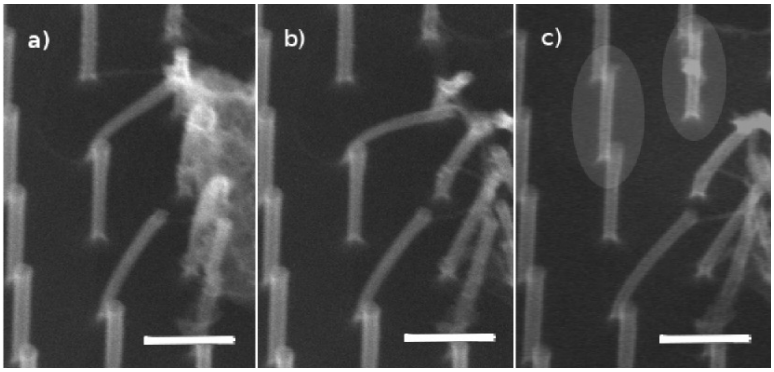


Figure 4.8: a) Clump of polymer stuck to top of pillars begins to bend the array b) Same array after full deformation c) Same array after polymer has been partially removed. Note the highlighted pillars have snapped back upright. Also note that the still bent pillars are held in place by strands of polymer.

polymer was attached to the entirety of the pillar and compressed with an electron beam (frame (a) in figure 4.8). Frame (b) shows the near-horizontal bending of the pillar and frame (c) highlights two pillars that have snapped back to their original configuration after full polymer removal. It is

important to note that the pillars still held in their bent configuration in frame (c) are held in place by still present strands of polymer.

4.3 Straining silicon nanopillars

An application of this procedure is the ability to predictably incorporate enormous amounts of strain into nanostructures. In order to estimate the strain induced in the pillars, we analyze the structure in a manner similar to Timoshenko's treatment of a bimetallic strip [44]. The actual geometry and material characteristics of the cross-linked region are difficult to measure and likely nonuniform, in reality behaving as a distributed film rather than an isolated region with clear boundaries. Additionally, the system could be complicated by slip at the interface, nonlinear elastic behavior of the polymer, and increasingly surface-dominated mechanical characteristics at the nanoscale. In spite of the simplified model, however, the proposed treatment shows excellent agreement with experimental data. Furthermore, the analysis predicts a constant radius-of-curvature, yielding a conservative estimate of the maximum strain.

We model the pillar as a cylinder with diameter d, and approximate the cross-linked region of PMMA which contributes to the deformation as a semicircular shell around the pillar with radial thickness t and originally spun to a film thickness L (4.9(a)). After exposure, an equivalent, free-standing cross-linked region would undergo a uniform vertical contraction by an amount ΔL, corresponding to a unit contraction $\alpha \equiv \Delta L/L$. The length mismatch between the submerged portion of the pillar and the contracted PMMA causes the pillar to bend to an angle θ relative to the original pillar axis and substrate normal.

Following Timoshenko, we find:

$$\frac{1}{\rho} = \frac{\alpha\left(C_p - C_s\right)}{\frac{I_s}{A_s} + \frac{I_p}{A_p} + \frac{E_s I_s}{E_p A_p} + \frac{E_p I_p}{E_s A_s} + \left(C_p - C_s\right)^2} \tag{4.2}$$

where ρ is the radius of curvature, $\alpha \equiv \Delta L/L$ is the unit contraction of the PMMA, C_p, C_s denote the center-of-mass coordinates, I_p, I_s the cross-sectional moments, A_p, A_s the areas, and E_p, E_s the Young's moduli for the PMMA and silicon, respectively. The arclength along the neutral axis remains at the original polymer thickness L, yielding an exit angle $\theta = L/\rho$:

$$\theta = \frac{L\alpha\left(C_p - C_s\right)}{\frac{I_s}{A_s} + \frac{I_p}{A_p} + \frac{E_s I_s}{E_p A_p} + \frac{E_p I_p}{E_s A_s} + \left(C_p - C_s\right)^2} \tag{4.3}$$

For the geometry described above and a coordinate system where $x = 0$ corresponds to the center

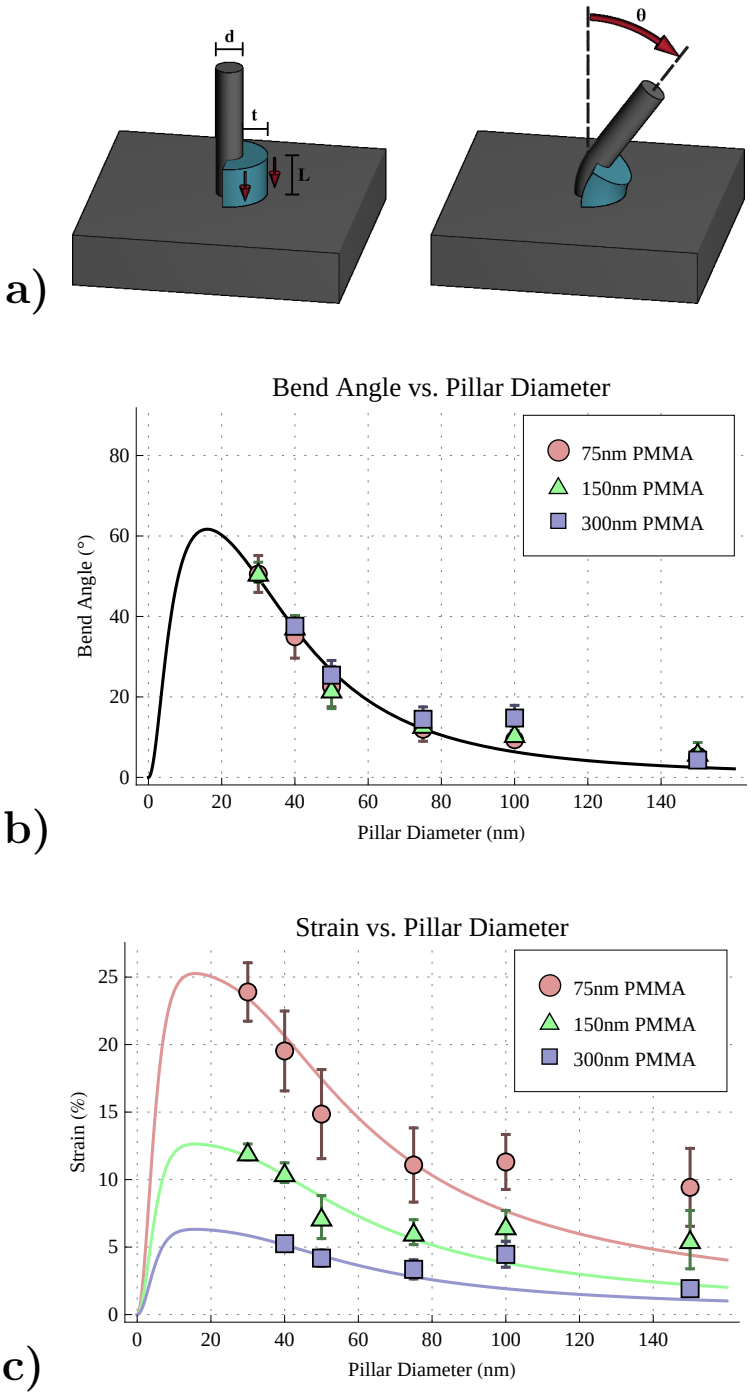


Figure 4.9: a) Diagram illustrating the theoretical model. A small, semicircular region of PMMA adjacent to a silicon pillar undergoes vertical contraction due to electron-beam–induced cross-linking, yielding large pillar deformation. In the experiment, the cross-linked region is controlled by asymmetric electron-beam exposure, and is embedded in a continuous polymer film. b) Variation of the maximum deformation angle with the diameter of the pillars, for various resist thicknesses. Theoretical model is independent of resist thickness. c) Variation of the estimated strain in the pillars with the diameter of the pillars, for varying resist thicknesses. Points represent averages over several measurements, with error bars indicating the standard deviations.

of the pillar, we have:

$$C_s = 0 \qquad C_p = \frac{3d^2 + 6dt + 4t^2}{3\pi\,(d+t)}$$
$$A_s = \frac{\pi d^2}{4} \qquad A_p = \frac{\pi t\,(d+t)}{2}$$
$$I_s = \frac{\pi d^4}{64} \qquad I_p = A_p\left(\frac{d^2 + 2dt + 2t^2}{8} - C_p^2\right)$$

Taking $E_s = 160$ GPa and $E_p \approx 5$ GPa as the Young's modulus for the overexposed PMMA[42], we solve for the remaining free parameters using a least-squares fit between the measured pillar angles and our analytic expression for θ, obtaining $\Delta L \approx 43$ nm and $t \approx 46$ nm. This contraction is on the order of the vertical contraction in overexposed PMMA reported elsewhere[42].

The results are shown in 4.9(b), which illustrates close agreement between the experimental and analytical bend angles. It should be noted that although the wires are approximately a micron in length the entire strained region is concentrated within the PMMA layer resulting in a large observed bend angle as the pillar leaves the PMMA. Interestingly, the bend angle data does not show any measurable dependence on resist thickness. In the analytic expression, this corresponds to a fixed ΔL rather than a fixed unit contraction (α) as one might expect. The exact cause of this behavior is unclear and requires further study, but might indicate that the deformation is occurring over a length which is smaller than the total film thickness. If this is the case, the strain required to accomplish the same deformation over a reduced distance would be higher than that estimated below. Were this distance also fixed, the strain curves would be independent of the PMMA starting thickness.

To provide a conservative strain estimate, we assume for now that the deformation is uniform and occurs over the entire submerged length of the pillar; we note that the portion of the pillar which extends beyond the PMMA remains unstrained. Using $\epsilon \equiv \Delta\rho/\rho$ for the strain, we find the maximum strain along the edge of the pillar:

$$\epsilon = \frac{\Delta L\,(C_p - C_s)\,(C_n - C_e)}{L\left(\frac{I_s}{A_s} + \frac{I_p}{A_p} + \frac{E_s I_s}{E_p A_p} + \frac{E_p I_p}{E_s A_s} + (C_p - C_s)^2\right)} \tag{4.4}$$

where $\Delta\rho = C_n - C_e$ is the distance between the neutral axis (C_n) and the far edge of the pillar (C_e):

$$C_n = \frac{E_s A_s C_s + E_p A_p C_p}{E_s A_s + E_p A_p} \qquad C_e = -\frac{d}{2}.$$

The results are plotted in 4.9(c), and demonstrate that we can controllably incorporate 23.9%

strain in 30 nm-diameter single crystal silicon nanowires. The strain profile within the pillar is anisotropic; based on the location of the neutral axis, it is possible to introduce both tensile and compressive strain or solely tensile. For large pillar diameters, the neutral axis lies inside the pillar, resulting in tensile strain at the outer edge and compressive strain on the inner. As the diameter decreases, however, the neutral axis moves toward the PMMA. For $C_n > d/2$, corresponding to $d \leq 17.6$nm, the strain is tensile throughout the pillar cross section.

Although these values may seem large it is important to recall that the entire strain is applied within the 75-300 nm of PMMA thickness. Furthermore, these values fall within the range of reported values for strain in silicon nanowires under fracture-free polymerization incited deformation[37, 38]. Possible mechanisms that could allow such extreme behavior have been studied previously[31, 32, 33] and rely on the relatively small volumes of nanowires resulting in the fabrication of statistically "defect-free" structures that lack sites for fracture nucleation. Additionally the small diameter of the nanowires allows for dislocates to be "annealed" out of a structure by diffusing to the perimeter[37].

Unlike these studies[37, 38], since our strain was applied within the PMMA layer while the exposed region remained unaffected, it was impossible to perform an in-situ HRTEM on the strained region to atomistically quantify the deformation as either elastic or plastic. However, to SEM resolution each pillar returned to its original position after being freed from the PMMA, even after several tens of bending and unbending cycles.

4.4 Applications

Anisotropic strain has recently been exploited as a method for breaking the inversion symmetry in silicon photonics [29, 30], introducing a second order non-linearity. Furthermore, such asymmetrically strained materials can exhibit interesting optical selection rules[28] based on the strained splitting of the degenerate light and heavy hole bands. Previously proposed methods to introduce strain typically rely on the deposition of lattice mismatched layers, a method which can incorporate only a few percent of strain, and which is fixed at fabrication time[27, 28]. In contrast, the method present in this work allows for the incorporation of several tens of percent of strain as well as being fully tunable and reversible.

Another application presented in this paper is the ability to monitor the manipulation of pillars in real time via SEM while capturing an object. Here we used an array of pillars that had been selectively actuated to capture a 300 nm aluminum oxide polishing bead (4.10(a)). During capture, the contraction of the pillars squeezed a collection of beads such that they were forced through the top of the closed pillars (4.10(b)). Once the pillars had been closed, the resist was selectively removed and the captured collection of beads remained trapped within the pillars. We expect this technique to have important biological applications such as capturing individual cells for further

study. Compared to electrically actuated nanotweezers[25], the polymer-controlled nanowires may be more densely packed, allowing the study of interactions between neighboring traps, and offer the ability to leave the tweezers closed without any external input.

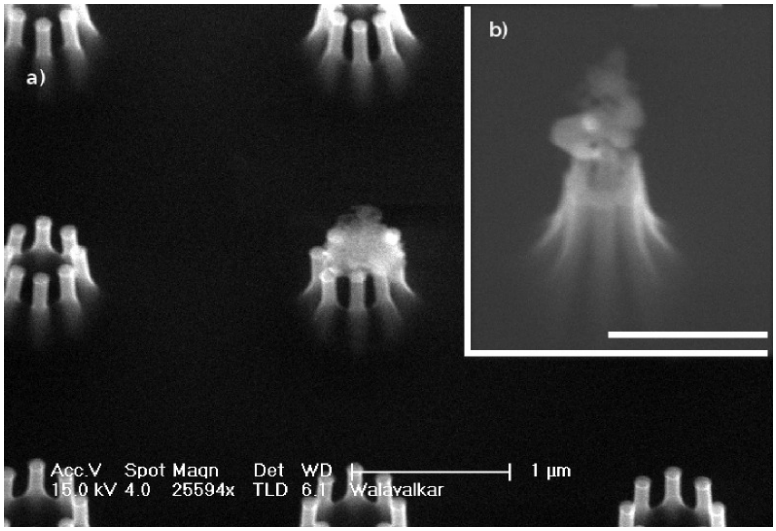


Figure 4.10: a) 300 nm alumina polishing bead caught by 100 nm pillars. b) 75 nm pillars catching a collection of smaller alumina polishing beads. The scale bar is 500 nm.

Chapter 5

Nanopillar Photoluminescence

In this section, we fabricate top-down, etched, silicon nanopillars and further thin them via self-terminating oxidation in order to demonstrate photoluminescence, as well as measure radiative lifetime with respect to reduction in pillar diameter. This behavior is obtained through the utilization of the self-terminating properties of nanopillar oxidation to fabricate uniform, 1 μm tall pillars with diameters between 2 and 8 nm.

5.1 Silicon and light emission

Silicon light emission is a rapidly growing area of inquiry. This field is uniquely important due to the dependence on silicon in the modern micro-electronics industry. In order to economically create optical interconnects and circuit elements, the development of a silicon-compatible light emitter is critical, and the last two decades have shown marked advancement in the field of silicon light emission[45].

Investigations into silicon light emission were instigated with the use of electrochemical reactions to etch large pores into single crystal silicon. The wafer of silicon was immersed in a bath of hydrofluoric acid as the anode with a platinum electrode as cathode. By passing current through the electrochemical cell it was possible to corrode deep pits into the silicon anode. An example of such an etch is shown in figures 5.1 and 5.2; under different constant current and voltage conditions it was possible to produce more uniform arrays of silicon pores[45, 46].

The remaining structure behaved similar to 1-D quantum wires, resulting in visible and near infra-red photo- and electro-luminescence [45, 47]. Although the porous silicon consisted of structures small enough to create quantum confinement effects, there was some ambiguity over the actual source of the light emission. Some work indicated that the emission was due to Si-H complexes rather than quantum confinement[48] with light emission disappearing after the surface passivating hydrogen was heated off the sample. Although there is still some work being done in this field the fact that the technique was both stochastic and not easily CMOS compatible has damped this area

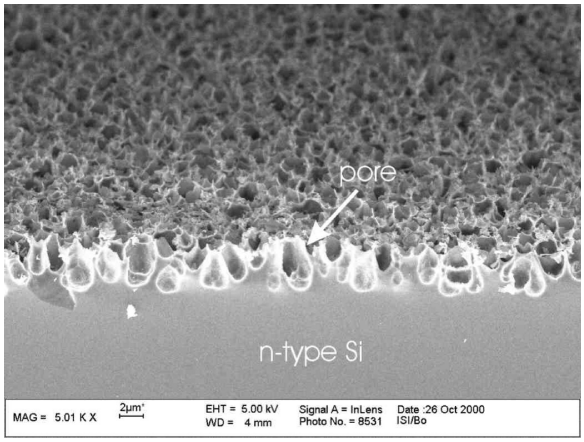


Figure 5.1: An example of a brief electrochemical etch into a silicon subtrate. From: *http://www.fz-juelich.de/ibn/sensorik/bcs-pen-e.html*

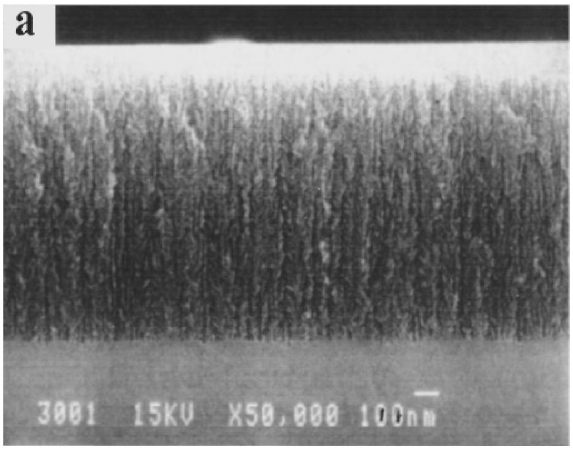


Figure 5.2: A cross-sectional SEM of a deeply etched porous silicon sample.

of inquiry.

In order to develop low-cost components, several groups utilized the technology developed for CMOS processing to design nano-scale structures. Low dimensional structures, such as nanopillars or nanocrystals patterned with "top-down" techniques are examples of these efforts[47]. Silicon nanocrystals have demonstrated both a wide emission bandwidth,[49] and chemical stability. Unfortunately, the requirement for a wide band-gap material as a cladding around the nanocrystal tends to prevent electrical excitation as wide band gap materials are typically insulators. Recent work, [3, 50] however, has shown promise in utilizing floating gate devices to reliably excite nanocrystals. In such a device holes and electrons are tunneled through a dielectric layer into the nanocrystals, where they recombine. The spectra of such emission is shown in figure 5.3 and a schematic from *Walters et al.*[3] describing the recombination procedure is shown in figure 5.4

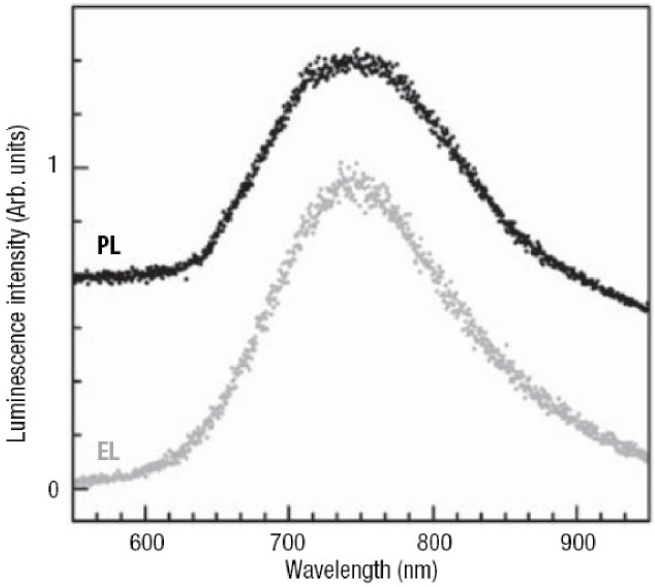


Figure 5.3: Photo and electroluminescence spectra from nanocrystals. From: *Walters et al.*[3]

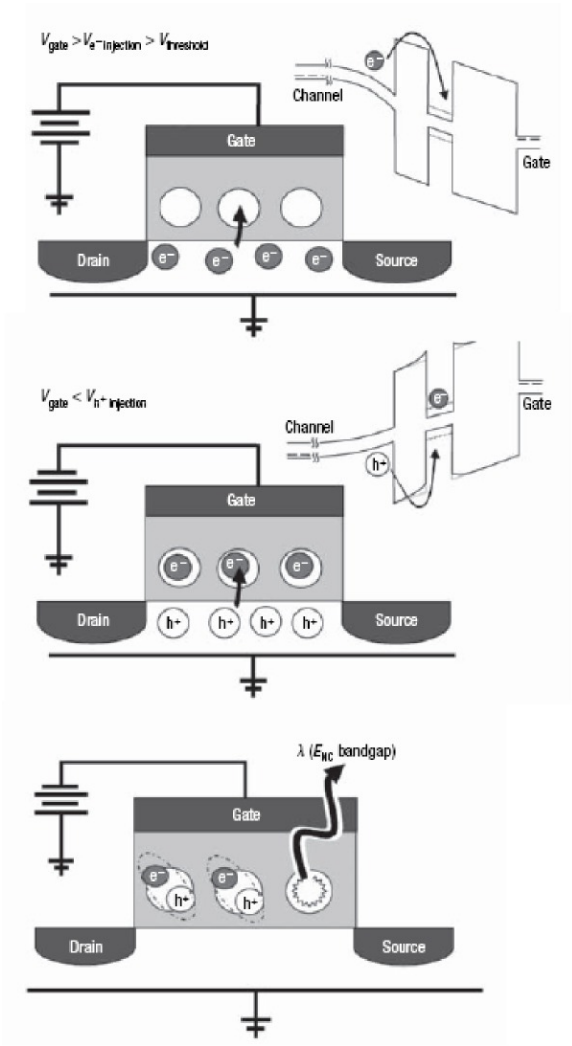


Figure 5.4: A schematic of the excitation of silicon nanocrystals using tunneling current. From *Walters et al.*[3]

A great deal of work has been done with grown[4, 51, 52, 53, 54] and etched [55, 56, 57, 58] nanopillars. The vapor-liquid-solid (VLS) grown nanowires can be assembled as single crystals and present interesting electronic, optical and structural properties. The VLS growth technique utilizes a supersaturated liquid metal catalyst to nucleate growth at the at the interface between seed metal and growth front. For silicon growth a thin layer of metal ($\sim$ 5 nm), typically gold, is evaporated onto a silicon wafer substrate. The wafer is annealed at a temperature higher than the metal-Si eutectic point allowing the metal-Si alloy to bead and form droplets on the surface of the substrate. In a heated vacuum chamber ($\sim$ 400-600 ^{o}C), such as a CVD reactor, $SiCl_4$:H_2 gas is decomposed and absorbed by the metal-Si droplet. The droplet serves to lower the activation energy of vapor to solid growth by presenting an intermediate liquid phase. In the liquid alloy the supersaturated silicon atoms precipitate out of solution at the solid-Si/alloy interface, causing the droplet to build vertically as more and more layers of silicon push the droplet further from the surface. Once a desired height is reached the metal droplet can be removed from the sample using a metal specific chemical etchant, leaving vertical silicon nanowires. Figure 5.5 shows an example of disordered silicon nanowire growth; it is possible by choosing fortuitous wafer orientations to grow well ordered arrays of nanowires as seen in figure 5.6.

The standard catalyst used when growing silicon nanowires (SiNWs) in a CVD reactor is gold; unfortunately, recent results have demonstrated[4] that states that such nanowires suffer from a deep-level trap resulting in a fast non-radiative decay, hindering PL. However, by using $TiSi_2$ as a catalyst[4, 59] *Guichard et al* have demonstrated size dependent PL in VLS grown nanowires. Figure 5.7 shows, from left to right, the as-grown nanowires, HRTEM of as grown nanowires, TEM of oxidized nanowires, and PL spectrum of oxidized nanowires. Depending on the crystal orientation of the substrate and the size of the catalyst particle VLS silicon tends to grow along the $< 111 >$ or $< 110 >$ crystal axes. Based on Density Functional Theory (DFT) and Tight Binding Method (TBM) simulations, wires grown along these axes have been predicted to not undergo a transition to a direct band-gap as the wire diameter is decreased[60][5] unlike wires grown along the $< 100 >$ direction[61]. An example of a tight binding calculation for various orientation of the nanowire is given in figure 5.8 .

The alternative to bottom-up nanowire growth is top-down patterning via etching. The works cited above have shown that etched silicon pillars will photoluminescence, however previous work has not examined the relationship between the PL spectra and the size and surface conditions of the pillars. Previous attempts[57, 55] have reported the spectral width of the PL emission to be greater than 1 eV. The wide spectral emission has been attributed to the distribution of pillar sizes in etched samples which masks the possible evolution of PL with respect to specific pillar diameter.

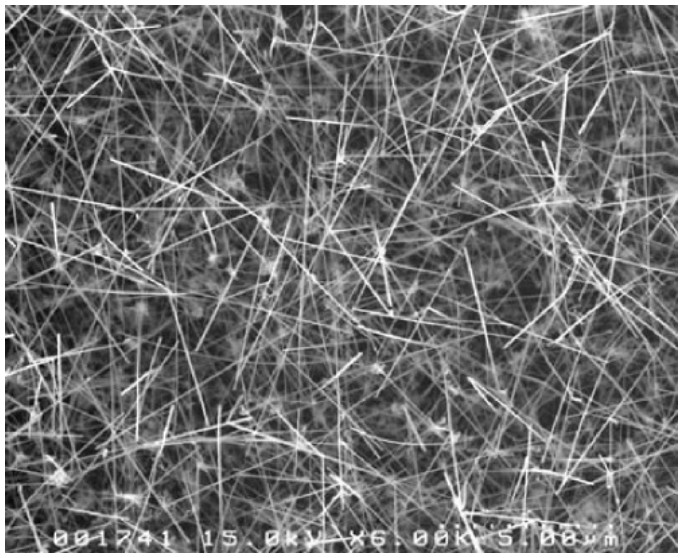


Figure 5.5: An example of disordered VLS growth of silicon nanowires.

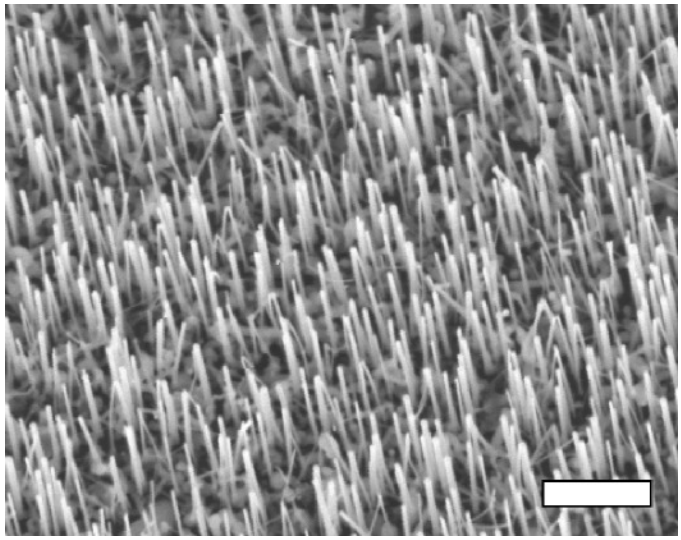


Figure 5.6: An example of ordered VLS growth of silicon nanowires. The scale bar is 500 nm.

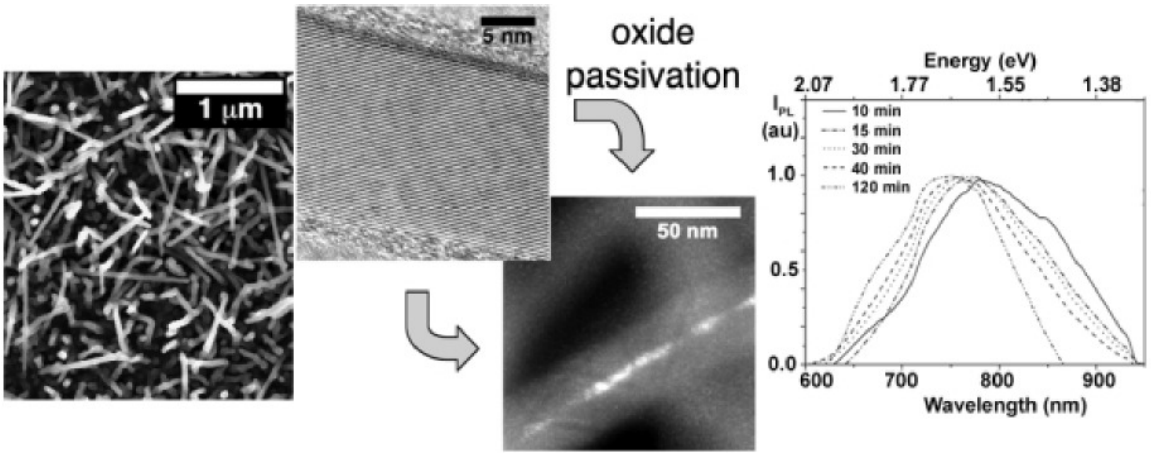


Figure 5.7: Luminescent $TiSi_2$ catalyzed, VLS grown nanowires from *Guichard et al*[4]

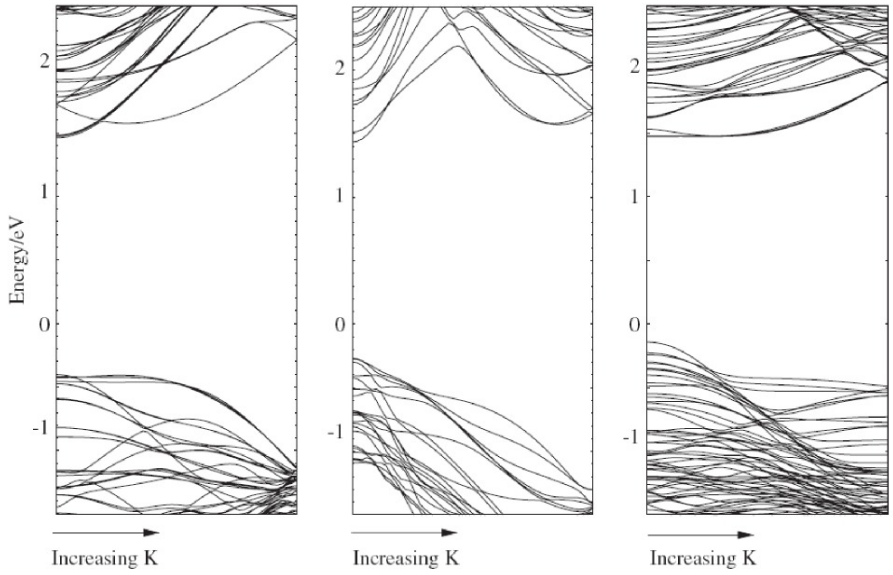


Figure 5.8: Theoretical band structure from *Harris et al*[5] for a 2 nm diameter nanowire with the long axis along [100], [110], and [111]. Note that while the [100] and [110] direction nanowires transition to a direct bandgap the [111] nanowires retain the indirect bandgap associated with bulk silicon.

5.2 Fabrication and oxidation

The fabrication of the luminescent nanopillars followed from the fabrication method outlined in chapter 2. Pillars were defined by e-beam patterning an array of 30-50 nm disks in 75 nm of Micro-Chem PMMA 950 A2 on $< 100 >$ silicon. A 25 nm layer of Al_2O_3 was deposited as a hard-mask via DC-magnetron sputtering of aluminum with a 5:1 Ar:O_2 process chemistry and patterned via lift-off. Etching was performed in an Oxford Plasmalab 100 ICP-RIE 380 machine running a "Pseudo Bosch" etch with simultaneous etching using SF_6 and passivation using C_4F_8. Sidewall profiles are controlled by adjusting the etch to passivation gas ratio. Figure 5.9 (a) shows the uniformity in post-etch profile of a pad of nanowires. After etching, the pillars were oxidized in a dry ambient in

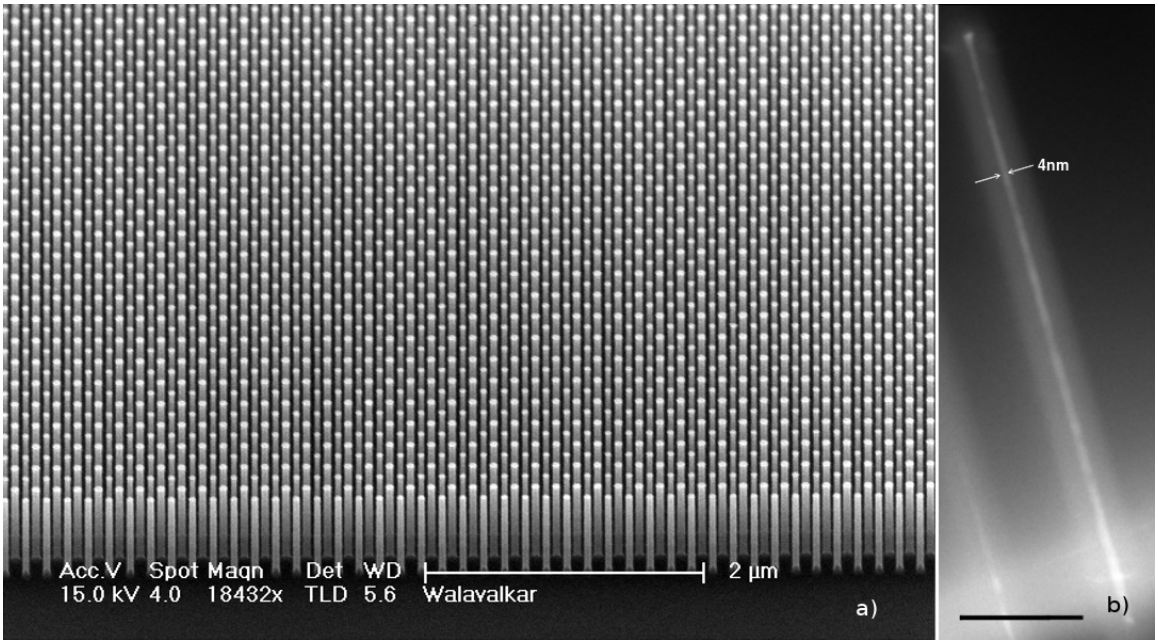


Figure 5.9: a) An array of 50 nm pillars etched into single crystal silicon b) Reflection mode TEM image of 4 nm wide silicon core in an oxidized silicon nano-pillar. Scale bar is 100 nm.

the temperature range of 850-950 ^oC. As mentioned in Chapter 3 the silicon core diameters were measured using reflection mode transmission electron microscopy (TEM) with the silicon pillars positioned perpendicular to the incoming electron beam. We were able to extract silicon core widths by utilizing the diffraction contrast between the crystalline Si and the amorphous SiO_2. A 4 nm wide silicon core imaged by this method is shown in 5.9 b). 5.10 shows the final pillar diameters as a function of initial diameter (35 or 50 nm) and oxidation temperature. Each data point represents the mean of 10-15 core diameters measured on a sample via reflection TEM and the error bars represent the standard deviation in the pillar size. Curves for oxidizing 30 and 50 nm pillars from *Liu et al.*[62] are included in 5.10 and we show good agreement with their predicted terminal core

diameters. Variation between our data and their theory may stem from the fact that their model utilized experimental data to fit theory and extract parameters, such as oxygen diffusivity and reaction rate vs. temperature, that would vary from furnace to furnace and rely on the accuracy of calibration of the temperature controller governing the furnace. Figures 5.10(a) and (b) shows TEMs of 50 and 35 nm initial diameter pillars that have been oxidized at 890 ^{o}C.

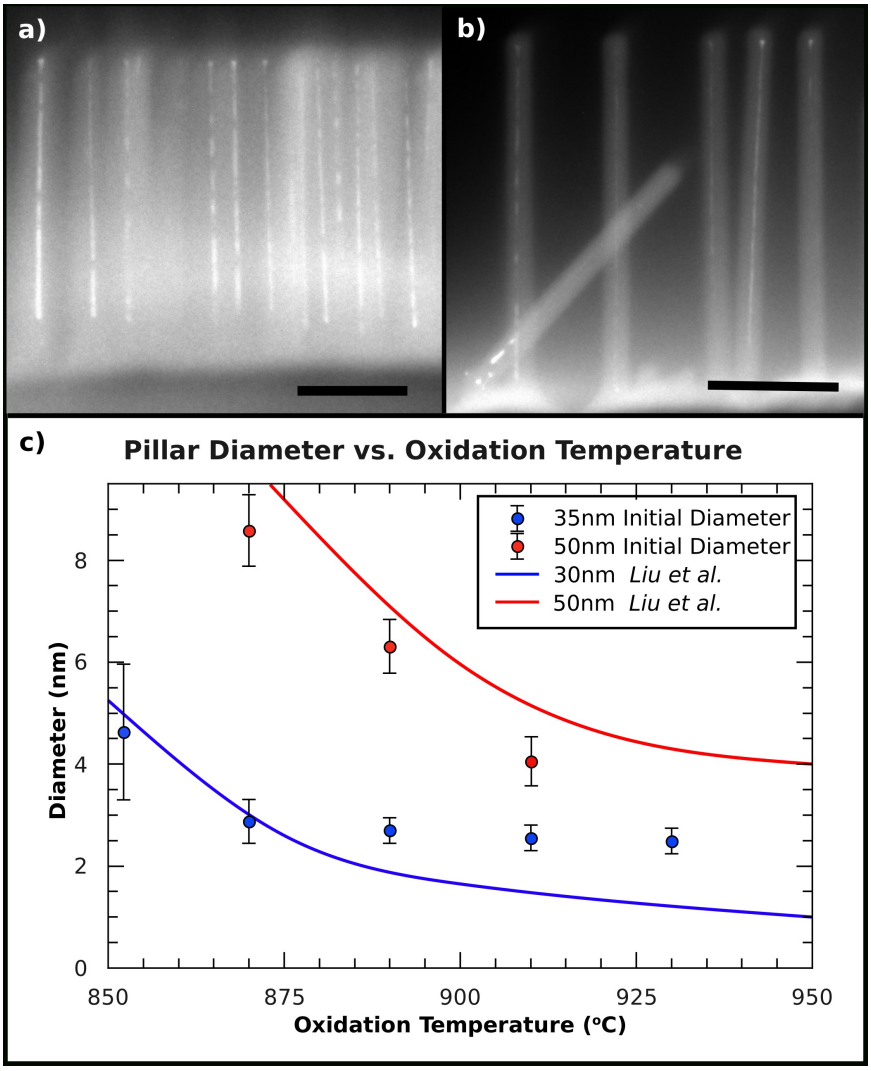


Figure 5.10: (a) TEM of a pad of 50 nm initial diameter pillars after oxidation at 890 ^{o}C. The single crystal silicon cores are bright compared to the amorphous silicon dioxide due to diffraction contrast. Scale bar is 200 nm. (b) TEM of the corner of a pad of 35 nm initial diameter pillars oxidized at 890 ^{o}C. (c) Tuning of pillar diameter based on oxidation temperature. The terminal pillar diameter is a function of both the initial diameter and the oxidation temperature. Included are the oxidation trends found in *Liu et al.* for 30 and 50 nm initial diameter pillars.

Figures 5.11 and 5.12 show several RTEM images of pads of pillars that were used to characterize and quantify the self-terminating oxidation.

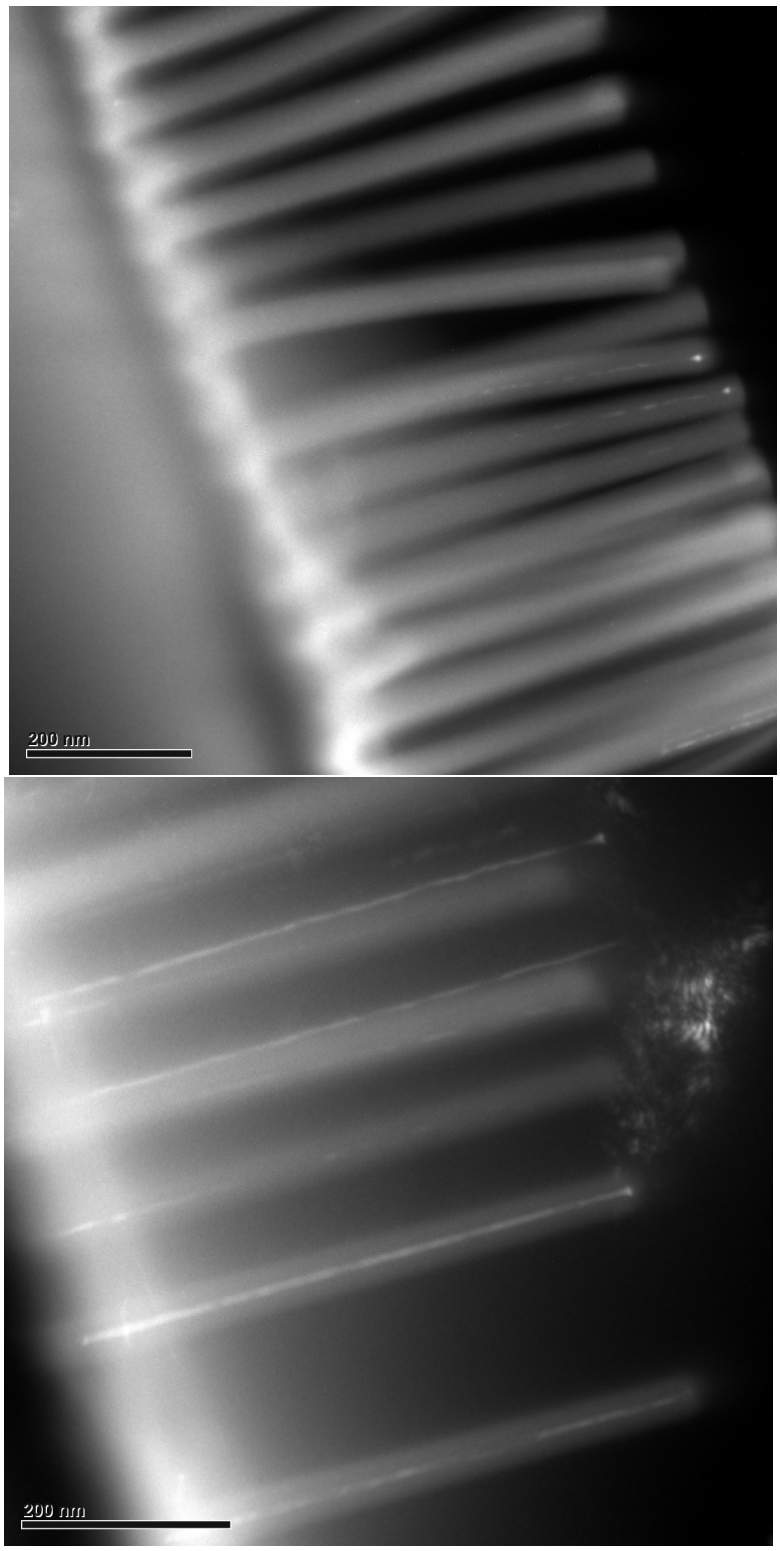


Figure 5.11: Two examples of RTEM images used to quantify oxidation data. Initial diameters were 35 nm in both cases. The top frame was oxidized at 910 ^{o}C and the bottom frame was oxidized at 890 ^{o}C.

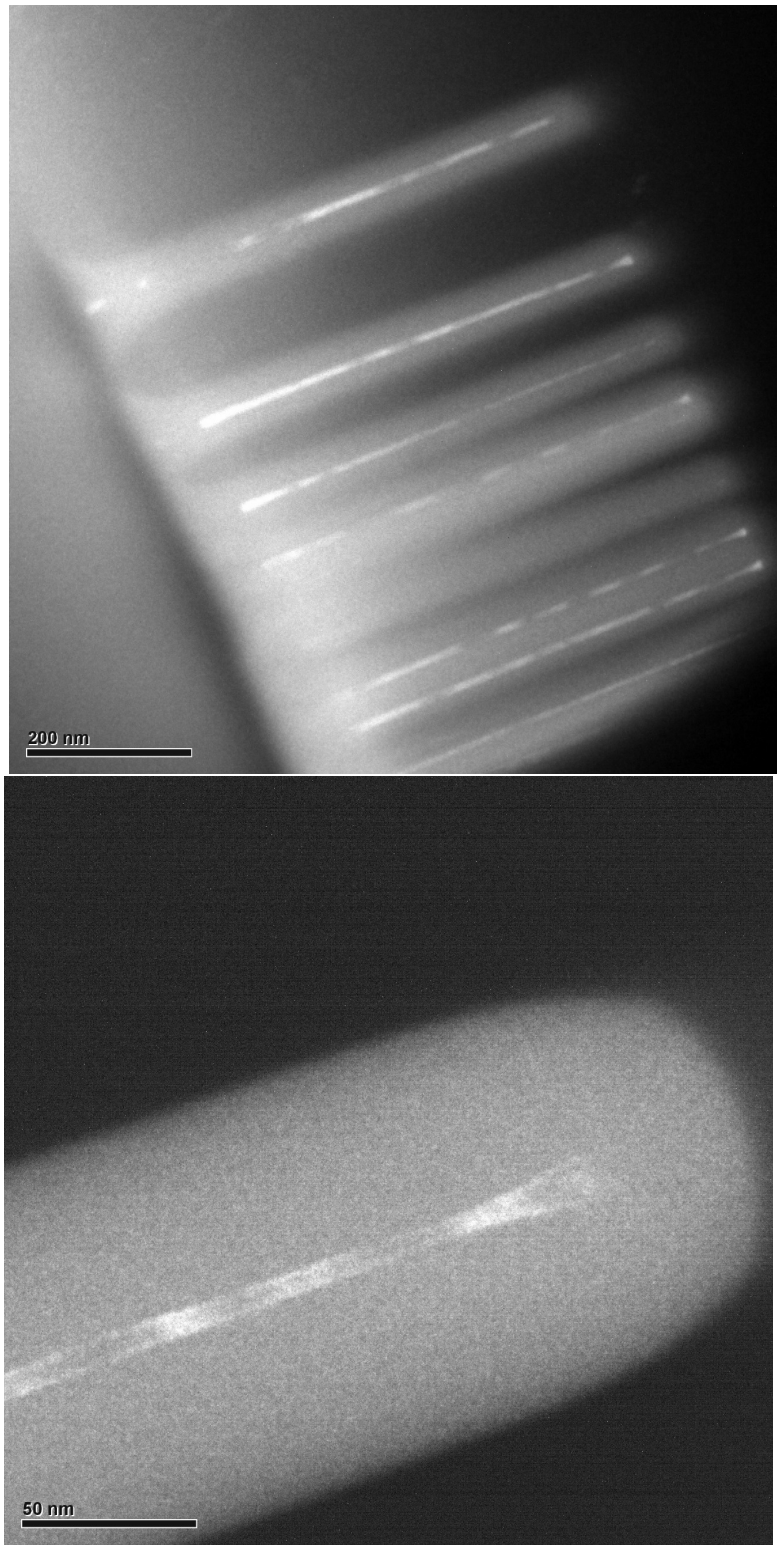


Figure 5.12: Wide angle and close-up view of 50 nm initial diameter pillars oxidized at 870 ^{o}C.

5.3 Measurement and discussion

Micro-photoluminescence was performed on the samples by pumping with a free space Ar^+ ion laser at 488 nm. The sample was mounted in an inverted optical microscope, and the laser was shined onto the chip and reflected out into a beam block at a 45^o angle to minimize the amount of laser light collected by the detection optics, 5.13. The light was collected by a 50x/.55NA objective and passed through a 550 nm long-pass filter to further block the laser light. Finally, the light was passed to a grating spectrometer and then onto a cryogenically cooled Si CCD array.

Photoluminescence was observed between 600-800 nm (1.5-1.9 eV), as shown in 5.14. The solid lines in 5.14 indicate pillars with original diameters of 35 nm while the dashed lines are pillars with original diameters of 50 nm. The data shows a strong blue shift in peak emission wavelength corresponding to a decrease the silicon core diameter. The peak wavelength vs. core diameter is plotted in 5.15 (a) and (b) with the x error bars showing the standard deviation in pillar size while the y error bars show the full width half maximum (FWHM) of the observed PL peak. From 5.15(a) and (b) the blue shift in peak PL energy correlates strongly with narrowing of the pillars, indicating that the emission energy is at least partially governed by a quantum confinement effect. We also note that our average FWHM is 240 meV with most widths at roughly 150 meV or less, roughly 30 to 50% narrower than previously reported results[4, 55, 56]. This narrow FWHM is indicative of a narrower size distribution of silicon pillar cores, an effect we believe is due in part to the better control over pre-oxidation pillar diameter via etching as well as allowing the pillars to reach a terminal diameter through a 7-10 hour oxidation time.

Several methods were investigated to provide an explanation for the blue shifted behavior of the peak emission, shown in 5.15 as continuous lines. The simple effective mass theory which treats the confinement as an infinite quantum cylinder with the bulk silicon band-gap as the un-confined ground state produced a trend that follows the $1/d^2$ expected of quantum confinement. As has been previously noted[63] this method underestimates the peak emission energy and a good description of the bands is required to model the emission of wires with diameters smaller than 10 nm. The second approach utilized a twenty band (ten valence, ten conduction) $sp^3s^*d^5$ tight binding approach[64, 65] to calculate the bands between the Γ and X symmetry points. The results from this simulation are plotted in 5.15. Although they provide a better fit to the data, this approach also tends to underestimate the emission energy. The final approach utilized the same tight binding simulation but incorporated the strain applied by the thermal oxidation to deform the lattice. The strain was calculated using the parameters, such as core diameter and final oxide thickness, extracted from the TEM images and the methodology described elsewhere [62, 21, 17] as well as a finite element (FEM) simulation to calculate the strain induced by cooling the sample from oxidation to room temperature. The model that utilized in-plane tensile strain to deform the tight binding lattice provides a better

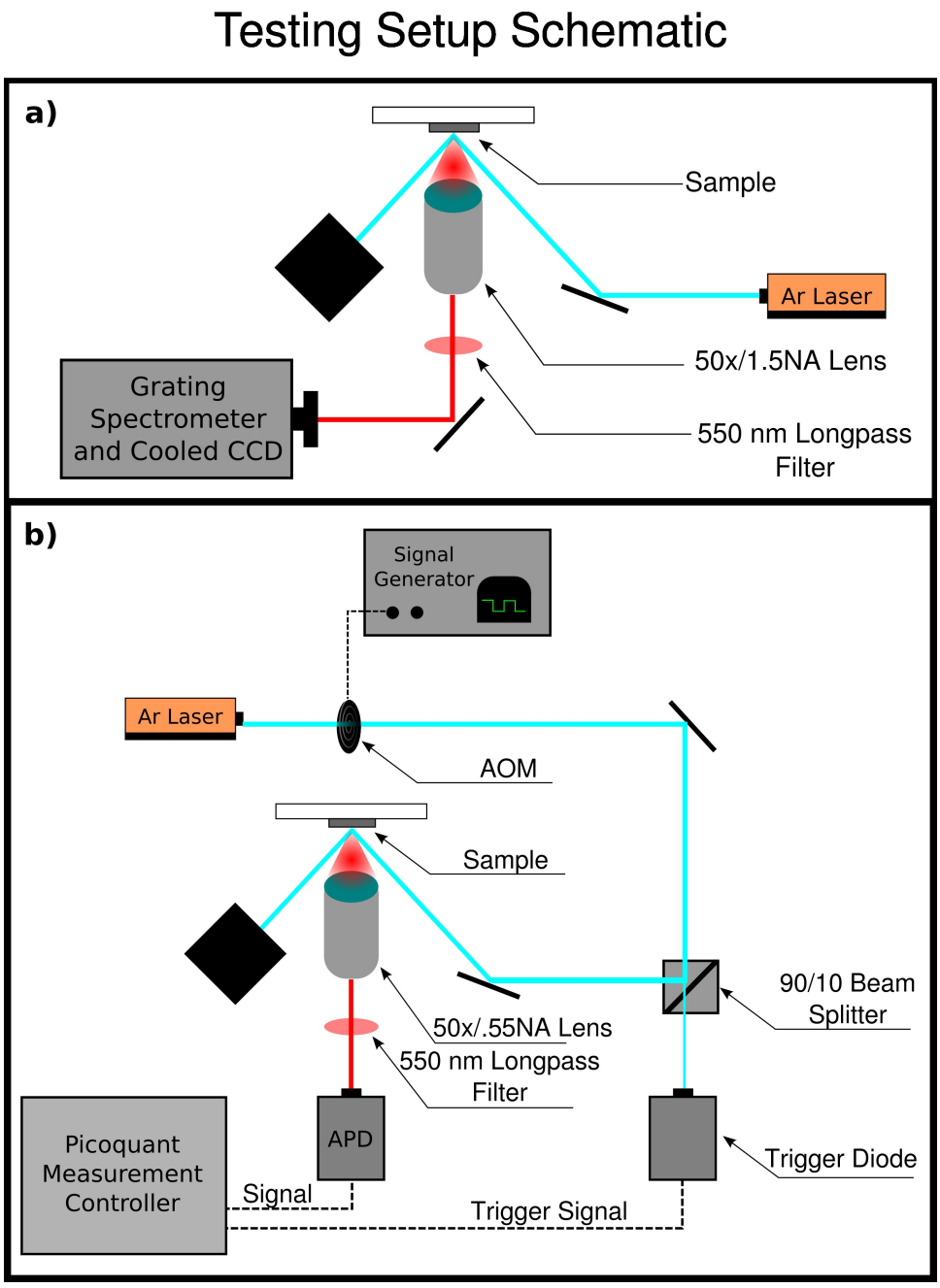


Figure 5.13: Schematic of the testing setup. a) In the photoluminescence setup, laser light is used to pump the sample at a 45 degree angle and sent to a beam block while PL is collected through a microscope and sent through a 550 nm long pass filter to the cooled CCD camera. b) For lifetime measurements, laser light is gated by an acousto-optic modulator (AOM) with a period of 20 μs and 50% duty cycle and split with 90% of the light being sent to the sample and 10% to a trigger diode. PL collected from the sample is sent to an avalanche photo-diode (APD) and the Picoquant controller uses the signal from the trigger diode to gate on and off the data collection from the APD in order to obtain lifetime measurements.

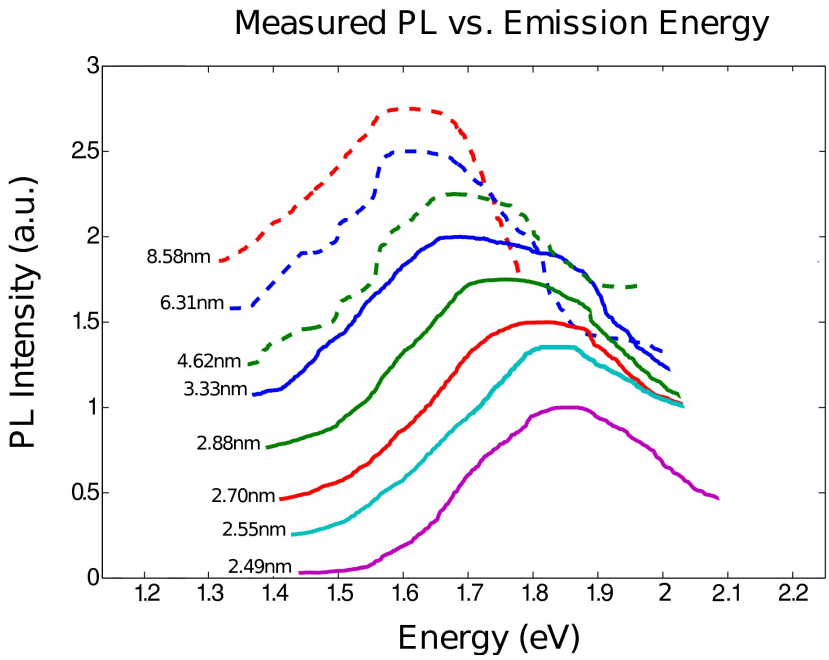


Figure 5.14: Normalized PL intensity from eight samples of various diameters. The variation in diameter was obtained by changing the oxidation temperature and the diameters reported are the average pillar size measured on a sample by reflection mode TEM. Dotted lines represent pillars with 50 nm initial diameters and continuous lines represent pillars with 35 nm initial diameters.

fit to the peak emission data and indicates that the blue shift in emission wavelength is caused by a combination of both the strain as well as the quantum confinement.

Previous theoretical [60] and experimental[4, 61] work has examined the role of strain in the energy and direct or indirect nature of the silicon band gap. While biaxial compressive strain tends to red shift the band energy, the biaxial tensile strain associated with oxidation [62, 21] tends to blue shift the band gap[60, 61] due to the bonding nature of the d orbital that contributes to the conduction band. From theoretical calculations based on *Kao et al.*[17] and *Cui et al.*[21] to estimate the strain applied during oxidation as well as FEM analysis and finding the best fit to the experimental data, we conclude that the pillars experience approximately 1.5% tensile strain in the radial and circumferential direction (5.15 (c))and negligible strain along the transverse direction. This is because the compressive strain associated with the thermal mismatch (between silicon and silicon dioxide) during the cool down to room temperature roughly cancels the tensile strain due to oxidation along the length of the pillar.

There has been extensive theoretical and experimental work that examines the role of oxidation and the silicon oxygen bond itself, in determining the band-gap and peak emission energy in silicon nanocrystals. Two studies[66, 67] have predicted that the presence of a silicon-oxygen double bond, as a result of the incomplete oxidation of silicon, creates a localized exciton state in nanocrystals

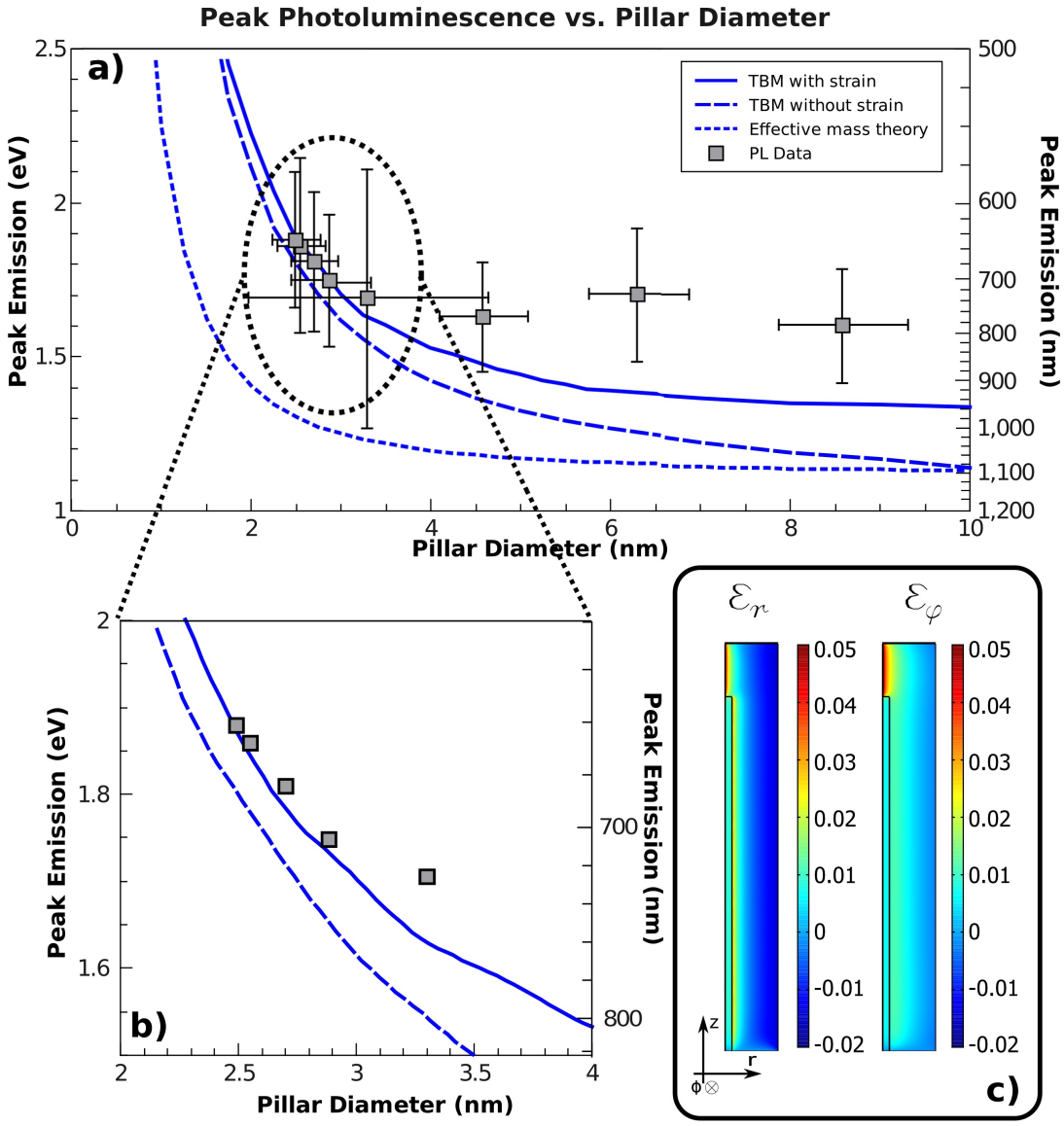


Figure 5.15: (a) Peak PL emission as a function of terminal core diameter. Continuous lines represent three different theoretical explanations for the blue-shifted emission energy. Error bars in the x-direction represent standard deviation in pillar size and in the y-direction the FWHM of the measured PL. (b) Magnified view of peak emission for pillars between 2-4 nm. (c) Finite element strain model used to calculate the strain in the nanowires after oxidation. Shown is the strain in the radial and circumferential direction; the strain in the z direction is negligible

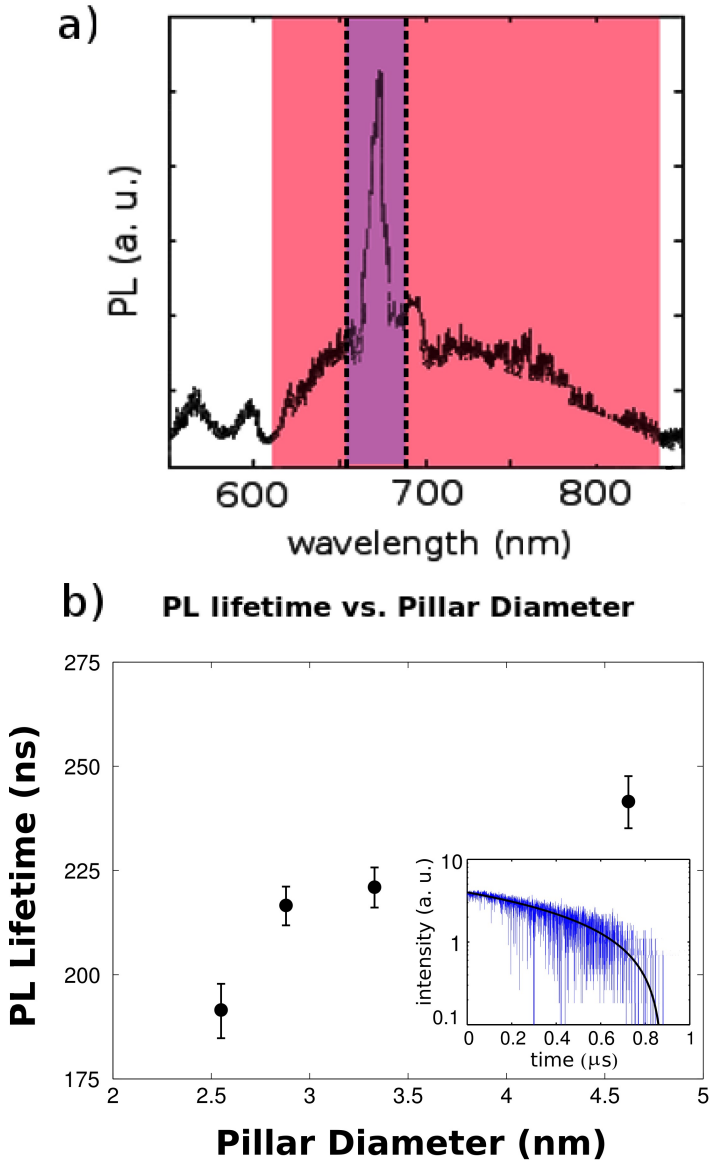


Figure 5.16: (a) Identification of PL peak associated with silica double bond defects. (b) Lifetime measurements for changing silicon core diameters. Error bars indicate uncertainty in the fit of the exponential decay time. Inset shows example of PL lifetime measurement with fitting curve in black.

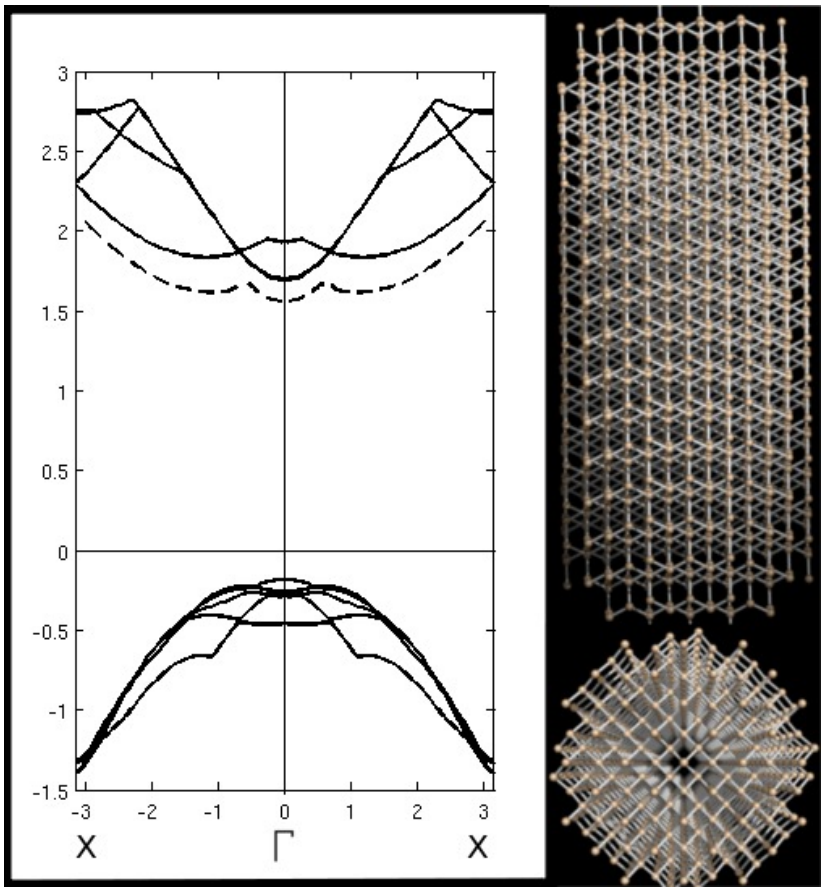


Figure 5.17: Band-structure (in eV) of a TBM simulation of a strained and unstrained 2.5 nm diameter silicon nanowire. The dotted shows the relative conduction band edge for the unstrained wire while the two insets show the axial and transverse structure of the nanowire.

with diameters of 2.5 nm or less. This state pins the band-gap at 2.1 eV with the creation of a fast radiative trap state and effectively stops the band-gap energy expansion due to quantum confinement. A variation of this effect was thought to be observed in these nanofabricated pillars when they were oxidized and allowed to return to room temperature in a nitrogen or oxygen ambient. A sharp peak was observed at 1.85-1.9 eV (650-670 nm) along with the wider peak associated with quantum confined PL. It was found that this sharp peak stayed at a fixed energy while the quantum confined PL would vary based on pillar size. Since the pillars were all larger than the threshold size of 2.5 nm, for the onset of the oxygen double bond pinning effect, and it was possible to see both sharp luminescence at 1.85 eV and broad band-to-band luminescence at longer wavelengths (5.16 (a)), an alternative but similar mechanism was proposed. The presence of a nonbridging-oxygen hole center (NBOHC), typically found in a compressively strained silica matrix[68], similar to the layers surrounding the silicon pillars under tensile strain, will serve to trap holes on isolated oxygen atoms and photoluminescence at 1.9 eV. Since the NBOHC is associated with localized states in the silica, and not with the silicon itself, it is possible to simultaneously see PL from both NBOHC and band-to-band transitions in silicon. When the pillars were cooled to room temperature in forming gas (5% H_2, 95% N_2), instead of nitrogen, the peak at 1.9 eV disappeared. The suppression of the peak corresponds to a protonation and quenching of the NBOHC[68] via reactions with the rapidly diffusing molecular and atomic hydrogen.

Lifetime measurements were also taken of the measured samples. A 488 nm Ar^+ laser was passed through an acousto-optic modulator (AOM) that was gated with a square wave with a period of 20 μs and 50% duty cycle. The beam was sent to a 90/10 beam splitter where the majority of the light was sent to the sample and the rest of the light was sent to a trigger diode. The PL from the sample was collected by a 50x/.55NA lens and passed through a 550 nm long-pass filter onto an avalanche photo-diode (APD). The signal from the APD was collected by the measurement controller (Picoquant Picoharp 300) when triggered by a signal from the trigger diode. Decay times were measured in the range of hundreds of nanoseconds and found to be decreasing with narrowing core diameter, 5.16 (b). The inset in 5.16 (b) shows an example of the PL decay of a set of pillars with 2.88 nm average core diameter. The decreasing of PL lifetime with core diameter as well as the relatively short lifetimes (200 ns) can be attributed to several possible factors. Since the pillars prepared for this work were etched from Czochralski (CZ) grown silicon wafers the upper bound of the fast mid-gap non-radiative defect density is less than $10^7 cm^{-3}$, corresponding to a non-radiative lifetime of roughly 1 ms[69, 70]. Based on diffraction contrast TEM images the core material remains single crystal, with any damage due to etching removed from the surface via oxidation. Furthermore the small volume occupied by the silicon cores would make it improbable to find such defects within the cores. This would indicate that PL lifetime in these etched pillars is governed by a radiative rather than non-radiative process. A possible mechanism for the transition to the radiative lifetime

limited regime could be related to the magnitude of the splitting between the direct and indirect valleys of the conduction band. Theoretical calculations have found the strain in nanowires to be important in increasing the splitting between the Γ conduction band valley and the bulk indirect X direction valley[60, 61]. For pillars with diameters less than 10 nm experiencing tensile strain in the radial and circumferential direction, the splitting between these two minima is several times the room temperature thermal energy (depending on the wire diameter and the amount of strain), as seen in the solid lines of 5.17. This large splitting allows the excited electrons to sit in the Γ valley, allowing for a faster, direct optical transition. For un-strained or compressively strained pillars (dotted line in 5.17) the splitting between the two valleys is closer to the thermal energy forcing carriers to sit both in the Γ as well as the X valley, requiring a longer phonon-assisted recombination. Furthermore, by tuning the size of the pillars to be on order of or smaller than the free-space electron wavelength, it is possible to increase the overlap between the hole and electron wave functions and therefore increase the recombination rate[70]. By examining the variation of radiative lifetime with temperature in future experiments it would be possible to determine the influence of the non-radiative decay as well. *Guichard et al.*[59] have shown that the bimolecular bound exciton Auger recombination coefficient of VLS-grown nanowires scales with both temperature and the density of excitons. Since the pillars investigated in our report are both larger and smaller than the 4.9 nm ground state exciton radius in silicon[71] it may be possible to see the onset of this effect as the size of the pillars crosses this threshold. Furthermore these pillars could serve as a platform to investigate the recombination dynamics of the "bulk-like" excitons (excitons in structures larger than the exciton Bohr radius) as they transition into their 1D counterparts.

5.4 Strain effects

Further experiments were performed to investigate the role of strain in determining the peak emission wavelength. There are several ways to to possibly modify the strain including silicon nitride deposition[29, 30], polymer mediated bending[72], and high temperature anneals. We chose to abate the strain built in during oxidation through a 1050 ^{o}C, 100% nitrogen anneal. At this temperature the silicon dioxide has passed its glass transition temperature[17][62] ($\sim$960 ^{o}C) and can flow to relieve the strain built in during oxidation. Based on the assumption that by keeping the pillars at such a temperature for an hour the built in strain was completely removed, we modeled the final strain as that due to the mismatch in thermal expansion coefficients as the pillars cooled to room temperature. A finite element model showing the distribution of strain in a 4 nm diameter pillar is shown in figure 5.18. It can be seen that after the anneal the magnitude of the strain is significantly smaller than before. A cross-section of the strain is shown in figure 5.19; based on modeling and peak emission the strain appears to be tensile in the silicon and rapidly becomes compressive in the

oxide.

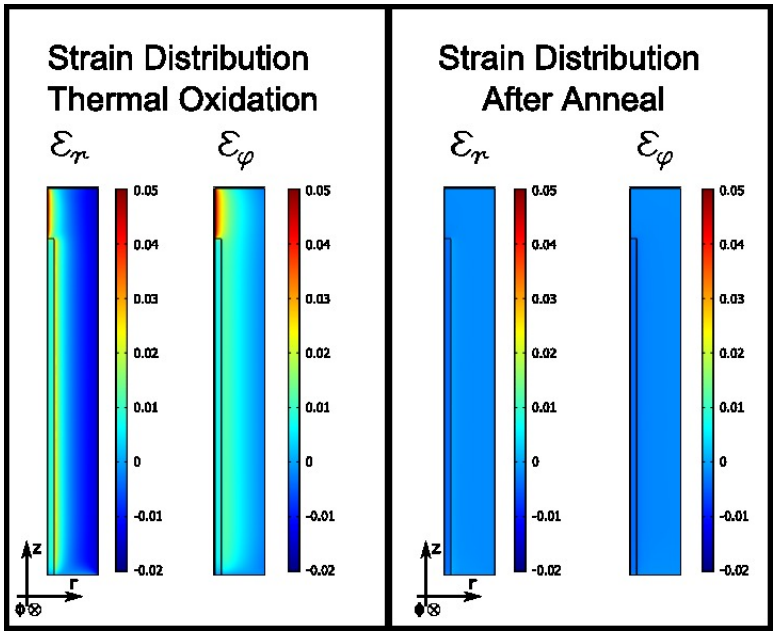


Figure 5.18: Finite element model of the strain distribution in a 4 nm diameter pillar before and after the anneal.

Once the high temperature anneal was performed, microphotoluminescence was once again measured. It was found that the pillars with core diameters in the range of 2-5 nm red-shifted roughly 100 meV after the anneal. Furthermore it was found that the larger core pillars ceased to emit light. Figure 5.20 shows the red-shift in the smaller core diameter pillars; as predicted by the tight binding simulations, relief of the strain would bring the conduction band edge closer to the valence band. Figure 5.21 shows the results of tight binding simulations for the effects of tensile (blue), neutral (black), and compressive (red) strain on the silicon core.

This result has several implications. The first concerns the fact that the larger diameter pillars ceased to emit light. It was found during tight binding simulations that more tensile strain on the silicon core would not only blue-shift the bandgap but also increase the splitting between the Γ and X direction valley. When that tensile strain was released through the anneal it is possible that the simple quantum confinement was not sufficient to make silicon behave as a direct bandgap material. If the bandgap of a sub-10 nm diameter silicon whisker has an indirect valley at or below the energy of the Γ valley then the material will have a blue-shifted (when compared to bulk silicon), indirect, bandgap. An indirect or almost indirect bandgap will quench the photoluminescence as excited carriers are more likely to thermalize down to the valence band instead of recombining with holes.

Furthermore the influence of strain on the peak emission wavelength gives us another degree of freedom in tuning the pillars to an ideal emission wavelength. Figure 5.22 illustrates the range of peak

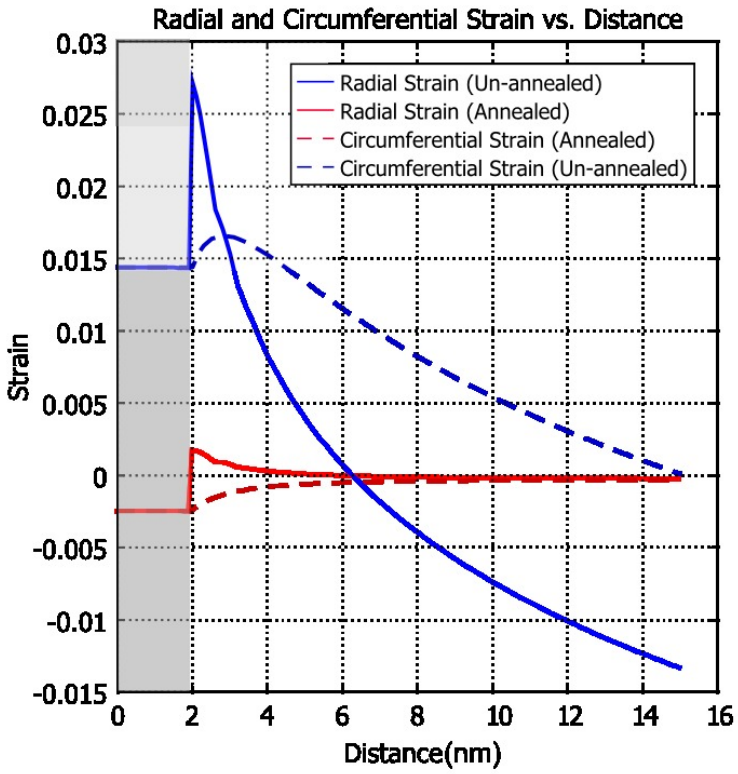


Figure 5.19: Lateral cross-section of the strain profile found in a 4 nm diameter annealed and unannelaed pillar.

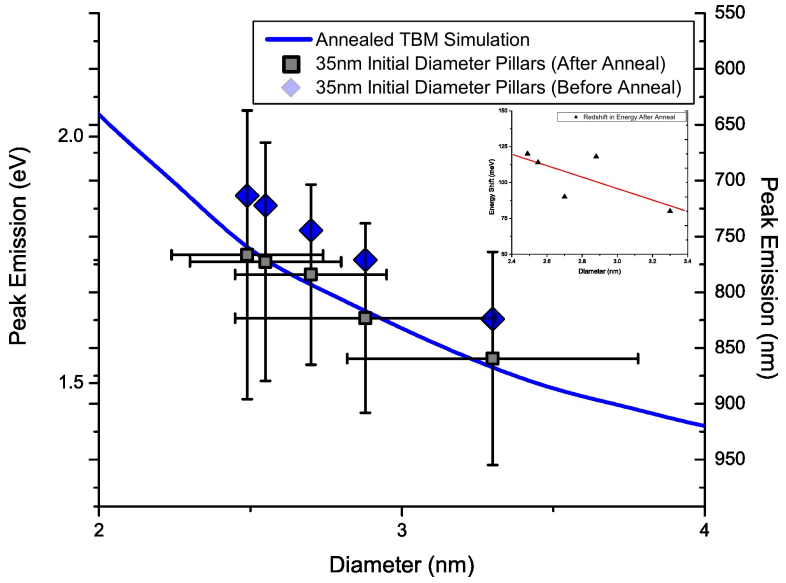


Figure 5.20: Peak emission energy before and after anneal. The theoretical plot was obtained by performing a tight binding simulation with a small amount of compressive strain imparted to the core.

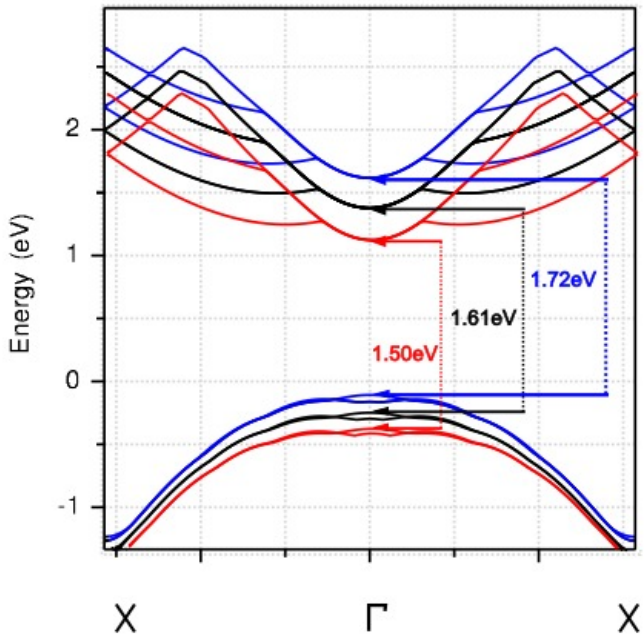
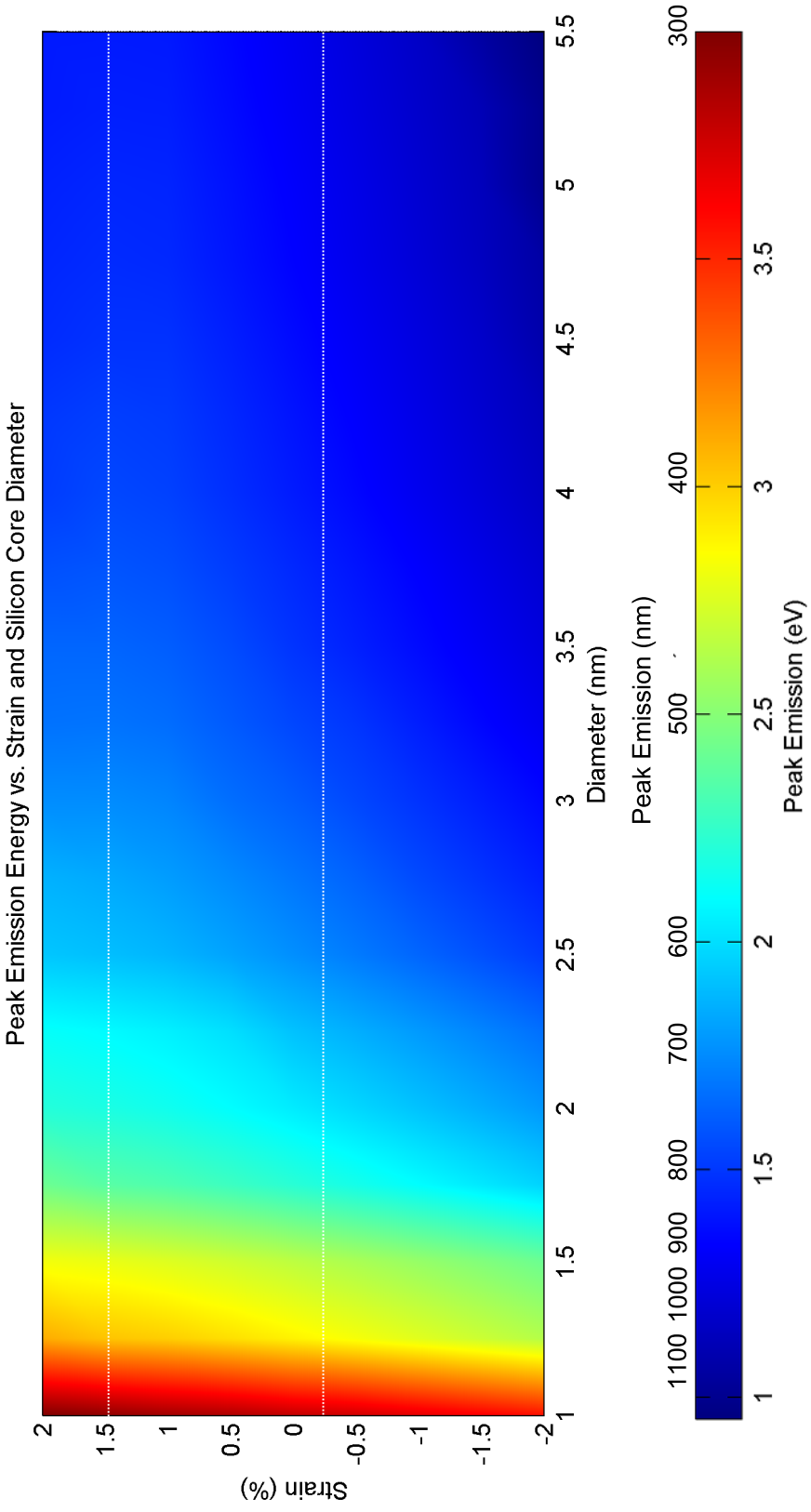


Figure 5.21: Calculated band-structure for a pillar under (blue) tensile, (red) compressive, (black) no strain.

emission energy that can be obtained by setting the core diameter with self-terminating oxidation and the residual strain. The two dotted lines show the regions of strain that were measured and plotted as a fit to data in figures 5.20 and 5.15.

This experiment should be repeated with a method to continuously vary the strain incorporated in the pillars in order to experimentally probe the effects of strain on the luminescent emission. Further work needs to be done to accurately quantify the strain found in the nanopillars. Raman or X-ray diffraction (XRD) techniques[73] can be used to probe deformation of atoms at the Si-SiO_2 interface. XRD techniques found in *Takeuchi et al.*[73] have shown that the interface and the body of the silicon core of oxidized nanowires are subjected to tensile strain as high as 0.5%. Unfortunately the nanowires studied in their work were horizontal and trapezoidal and an order of magnitude larger than those we fabricated and were not oxidized to their self-limiting state as seen in 5.23; it is found that the strain scales as the inverse square of the decreasing radius of curvature[17, 18] so size effects are more severe in our case. For the luminescent nanopillars accurate TEM studies need to be performed to actually examine the lattice deformation and lattice spacing of the silicon cores. Unfortunately the scattering of electrons in the amorphous oxide prevents precise HRTEM measurements; however we could thin the oxide with a gentle hydrofluoric acid vapor based etch to decrease the amount of oxide the electrons have to pass through.


Peak Emission Energy vs. Strain and Silicon Core Diameter
Strain (%)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
1
1.5
2
2.5
3
3.5
4
4.5
5
5.5
Diameter (nm)
Peak Emission (nm)
1100
1000
900
800
700
600
500
400
300
1
1.5
2
2.5
3
3.5
Peak Emission (eV)

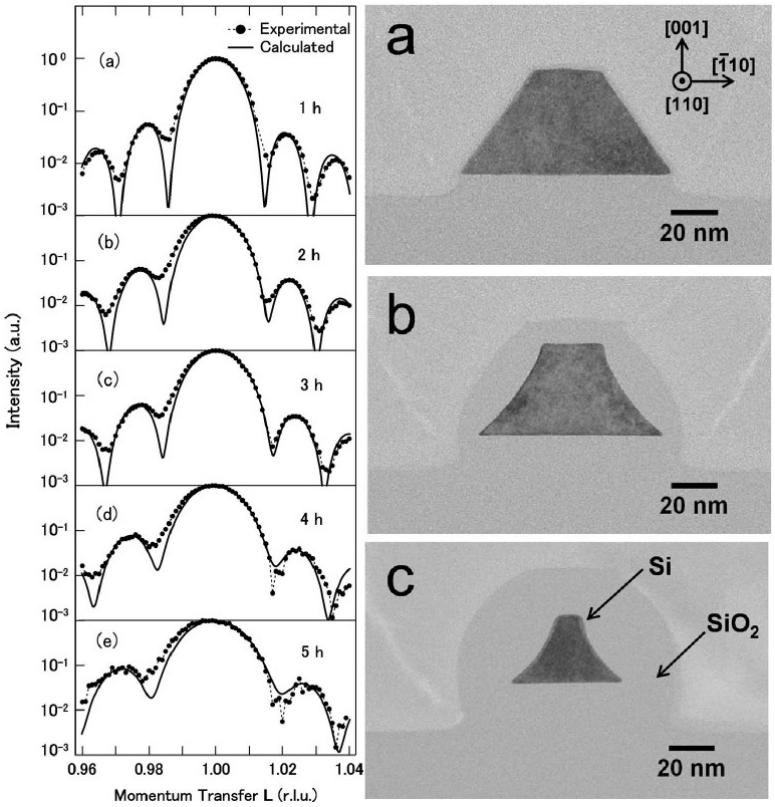


Figure 5.23: Lateral cross-section TEM of the oxidation of a trapezoidal nanowire. The pictures are taken pre-oxidation, 1 hour into oxidation and 5 hours into oxidation. The left frame shows the XRD diffraction curves for different oxidation times used to estimate the interfacial strain. Oxidation in this work was performed at 850 ^{o}C.

5.5 Future directions

Showing that it is possible to fabricate wavelength tunable, CMOS compatible, top-down, luminescent structures out of silicon is an important step in achieving silicon based, on-chip light sources. Given that these nanopillars are luminescent, the immediate thought is to place them into a cavity and examine their gain properties. Figure 5.24 shows a prototype of a structure used to test the gain properties of nanopillars. The pillars are fabricated on an SOI wafer with 335 nm Si on 2 microns of SiO_2 on a 550 micron silicon handle. The original pillar diameter was 35 nm. Frame (a) in 5.24 shows the entire pillar arrangement after oxidation. Frame (b) in 5.24 shows a close view of the regularity of the fabricated pillars. Frame (c) in 5.24 shows the resulting ring resonator after 150 nm plasma enhanced vapor deposition (PECVD) deposition of unstrained SiN_x. The PECVD deposition is conformal, filling the spaces between the pillars and forming a smooth ring. The silicon nitride is used to raise the effective index of the ring resonator so that the structure can confine light between an oxide surface and air on three surfaces. To enhance the confinement a filled circular arrangement of pillars can result in a disk instead of a ring resonator; this structure could be undercut with hydrofluoric acid making the index contrast much higher since the structure is confined by air. The improved confinement is illustrated schematically in figure 5.25.

In addition to lasing, the creation of an efficient CMOS compatible Si LED would be a useful on-chip light source. The conversion of the nanopillars to electroluminescent structures is a project itself and is covered in the Electronics chapter.

In conclusion, this section of work has demonstrated room temperature photoluminescence from silicon nano-pillars etched from wafers of single crystal silicon. The uniformity in pillar diameter has allowed us to investigate the role of pillar diameter as well as oxidation strain in determining the peak emission energy. By varying the oxidation temperature we were able to show a blue-shift in energy with decreasing core diameter that agrees with previous experimental work as well as tight-binding simulations. The fabrication process to create these pillars is fully CMOS-compatible and is a promising method to create integrated, visible and near-IR, on-chip silicon LED or laser devices.

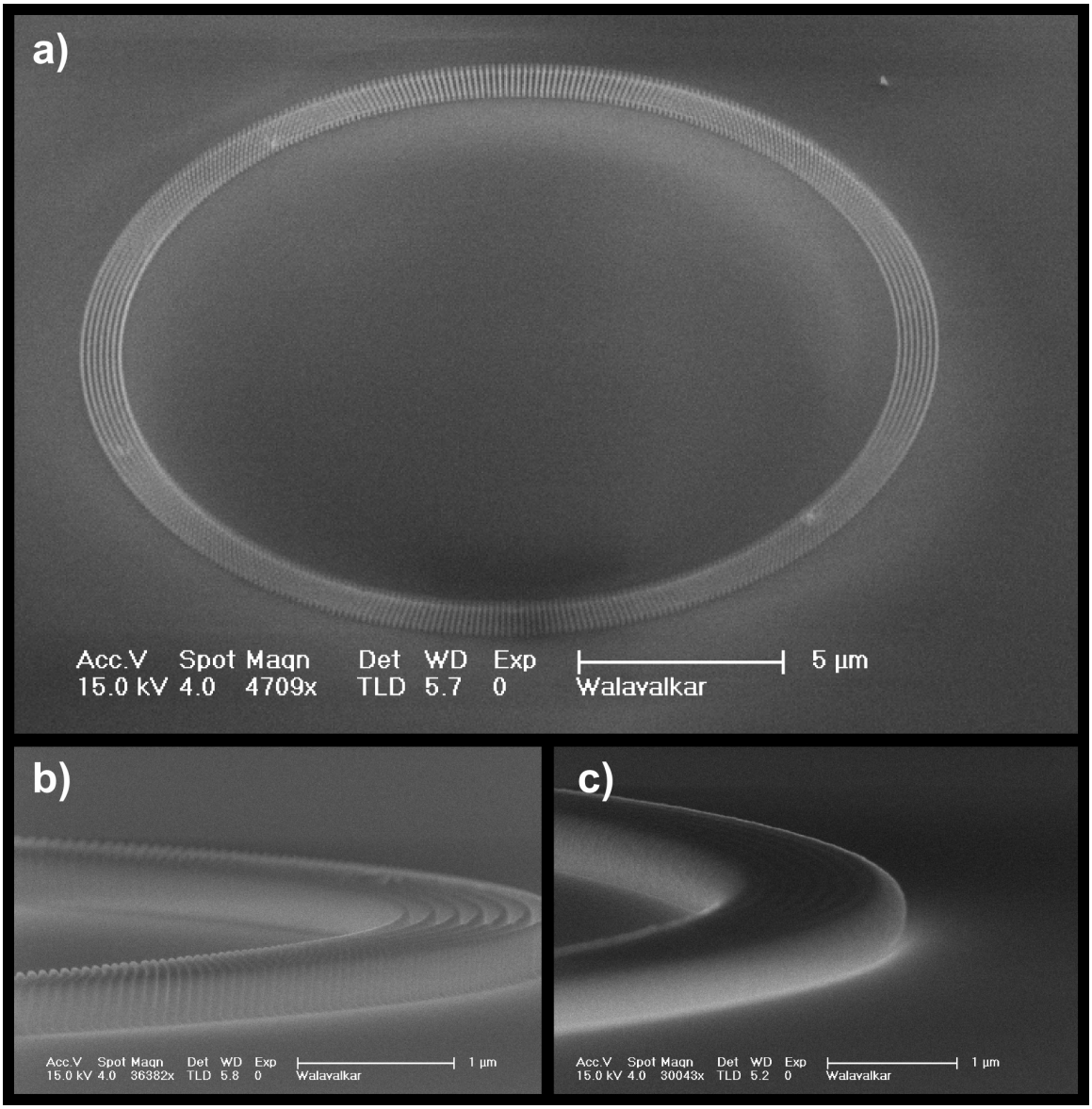


Figure 5.24: (a) Circular array of 50 nm diameter pillars on SOI (b) Close-up of oxidized 50 nm pillars on SOI. (c) Silicon nitride used to pattern a ring resonator containing the oxidized pillars

Figure 5.25: The left structure shows the cross-section of a ring resonator built around pillars. The right structure shows the improved confinement afforded by an undercut disk resonator.

Chapter 6

Fabrication of and photoluminescence from etched silicon quantum dots

As mentioned in previous chapters silicon quantum dots have shown extensive photo- and electroluminescent properties[49, 3, 50, 74]. Specifically silicon nanocrystals embedded in a dielectric matrix such as silicon dioxide or silicon nitride have been used as a convenient method to generate CMOS compatible layers of light emitting material. The most popular technique to fabricate these nanocrystals has been to deposit a layer of silicon rich oxide or nitride and anneal at above 1100^oC, allowing the excess silicon to precipitate into clusters within the dielectric[75, 76, 77, 78, 79, 80, 81, 82]. TEM images of an example of this technique are shown in figure 6.1. Depending on the annealing temperature a statistical distribution of quantum dot sizes is found. It has been shown that these dots can be made to luminesce by optical pumping as well as through electrical excitation by tunneling electrons and holes through the dielectric and allowing them to recombine in the dots. Although this precipitation technique has been improved and well characterized over the years, it comes with some key limitations. For example, the spatial distribution of these dots cannot be controlled accurately which makes addressing individual quantum dots difficult. Furthermore, the inherent size distribution of the precipitated nanoclusters leads to inhomogeneous broadening and artificially widened emission spectra; an example of this size distribution can be seen in the last frame of figure 6.1.

Recent work[83] has shown a remarkable effort into the fabrication and characterization of single etched quantum dots. These top-down devices have demonstrated narrow line-widths and 'blinking' behavior associated with emission from single nanocrystals[83, 7, 84]. An example of these etched quantum dots is shown in figure 6.2.

In this chapter we will demonstrate the ability to fabricate uniform arrays of stacked pillars of silicon quantum dots whose size (and thus peak emission wavelength) can be precisely tuned via etching parameters and oxidation conditions. These vertical quantum dots exhibit bright photo-

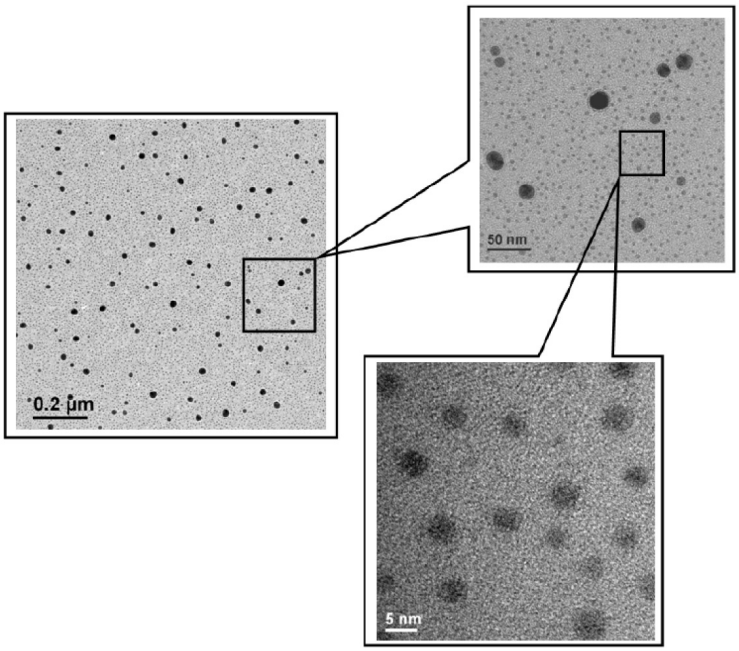


Figure 6.1: TEM images from *Das et al.* [6]. The images are shown with decreasing size until the quantum dots are visible. Note the irregularity in dot size in the final image.

luminescence from the visible to the near infrared and can be predictably and repeatably placed through lithographic techniques.

6.1 Fabrication

6.1.1 Patterning

Patterning was performed with e-beam lithography as was explained in the previous chapter. The masking material was once again aluminum oxide patterned via lift-off of e-beam resist (PMMA). Some of the SEM/TEM images to follow were etched after e-beam evaporation of aluminum oxide as the sputtering chamber was down while this work was being done.

6.1.2 Etching

The novelty of this technique sits with the ability to etch these stacks of quantum dots from single crystal silicon in a completely CMOS compatible way. The etching procedure follows the 'pseudo-Bosch' etching method, however in this case the etching conditions were modulated with time. It was possible to controllably modulate the etching rate and undercut depth by tuning the passivation gas flow rate and/or the forward power of the etch.

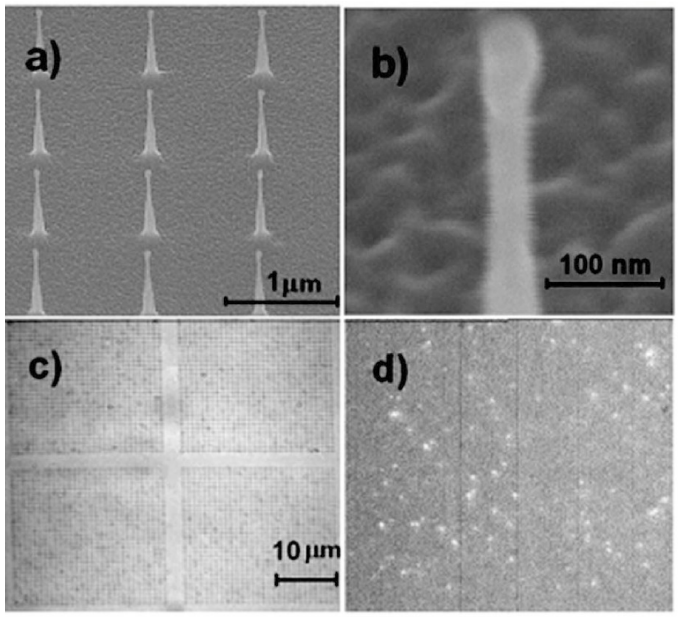


Figure 6.2: SEM images from *Sychugov et al.*[7]. (a) SEM image of quantum dots at the tips of pillars. (b) SEM close-up of a quantum dot on a pillar. (c) Optical photograph of array of quantum dots. (d) Same array under UV light excitation, bright spots are luminescent dots.

6.1.2.1 Principle

As mentioned previously, the C_4F_8 serves to passivate the faces of the pillars as they etch, creating a vertical sidewalls with aspect ratios measured as high as 60:1 (in that case they were 20 nm diameter pillars etched 1.2 microns tall). Our 'pseudo-Bosch' recipe runs with developed parameters for the chamber pressure, gas flows, forward power, and ICP power. A representation of this etch is shown in frame (a) of figure 6.3 and an SEM is shown in frame (a) of figure 6.4. For this project the chamber pressure and ICP power were kept constant from the previously developed etch. For clarity we will talk about the flow ratios of SF_6/C_4F_8 (developed value is 32:55 sccm) and the forward power (developed value is 23 W).

Typically our etch is run at gas ratios well into the passivation saturation regime; if we were to lower or raise the C_4F_8 flow $^+/_-$ 5 sccm, the morphology of the etch would stay the same, however the etch would speed up or slow down, respectively. When we change the gas ratio to 32:45 we begin to see an etch profile like that of frame (b) of figure 6.3 and frame (b) of figure 6.4 if this changed gas ratio is implemented in the middle of the etch. The polymer passivation is shown on the schematics in bright green; in frame (b) of figure 6.3 it is possible to see how the narrowing begins at a depth where the passivation is completely milled away. This narrowing phenomenon is a result of the increase in lateral etching the deeper the etch proceeds into the silicon; this is a function of the ion angular distribution function (IADF). There are many factors that control the IADF including the

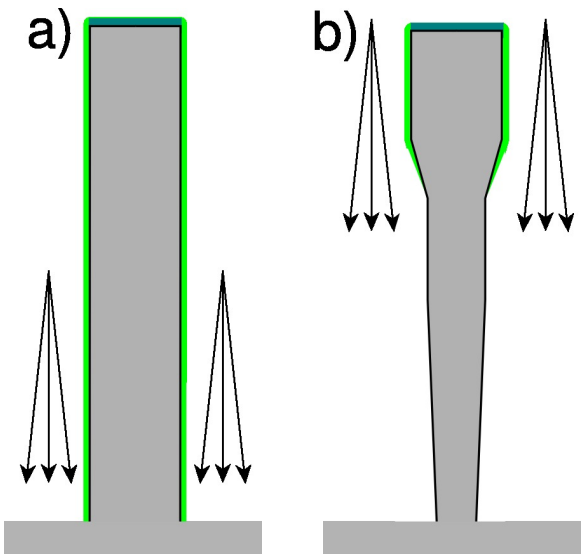


Figure 6.3: Schematic profiles of mixed mode etching. The dark blue on top of the pillars is the alumina mask and the bright green is the C_4F_8 passivation. a) Previously developed 'pseudo-Bosch' etch morphology. b) Morphology of etch by only reducing the flow rate of C_4F_8. Note that the bright green passivation has been stripped away the deeper the etch proceeds into the silicon.

forward power, plasma ion density, and mean free path, which in turn is governed by the constituent gas composition and pressure. In our case the biggest impact imparted on the etching morphology was increasing the forward power. For a relatively wide sample the power could merely be increased from 23 to 24 W in order to ensure a vertical etch; schematically this is represented in frame (a) of figure 6.5 and an SEM is shown in figure 6.6. The pillar would still be slightly re-entrant but a 1-2 nm undercut on a 1 micron tall, 100 nm wide pillar was acceptable. The effect of the increase in forward power is to collimate the ions impinging on the surface of the chip; in other words to decrease the spread of the IADF and increase the verticality of the etch. It is important to note that the increase in forward power also resulted in an increase in etch rate.

When we wanted to construct samples with diameters as small as 10 nm using this controlled undercut we needed to take some special precautions. It was no longer acceptable to have a 1-2 nm undercut on the pillar as it would result in ∼40% decrease in diameter of the 10 nm pillar, either destroying the pillar due to ion bombardment or causing it to buckle; an SEM of this is shown in frame (a) of figure 6.7. We improved our results by increasing the forward power by 0.5 W *and* increasing the passivation gas by 1 sccm for every ∼200 nm etched into the silicon. This can be seen in frame (b) of figure 6.7; note that the pillars in this SEM image have a narrowed diameter of roughly 20 nm. By perfecting the etch we were able to make flawless pillars with heights of 1 micron and widths down to 15 nm. A set of pillars made for the electroluminescent excitation of silicon (explained in the next chapter) are shown in figure 6.8. The tops of the pillars were intentionally

widened to allow for improved electrical contacting. Figure 6.9 shows an example recipe for etching such 'wine-glass' pillars.

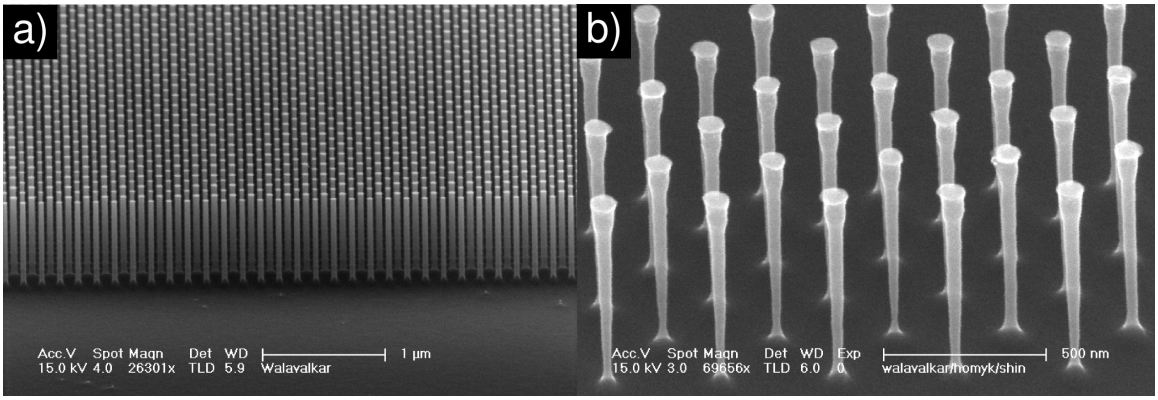


Figure 6.4: (a) SEM of the etch profile of a standard 'pseudo-Bosch' etch. (b) SEM of a mid-etch switch to underpassivation; the deeper the etch gets the thinner the pillar gets. The gas ratio in this etch was SF_6:C_4F_8 of 32:42 and the forward power was kept at 23 W.

6.1.2.2 Going from pillars to quantum dot templates

As is seen in figures 6.7 and 6.8 it is possible to make the widths of the pillars much narrower than their mask diameters. The primary consequence of this is the ability to fabricate 20 nm wide pillars with a 75 nm wide mask; allowing one to remove finicky sub-50 nm electron beam lithography and improving yield. The phenomenon that was particularly useful for this project was to arbitrarily change the diameter of the pillar in the vertical direction. This 'silicon sculpting' has proved to be valuable for a variety of projects. A simple representation of a simple in-down-out structure is shown in frame (b) of figure 6.5. An SEM image of such a structure is given in figure 6.10; note that the notch put into the pillars did not affect the vertical etching of the rest of the pillars. This narrow divot shape can be accomplished by dropping the passivation gas level to 42 sccm for 30 seconds and then switching it back to 55 sccm. The angled sidewalls indicate that there is a roughly 35 nm distance over which the etch changes from correctly passivated to under-passivated or from under-passivated to correctly passivated.

In order to turn this simple trick into a generator for quantum dots we needed to stack many copies of this notch on top of each other to make the remaining silicon look like beads on a string. The first few efforts resulted in beads that were the same diameter as the mask. The etch was just multiple copies of the 30 second oscillation of changing the gas flow of passivation to 42 sccm of C_4F_8. Since we did not change the forward power the etch began to narrow as we got deeper into the silicon. This procedure of a single quantum dot is shown in frame (a) of figure 6.11 and multiple dots in frame (b) of the same figure. SEMs of such pillars are shown in figure 6.12. When creating

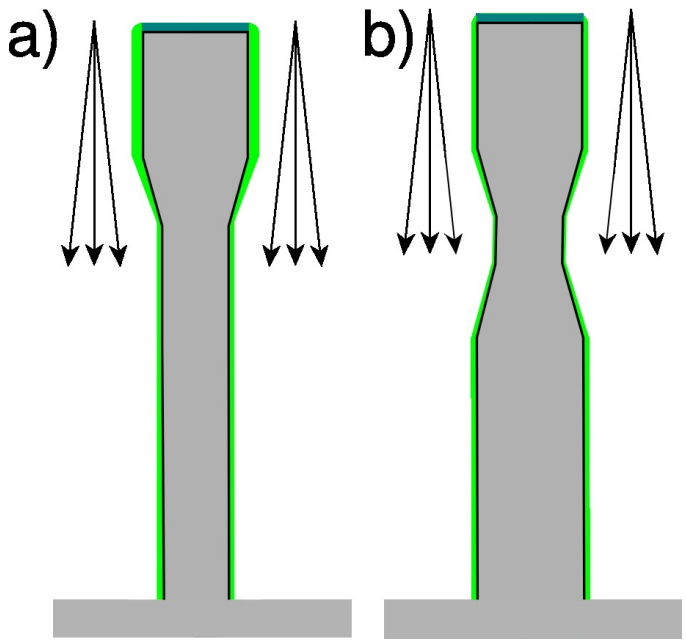


Figure 6.5: Schematic profiles of mixed mode etching. The dark blue on top of the pillars is the alumina mask and the bright green is the C_4F_8 passivation. (a) Previously developed 'pseudo-Bosch' etch morphology. (b) Morphology of etch by only reducing the flow rate of C_4F_8. Note that the bright green passivation has been stripped away the deeper the etch proceeds into the silicon.

a single quantum dot if we increased the forward power by 1 W and the passivation gas by 1 sccm when creating the second notch it was possible to make the two segments of 'string' attached to the 'bead' of even size and length. Examples of these 'bow-tie' shaped pillars are seen in frame (a) of figure 6.13. When we stacked multiple corrugations on top of themselves the structures began to look like the pillar drawn schematically in figure 6.14 and shown in an SEM image in figure 6.15.

Although these images look promising, they are not sufficient to create quantum dots after oxidation. Since the dots are the size of the mask, which is 50-75 nm, after oxidation they do not reach a small enough diameter to induce silicon to a direct band-gap material. The target diameters of the dots, after oxidation, are between 2-3.5 nm with a height of less than 5 nm. Schematically single dots and a stack of dots are drawn in figure 6.16. The first attempt involved rapidly oscillating the underpassivation (shorter than the time it took to etch 35 nm downward) so that the passivation condition would remain below normal the whole time both notches were etching. This did not end up producing the results we wanted but it did produce beautiful structure with very smooth, sculpted curves. An example of these structures are seen in frame (b) of figure 6.13, and for a narrower mask in figures 6.17 and 6.18. It was proposed that the time lag between the change in gas flow resulting in a change in lateral etching was responsible for allowing the diameter of the beads in the middle to widen to the diameter of the mask.

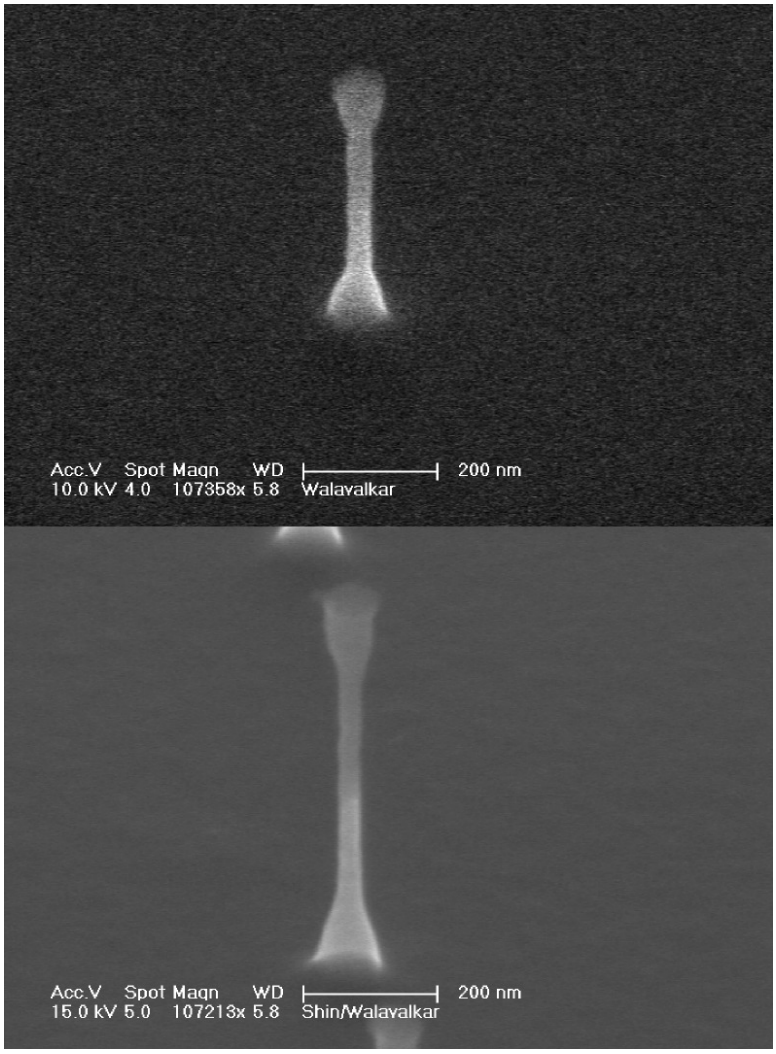


Figure 6.6: Two SEM images showing the ability to etch vertically at diameters smaller than the original mask diameter. The top image was etched at half the time of the bottom image; not that the thin portion of the pillar remains the same independent of height. The head and feet of these pillars are added for stability.

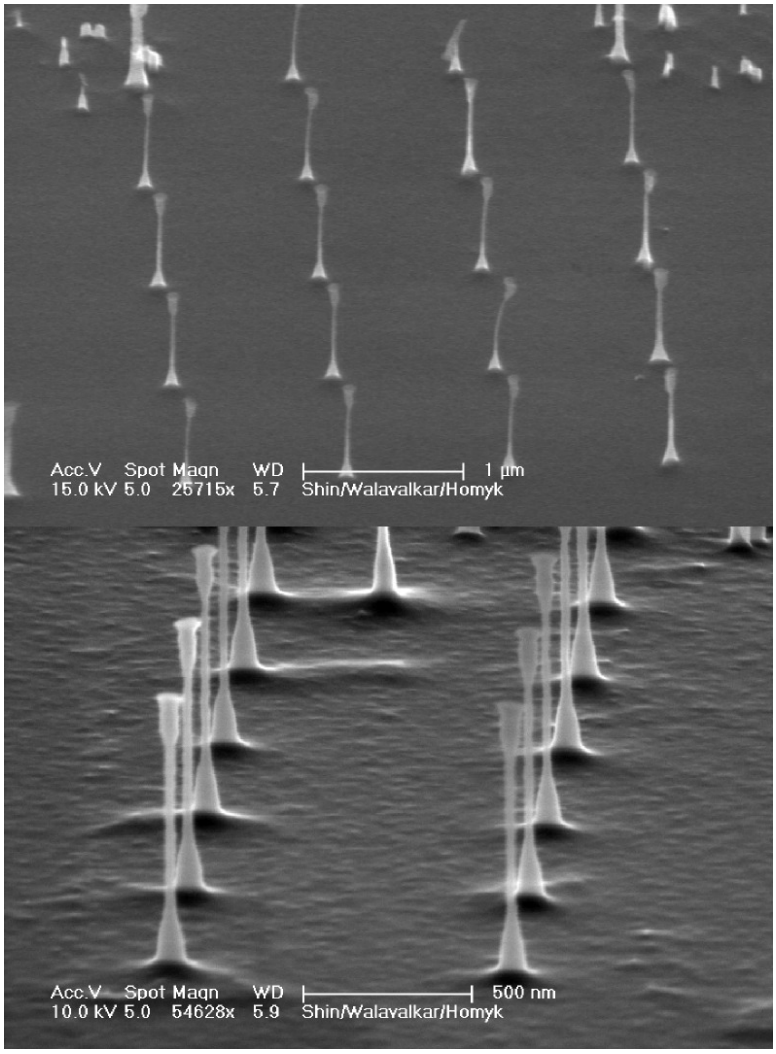


Figure 6.7: (a) SEM of pillars with diameters ($\sim$ 10 nm) that are getting close to being too narrow to support their own weight or have buckled due to local heating/cooling strain during the etch. (b) Thin diameter pillars with enough structural support to handle their weight and the tribulations of etching.

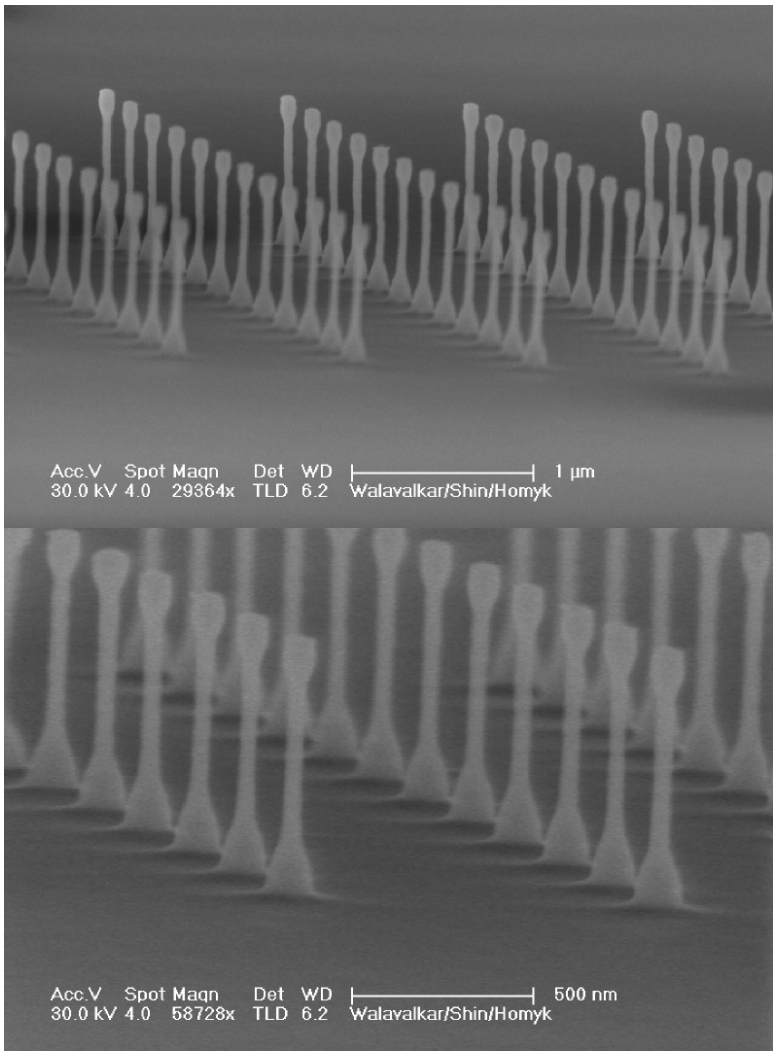


Figure 6.8: Slightly larger 'wine-glass' shaped pillars that are used for electrical contacting as described in the next chapter. In this case the head is for easier electrical contacting.

Time	Depth	Gas Ratio	Fwd Power
0.0-0.5 min	075 nm	32/55	23.0 W
0.5-1.5 min	275 nm	32/42	23.5 W
1.5-2.5 min	475 nm	32/43	24.0 W
2.5-3.5 min	675 nm	32/44	24.5 W
3.5-4.0 min	750 nm	32/56	23.0 W

Figure 6.9: Recipe for etching a wine-glass shaped pillar with a head the size of the mask, a thin body, and a mask sized foot for stability. An example of the use of such a recipe is shown in 6.8

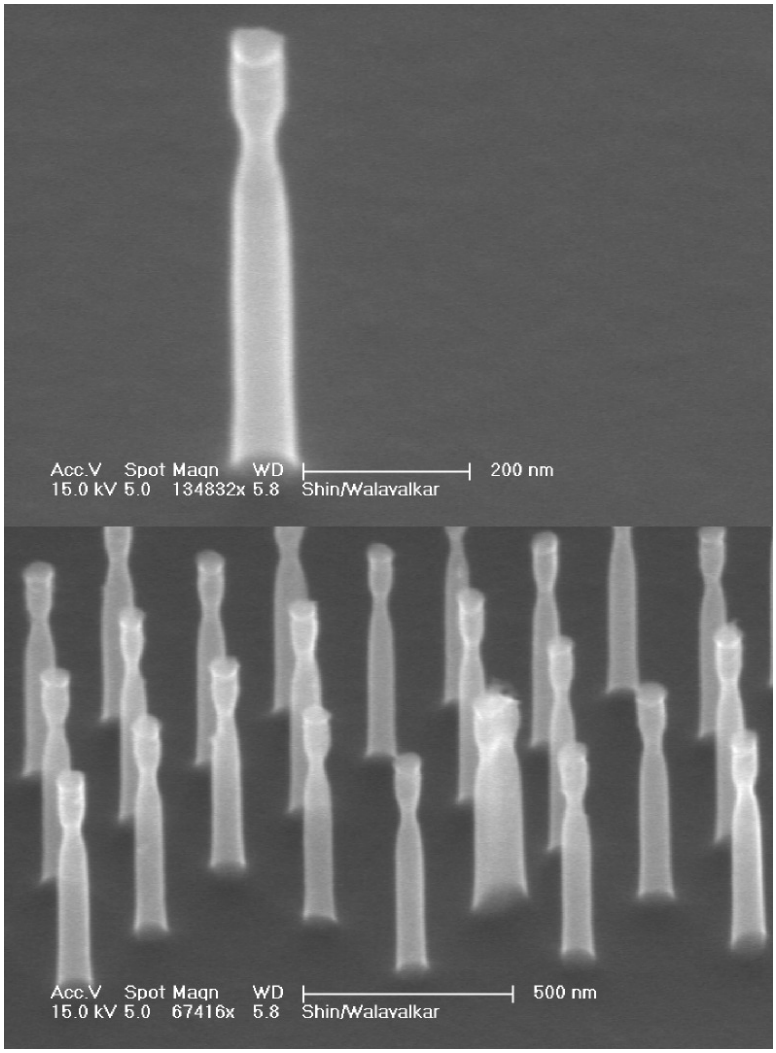


Figure 6.10: (a) SEM of a pillar with a single notch carved out as the etch progressed downward. (b) SEM of an array of notched pillars; note the uniformity across the set of pillars.

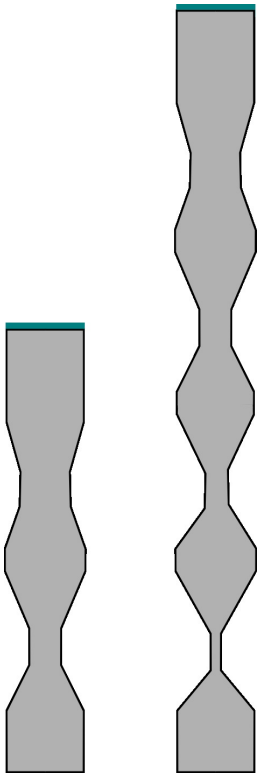


Figure 6.11: Schematic diagram of a single dot structure (left) and a multiple dot structure (right). In this case only the passivation was changed to create multiple dots and therefore the undercut sections begin to narrow as the etch progresses deeper into the silicon.

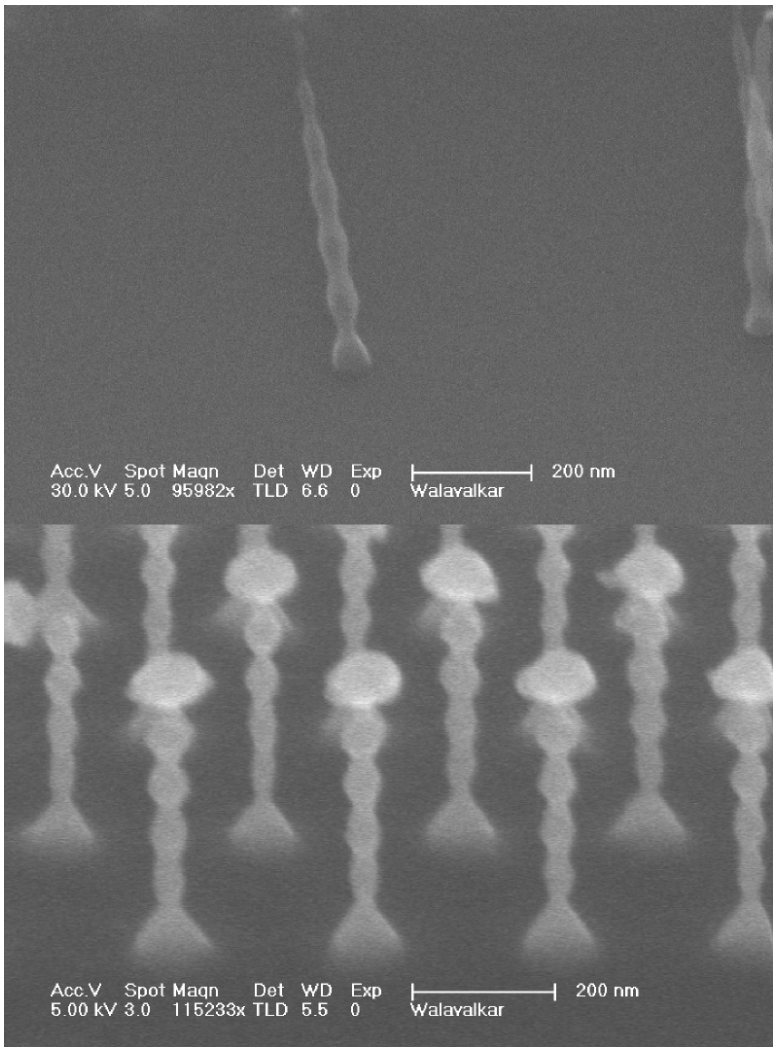


Figure 6.12: Examples of etches done with only passivation modification to produce numerous dots. In the top picture the pillar has become so narrow that it has snapped off its base. In the bottom picture one can see the dots decreasing in size the deeper the etch proceeds into the silicon.

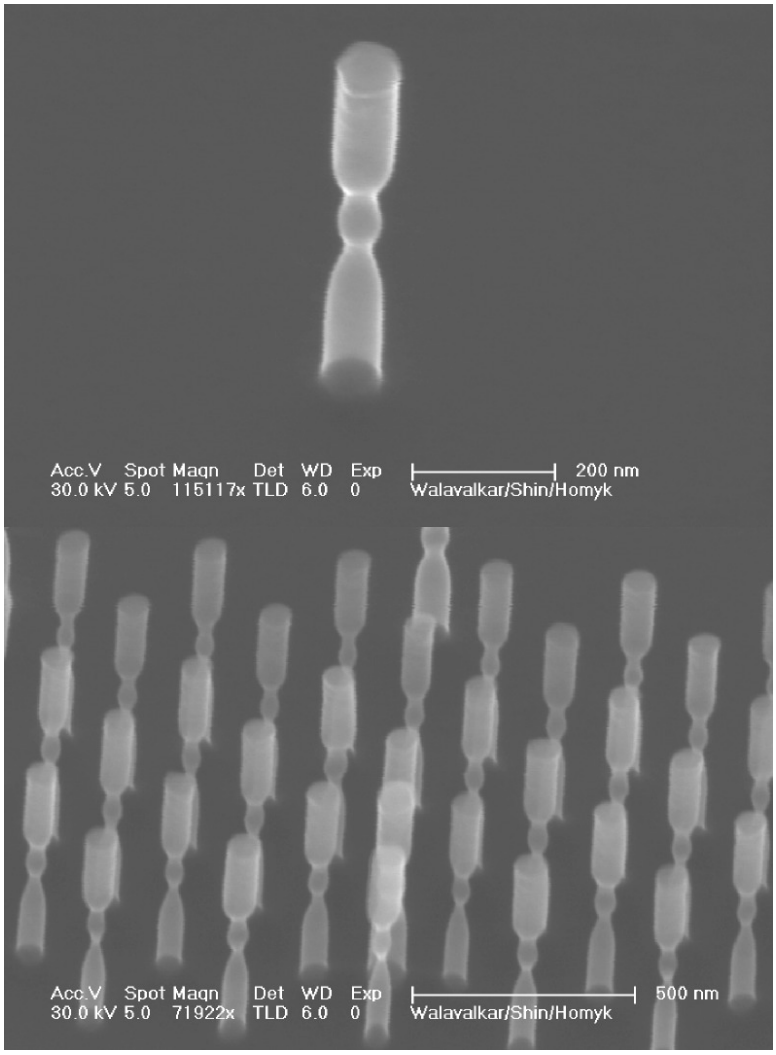


Figure 6.13: Single dot structures made by modulating both the passivation and forward power. Note, however, that the dots in the middle have diameters roughly equal to the original mask.

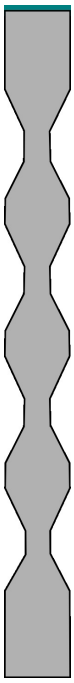


Figure 6.14: Schematic of a vertical stack of dots with equal 'bead' and 'string' diameters made by a modification of both the forward power and the passivation gas flow.

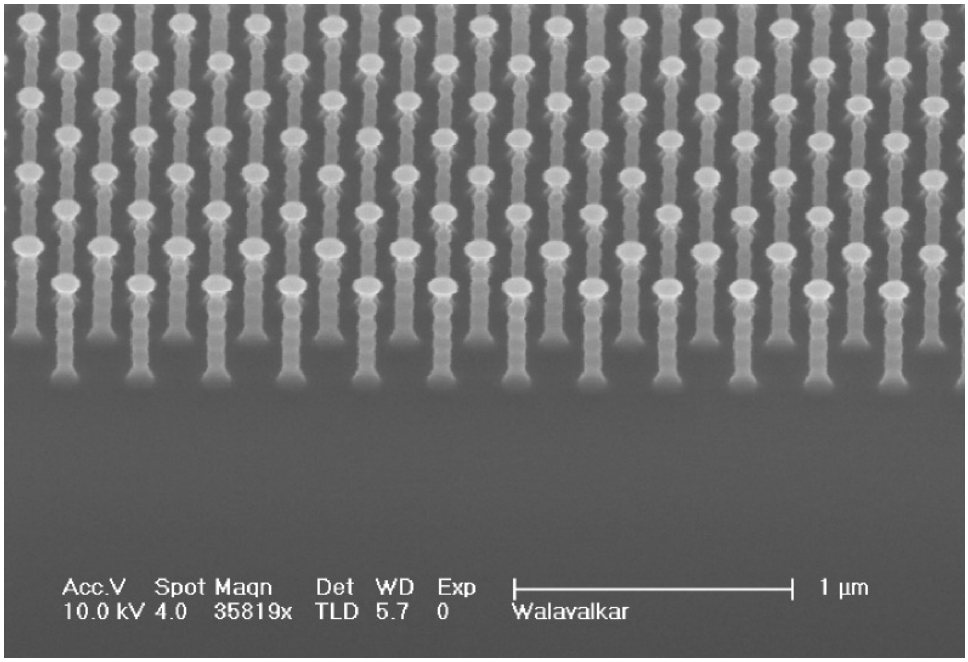


Figure 6.15: Pad of pillars with multiple, evenly sized dots that are slightly smaller than the mask diameter.

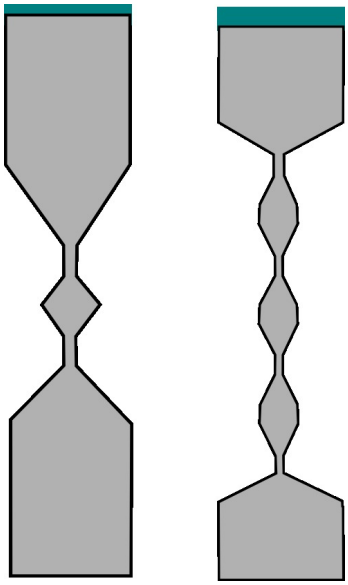


Figure 6.16: Schematic drawing for a vertical single quantum dot and for a vertical stack of three quantum dots.

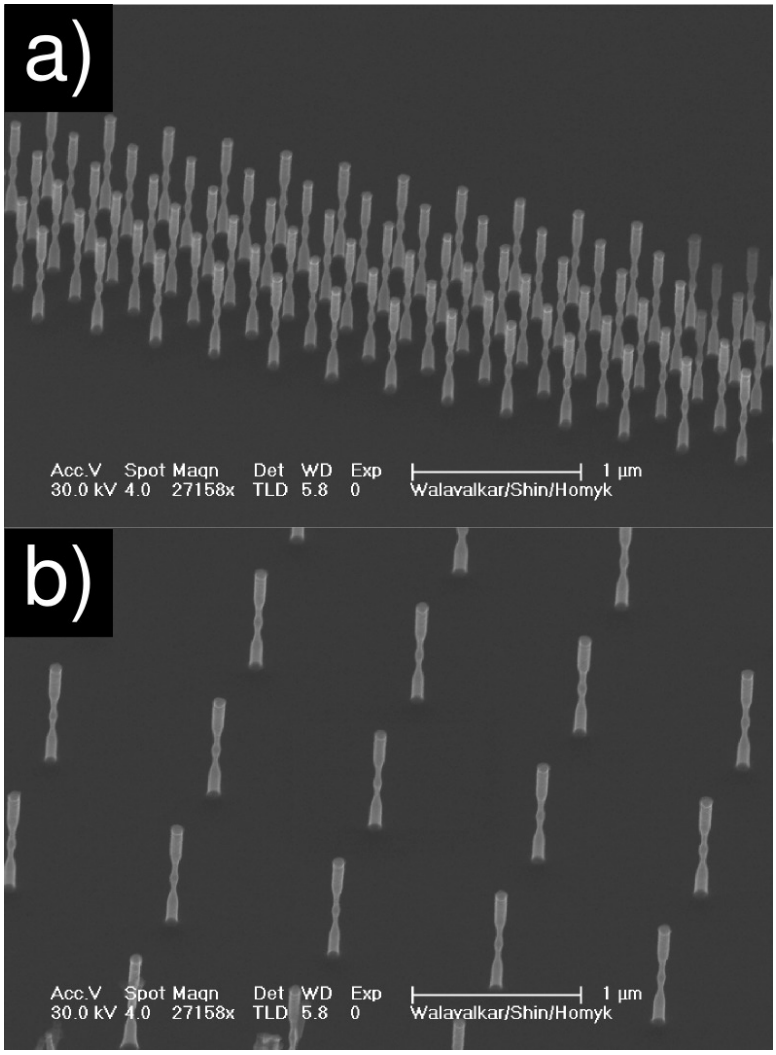


Figure 6.17: Pads of numerous single dot structures etched by oscillating the passivation from under to correctly passivated twice. Note that the size of the dots are still roughly the size of the mask.

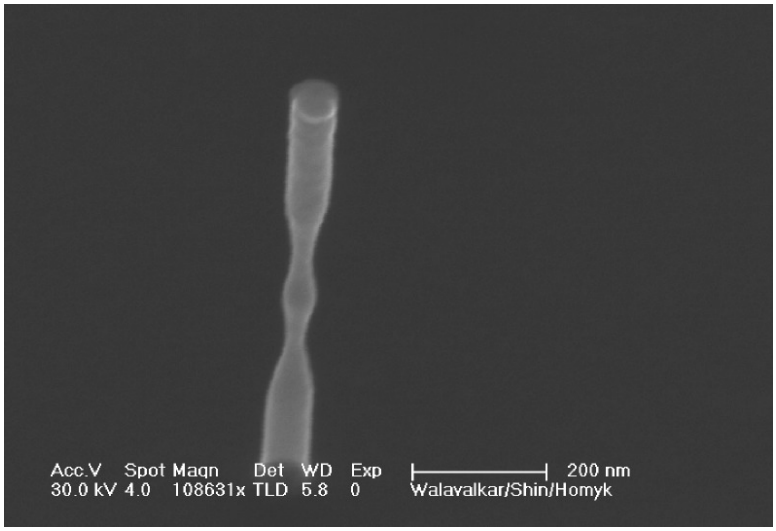


Figure 6.18: A close up on a single dot structure etched by oscillating the passivation from under to correctly passivated twice. Note that the size of the dot is still roughly the size of the mask.

The solution that was found was to make asymmetric notches. After etching a head on the structure the pillar would be undercut to a very thin diameter (∼20 nm) and the bead was fabricated by only increasing the passivation gas flow by ∼5 sccm then down to the same 'string' diameter and back to standard etching conditions to make a foot-like support for the dot in the middle. The result is shown in figure 6.19.

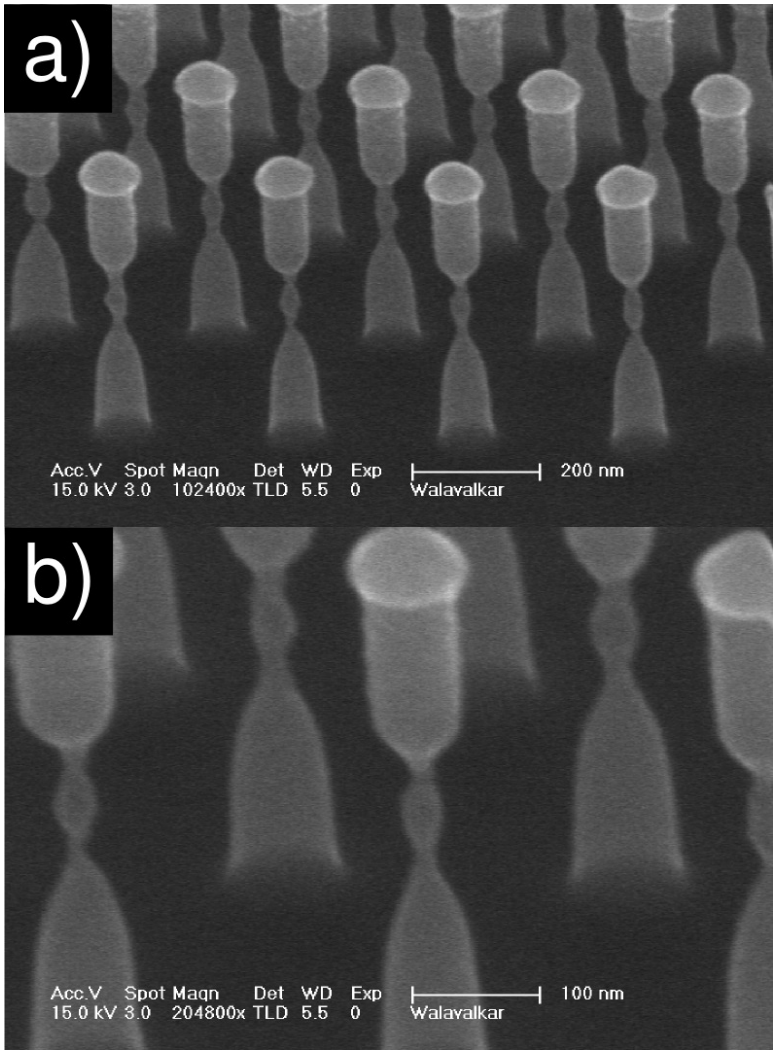


Figure 6.19: Wide and close-up SEM of 'bow-tie' pillars that can be used for testing of room temperature quantum phenomena.

These types of 'bow-tie' structures are interesting in terms of designing a vertical, tunneling current, transistor that can probe the Coulomb effect or other quantum phenomena. A schematic representation of the oxidation of a bow-tie pillar and the fabrication of such a device is given in figure 6.20; fabrication of the vertical gates and spacers is described in the next chapter. Note that to increase the magnitude of the tunneling current it is important to shorten the connectors to

the beads as tunneling current (I) typically drops exponentially with distance following a behavior roughly described as:

$$I \sim const \times V_{applied} \times \exp(-C \times d), \tag{6.1}$$

where $V_{applied}$ is the applied voltage, C is a constant and d is the distance. Unfortunately these structures are not ideal for PL as the large amount of silicon left over after oxidation in the head and foot serve to screen out much of the absorption and emission.

If we wish to stack numerous identical quantum dots atop each other we need to repeat this narrowed bead structure several times in the vertical direction, as drawn in figure 6.16; we need to take into account the increased lateral etching the deeper we carve into the silicon. An example recipe for fabricating the structure seen in figure 6.16 is given in figure 6.21. We note that since the height of these kinds of pillars is relatively short, we only have to increase the power by 1.0 W during the etch. SEMs of structures etched in this manner are shown in figures 6.22 and 6.23. Note that the dots in these structures are very close in horizontal diameter for each pillar/array allowing for the terminal diameters after oxidation to have a narrow distribution.

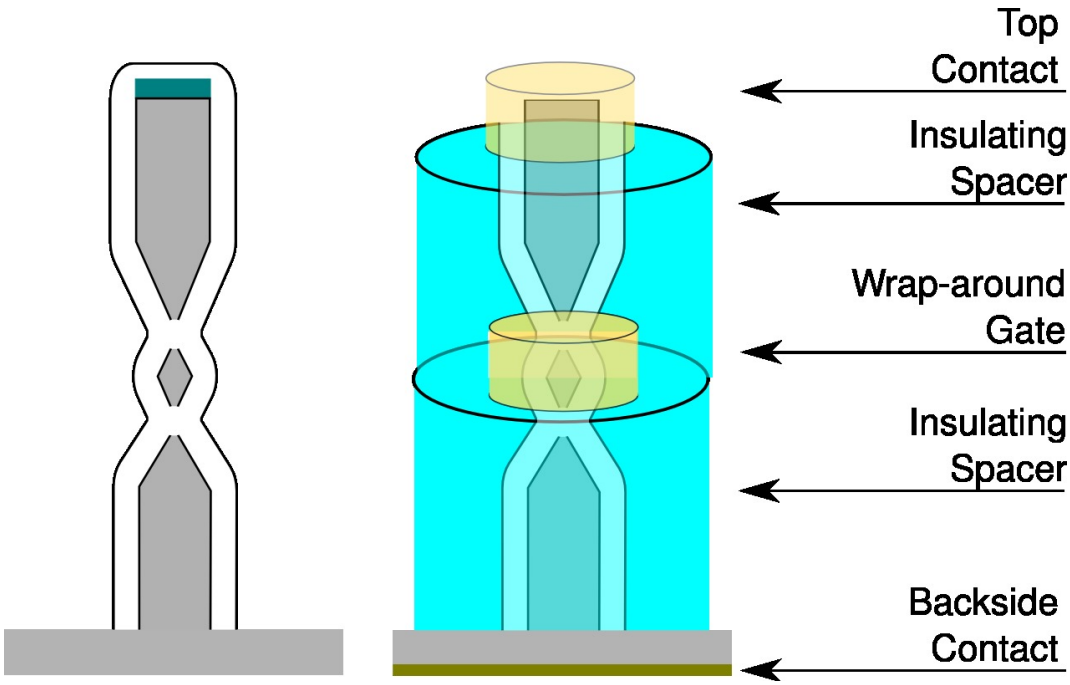


Figure 6.20: Schematic of bow-tie pillar after oxidation and an example of a tunneling current transistor.

Step Time	Depth	Gas Ratio	Fwd Power
30 sec	075 nm	32/55	23.0 W
07 sec	095 nm	32/35	23.0 W
10 sec	135 nm	32/40	23.5 W
07 sec	155 nm	32/35	23.5 W
10 sec	190 nm	32/40	23.5 W
07 sec	210 nm	32/35	23.5 W
10 sec	245 nm	32/40	24.0 W
07 sec	260 nm	32/35	24.0 W
30 sec	335 nm	32/56	23.5 W

Figure 6.21: Recipe for etching three dots that are significantly smaller than the original mask diameter bracketed by a head and foot.

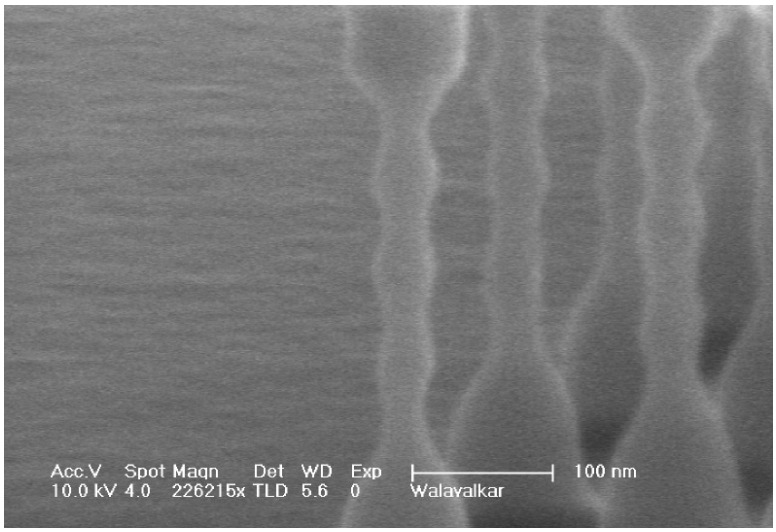


Figure 6.22: Large set of dots fabricated with a modification of the recipe given in figure 6.21 in order to slightly increase the pre-oxidation dot diameter.

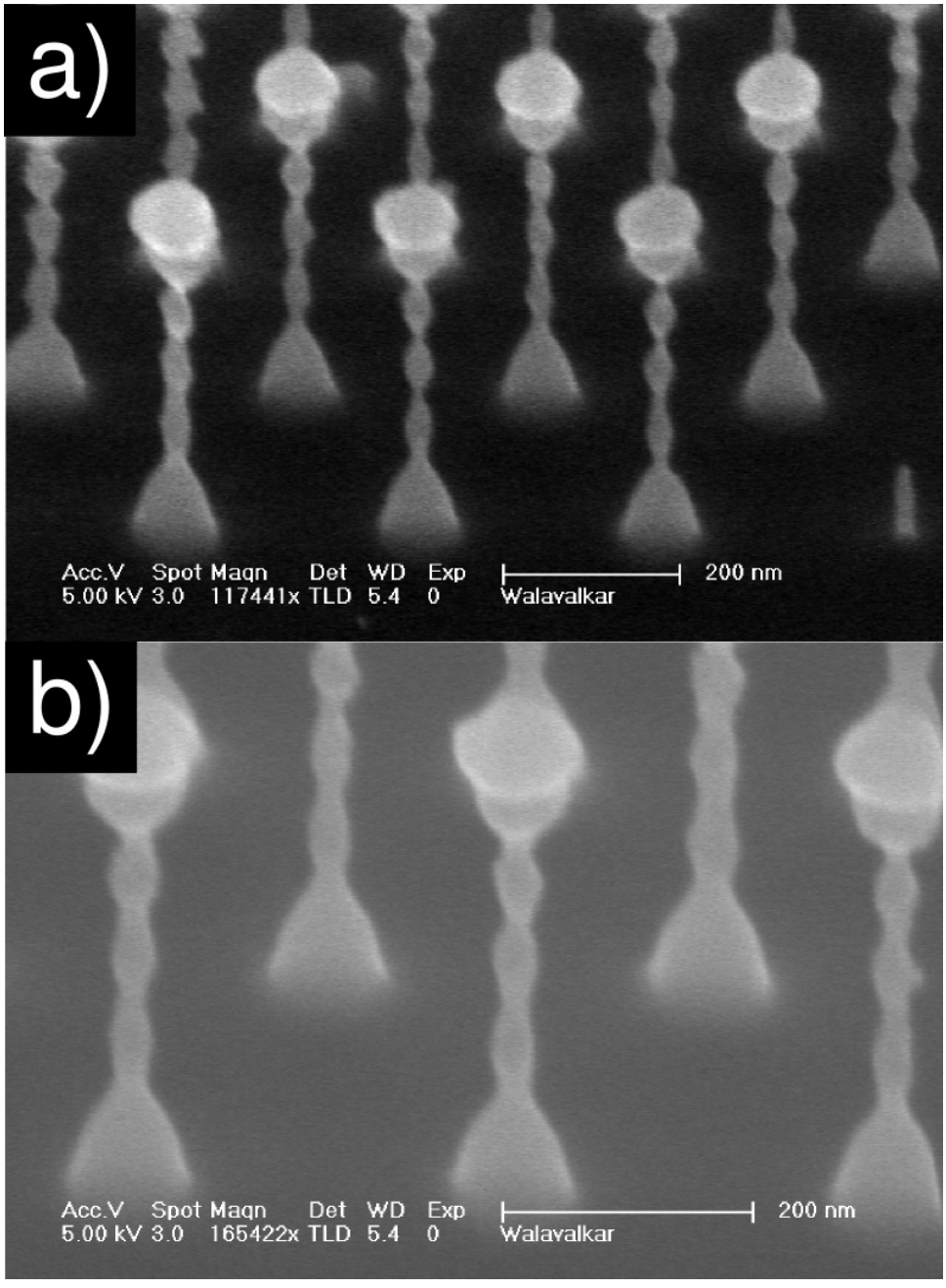


Figure 6.23: (a) Set of pillars etched with the recipe given in figure 6.21 except with etch times doubled. (b) A set of pillars with slightly larger dots etched with a variation of the recipe given in figure 6.21.

6.1.3 Oxidation and characterization

The quantum dot pillars were oxidized similar to the way the vertical side-wall pillars were oxidized in the previous chapter. Some differences to note were that the initial diameters of the dots were smaller than those of the vertical side-wall pillars and that the shape of these dots made the oxidation both three-dimensional, as well as anisotropic due to the longer vertical length in comparison to the horizontal diameter. The final shape of the dots after oxidation tended to be that of a vertically oriented football. A schematic of the desired post-oxidation shape of the pillars is seen in figure 6.24. The immediate viewable consequence of the oxidation was to round the sharp curves of the as-etched samples.

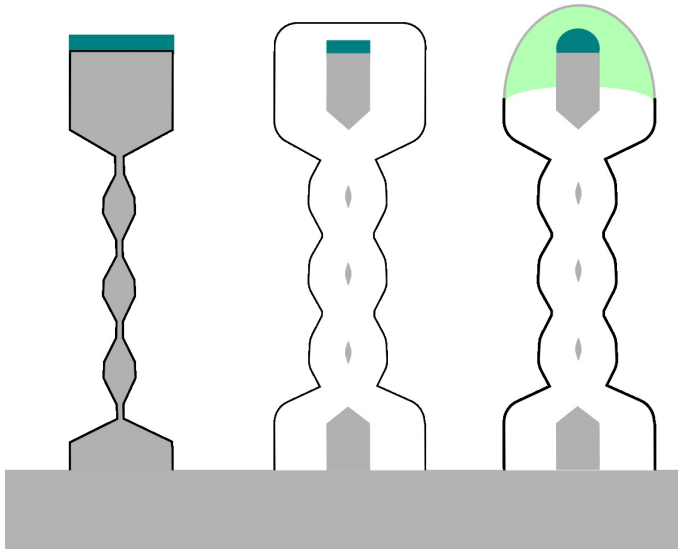


Figure 6.24: Schematic of the desired post-oxidation TEM image. The pillar on the left is pre-oxidation. The middle pillar is the oxidized version of the left pillar. The rightmost pillar is the resultant oxidation of a pillar with a hemispherical e-beam deposited alumina mask.

Figure 6.25 shows a RTEM image of a square pad of pillars; taken through a corner of the square. The rings are a result of electron diffraction by the single-crystal silicon lattice. Frame (b) gives a closeup of the right-most pillar; highlighting its diffraction pattern. It is also possible to see two broken pillars that were snapped, possibly during the scribing of the sample down to 2 mm $\times$ 1 mm in order to mount it on the RTEM stage in the TEM.

Figure 6.26 shows three conditions of RTEM exposure to extract details from an oxidized pillar. Frame (a) shows the pillar in a standard light-field, density map condition. Note that this pillar has very smooth curvature; a consequence of the oxidation process. Furthermore, due to the sputtering machine being down for repair, electron beam evaporated alumina was used as a mask, resulting in the 'hat shaped' cap on top of the pillar. Frame (b) shows a dark-field image where diffraction

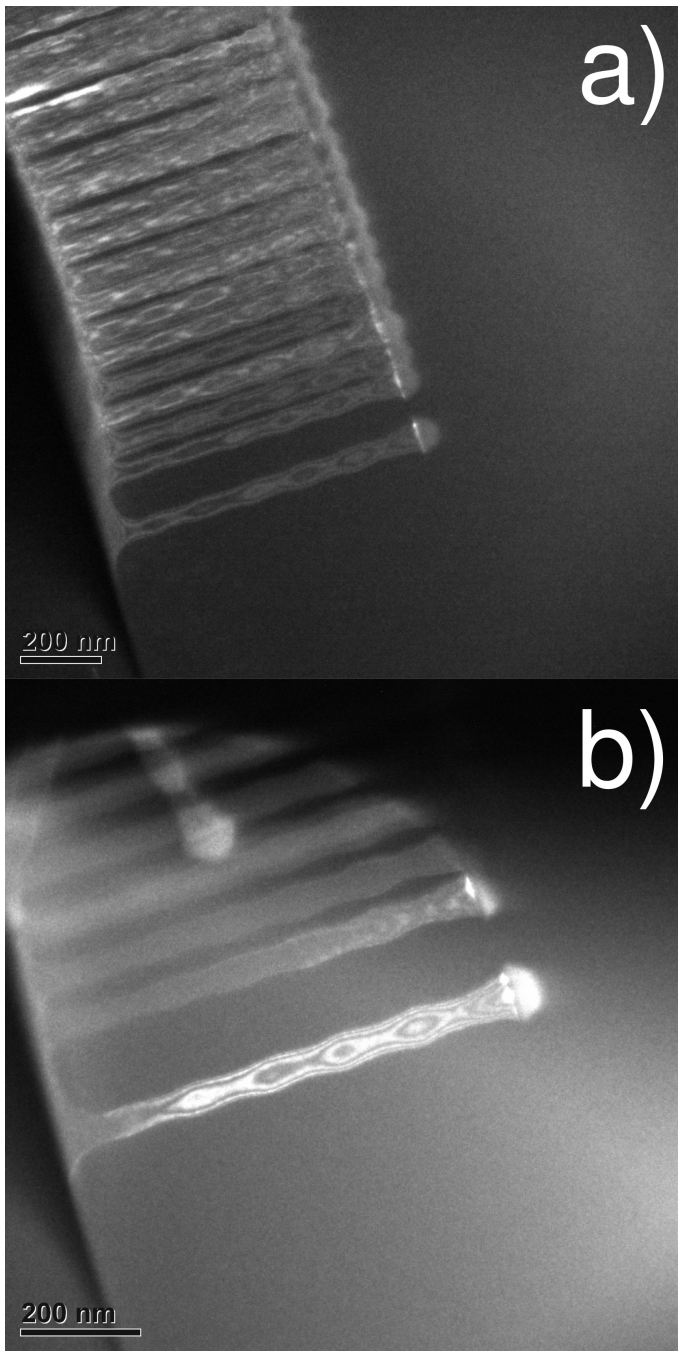


Figure 6.25: Reflection TEM images of corrugated pillars after etching but before oxidation; the caps are the e-beam deposited alumina mask. The light and dark fringes are indications of the single crystal nature of the silicon.

contrast has been used to pick out portions of the polycrystaline alumina in the mask. The final frame shows a different diffraction condition which attempts to pick out the single crystal silicon dots within the oxidized sheath. One dot is seen near the top of the pillar and the dotted box is blown up in the inset. The RTEM method, while useful for non-destructive TEM measurements, often had difficulty maintaining a precise enough focus to pick out quantum dots, even with the diffraction aperture in place. Furthermore an exceptional amount of beam current was required to see the dots with simple density mapping. Figure 6.27 shows a sequence of photographs that show the result of imaging a quantum dot with R-TEM. A wide angle view of a set of pillars is shown in the top frame. A close up on square box on the left-most pillar shows the large, (too large to photoluminesce due to lack of size dependent band modification) football-shaped, quantum dot. The final frame shows the result of such a high beam current being focused down to such a small radius; showing the oxidized pillar has melted and begun fall over. In this condition it was not possible to see the quantum dot anymore.

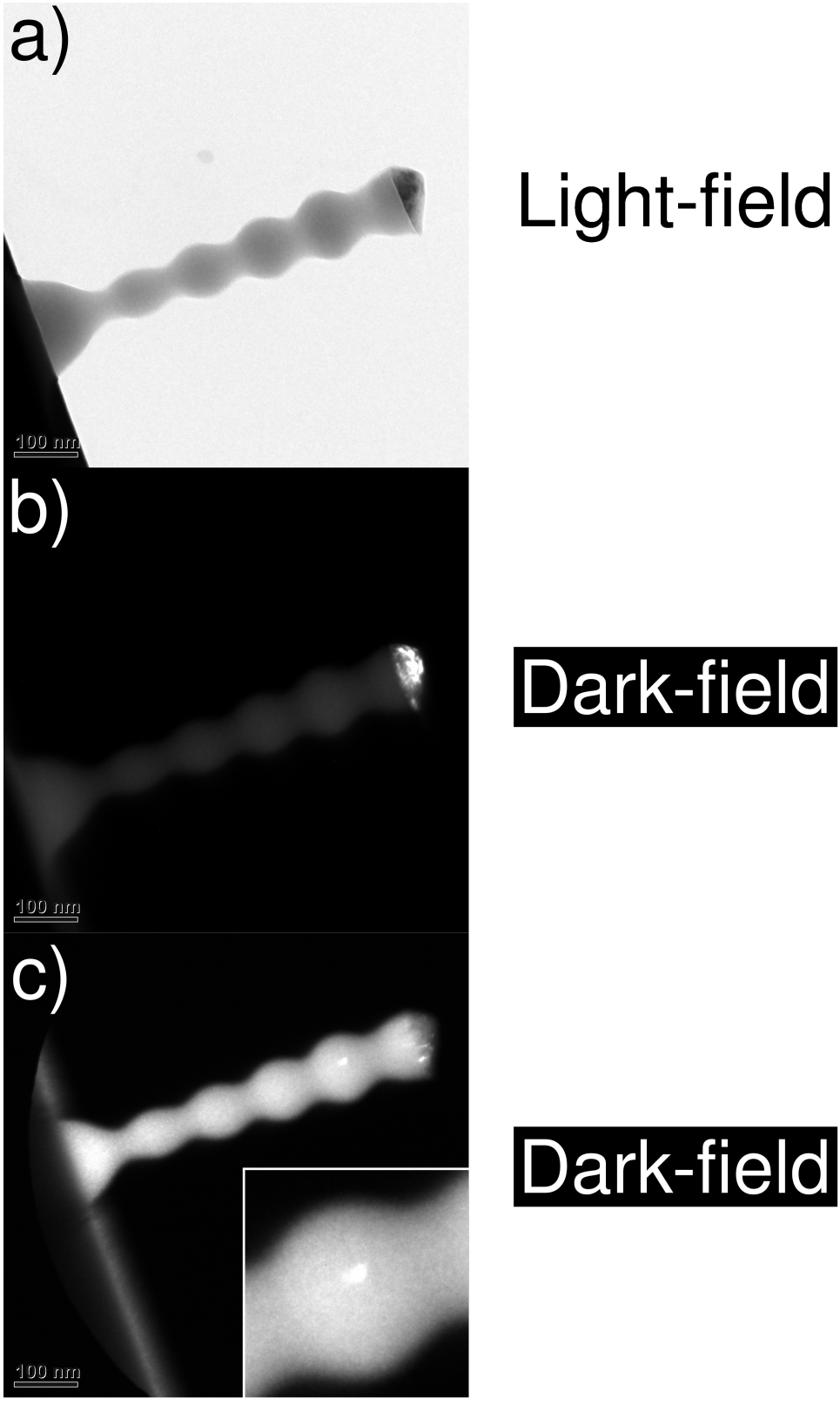


Figure 6.26: Three images of the same corrugated pillar. (a) Light-field density mapping. (b) Dark-field with diffraction contrast to highlight the mask. (c) Dark-field with diffraction contrast to highlight the small quantum dot in the topmost bead. The inset shows the diffraction from the silicon inside the amorphous silica.

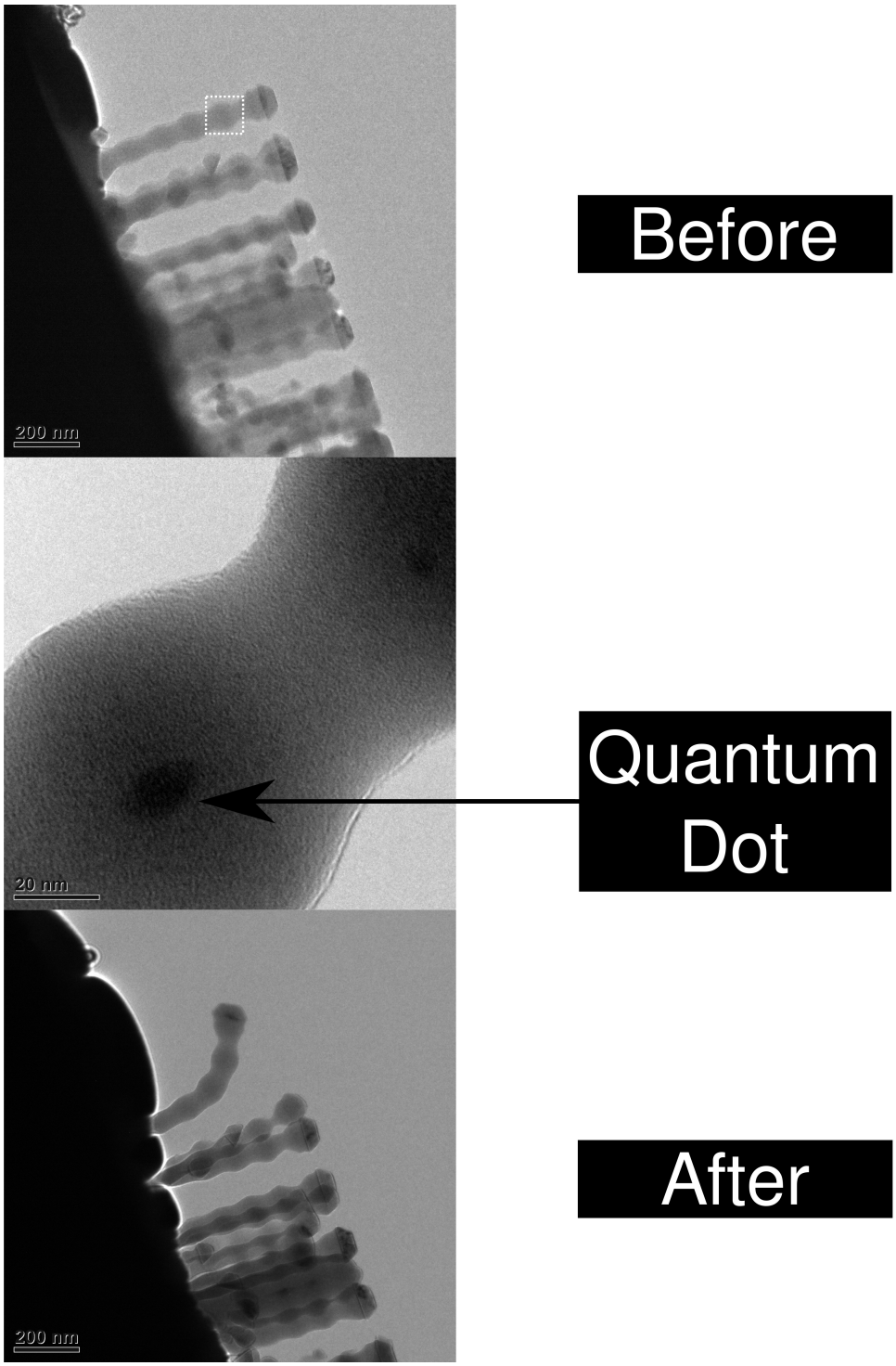


Figure 6.27: The consequences of imaging oxidized pillars with high beam current in reflection mode. The pillar is imaged with a lower maginification in the top image. The middle image shows the quantum dot present in one of the corrugations. The bottom image shows the melted pillar due to electron imparted heating.

To obtain better images of the quantum dots within the silicon dioxide it was necessary to cleave the pillars off of the substrate and onto a copper TEM grid. Since this method was destructive to the sample it was only done after the testing of a given sample was completely finished. Figure 6.28 shows the improvement in image quality with pillars sitting on the copper grid. In this image it is possible to see the remnant, acorn shaped silicon in the head of the pillar and it is possible to make out the much smaller quantum dot in the first bead. Note that this sample is an oxidized example of the pillars in frame (b) of figure 6.23.

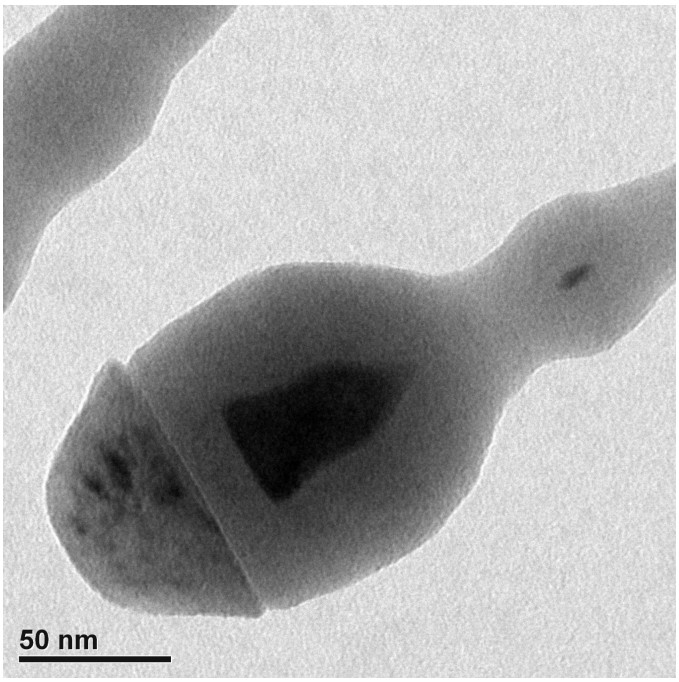


Figure 6.28: Image of the head of the pillars etched in frame (b) of figure 6.23. Note the acorn shape of silicon in the head of the pillar and the football shaped quantum dot in the first bead.

Even with this method it was difficult to make out the oxidized quantum dots. We atempted to make direct measurements of the size of the embedded quantum dots, however as explained later, this size estimation was to inaccurate and the actual size estimation was conducted with another method. In figure 6.29 frame (a) shows the image as taken from the TEM. It is barely possible to make out the three quantum dots in the three oxidized beads; depending on the medium in which this work is read the contrast may be too low to see them. Frame (b) consists of the same image, made translucent, with post-processed contrast/brightness tweaking, laid over the original image in frame (a). Dotted circles are added as guides for the eye. With this enhancement it is easier to see the general position of the quantum dots, although their size remains ambiguous. Figure 6.30 shows a similar TEM and processed image with dot locations circled with a white dashed line. Both of these figures highlight the difficulty in measuring the actual quantum dot size through 50-100 nm

of thermal oxide, using density mapping alone.

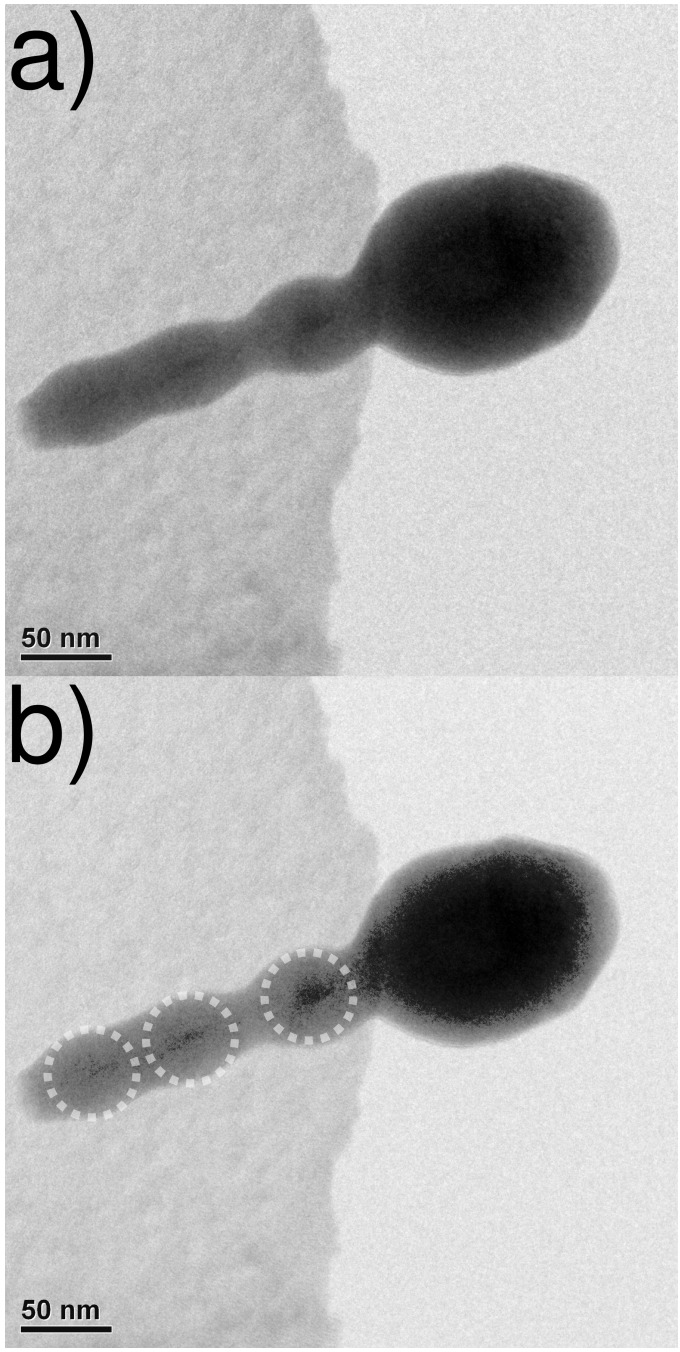


Figure 6.29: (a) TEM image of a corrugated pillar on a copper grid. The quantum dots are present but are only weakly visible. (b) Enhanced image of the quantum dots with their general locations circled.

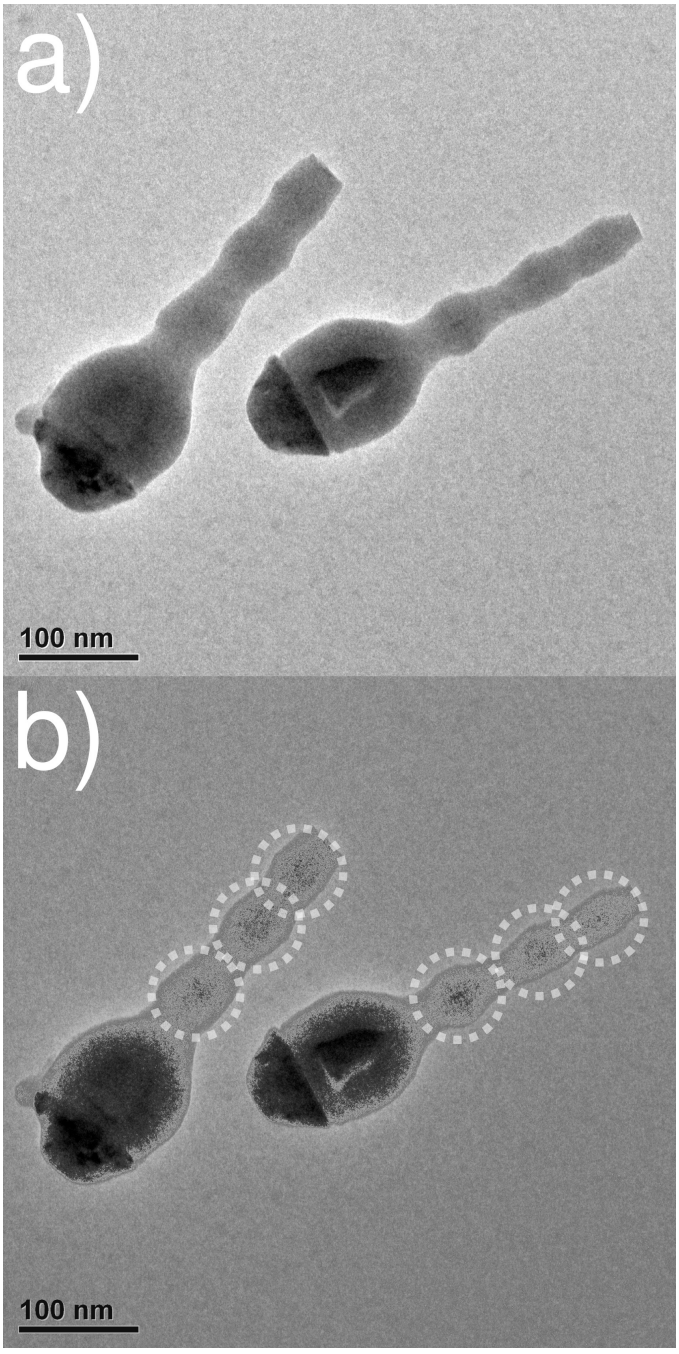


Figure 6.30: (a) TEM image of a corrugated pillar on a copper grid. The quantum dots are present but are only weakly visible. (b) Enhanced image of the quantum dots with their general locations circled.

In order to increase the visibility of the oxide encapsulated dots a dark-field, diffraction contrast method was used. The diffraction aperture was used to preferentially pick out electrons diffracted from the single crystal silicon inside the pillar showing up as bright white sections, while the randomly scattered electrons from the amorphous silicon dioxide show up only as a darker gray pattern. An example of this is seen in figure 6.31. In both the images in that figure the bright white ball visible in the center of the oxide is the acorn shaped remnant of the head of the pillar from the sample seen etched in frame (a) of figure 6.23.

Figure 6.32 shows a pillar under two different diffraction conditions. In frame (a) only the electrons passing through the silicon chunk in the head are seen. The fact that the structures retain their single crystal behavior even after etching and oxidation is shown by the diffraction rings appearing on the silicon in the image. Frame (b) shows a second diffraction image where the electrons scattered through the first dot are collected by the detector. Uniform illumination from the first dot is an indication that the silicon remains a single crystal even after etching and oxidations; illumination at a different diffraction condition than the silicon in the head implies that although the silicon remained crystalline perhaps the oxidation related strain deformed the lattice.

The images in figure 6.33 show the quantum dots within the pillar by utilizing the diffraction aperture. It is, however, not advisable to use such an image to estimate the size of these dots as their extent is roughly the precision of the focus. If 10 images are taken there could be a variance as large as 1 nm; with the dots being 2-4 nm in diameter this is far too large of a variance to use to size the dots. This technique does, however, provide a useful method to show (after optical testing) that quantum dots were in fact present in the pillars

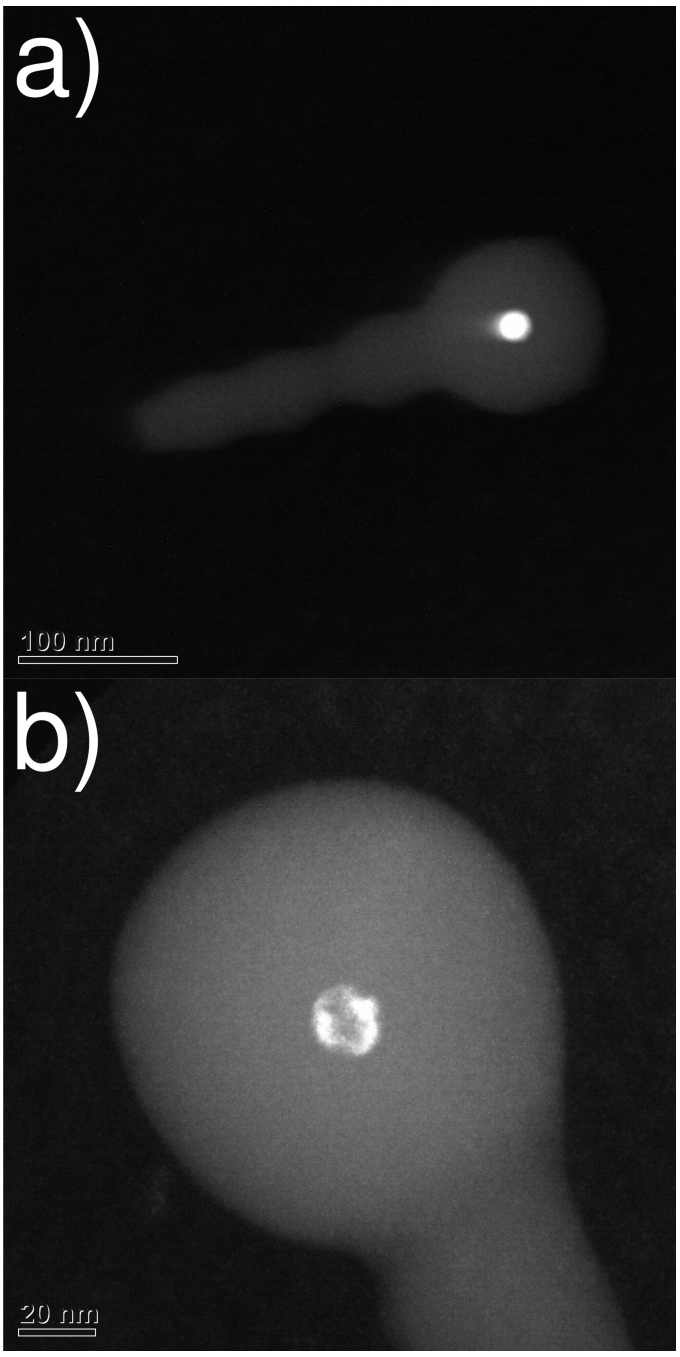


Figure 6.31: (a), (b) TEM images of oxidized pillars from the sample seen in frame (a) of figure 6.23. The dot seen is actually the remnant of the silicon chunk in the head; with a final diameter of slightly less than 20 nm.

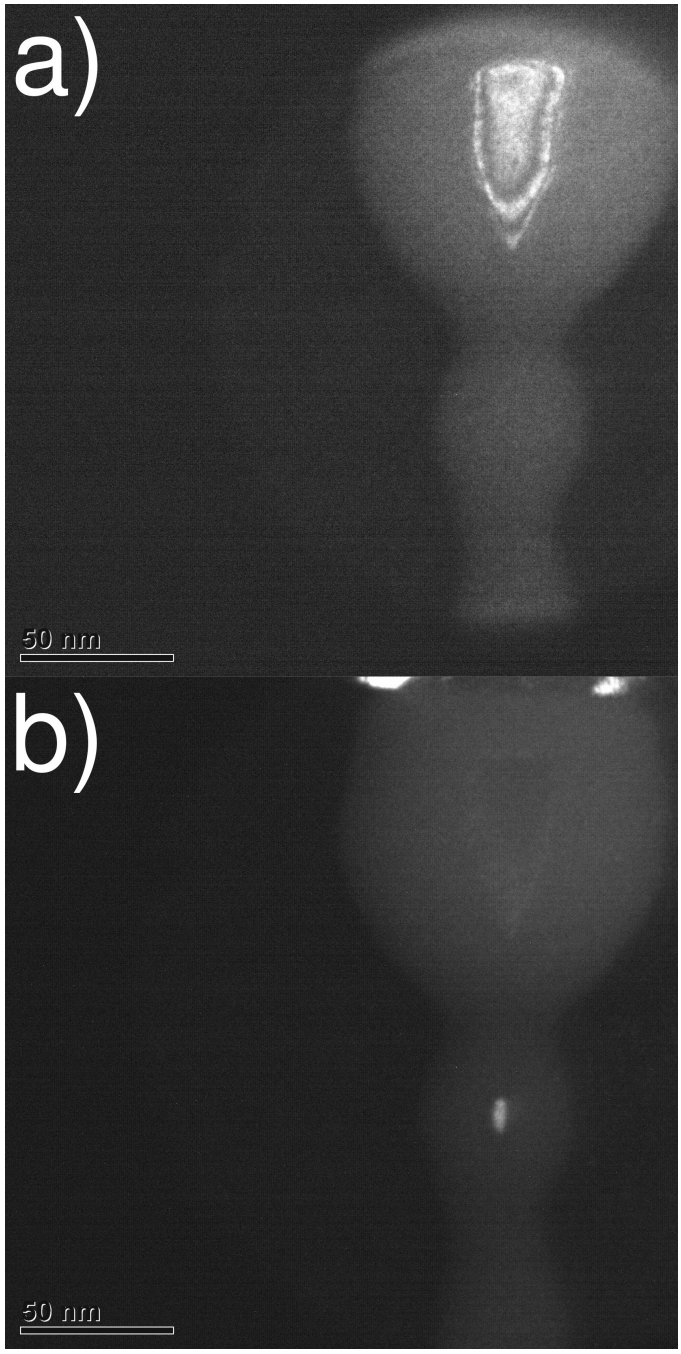


Figure 6.32: A pillar under two different diffraction conditions: (a) Only the electrons passing through the silicon chunk in the head are seen. Note the diffraction rings present in the silicon chunk at the top. (b) The same pillar under a different diffraction condition which highlights the first quantum dot.

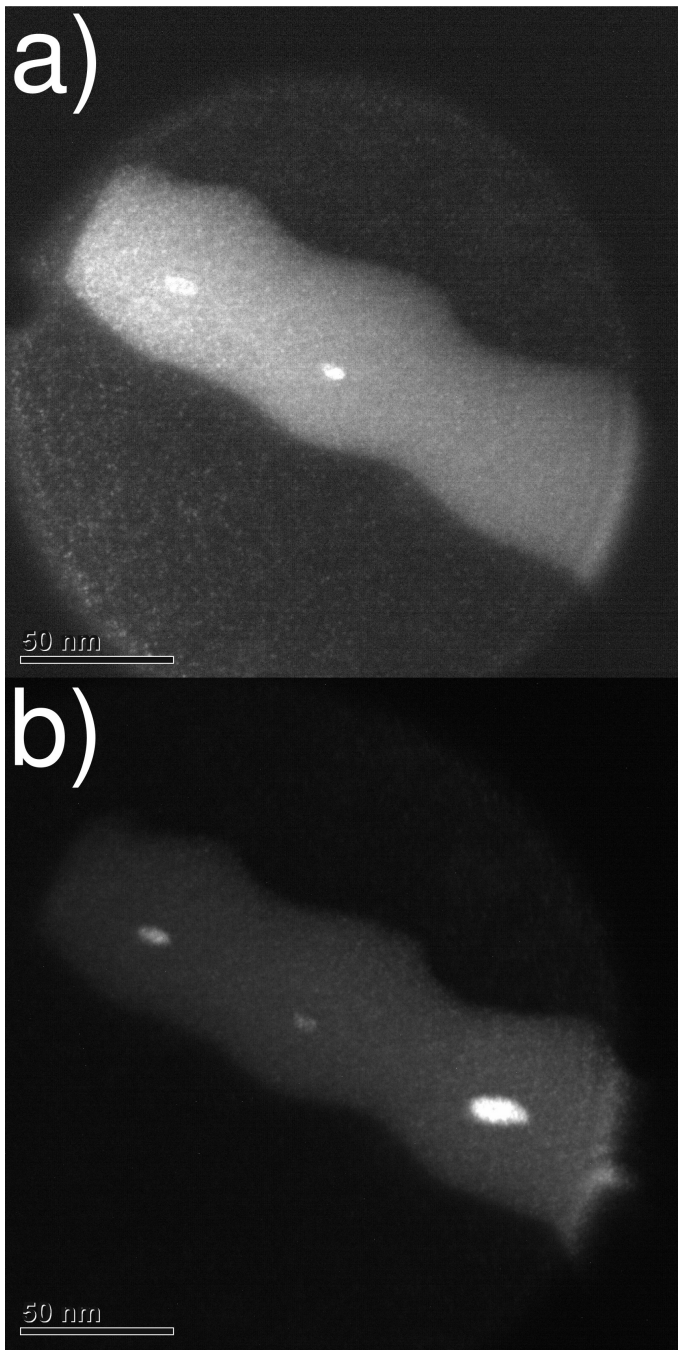


Figure 6.33: TEM image of the same pillar under two different diffraction conditions: (a) Condition which only shows the bottom two dots. (b) Condition where all three dots are visible with better contrast to the amorphous silica.

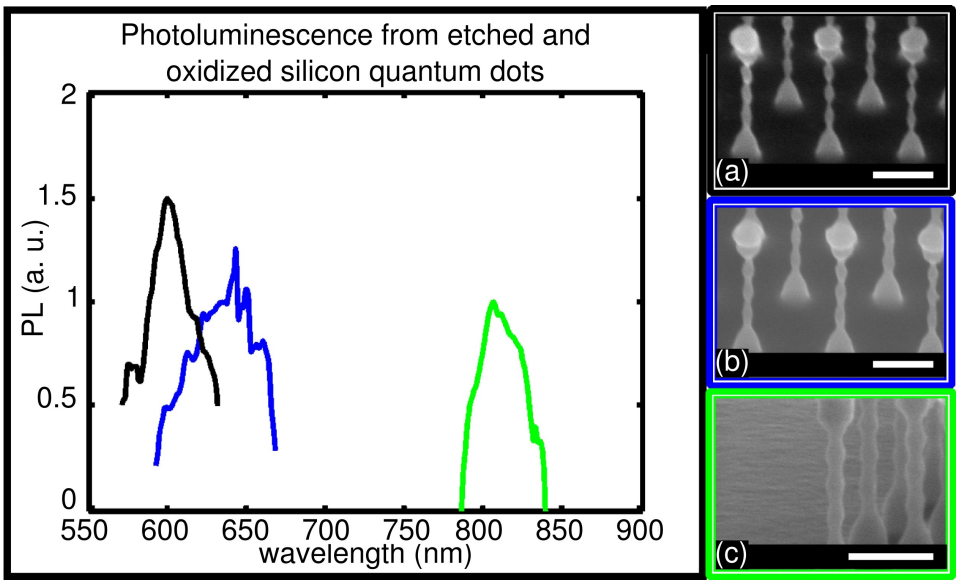


Figure 6.34: Photoluminescence spectra of three samples of etched and oxidized quantum dots of with different initial corrugation diameters. The colorized frame of the SEM images correspond to the measured, plotted spectra. The pre-oxidation size is 30 nm, 37 nm, and 45 nm for the (a) black, (b) blue and (c) green samples, respectively. Note that the larger the pre-oxidation size of the corrugated pillars the longer the peak emission wavelength. Scale bars are 200 nm in each frame.

6.2 Testing

The three samples tested are shown before oxidation as colored frames in figure 6.34, the diameters are roughly (a) 30 nm (black), (b) 37 nm (blue), and (c) 45 nm (green), and the corrugations have a period of approximately 60 nm for each sample. Microphotoluminescence (μPL) was performed in an inverted optical microscope setup with a 457 nm free-space argon ion laser used to pump the sample; the full experimental setup is described in the previous chapter. The 457 line of the argon laser was used in this case to ensure that there was enough spacing between the laser line-width, the filter cut-on, and the emission from the quantum dots.

6.3 Results and discussion

The data collected from three samples with different pre-oxidation sizes is shown in figure 6.34. The color of the frame around the SEM images corresponds to the curve plotted in the figure. It can be seen that there is a correlation between the original size of the etched corrugations and the peak emission wavelength of the oxidized quantum dot. Peak emission was found to be at roughly 600 nm (2.06 eV), 640 nm (1.94 eV), and 810 nm (1.53 eV), for the samples with initial diameters of 30 nm (black), 37 nm (blue) and 45 nm (green), respectively, with a full width half maximum (FWHM) of 150 meV or less for each sample. Size control of the pre-oxidation diameter of the

etched quantum dots allowed for the overall FWHM to be smaller than other quantum dot PL measurements [75, 76, 77, 78, 79, 80, 81, 82] as a whole. While, the multiply-peaked structure of the PL curves is shown in some previous experimental work but it still requires a possible explanation.

Although careful effort was made to produce quantum dots with diameters that had as narrow a size distribution as possible, the peak emission wavelength is a strong function of dot size[78, 85] and even a change in diameter of 0.25 nm (about one monolayer of Si) can shift the peak emission energy up to 100 meV (30 nm)[78]. Several causes, including non-circular mask patterning, debris on the wafer, and local etch variation could have such an impact on the peak emission wavelength. Furthermore, it has been shown[20, 4] that the strain incorporated into thermally oxidized sillicon nanostructures can have a significant impact on the bandgap, shifting the peak emission energy by 200 meV between 1% compressive and tensile strain. The assumption made in this work is that the three stacked quantum dots have the same size and strain conditions; however this is not neccessarily true, especially when it is considered that the top and bottom quantum dots are capped with a head and tail, while the central quantum dot is bracketed by two other dots. Such anisotropic strain conditions could easily result in shifts in the peak emission wavelength between the top, middle and bottom dots. These two causes can possibly account for the multiply-peaked structure of the three measured emission spectra. This explanation is consistent with the observations that the individual peaks, which make up the total curves, have widths that fall within or close to the previously measured[7] 75-100 meV (20 - 30 nm) line-widths of individual, room temperature, etched quantum dots.

The sharp peaks seen in the blue curve in figure 6.34 can be attributed to such a cause or to a similar effect combined with a limitation of the experiment. Converting the number of fabricated pillars per pad into an areal density yields a value of $\sim 5 \times 10^9 \mathrm{cm}^{-2}$; roughly three orders of magnitude less dense than coalesced nanoparticles [79]. In our case, the 50x objective we used allowed sampling a 5 μm by 5 μm area corresponding to between 300 and 500 pillars, leading to a relatively discrete spectrum where each pillar could significantly contribute to the total signal. The relatively low collected signal from the few pillars in combination with the preferential scattering of the light from certain quantum dot pillars could give those pillars an unequal contribution to the signal; resulting in such peaks. Future work is needed to quantitatively explain these spectral details; performing measurements at cryogenic temperatures could narrow the linewidths and allow the emission from individual quantum dots to be assessed. Similar effects, resulting in multiply and sharply-peaked spectra, have been seen in previous work[83, 75].

From the dark- and light-field TEM images it is possible to estimate the size of the quantum dots in the oxidized pillar; however the distortion found in each image due to the image being taken through about 50 to 75 nm of silicon dioxide makes the bounds of error too large for a meaningful size measurement. Instead, dot sizes were determined by comparing the peak emission energy with

the band-gaps obtained by previous theoretical and experimental work[86, 78].

It is also critical to note that these dots are embedded in an oxide matrix which has been found[86, 85] to red-shift the peak emission by almost 1 eV compared to bare quantum dots or those with a hydrogen terminated surface. Based on data presented in[86, 7, 78, 85] we estimate that the measured nanocrystal sizes are centered around 2 nm (black), 2.4 nm (blue) and 5 nm (green) in diameter.

6.4 Conclusion and future directions

The ability to fabricate silicon quantum dots with predictable sizes could prove to be useful when attempting to incorporate them with existing silicon photonic structures such as waveguides or photonic crystals. Instead of using a stochastic distribution of nanocrystals, these can be placed lithographically to coincide with the peak of the optical mode. The ability to tailor the peak emission of the quantum dots allows one to select the emission wavelength to suit a task or create a vertical stack of different dot sizes to allow for broad spectral emission creating white light. Furthermore, there has been interest in producing transistors with quantum dots that demonstrate quantum effects and Coulomb blockade at non-cryogenic temperature.

To retain quantum behavior at room temperature the quantum dot must be aligned between two electrodes and smaller than 5 nm in diameter [87]. By turning the fabrication vertical, structures similar to those described in this paper could overcome the challenge of patterning gates with difficult, lateral electron beam lithography. Furthermore, the vertical, pre-positioned orientation of these pillars allows for parallel processing of numerous pillars or pads of pillars with optical lithography. As shown in the next chapter, it is possible to pattern a self-aligned gate without having to use 'hunt and peck' electron beam lithography; rather we can use optical lithography with micron sized alignment marks to pattern layers of material. Furthermore with this method of lithography the gate length is determined by much simpler dielectric and metal layer deposition and the quantum dot is self-aligned with the oxidized quantum dot.

In conclusion, we have presented a CMOS compatible method to fabricate narrow band, luminescent silicon quantum dots. By controlling the size during lithography and etching, it is possible to utilize the self-terminating nature of convex silicon oxidation to predictably tune the peak emission wavelength. We have also demonstrated the ability to stack quantum dots of various predictable sizes in order to tailor the spectral behavior of these corrugated pillars. These devices and behaviors may have important applications in both future nanophotonic and nanoelectronics devices.

Chapter 7

Silicon nanopillars and electrical pumping

In this section we explore work done to electrically excite silicon light emission. We will cover previous successful attempts at creating silicon LEDs and our current work to induce the etched nanopillars to emit light. We will also discuss the use of these nanopillars as platforms for vertical transistor-type structures.

7.1 Previous silicon LEDs

There have been several attempts to create electrically pumped luminescent silicon devices. There was initial excitement over the use of electroluminescent porous silicon[46], however the unreliability in fabrication and debate over luminescence mechanism has cooled interest in this field. As mentioned in the nanopillar luminescence chapter there have been recent advancements using floating-gate type structures to tunnel charge into precipitated silicon quantum dots[3, 8]. Spectra and schematics from *Walters et al.*, which showed EL excitation with oscillating voltage, can be found in figures 5.3 and 5.4. Recent work has shown bright, visible luminescence in similarly fabricated silicon quantum dots embedded in silicon dioxide when excited with a unidirectional voltage. The geometry, spectra and an image of the light emission from *Fernandez et al.* can be seen in figure 7.1. This floating-gate, embedded quantum dot technology is a promising method to obtain CMOS compatible on-chip light emission.

Etched nanopillars have previously been used to obtain light emission, most notably *Nassiopoulos et al.*[9]. This work used an SF_6/CHF_3 etch chemistry to fabricate vast arrays (2-3 mm^2) of nanopillars which they oxidized to sub-10 nm diameters, planarized with PMMA, and decapitated to make contact. These structures demonstrate rectifying behavior and emit light in the visible regime centered around 650 nm. The fabrication flow, sample SEM image, and electroluminescent spectra are seen in 7.2 a, b, and c, respectively. Unfortunately there was no mechanism proposed

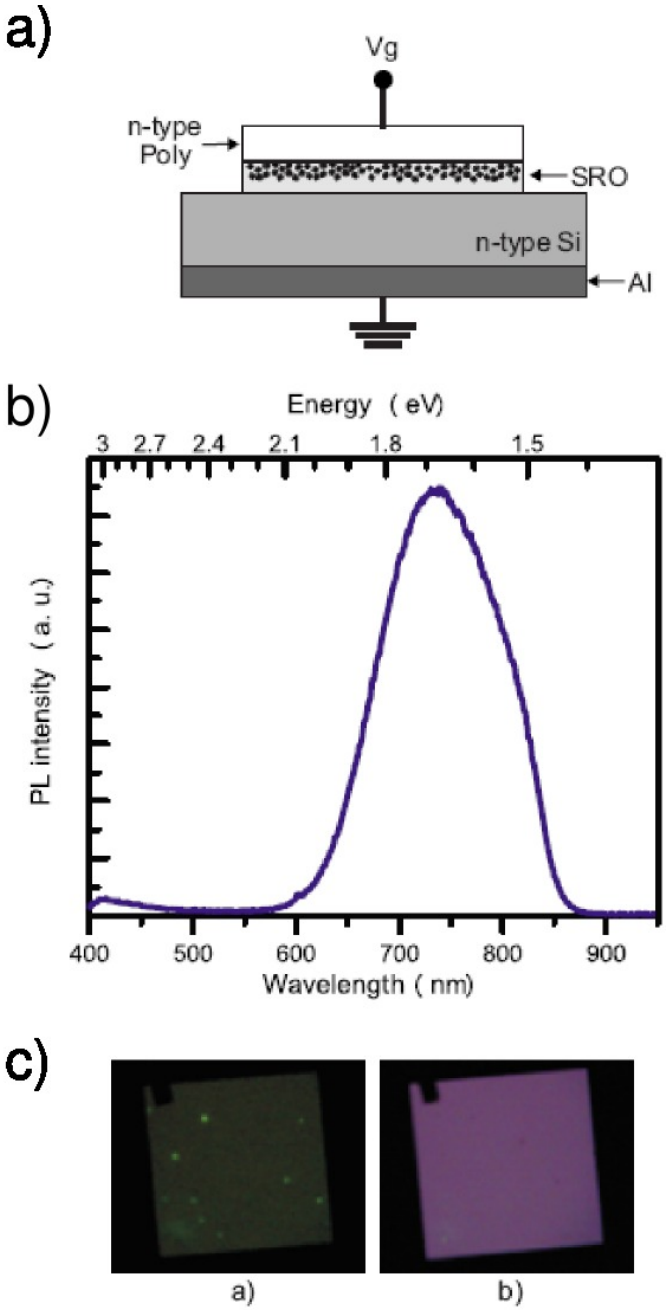


Figure 7.1: (a) Geometry of unidirectional applied voltage device. (b) Sample spectra of the same device. (c) Images of the electroluminescence obtained from these devices with different voltages applied to the gate. From *Fernandez et al.*[8]

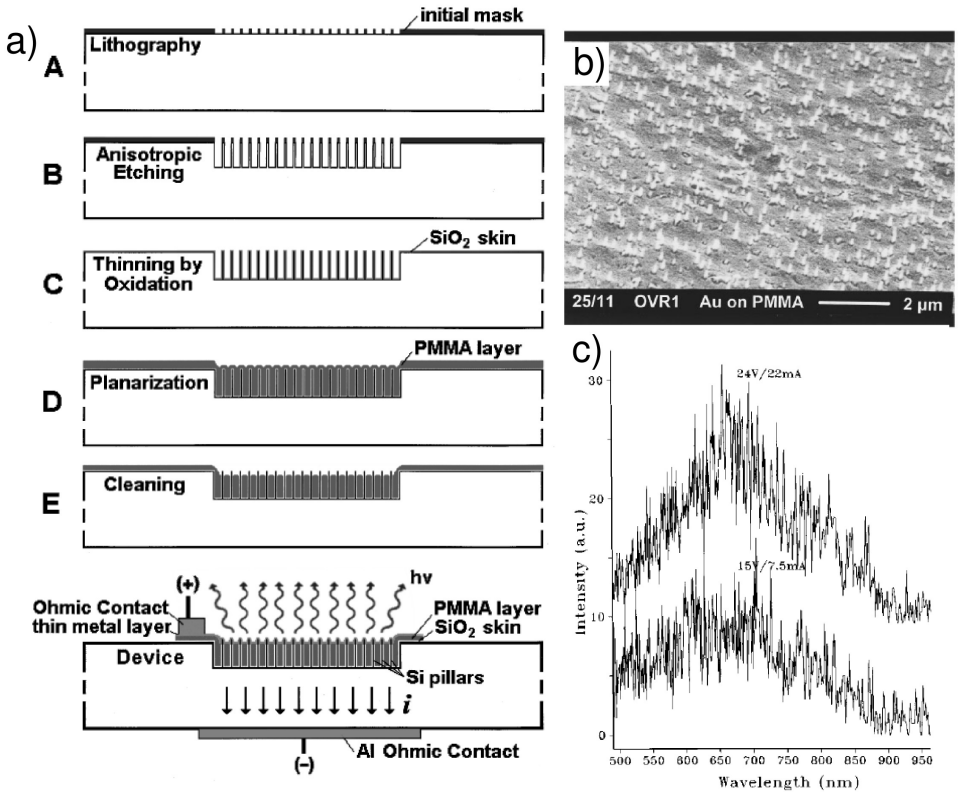


Figure 7.2: (a) Fabrication flow for electroluminescent nanopillars (b) SEM of the surface of the top contact at the end of fabrication. (c) Spectra obtained by forward biasing the resulting structures. From *Nassiopoulos et al.*[9]

for the light emission; it is uncertain as to where the injected electrons found holes with which to recombine as there was no corresponding p-type segment of nanopillar or substrate. However, this method of planarization and decapitation is similar, albeit less complicated, to the work we have done to fabricate electroluminescent devices.

We propose here a dual gate structure fabrication scheme to make efficient, silicon based nanopillar LEDs. By using previous methods to fabricate and thin silicon pillars combined with techniques explained below we believe that we will be able to construct CMOS compatible, top-down LEDs that emit in the visible to near-IR.

7.2 Attempts at electroluminescence

The first attempt taken to obtain EL was similar to that taken by *Nassiopoulos et al.*; we used n-type ($N_d \approx 10^{17}cm^{-3}$) wafers with 300 nm of epitaxially grown p^+ ($N_a \approx 10^{19}cm^{-3}$) silicon grown on top. We etched 750 nm long pillars into these samples and oxidized them down to 2-15 nm in diameter. By utilizing the same PMMA planaraization scheme of [9] we attempted to pass current through these devices. The decapitated pillar and current direction is shown in figure 7.3; the PMMA planarization used to decapitate the pillar with HF and top contact are omitted for clarity; the disk of material around the pillar is thermal oxide. It was noted that current would pass and rectifying behavior was observed for the larger (> 10 nm) core diameter pillars; however these were not expected to luminesce as they were too large to exhibit the size dependent modification of band-structure found in narrower core pillars. Unfortunately it proved impossible to pass a measurable amount of current through 2-5 nm wide silicon cores. No current would be observed with increasing voltage until the PMMA and thermal oxide would undergo dielectric breakdown and current would spark between the top contact and the substrate, destroying the device. It is postulated that there are two main

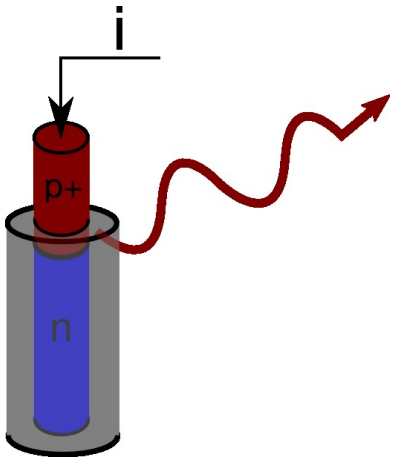


Figure 7.3: Schematic representation of decapitated PN doped nanopillars.

reasons that current conduction was prevented in narrow pillars. The first focuses on the influence of trapped surface charges on the effective conducting cross-section of a nanopillar. Experimental studies[88, 89, 90] have shown that trapped charges at the surface of a nanopillar/nanowire set up a depletion region that extends towards the center of the pillar. We represent the cross section of a (p-type) nanopillar as depicted in figure 7.4, the trapped surface charges are drawn as the positive space charges at the perimeter of the silicon core, the oxide in white, the depleted region in light gray, and the effective conducting cross-section in dark gray. It has been reported that in oxidized silicon wires these interfacial charges tend to be positive[88] as they are typically a symptom of excess silicon or the loss of an electron from an oxygen atom. We can write the areal concentration of trapped charge as N_s and the doping density of the core as N_a. As the depletion region arises from charge balancing we can find the position of the neutral interface by integrating and equating the surface and space charge density.

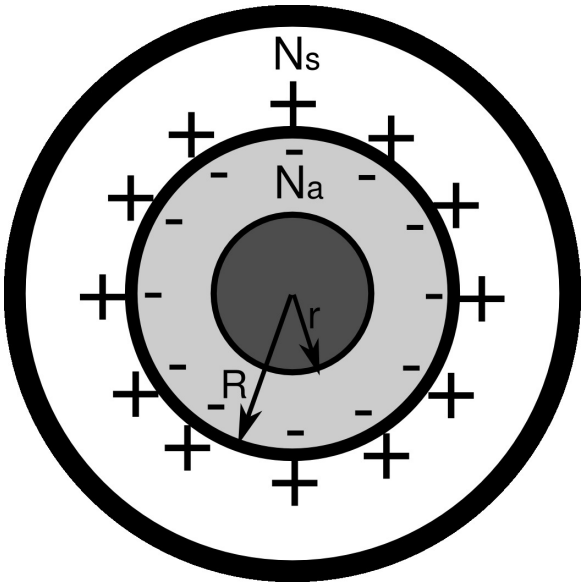


Figure 7.4: Schematic cross section of the surface state modulated depletion region. The white is silicon dioxide, the light gray is the depleted region and the dark gray is the conducting core.

$$\int_s N_s dA = \int_V N_a dV \tag{7.1}$$

Assuming the pillar has some height h, physical core diameter of R, and effective conduction diameter of r equation 7.1 becomes:

$$N_s 2\pi R h = N_a \pi \left(R^2 - r^2\right) h \tag{7.2}$$

Simplifying we can write:

$$\pi r^2 = \pi R^2 \left(1 - \frac{2N_s}{RN_a}\right) \tag{7.3}$$

or in terms of calculating resistance of the pillar:

$$A_{eff} = A_{act}\left(1 - \frac{2N_s}{RN_a}\right) \tag{7.4}$$

giving (as a simple model) the effective resistance of the pillar to be:

$$R_{eff} = \rho\frac{h}{A_{eff}} = \rho h\left[\pi R^2\left(1 - \frac{2N_s}{RN_a}\right)\right]^{-1}. \tag{7.5}$$

For reported values of N_s[88, 89] and parameters from our work:

$$N_s \sim 1 \times 10^{12} cm^{-2},$$
$$N_a = 1 \times 10^{19} cm^{-3},$$
$$2R = 5 \text{ nm},$$
$$h = 700 \text{ nm},$$
$$\rho = .025 \Omega cm$$

the effective nanopillar diameter is 2.22 nm and the effective resistance is 44.5 MΩ.

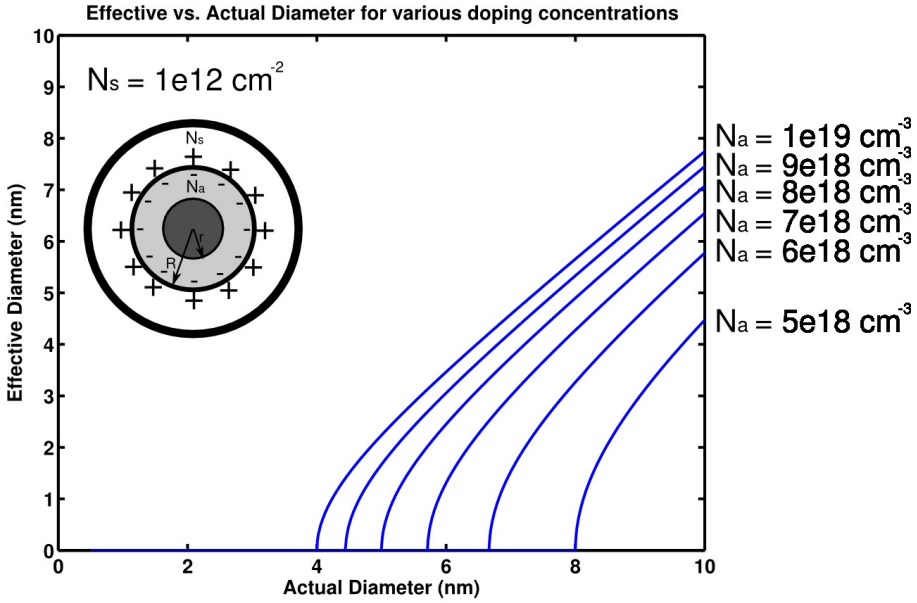


Figure 7.5: Effective vs. Actual diameters for various doping levels. Note that when the effective diameter is zero the silicon core is fully depleted.

Figure 7.5 shows the dependence of conducting diameter on doping and actual diameter. When the effective diameter drops to zero the pillar is considered completely depleted.

Although the previous model can be used to approximate the conduction cross section and serves to estimate the point that a pillar becomes completely depleted it is better suited to nanopillars

with diameters greater than 10 nm. If we consider a 700 nm tall, 3 nm diameter pillar with a doping concentration of $N_a = 1 \times 10^{17}$ cm^{-3}, and take the density of silicon to be $N = 5 \times 10^{22}$ cm^{-3} the number of atoms contained in the actual diameter of the nanopillar is approximately 247,000. Of those, based on the doping, one in every 500,000 is a dopant and therefore there are on average 0.5 dopants in the entire pillar. Consequently for a standard 1-10 Ω·cm wafer the distribution of the number of dopants shifts from a normal to a binomial distribution as now dopant presence is a discrete trial. Estimated numbers of dopants are plotted in figure 7.6.

This problem can be somewhat offset by using a heavily doped wafer, as was done with this work. However, if we now consider the handfull of ionized charge centers from the dopants that may be found in a pillar they can no longer be considered to have an even distribution along the length of the pillar; instead of presenting a (roughly) uniform field to neutralize the trapped charges there exists a sparse distribution of point charges that would indicate that a portion of the pillar can be fully depleted while another portion can remain conducting due to the presence of a local ionized impurity. There are several other cases that need to be considered including the radial location of the dopant and the type of dopant, as it may preferentially segregate into the oxide or silicon [91].

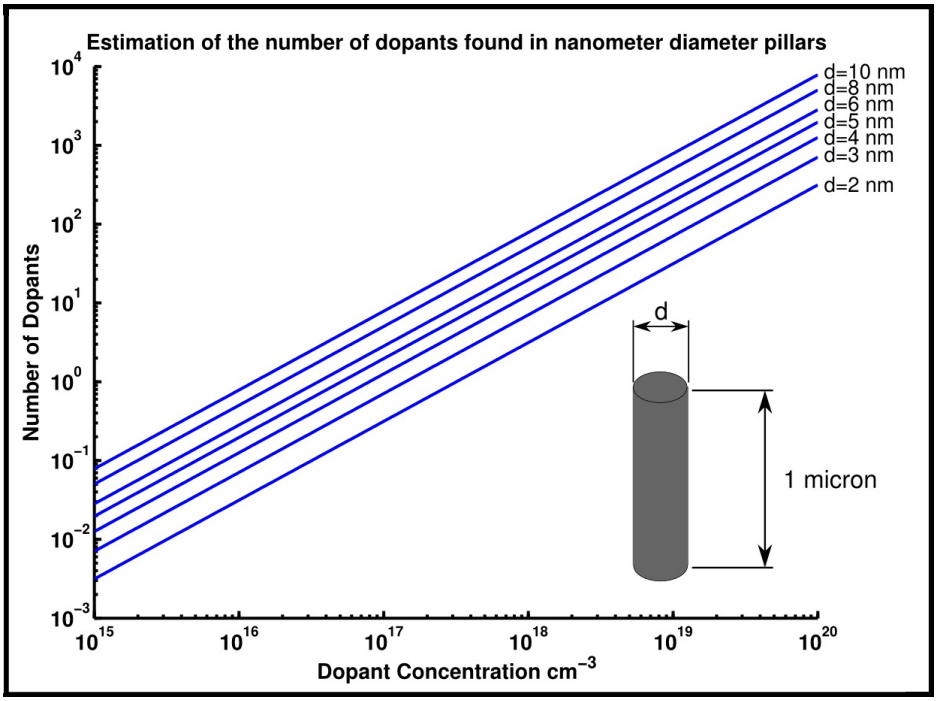


Figure 7.6: Estimation of the number of dopants in a silicon core of a given diameter.

7.3 A possible solution

7.3.1 Motivation

Since it is very difficult to reliably recreate doping conditions in nanoscale structures, an alternative method needs to be found. This method follows the work of *Mueller et al.*[10]. In their work they use two gates to electrostatically dope a single wall carbon nanotube (SWNT), both p and n-type, and then apply a transverse voltage to drive the two charge types together and emit light. Figure 7.7 shows a schematic of the SWNT, ambipolar, PN diode, as well as a rough bandstructure. The positive bias on one gate draws electrons to that region and the negative bias on the other brings holes to the vicinity. By appropriately biasing the source and drain it is possible to bend the bandstructure enough to bring the two carrier types together and induce radiative recombination.

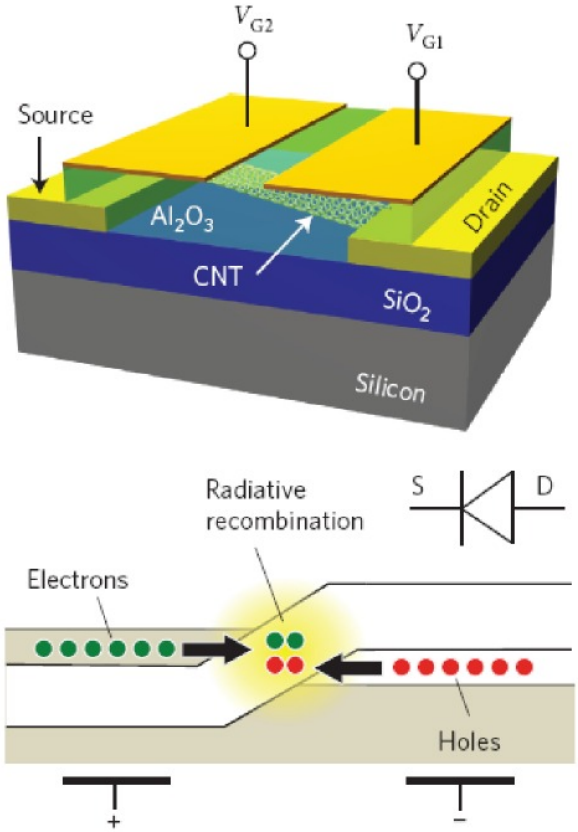


Figure 7.7: Schematic of the dual-gate, ambipolar SWNT LED and rough sketch of its bandstructure. From *Mueller et al.*[10].

Figure 7.8 shows the I-V characteristics of the LED under two different gate biases. When the gates are both biased at -8 V the device behaves as a resistor; when the gates are biased at +8 V

and -8 V the device shows rectifying behavior indicative of a diode. Also shown in figure 7.8 is the emission spectra resulting from operating the LED in forward bias with the peak at around 0.65 eV (1.9 μm). The devices measured exhibited external quantum efficiencies of $\sim 1 \times 10^{-4}$.

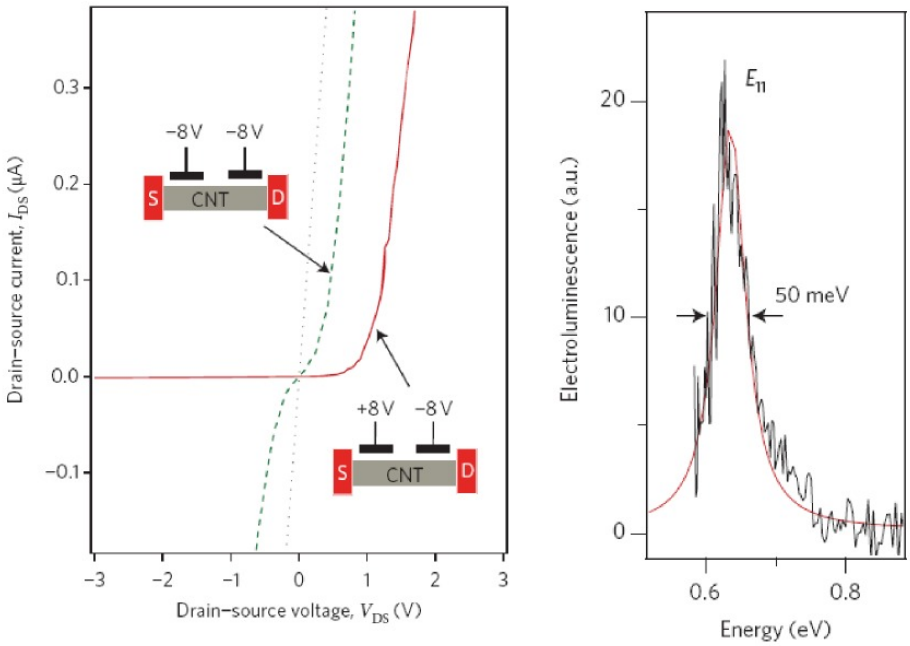


Figure 7.8: I-V characteristics and photoemission from a dual-gate, ambipolar SWNT. *Mueller et al.*[10]

If this same biasing scheme could be used to excite photoemission from silicon nanowires it would be possible to create an efficient silicon LED, a goal which has been elusive for the last 60 years.

7.3.2 Design

In order to adapt the work done by *Mueller et al.* for our etched nanopillars we decided to turn the fabrication sideways. Instead of requiring difficult, aligned electron beam lithography we can set gate lengths and spacing by controlling well-characterized deposition. Figure 7.9 shows a schematic of a vertical, ambipolar, silicon LED. Metals for contacts and gates as well spacing insulators were specifically chosen to be compatible with each other as well as standard CMOS fabrication lines. Some design obstacles to note:

- Many coating techniques (sputtering, PECVD, CVD, ALD) conformally coat the sample; even non-conformal deposition methods (thermal evaporation, electron beam evaporation, ion beam evaporation) will still deposit on side-walls. Metal traces up the sides of the pillars need to be etched back or well insulated from each other to avoid shorting between gates/contacts.

- Similar materials deposited with different deposition techniques can have vastly different etch rates and chemistry. An example of such an effect that cropped up was the unexpected etching of PECVD SiN_x in both buffered hydrofluoric acid (BHF) and KOH when SiN_x deposited by LPCVD is completely resistant to both wet etches.

- It is very difficult to find, let alone make contact to, a 2 nm diameter structure. In order to develop the correct etch recipes we looked to see when the core became visible, however this proved impossible as almost no etch technique would give the selectivity and smoothness to leave a 2 nm silicon structure while etching away the SiO_2/SiN_x around it. A corrugated etching technique was developed specifically to deal with this problem and will be covered briefly in this chapter and in more detail in the next chapter.

- Techniques that involve high-temperature anneals (spin on glass anneal, dopant drive-in) cannot be used as the CTE between the metals and insulators used can cause layers to delaminate and peel off the substrate.

- In order for compatiblity and integration with standard CMOS processing no methods or materials not typically found in a fabrication foundary will be used.

7.3.3 Fabrication procedure

This chapter will focus mainly on the order and methods used to construct ambipolar silicon LEDs while specific techniques are omitted for clarity. All references to steps are numbered and given in figures 7.21, 7.22, and 7.23.

- **Steps 1-2: Initial fabrication:** Pillars are fabricated in a square array, next to alignment marks to be used for optical lithography; an example of this is shown in figure 7.10. The pad of pillars is written with a 1-2 nA electron beam while the alignment marks are written with $\sim$ 200 nA. On a 1 cm $\times$ 1 cm chip 9 patterns are written with 3 mm spacing. The fabrication of these pillars and their oxidation are explained in chapters 2 and 3, respectively.

- **Step 3: Gate metal deposition:** Various metals were tested for suitability in terms of chemical compatibility, ease of patterning, and ease of deposition. Copper and tungsten are two metals that can be evaporated or sputtered quite easily and patterned with CR-7 and a fluorine dry etch, respectively. The top frame of figure 7.11 shows the deposition of sputtered tungsten while the bottom frame shows sputtered copper; note the conformal coating of both sets of pillars. It was found that as long as the sputtering rate was kept low the grain size of the deposited material could be less than 5 nm. The inset shows an example of thermal evaporation of copper; the pyramid is formed at the top since evaporation is directional and the sample was on a rotating, tilted stage in order to get wrap-around coverage.

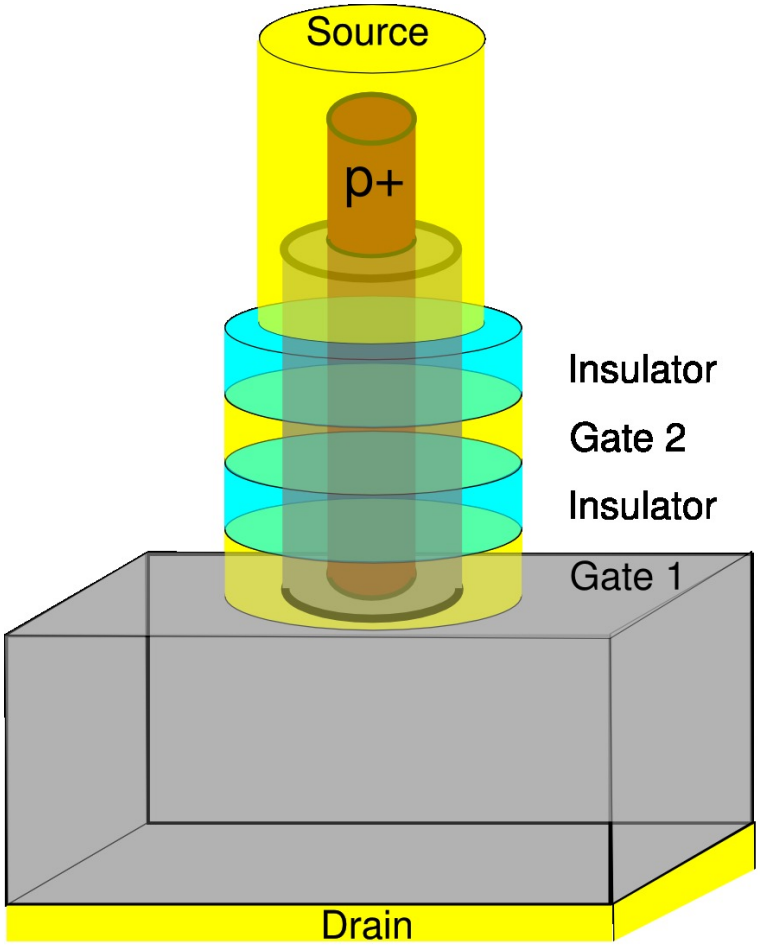


Figure 7.9: Schematic of the fabrication of a vertically stacked, ambipolar, silicon LED.

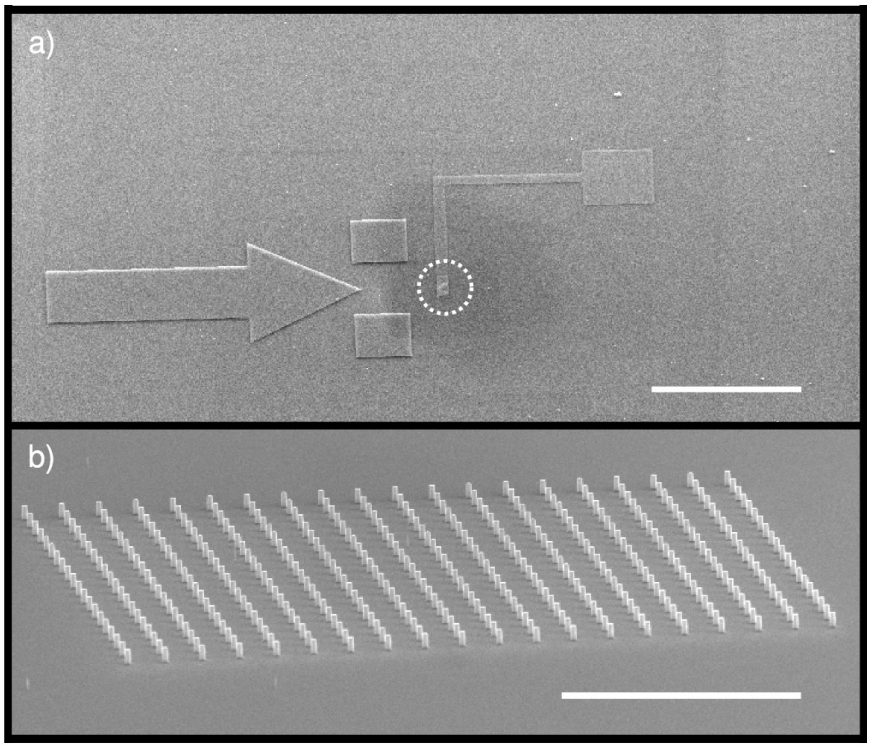


Figure 7.10: (a) Wide angle image of pillars and alignment marks. Also note the presence of a patterened gate. Scale bar is 200 microns (b) Close up of square pad of pillars taken at 75^o. Scale bar is 10 microns.

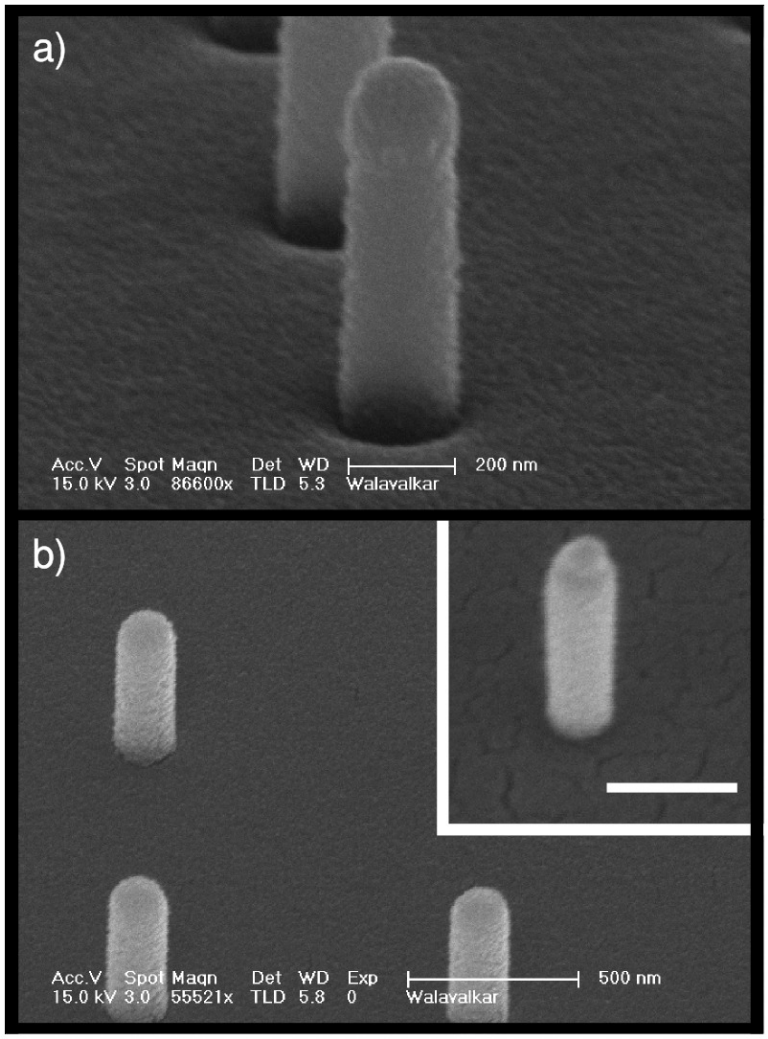


Figure 7.11: (a) Pillars covered with sputtered tungsten. (b) Pillars coated with sputtered copper. Inset shows the directionality of copper evaporation can lead to the formation of a pyramid structure on the top of the pillar. Scale bar is 250 nm.

- **Steps 4-5: Gate and sidewall patterning:** It was important, while patterning the gate, to clear the conformally deposited metal off of the sidewalls of the pillars, as it could easily cause shorting between the two gates or the gates and top contact. This was achieved through a bi-layer lithographic process. First a layer of PMMA was spun on the wafer to the desired height of the wrap-around gate and soft-baked at 180 C^o. This height would be less than that of the pillar, typically in the range of 50-100 nm so that the rest of the pillar could protrude from this surface. The PMMA was then planarized with an oxygen plasma, this had the added benefit of cleaning the protruding tips of the pillars. Photoresist was then spun on the chip and patterned in the shape of the gate seen in the top frame of figure 7.12. The photoresist was used to pattern the PMMA underneath with an oxygen RIE and then stripped in IPA; as the baked PMMA is tolerant to IPA the chip could be soaked until the photoresist came off completely. The thin layer of PMMA was then used to pattern the metal gate; with tungsten this was achieved with a low power SF_6 etch. The low power ensures that the PMMA does not erode and there is minimal etching of the silicon dioxide (the bond-strength of SiO_2 requires a very high forward power to etch with SF_6), while the tungsten is quickly and chemically etched. Figure 7.13 and the top frame of figure 7.16 show the result of this bi-layer etching. The PMMA is then stripped with an oxygen RIE. If only photoresist is used to pattern the gate the resulting pad of pillars looks like the bottom frame in 7.12. In this image it is possible to see the outline of the gate itself and the metal that remains on the sidewalls.

- **Step 6: Insulator deposition:** To isolate the two gates and the upper gate from the top contact an insulating layer was deposited. The initial effort was to use spin-on glass (SOG) or PECVD/sputtered SiN_x. In order to make the SOG have properties similar to thermal oxide a high-temperature anneal was required. This caused the metal traces to peel off and the contraction of the SOG caused the pillars to bend, similar to the method in chapter 3. Unfortunately as these pillars had roughly a 50 nm thermal oxide coating, the pillars would not restore their shape but rather snap. Reactive ion sputtered SiN_x produced a very large grain film that, based on EDAX results, was shown to be a SiO_xN_y, making it vulnerable to HF as well as SF_6. This large grain film can be seen in the top frame of 7.14; the large grains made it possible for the gates to short through the grain boundaries. PECVD SiN_x was tried to produce a more conformal, smaller grain-size film. Unfortunately the PECVD SiN_x would nucleate a ball of material on top of each pillar that was almost impossible to etch through without destroying the pillars. This ball shape can be seen in the bottom frame of figures 7.14 and 7.15. Note in figure 7.15 the nitride was deposited directly on p+ silicon so it is possible to see the pillar within the insulator as a bright conductor. The material that we have found to meet our demands has been PECVD deposited SiO_2. It is clear at the emission wavelengths of the oxidized pillars, it stands up to the tungsten or copper etching, and it can be etched

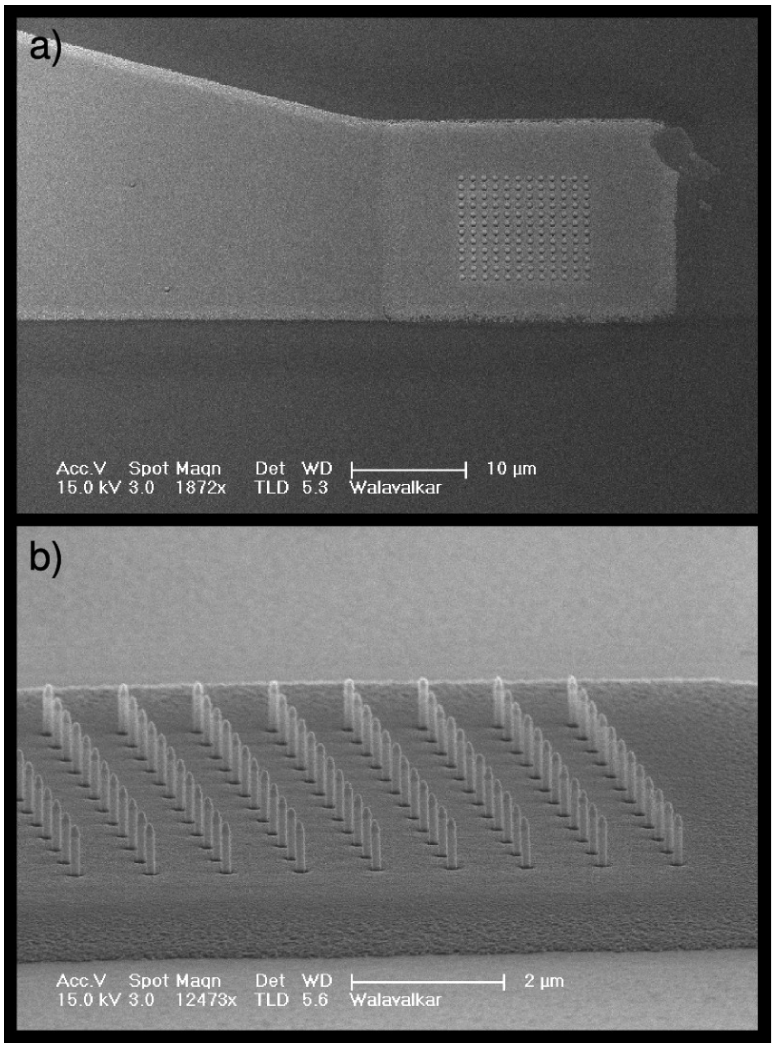


Figure 7.12: (a) Bi-layer patterned tungsten gate. (b) Single-layer patterned copper gate. Note that the rough region at the edge of the gate results from undercut as the copper etch process is a wet etch with CR-7.

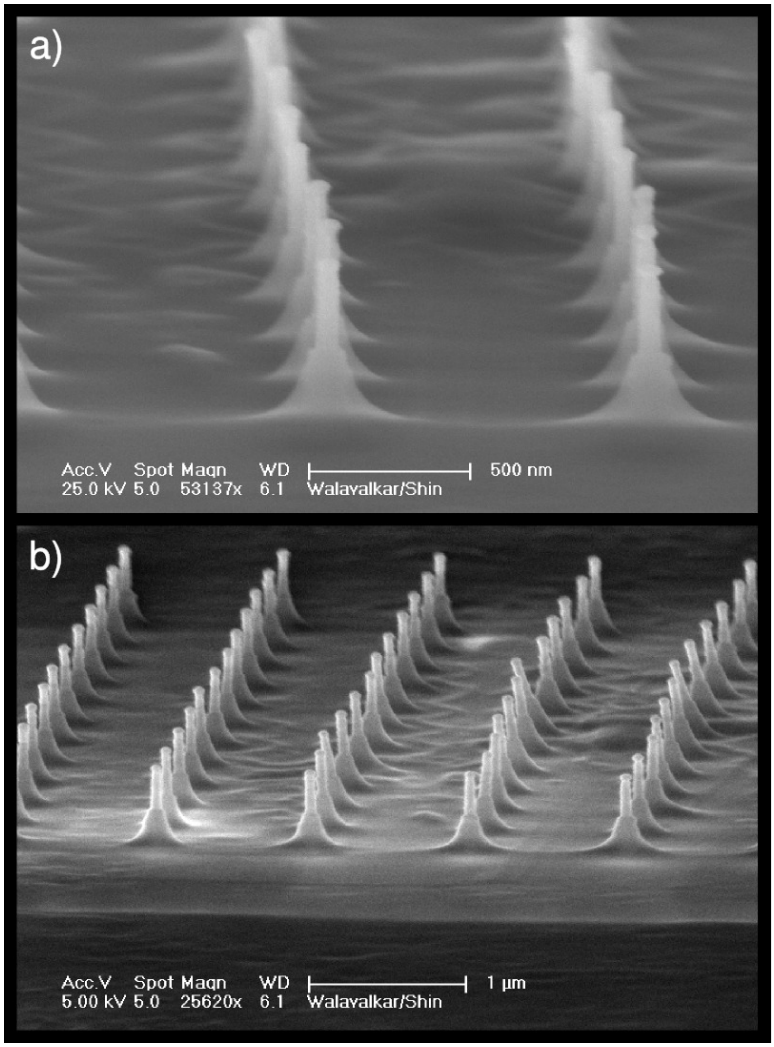


Figure 7.13: (a),(b) Tungsten wrap-around gate etched with a PMMA/PR bi-layer process.

orthogonally to both tungster and copper with a C_4F_8/O_2 etch. An example of this deposition can be seen in figure 7.16; the top frame shows the thermal oxide surrounded pillars with a tungsten wrap-around gate, and the bottom frame shows pillars after coating with 75 nm of PECVD oxide. Note that the contour of the deposited film follows the shape created by the metal on the side-walls.

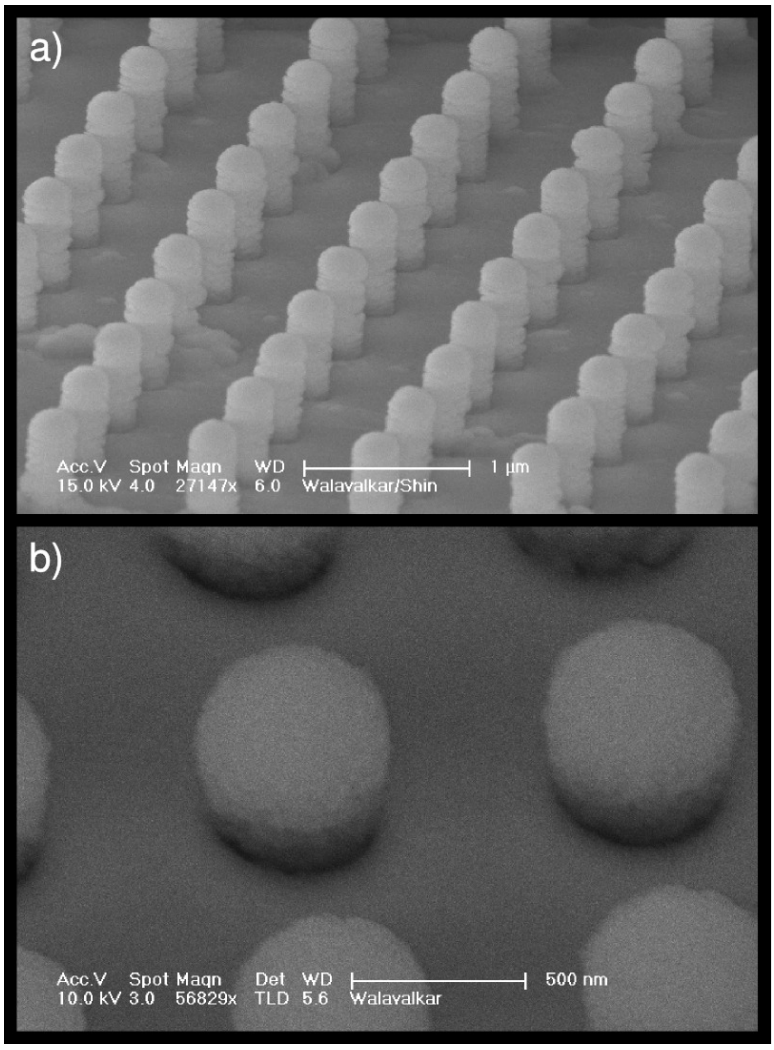


Figure 7.14: (a)Sputtered SiN_x; note the uneven deposition and large grain size. (b) PECVD SiN_x; note the creation of a dome-like structure on top

- **Steps 7-10: Second gate and insulator layer:** These steps repeat the previous four steps to pattern a second gate on the opposite side from the first gate. An optical micrograph and SEM image of two gates surrounding a pad of pillars are given in figure 7.17. In the optical image both gates are made out of copper, the gate that extends towards the bottom of the image is colored green due to a 100 nm layer of SiN_x above it. The bottom frame shows two

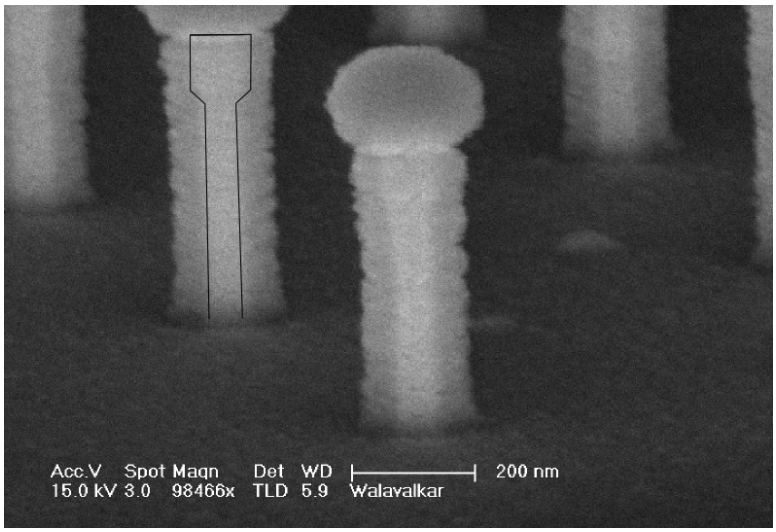


Figure 7.15: PECVD SiN_x onto bare silicon. Note the formation of a ball on top the pillar. The bare silicon shows up as a bright area inside the SiN_x; one of them is outlined in black.

patterned gates; the bottom one is made of chrome-gold and the top is made of copper.

- **Steps 11-12: Decapitation:** These steps are the trickiest in the fabrication process. We have to expose the silicon pillar underneath the layers of insulator without exposing or shorting any of the gates. PMMA is spun to cover half of the remaining pillar height and the insulator is etched. It was posited that a wet etch would work best for this as it would etch the sidewalls and top of the pillars evenly resulting in the full exposure of the upper portion of the pillars. Unfortunately, as can be seen in the top frame of figure 7.18, the BHF used to slowly remove the SiN_x would create channels around each pillar and begin to attack the insulating layer along the pillar as well as the layers on the substrate, allowing the gates to short together. Several attempts were made to remedy this with PMMA reflow techniques or vapor phase HF etching or different, selective etchants. None of these wet processing methods ended up working; the etchant too easily slipped past the PMMA and etched the insulator off the substrate. The next attempt utilized high forward power CF_4/O_2 etching to anisotropically remove the insulating layers. This seemed to work well and compensate for the nucleation of the SiN_x ball on top of the pillar; however the differential etch rate between the thermal oxide and SiN_x was so great that by the time the etchant went through the oxide the nitride was completely destroyed. In figures 7.18 and 7.19 we can see the result of this dry etching technique. The bottom frame of 7.18 shows an image with the PMMA mask still in place and 7.19 shows the structures after removal of the PMMA. These images appear to indicate a successful etching scheme, however when the real estate gets crowded towards the top of the height of the pillar the differential etch rate causes the nitride to vanish down to the top gate before etching through the oxide.

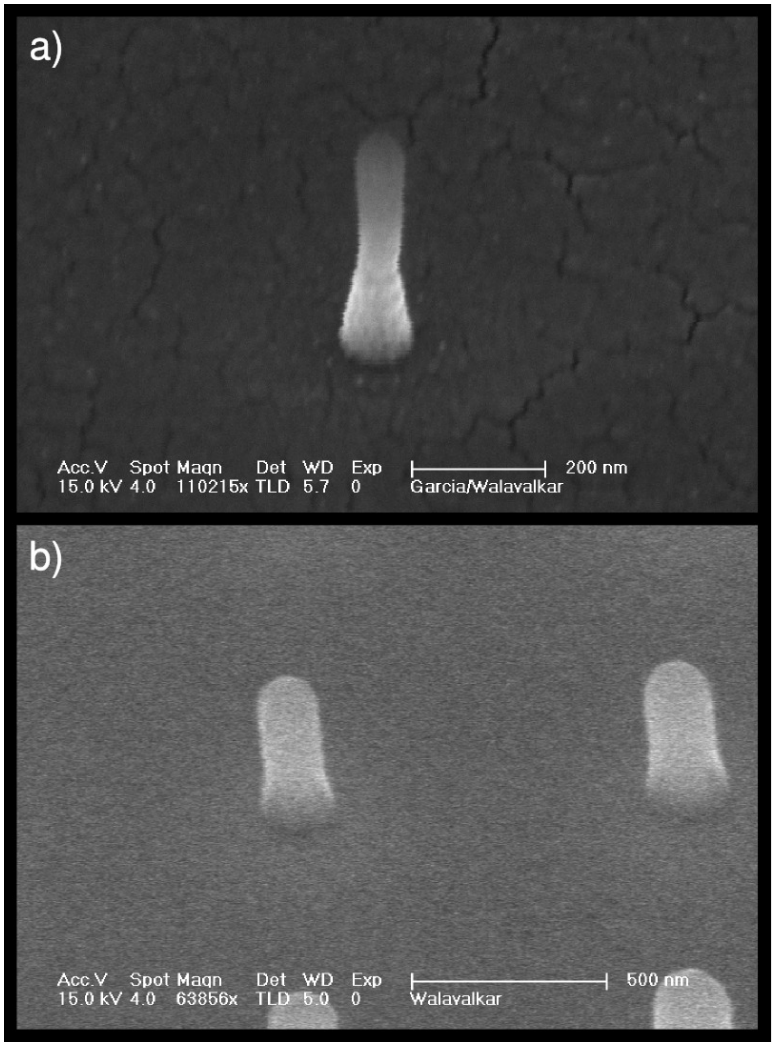


Figure 7.16: (a)Tungsten wrap-around gate etched with a PMMA/PR bi-layer process. (b) Similar pillars coated with 75 nm of PECVD SiO_2; note the small grain size and how the film follows the contour of the gate.

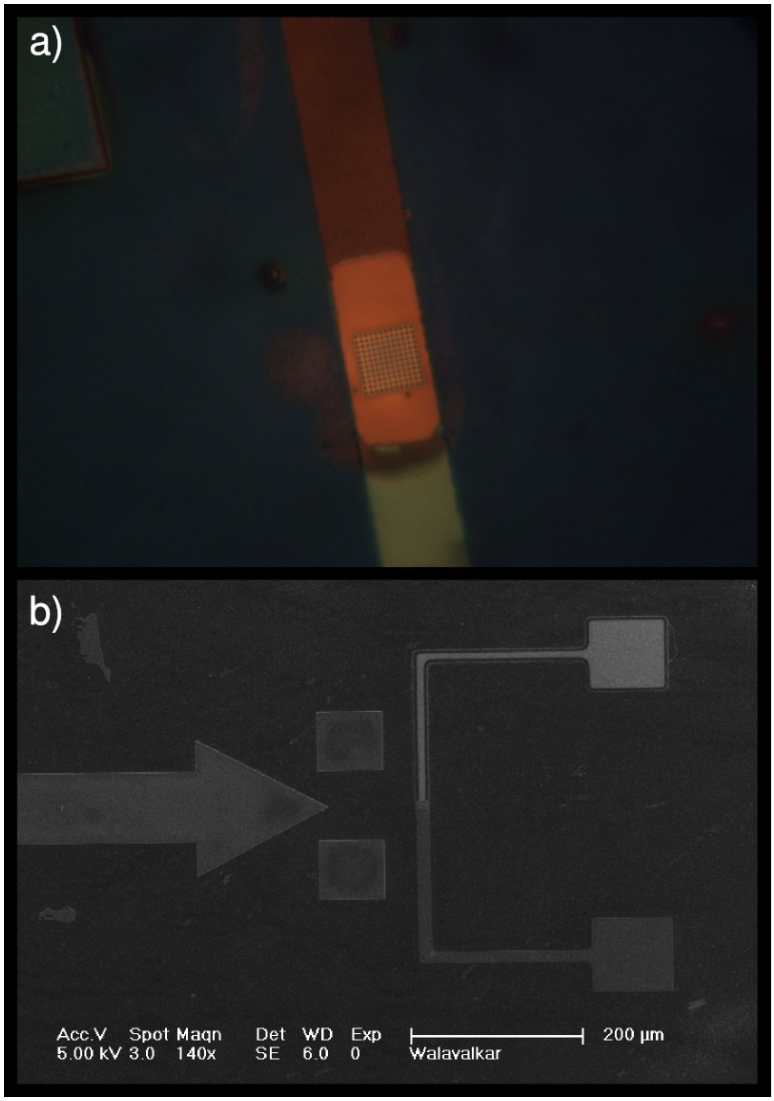


Figure 7.17: (a) Optical image of two copper gates. Note that it is possible to see the outline of individual pillars as they have gotten larger due to several conformal coatings. (b) SEM image after the patterning of the second gate; the top gate is copper and the bottom is chrome-gold. Note the gold was over-etched in KI leading to the narrowed gate; however the chrome still remains.

The images shown in those figures are of pillars with no gates and thus having plenty of real estate on top to waste etching through the insulators.

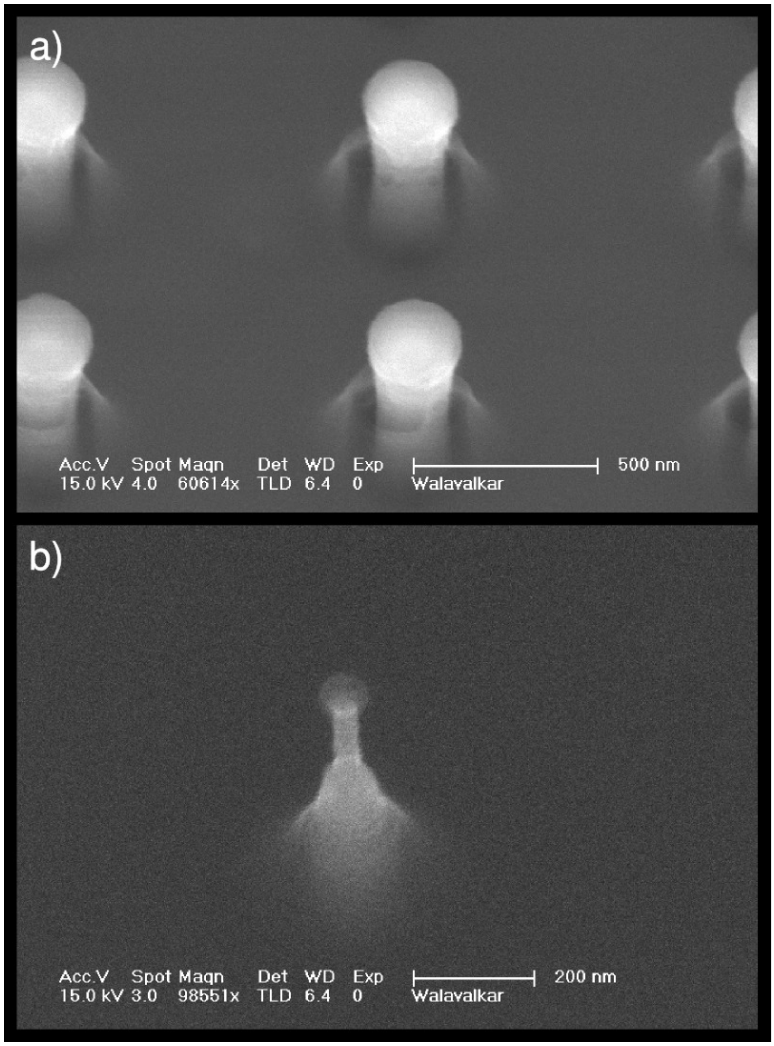


Figure 7.18: a) SEM of a pad of pillars in the middle of BHF etching to remove the SiN_x insulator over the top of the pillar. The channels cut into the PMMA mask allow the BHF to etch the substrate, as a result of the pillar no longer being flush against the PMMA.. b) Image of pillar (with PMMA mask) after CF_4/O_2 etch.

- **Steps 13-15: Top contact patterning:** The top contact is patterned with standard photolithography. The two optical images in 7.20 show the intersections of the gates and top contact with the pad of pillars. As these were taken during process development the quality of the final product is not perfect. When conducting electro-optical measurements we used indium tin oxide (ITO) as the top contact to allow for easy light emission. ITO is sputtered onto the surface in an atmosphere of 100:1 sccm of $Ar:O_2$, in an RF gun, with a 200 W plasma. ITO can be etched and patterned quite easily in HCl.

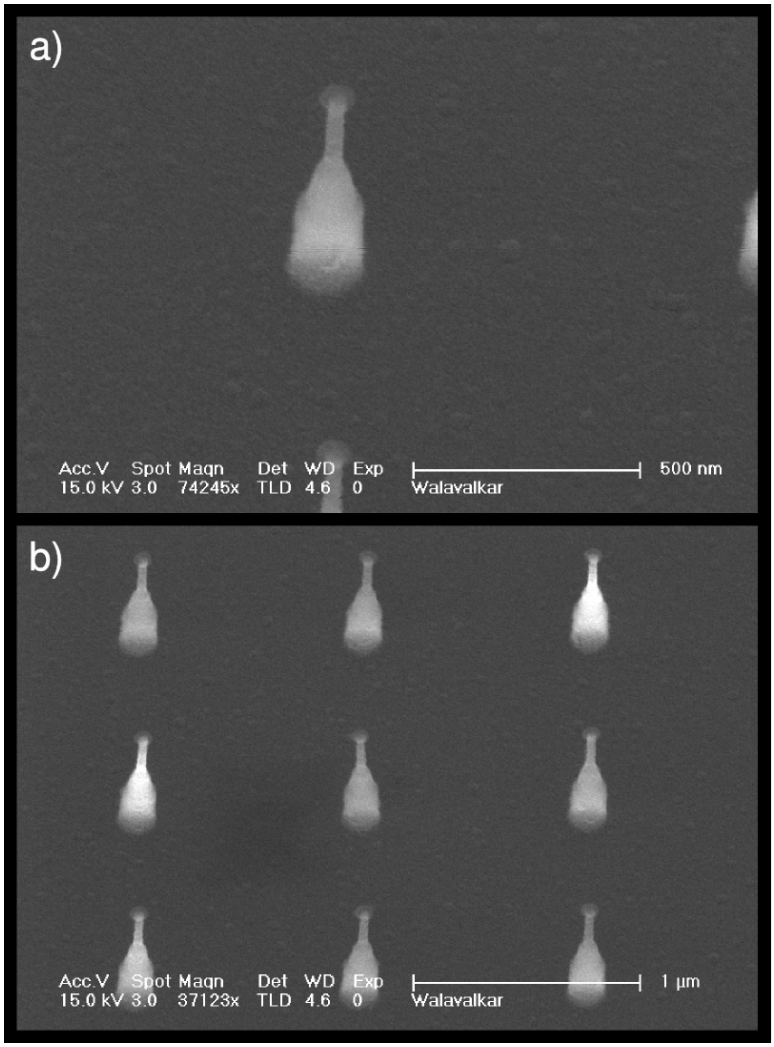


Figure 7.19: (a),(b) Nitride coated pillars after CF_4/O_2 etch and removal of the PMMA mask.

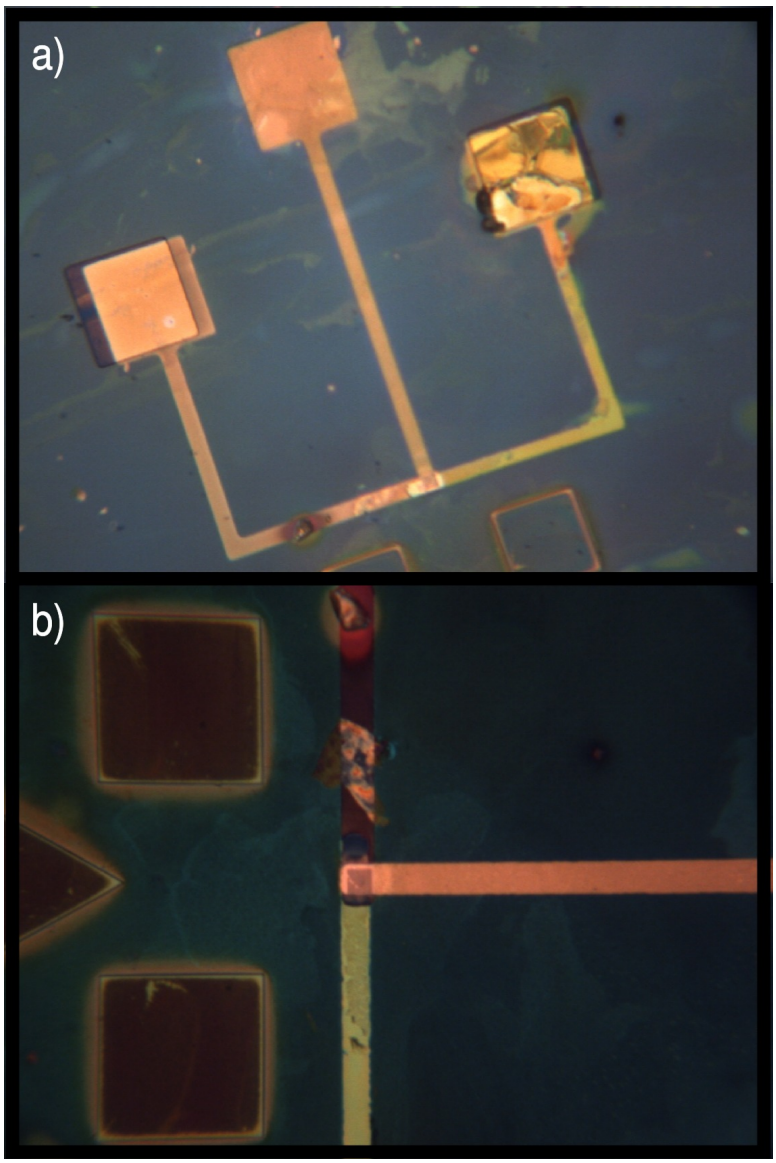


Figure 7.20: (a),(b) Images of two separate pillar arrays with both gates and a top contact; all metals used in this fabrication run were copper.

- **Step 16: Backside contact:** Gold is electron beam evaporated onto the backside of the wafer due to its ability to make ohmic contacts with p^+ silicon [92]. However to retain CMOS compatibility, a metal such as aluminum could be deposited on the backside and then driven into the silicon to make an ohmic contact.

- **Step 17: Opening windows to gate contact pads:** As the gate contacts are buried under one or two layers of insulator, a photoresist mask is used to drill down through the insulator over each contact pad to free them for probe tip contacting. An example of this can be seen in figure 7.20 a); note that the alignment is not quite perfect but since the pads are 100 microns wide there is still plenty of room to touch the metal gate contact pads.

The final layout of the ambipolar LED, with source, drain, and gates labeled, is given in 7.24

7.4 Theoretical analysis

In order to predict the behavior of this device we have constructed a relatively simple theoretical model of the ambipolar diode. We note several differences between this structure and standard diodes and MOSFETs that lead to the following considerations and assumptions:

1. The planar MOSCAP model no longer applies and equations have to be modified to take into account the cylindrical shape of the device.

2. Although the length of this diode is smaller than the diffusion length for carriers in bulk silicon there has been work[93] that shows that the diffusion length scales downward with decreasing pillar diameter. In our case we are sitting at diameters of approximately 3 nm meaning that surface state scattering will be a huge effect; therefore we assume that the concentration of minority carriers drops to zero before they reach the contacts.

3. The regions around the gates will be treated as MOS capacitors and the interfacial trapped charges will serve to modulate the 'threshold voltage' of these regions. In our case the threshold voltage will be reached when the applied voltage is greater than the contributions of both the work function mismatch and the depletion potential.

4. The metal used for defining the gates is tungsten, the back contact is gold, and the top contact is ITO on a thin layer of gold. As mentioned before gold is chosen to create an ohmic contact to p-type silicon.

5. The model pillar will have a core diameter of 3 nm, gate height of 50 nm, insulation height of 30 nm, and a 50 nm thick oxide cladding.

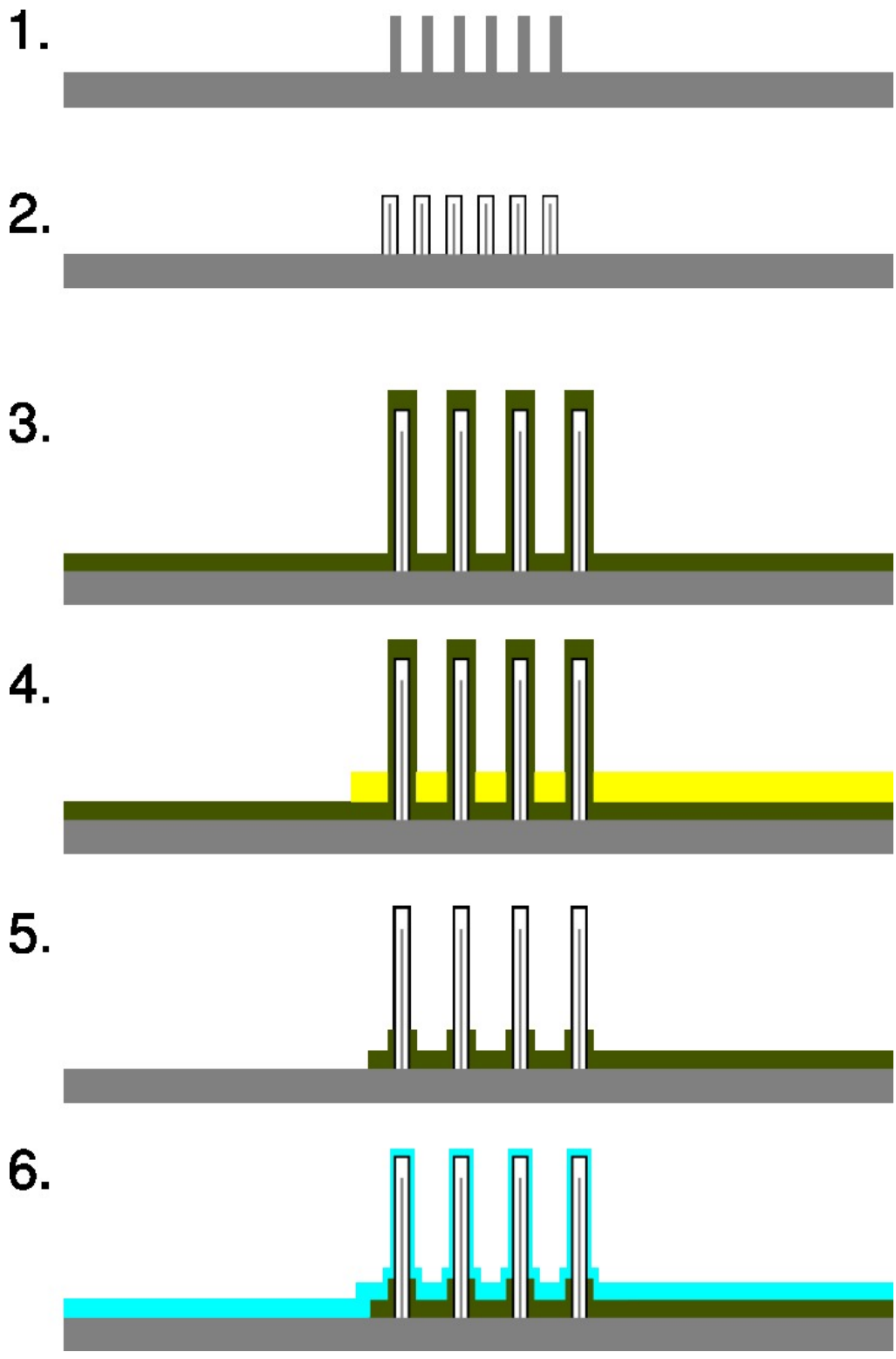


Figure 7.21: Schematic of the fabrication of a vertically stacked, ambipolar, silicon LED.

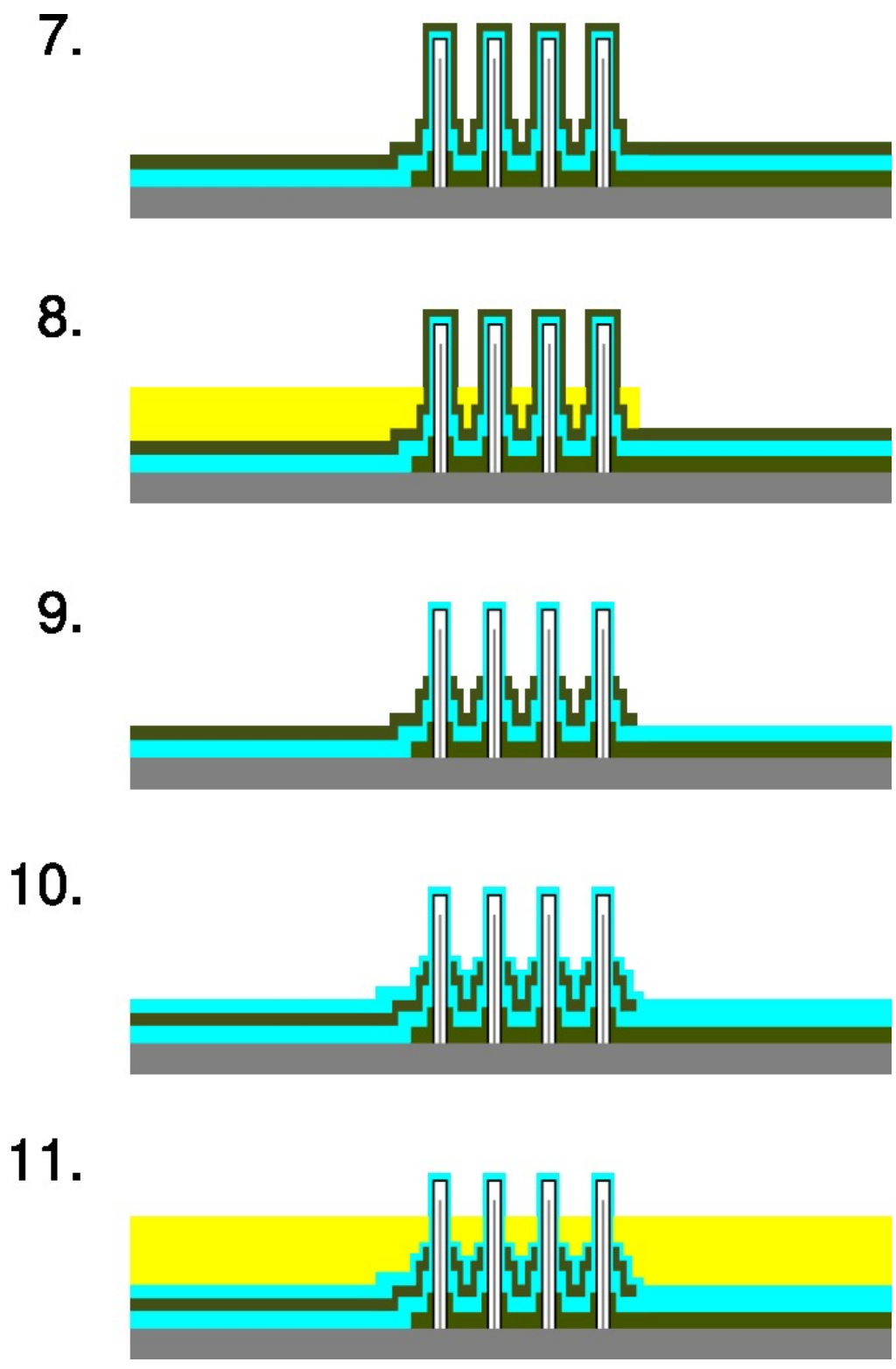


Figure 7.22: Schematic of the fabrication of a vertically stacked, ambipolar, silicon LED.

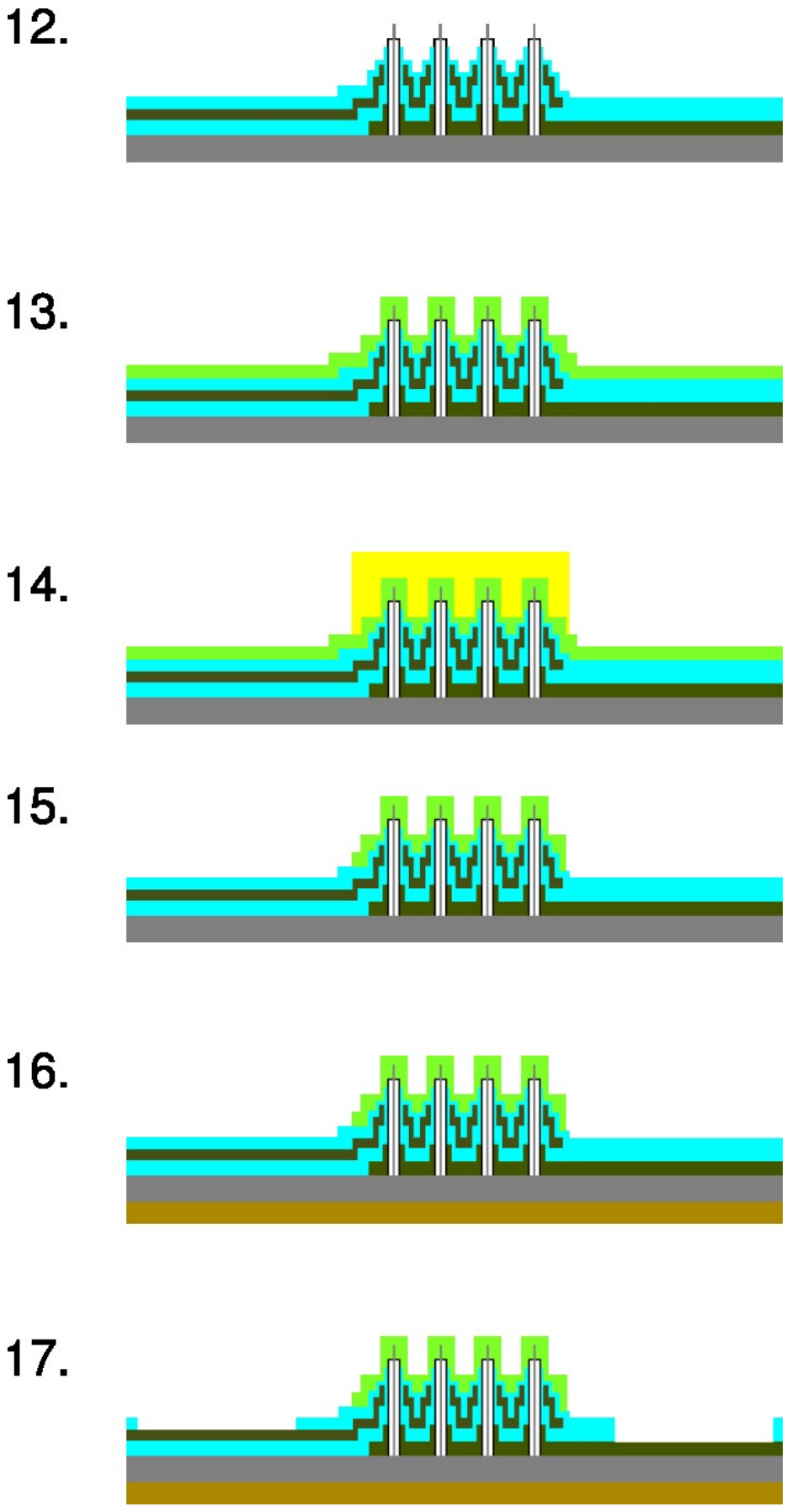


Figure 7.23: Schematic of the fabrication of a vertically stacked, ambipolar, silicon LED.

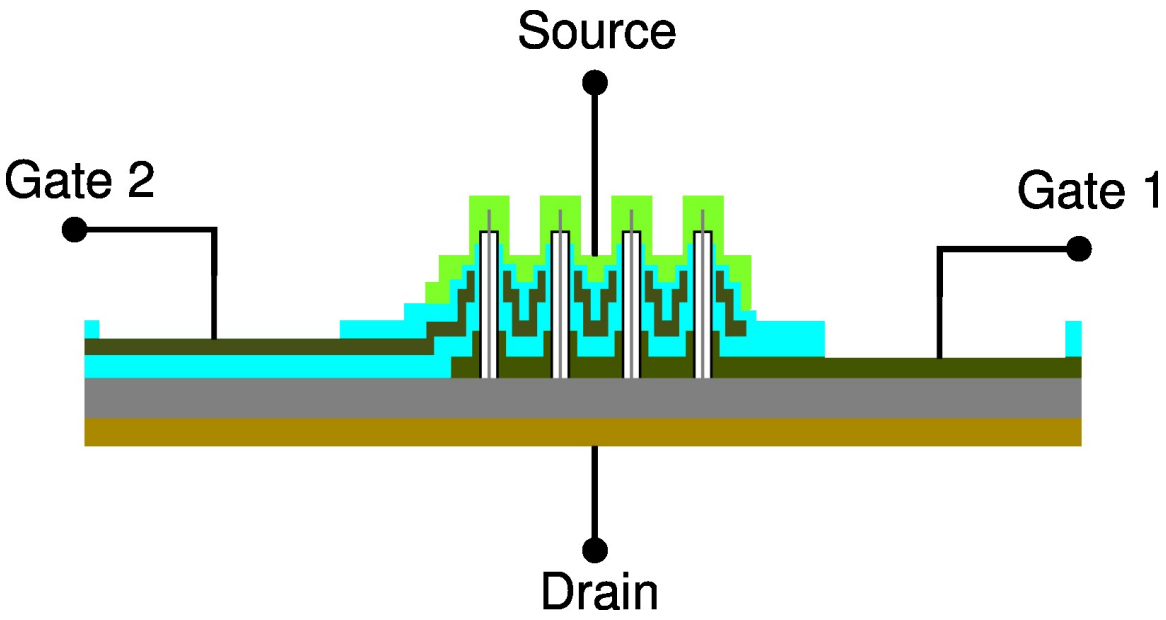


Figure 7.24: Schematic of vertically stacked, ambipolar, silicon LED.

7.4.1 Charge Accumulation

The regions enclosed by the wrap-around gates are treated similar to a MOSCAP. If the devices we fabricate are ideal (no work function mismatch or trapped charges) electrons and holes should begin to accumulate immediately after a positive or negative voltage is applied, respectively. For a W-SiO_2-Si interface it has been experimentally determined that the work function offset is about -0.3 V [94]. In order to calculate the effect of the interfacial charges we must take into account the cylindrical geometry of this MOSCAP. We can write:

$$\frac{dE_{ox}(r)}{dr} = \frac{\rho_{ox}(r)}{\epsilon_{ox}} \tag{7.6}$$

or

$$\int_S E_{ox} da = \frac{1}{\epsilon_{ox}} \int_V \rho_{ox}(r) dr. \tag{7.7}$$

Assuming that the gate has height h_g and that the interfacial charge is all concentrated in a thin ring around the silicon core, we can write:

$$E_{ox} = \frac{Q_{enc}}{2\pi r h_g \epsilon_{ox}}, \tag{7.8}$$

where Q_{enc} can be written in terms of the surface areal charge density N_s:

$$Q_{enc} = 2\pi R h_g N_s. \tag{7.9}$$

The change in potential across the oxide can be written by integrating the electric field once again in the r-direction:

$$\Delta V = \int_R^{R+t_{ox}} E_{ox} dr = -\frac{Q_{enc}}{2\pi h_g \epsilon_{ox}} \int_R^{R+t_{ox}} \rho \frac{dr}{r}, \tag{7.10}$$

where R is the radius of the silicon-silicon dioxide interface and t_{ox} is the thickness of the oxide. This gives:

$$\Delta V = -\frac{Q_{enc}}{2\pi h_g \epsilon_{ox}} \ln(\frac{R + t_{ox}}{R}). \tag{7.11}$$

For the example pillar and N_s of 10^{12} cm^{-2} the ΔV associated with the trapped charges turns out to be $\sim$ -0.246 V. So we can approximate the voltage used to draw carriers towards the gate as V_{gtot} = $V_{gapplied}$ - 0.546 [V] (remembering that the extra 0.3 V comes from the natural work function mismatch of silicon and tungsten [94]). In order to find the 'effective doping' of the region beneath the gate we can utilize the simple relationship that Q = CV, where the capacitance in our case is:

$$C = \frac{2\pi\epsilon h_g}{ln(\frac{R+t_{ox}}{R})}. \tag{7.12}$$

This trend is plotted for applied voltages between +/- 10V:

Unfortunately this simple model fails to accurately predict the carriers drawn to the gate as the

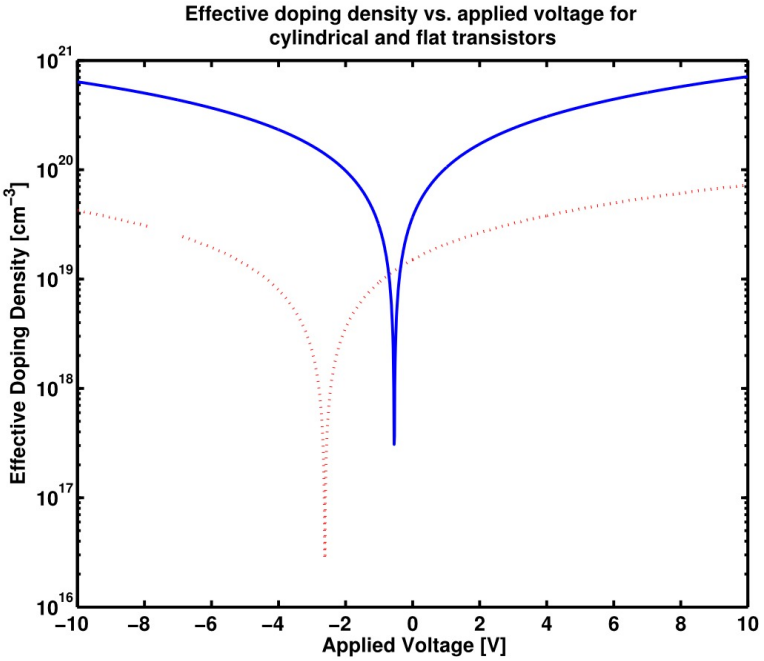


Figure 7.25: Effective doping density found under a wrap-around gate. The standard planar MOSCAP model with the same parameters is given as a dotted red line to show the large variation based on geometry.

assumption is a metal-like availability of carriers to screen the voltage applied at the gate. Since

the pillar is considered to be fully depleted, a more thorough analysis of the availability of carriers as a function of band bending needs to be performed. Although this model gives an idea behind the performance of the device, we created a more exact simulation of the whole device with finite element modeling.

7.4.2 FEM Model

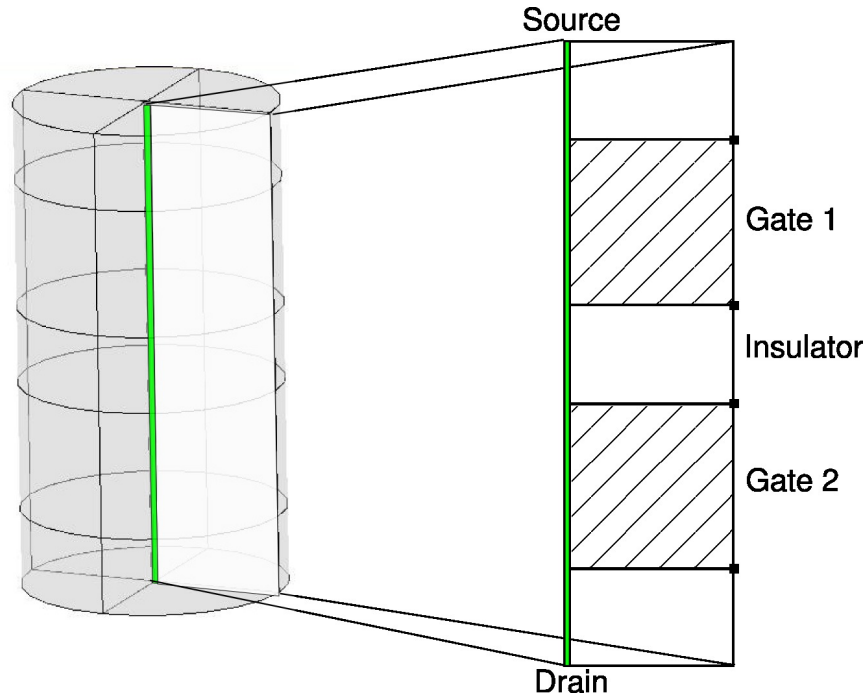


Figure 7.26: Schematic of model used to simulate the behavior of a dual gate diode.

The model used for the simulation can be seen in figure 7.26. It has axial symmetry and the carriers are confined to the bright green core in the middle of the structure. The white region is the thermal oxide that has been grown on the silicon nanopillar while the cross-hatched regions show the area of the oxide underneath the gates. The gate voltage is applied at the outside boundary of the oxide and the source and drain voltages are applied at the top and bottom boundaries of the silicon core as seen in figure 7.27.

For the device under simulation it was assumed that the bandgap was at 2 eV [20] and that due to both depletion and low dopant concentration, the Fermi level sits in the middle of the bandgap. The expressions used to calculate the carriers induced by the gate potential are:

$$n = N_C \exp\left[\frac{E_f - E_c}{kT}\right],\ p = N_V \exp\left[\frac{E_v - E_f}{kT}\right] \tag{7.13}$$

where $N_{C,V} = (2.51 \times 10^{19} cm^{-3})(m^*_{n,p}/m_o)^{3/2}$ for bulk silicon. We use these numbers in our case for

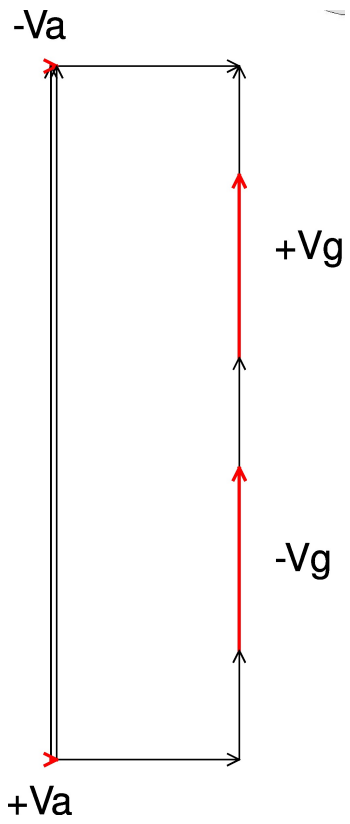


Figure 7.27: The biasing scheme for the simulation.

simplicity; for a more exact model these will have to be recalculated to take into account the lack of the six fold degeneracy of the conduction band. The finite element model applies the gate voltage, uses the resultant potential distribution to find the distance between the Fermi level and the band edges, calculates the local concentration of carriers and then uses this concentration to modify the original potential distribution. This process is repeated until a stable potential/carrier distribution is obtained. Figure 7.28 shows a potential distribution for +/- 1V applied to the gates and the source and drain fixed at 0 V. The built-in potential, calculated from the shape of the potential in the silicon core, is about 1.7 V.

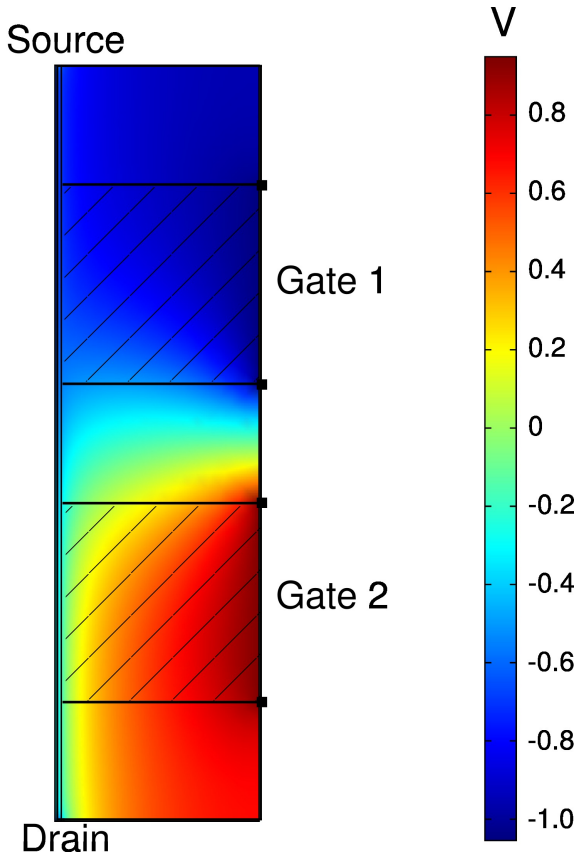


Figure 7.28: Potential distribution for Vg = +/- 1V and Vs = Vd = 0V. The z-axis goes from the bottom to the top of the page and the r-axis from left to right

Figure 7.29 shows the unit charge density under the previously mentioned biasing scheme. Note that the applied gate voltage is modified to take into account the flat-band voltage from trapped charges so that carriers are induced evenly on either side of the junction.

Plotting the carrier density with respect to the outline of the device (figure 7.30) shows that, under an applied bias of 0 V, the carriers are concentrated between the gate and source or gate and drain.

Since this device is effectively a 'PN'-type device the dominant current comes from minority

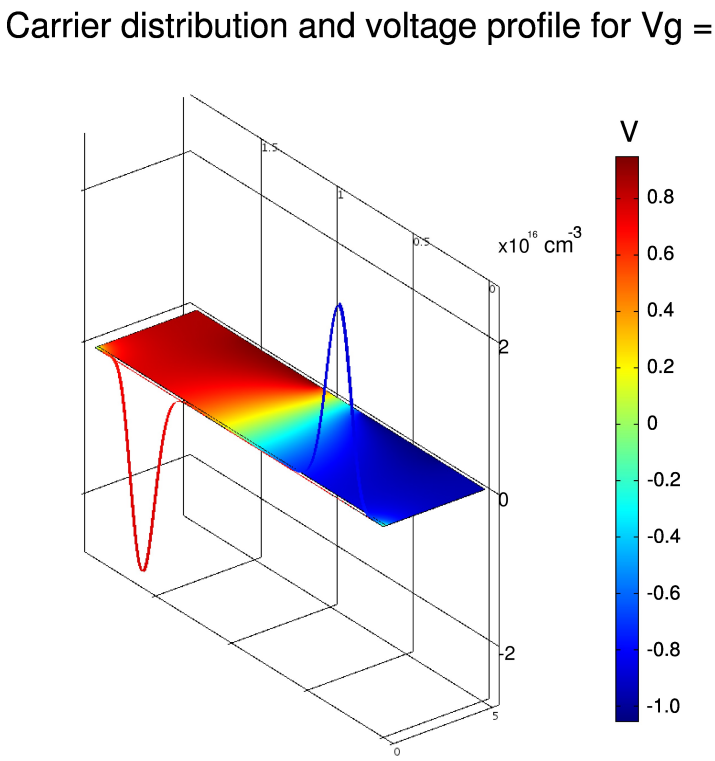


Figure 7.29: Potential and carrier distribution for Vg = +/- 1V and Vs = Vd = 0V.

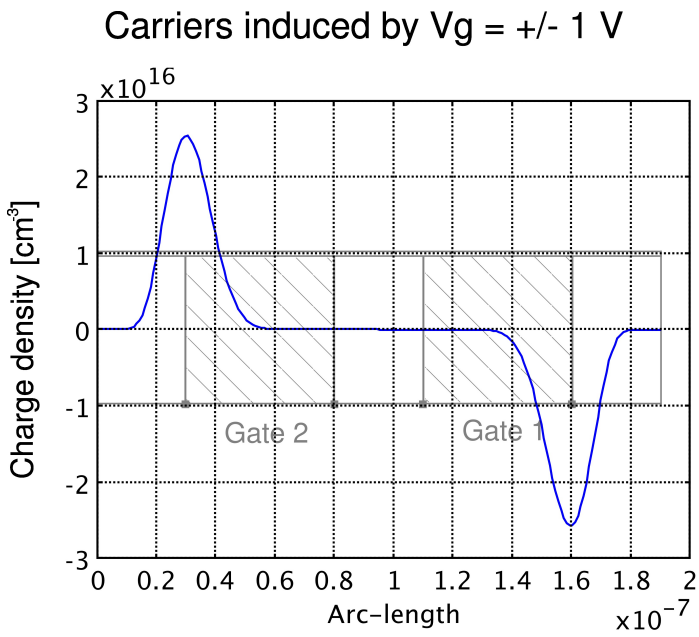


Figure 7.30: Carrier distribution for Vg = +/- 1V and Vs = Vd = 0V. The arc-length in this case is taken at r = 0 and goes from the drain to the source or z = 0 to the height of the structure (200 nm).

carrier diffusion. Unfortunately carrier diffusion was left out the simulated model, to be added in a future version of the simulation. However it was still possible to estimate the current under forward and reverse bias by examining the change in carrier concentration under different source-drain voltages. Since there were no efforts made to create sources and sinks of charges, excess charges were swept to the electrodes and gathered; so long as the excess charge concentration was several orders of magnitude less than the effective 'doping' concentration, the excess minority carriers did not perturb the potential distribution or doping and the device behaved similar to a PN diode. Figure 7.31 shows the carrier distribution with Vg = +/- 1V and Vs = Vd = 0V (blue) or Vs = -Vd = 1 V (green). The inset shows the excess, minority, hole concentration at the right hand, 'n-type' region of the device. The minority carrier density is calculated by integrating the total number of excess carriers (holes in the example) and dividing by the volume of the region where the carriers are in the minority; in this case the n-type region.

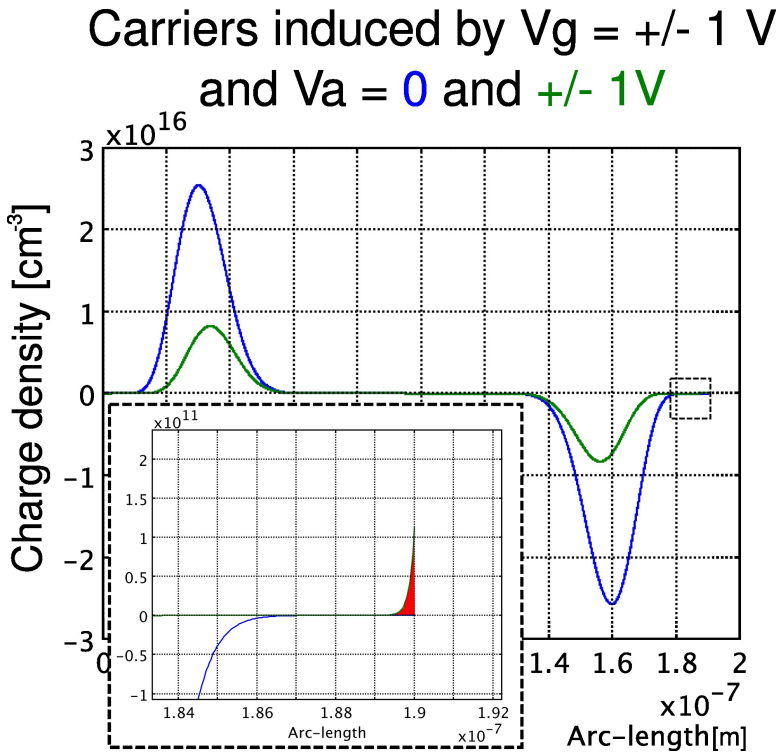


Figure 7.31: Carrier concentration at forward bias (green) vs. zero bias (blue). The arc-length in this case is taken at r = 0 and goes from the drain to the source or z = 0 to the height of the structure (200 nm). The inset shows the excess holes found at the drain electrode in the n-type region under forward bias. The arc-length in this case goes from the left to the right side of the dotted box.

Figure 7.32 shows a log-plot of the excess carrier concentration found in the FEM model for various applied biases. An exponential is fit to the linear region of the plot and has the form $\Delta n_p = \Delta p_n = 4.353 \times 10^{-38} \exp(V_a/kT)$. Following the trend presented in *Allen et al.*[93] we make

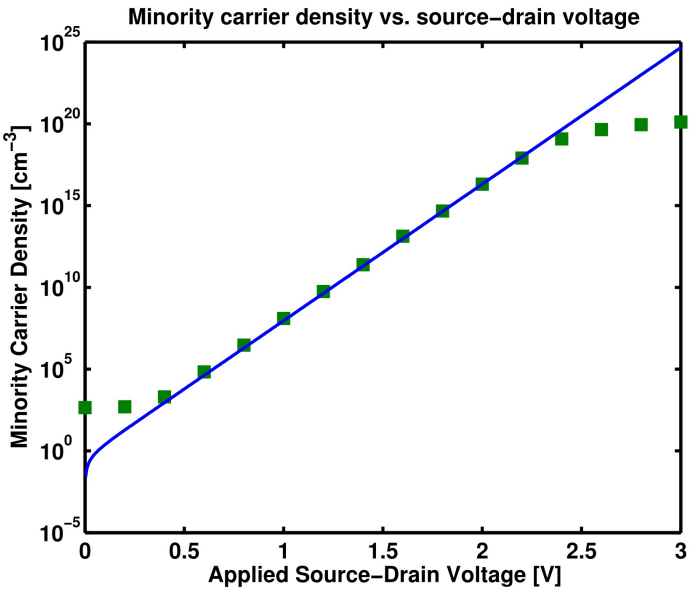


Figure 7.32: Log-plot of the excess minority carrier concentration for Vg = +/- 1V under forward bias (green squares). The blue line is an exponential fit to the linear portion of the excess carrier concentration. For simplicity, the applied voltage is split evenly between the source and drain; Vs = -Vd = Va/2.

the assumption that the diffusion length of electrons and holes is equal to the shortest dimension in the silicon core, in this case $L_n = L_p \sim 3$ nm. Assuming that the electron and hole recombination time is 1 ns we get diffusion constants of $D_n = D_p = 9 \times 10^{-9} m^2/s$. We can calculate the total current as:

$$I_{tot}(V_a) = qA \left[\frac{D_n}{L_n} \Delta n_p(V_a) + \frac{D_p}{L_p} \Delta p_n(V_a) \right] \tag{7.14}$$

where both Δn_p and Δp_n are calculated from the simulation and given by the green squares in figure 7.32. Plotted in 7.33 is the simulated current under forward bias. The blue line represents the current calculated from the fit in figure 7.32 and the red squares are the current calculated directly from the FEM simulation.

We can see that the current reaches high level injection at above 2 V of forward bias or roughly as the applied voltage reaches the value of the built-in potential. The leakage current under reverse bias is on the order of 3×10^{-27} A, a somewhat non-physical number. However this fits with the simple model under investigation that does not take into account any tunneling or recombination effects which greatly increase the leakage current. Recent work[95] has shown that SWNT ambipolar devices that can pass μA of forward current have leakage currents in the pA range.

In order to estimate the number of photons generated from such a device we assume a quantum efficiency of 0.1%, a reasonable number given a total carrier recombination time of 1 ns and published radiative recombination time of about 100-200 ns [20]. This corresponds to roughly 10 million

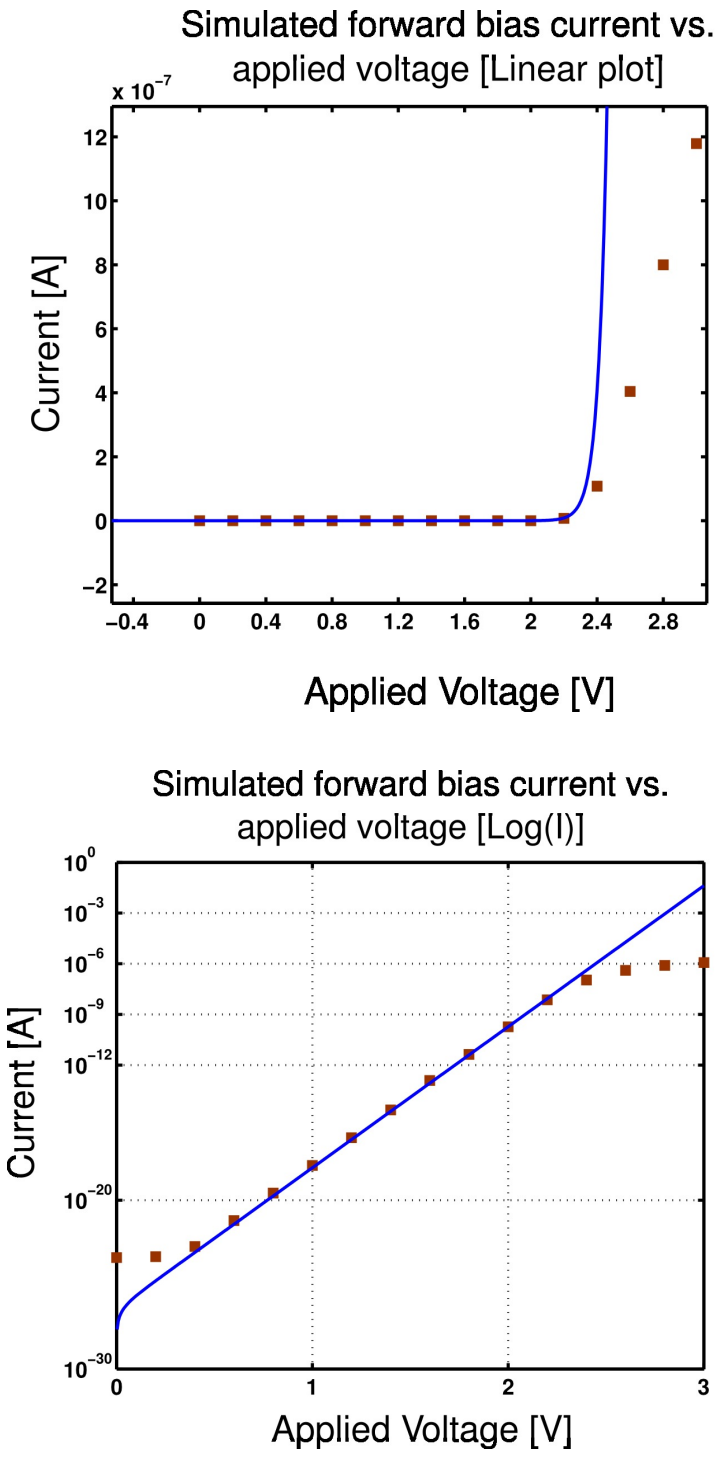


Figure 7.33: Linear and log plot of the I-V relationship under forward bias for a simulated ambipolar LED. The red squares are the results of the simulation and the blue line is from the best-fit curve in 7.32. Note that under greater forward power the simulation begins to diverge from the best fit line and decrease its slope. This is at roughly the point where the applied source-drain voltage approaches and exceeds the buil-in voltage. The equations (based on the Boltzman approximation) used to estimate the carrier distribution are no longer valid as the band-bending results in the fermi level crossing into both the conduction and valence band.

photons generated each second; for an emission wavelength of 600 nm the output power is in the pW range. However we can excite several thousand to million of these pillars at once by patterning over arrays of pillars instead of single pillars to directly increase the output power for a given applied voltage and current.

7.5 Current results and future directions

Fabrication difficulties have hampered the previous iterations of these devices with only one instance of a device working, shown in figure 7.34. Figure 7.35 shows a FIB-cut cross section of an array of pillars with two fabricated gates. The recipes for fabricating the two gates as well as back contact, contacting windows and patterning of the top contact have been developed and successfully implemented. There is, however, still difficulty with making the final, top contact, as it is difficult to remove all the layers of insulation to expose the 3 nm silicon core without damaging or destroying it. A new pillar fabrication technique, explained in the previous chapter, is being investigated as a means to more easily make contact to the silicon core. Figure 7.36 shows a schematic outline of how a larger head on the pillar could make contact the silicon core much easier. Instead of having to find the 3 nm, self-terminated core, the larger head does not narrow as much under oxidation. Figure 7.37 shows a pillar that has been etched to leave an expanded head and foot to simplify contact. After oxidation the larger head narrows down to a diameter of several 10s of nanometers making it much easier to contact than the 3 nm diameter core.

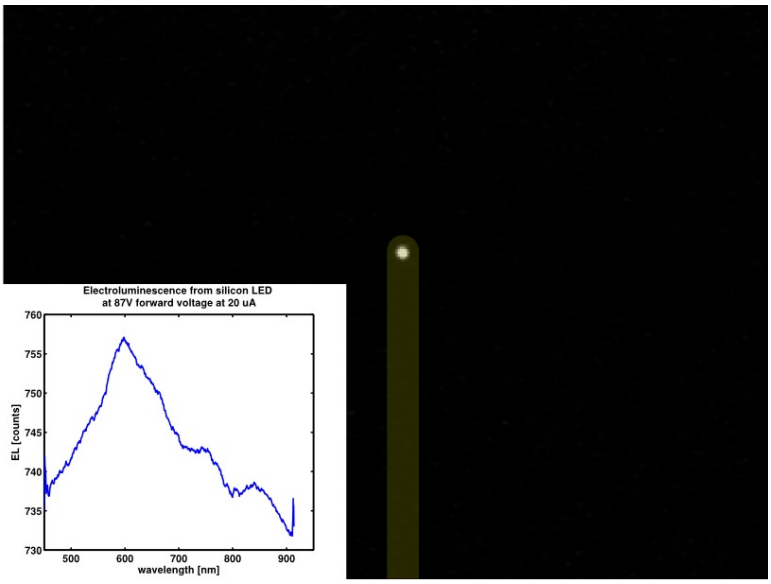


Figure 7.34: Spectrum and image of electroluminescent pad of silicon pillars. The coloring shows the location of the top contact with respect to the bright area.

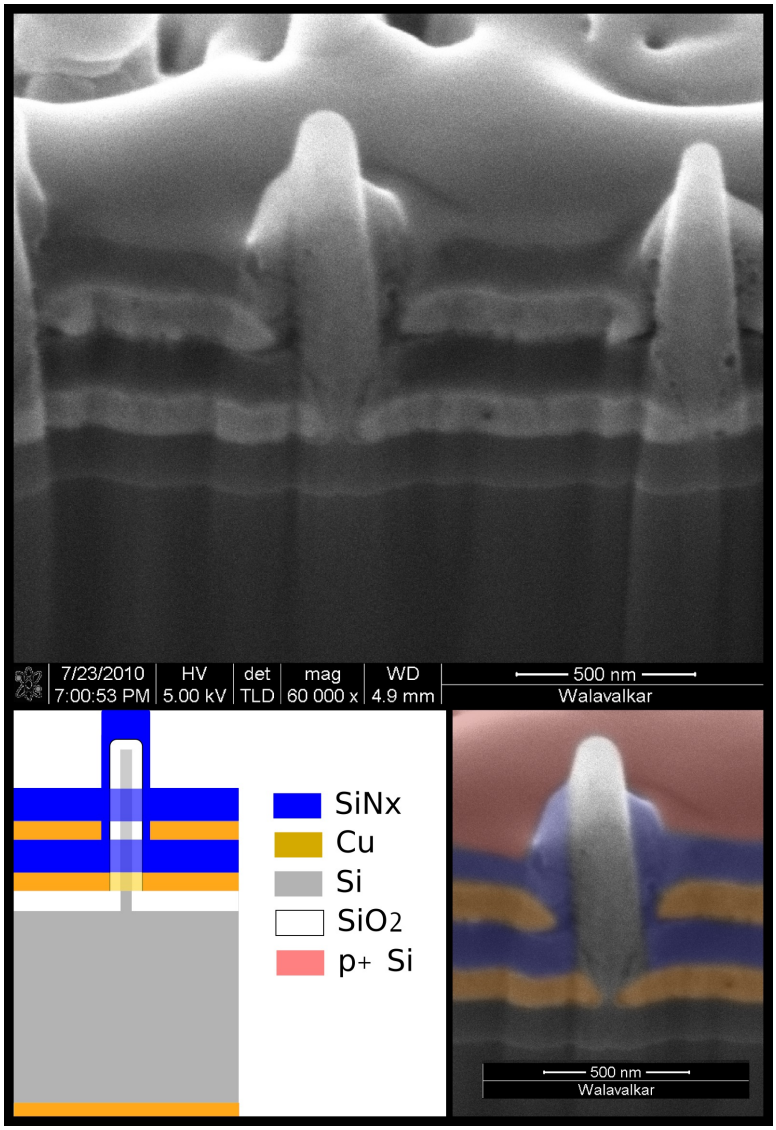


Figure 7.35: The top frame shows a FIB cross section of an array of dual gated pillars. The colorized SEM and the diagram outline the layers present in the image.

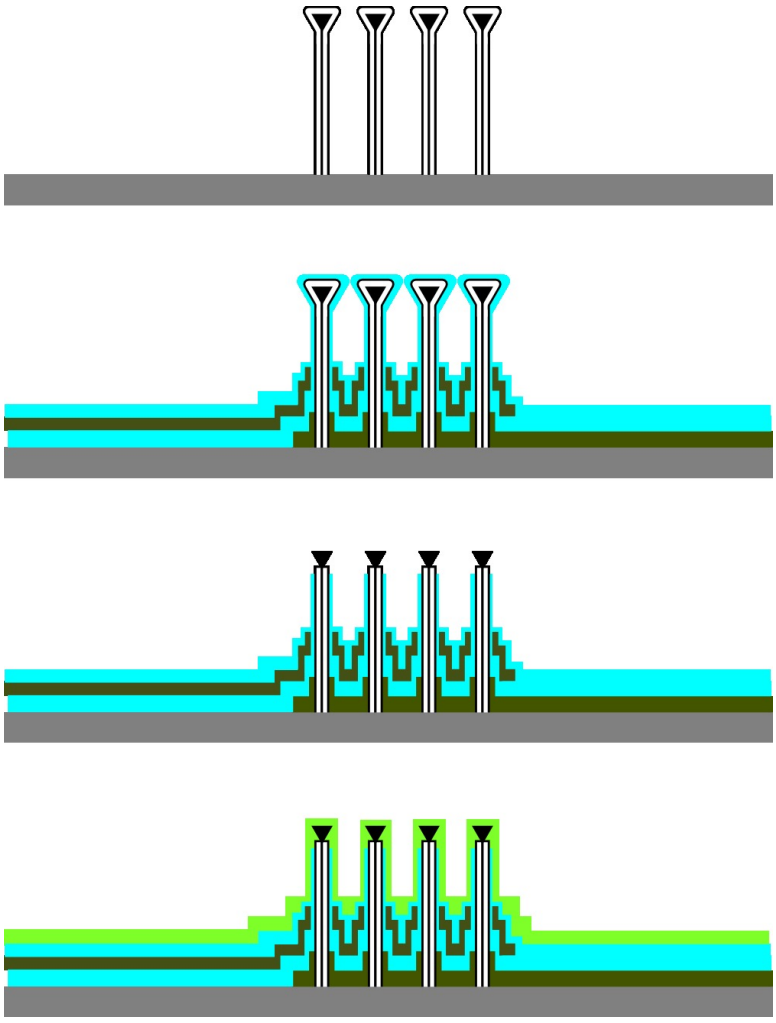


Figure 7.36: Fabrication schematic utilizing wine glass shaped pillars to simplify making contact to the top of the silicon core. These could be inserted at step 10 of the fabrication procedure in the previous section.

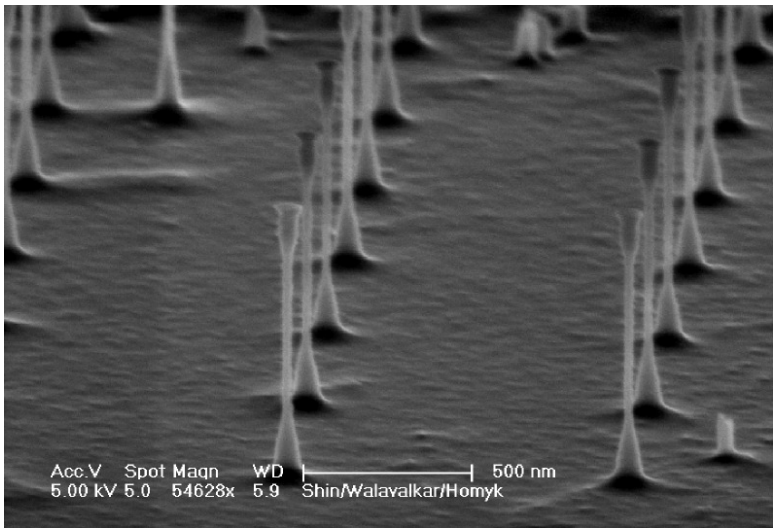


Figure 7.37: Wine glass shaped pillars to simplify fabrication of top contacts.

These devices can also be used in the future as fully reprogrammable logic elements. By changing the biasing on the two gates it is possible to use the device as a resistor, a diode in both directions, and a FET. Since the footprint of such a device can be quite small (as the contacts and gates take little more area than the pillar itself) it could be possible to use such pillars as a platform of future CMOS design technology.

Chapter 8

Concluding remarks and expanded applications

Exploring things deeper

This thesis presents an initial, broad foray into the study and fabrication of etched silicon 1-D nanostructures. Topics covered here include the mechanical, luminescent, and electronic properties of silicon nanopillars and stacked quantum dots. The works presented here cover only the portion of the work that has been completed and published or almost completed.

There are several directions that can be explored in the topics mentioned above, and most of these were talked about in the 'future directions' section of each chapter. However these do not encompass the whole spectra that can be examined. Quite a few of the experiments done were focused on attempting to break into new fields, however, this meant the initial papers, while interesting, featured theoretical explanations that fit the data, but perhaps did not contain all the underlying science.

In the mechanical deformation paper we quantified the strain using Timoshenko's bimetallic material theory[44]. However we did not actually measure the strain itself. The standard way to measure the strain is by TEM analysis of the deformation of the crystaline lattice or by Raman or X-ray diffraction (XRD) techniques. While the TEM measurement is not suitable for our samples, as the strained region is within the PMMA and nearly impossible to image, Raman spectroscopy and XRD could be used in future work to quantify the amount of strain in the pillars and develop a more involved theory.

In the pillar photoluminescence sections we performed a TBM simulation that incorporated strain to estimate the band-gap energy. When fed the pillar diameter (from TEM) and the strain (from theory[17]) the TBM method fit the data quite well and showed the red-shift in emission wavelength seen in experiments following a high temperature anneal to remove strain. However this model did not take into account the various other physical processes that were at work. For example the

increase in overlap of electron and hole wave-function causing the dipole matrix element to go up in magnitude was posited to be the reason that the PL lifetime decreased with the size of the pillars. However it was possible that this was caused by a variety of other sources like an increase in the non-radiative recombination rate due to the vicinity of the carriers to the wall of the pillar, causing the non-radiative rate to become dominant, and we would no longer be measuring the PL lifetime but rather the *carrier* lifetime; or the decrease in size increased the splitting between the Γ point and the X-direction valley improving the PL lifetime by separating the two valleys by several times the thermal energy.

There are also several interesting areas of this project that we can go deeper into. Redoing this experiment on <100>, <110>, and <111> oriented wafers could be interesting. In nanopillars in both the <100> and <110> direction the bandgap is theoretically found to become direct as the pillars decrease in diameter, however the bandgap remains indirect for nanopillars pointed in the <111> direction. It would also be useful to perform a gain/length measurement to view the suitability of these structures for low threshold laser devices. Finally, it would be quite interesting to see how the surface passivation affects the nanopillar emission; one could measure the PL while the pillar is covered in oxide, use vapor-phase HF etching to free the pillar from the oxide without destroying the thin whisker in the middle and remeasure the PL, and finally measure the PL after a hydrogen anneal to quench surface recombination.

For the etched quantum dots there are several PL measurements that could be taken, including single quantum dots or a single quantum dot pillar containing multiple dots under a variety of temeratures, or looking at the influence of an electrical gate on the peak emission wavelength, or as with the pillars, working out the gain/length of these structures.

Quantum tunneling measurements would be a very interesting direction to take with single quantum dot structures. These could be performed in the vertical or horizontal direction and over a wide temperature range within a simple cryostat. If quantum behavior can be maintained at room temperature these devices could be used as a basis for resonant tunneling transistors.

In terms of the chapter dedicated to the LED actual measurements of such a dual gated system have just begun to be performed but there is quite a bit of depth and theory that could be investigated in this direction in terms of working out the various electronic and luminescent parameters such as lifetimes or quantum efficiency. If we can make the devices efficient, cheap and completely CMOS compatible then there would be a huge interest in their use. Furthermore by being able to switch the biasing on each gate on the fly the same device could work as an LED in either direction, a transistor, a resistor, or an open circuit.

Extended applications

The size of these nanopillars puts them at a unique advantage to interact with biological strucutures and molecules. As cellular probes they are significantly smaller than cells, allowing them to be pressed into and through cell walls with little leakage. Figure 8.1 shows a set of pictures that show nanopillars placed on top of long, micron sized pillars. These structures were fabricated by first patterning aluminum oxide disks to mask the nanopillars, then aligning the micron sized photoresist mask to these pads of alumina. Then the micron sized pillars were etched with a cryogenic silicon etch as described in *Henry et al.*[13], and finally the nanopillars were etched using the standard 'pseudo-Bosch' technique described in Chapter 2. The micropillars could be used as a stand-off from the electronics of a chip while the nanopillars would serve as tiny probes that could puncture the cell membrane. The figure shows an array of micron sized pillars as it was a calibration run; however simple aligned optical lithography could be used to line up a single micropillar to a single pad of nanopillars and create a single micro/nano probe instead of an array. By patterning arrays of these pillars with spacing large enough to allow contacting to individual or groups of pillars we can electronically monitor the movement or growth of cells. Such a previous test was done to measure cell traction force by directly imaging polymeric SU-8 arrays of nanowires[11]. An example of two of their images is shown in 8.2. By knowing the strain dependent conductivity of a silicon nanopillar we can extract the deformation of the pillar in-situ and much more exactly than previously done.

The ability to fabricate structures as small as 1-2 nm gives us a unique tool to approach an outstanding problem in biology; the rapid sequencing of the genome. There has been a great deal of interest and work[96] recently in using solid state fabrication technology to tackle this important task. The most promising approach has been to fabricate small pores (about 2-4nm) in a dielectric membrane, such as silicon nitride, and drag single stranded DNA (ssDNA) through the holes. Since ssDNA has an overall negative charge and is narrower than 2 nm in diameter, a simple DC voltage in a salt solution can be used to translocate the strand from one side of the pore to the other. As the ssDNA moves through the pore the different base pairs block the ionic current through the pore differently, based on their atomic structure. It is believed that by tracking the ionic current that is passing through the hole it is possible to read off the sequence of base pairs based on characteristic dips in the transmission current. It has been shown [96] that it is possible to tell apart homo-type ssDNA (all A,C,G, or T) with this method. The fundamental problem with this method is that the membranes that contain the pores are at least tens of nanometers thick and so several base pairs are blocking the pore at once, making it impossible to distinguish between adjacent base pairs. Furthermore, the fabrication of these pores has traditionally been done with a serial process such as a FIB, limiting these devices to lab-scale testing and preventing their realization in a more traditional commercial CMOS fabrication line.

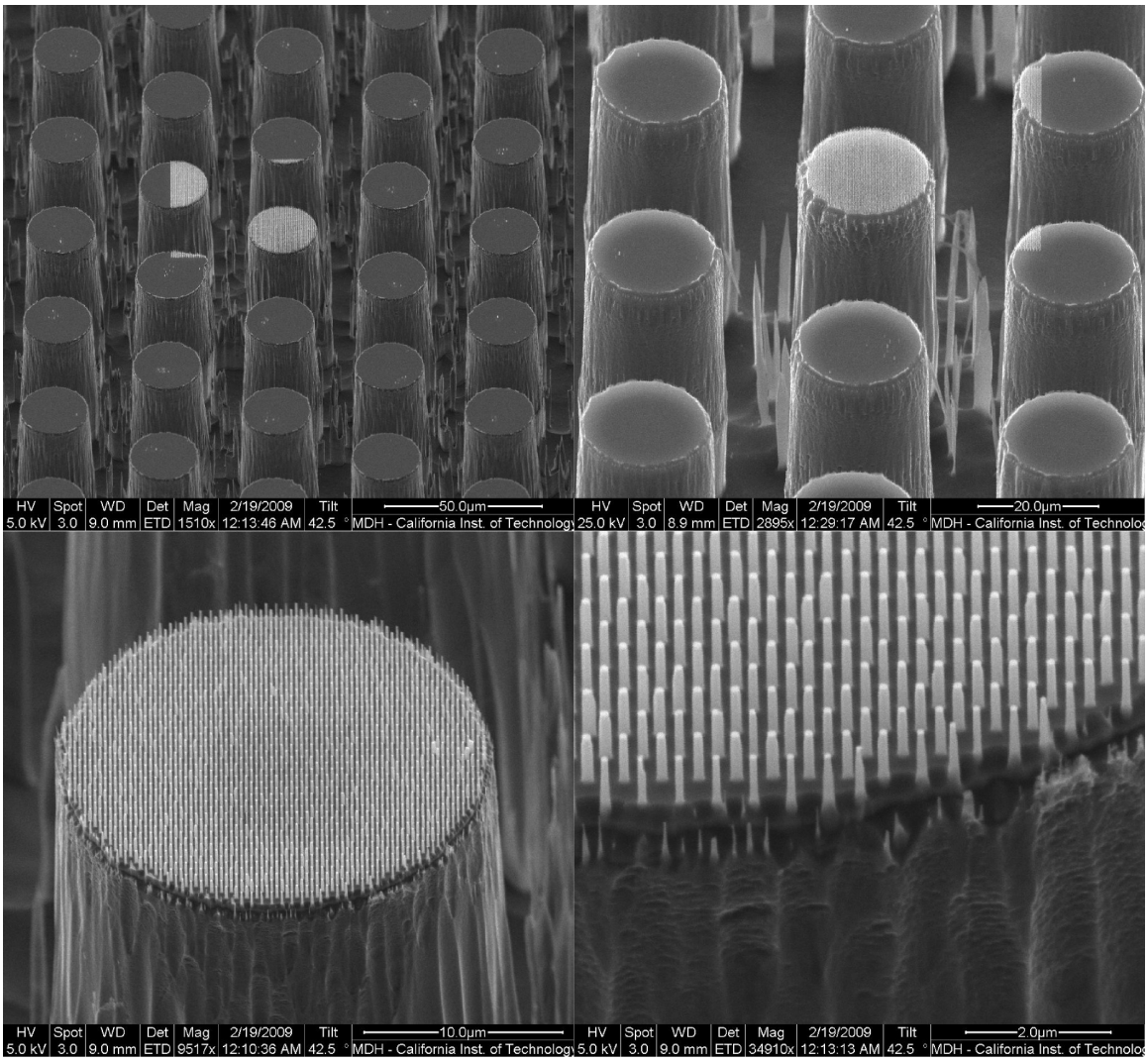


Figure 8.1: Images of various magnifications showing 100 nm diameter nanopillars placed on top of 20 μm diameter and 75 μm tall micropillars.

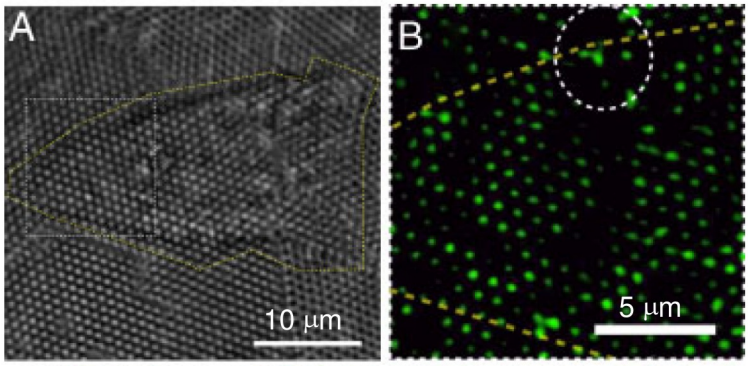


Figure 8.2: Image from *Kuo et al.*[11] showing (a) a transparent cell on an array of SU-8 nanopillars and (b) the same cell under higher magnification and excitation of the quantum dots placed at the tips of the pillars.

We propose a method that would use the confinement of nano-pores combined with our ability to fabricate thin, stacked layers to more accurately sequence ssDNA. Figure 8.3 shows a fabrication schematic to fabricate 2 nm pores in a top-down method; A pillar is fabricated on the front-side of a wafer and oxidized down to its terminal diameter of 2 nm. After oxidation the pillar is snapped off with a blade or polishing method. Then with back-side aligned photo-lithography it is possible to use a deep silicon cryo-etch to etch a 30 micron sized hole through the majority of the bulk silicon. The fabrication is finished by a dry XeF_2 etch that isotropically etches from the backside and through the 2 nm silicon core on the front-side. Figure 8.4 shows a TEM image taken through a hole cut in a bulk silicon chip that shows a 5 nm wide, top-down patterned hole in a silicon dioxide membrane, while the bottom pictures show optical micrographs of the top of 30 micron wide, aligned, suspended silicon dioxide membranes with fabricated nano-pores.

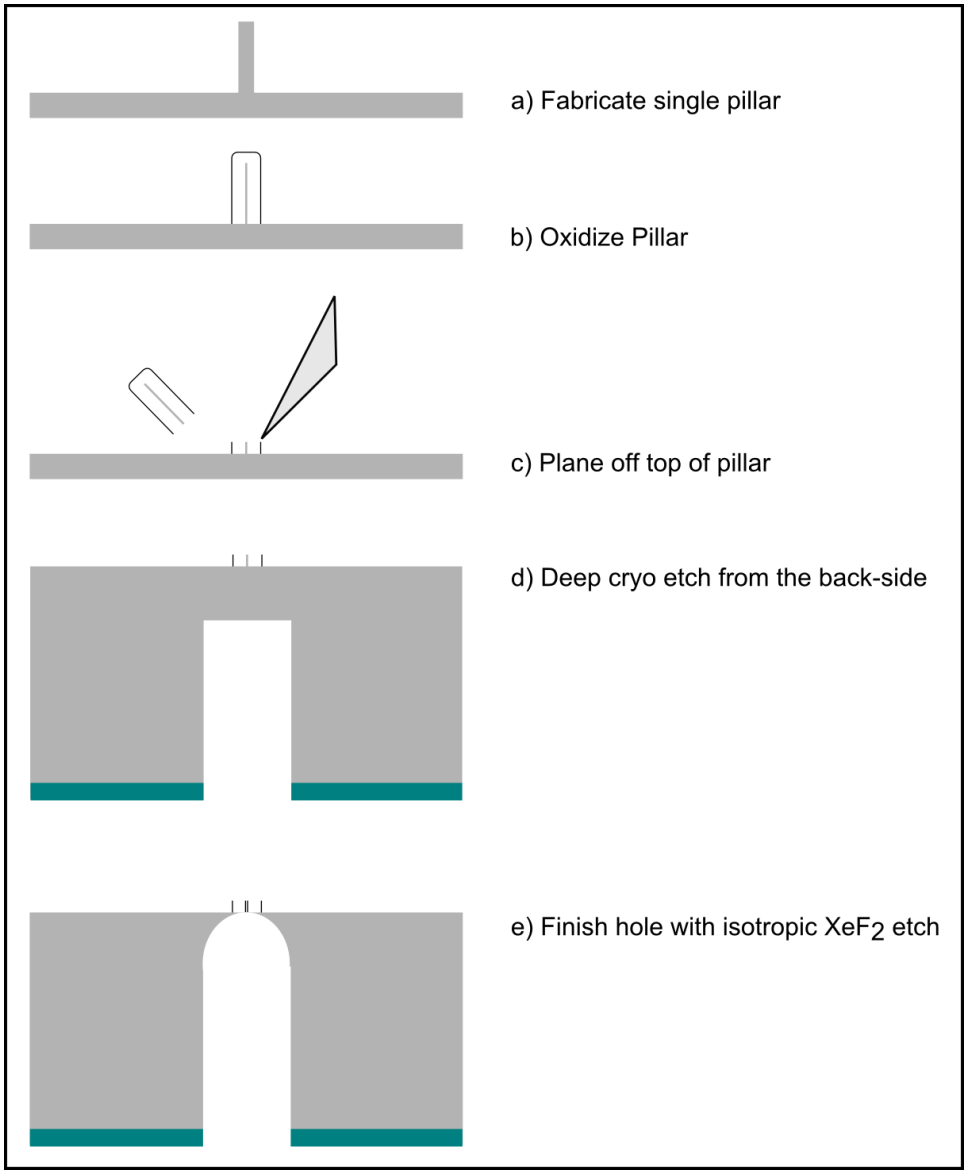


Figure 8.3: Process flow for fabricating 2 nm pores.

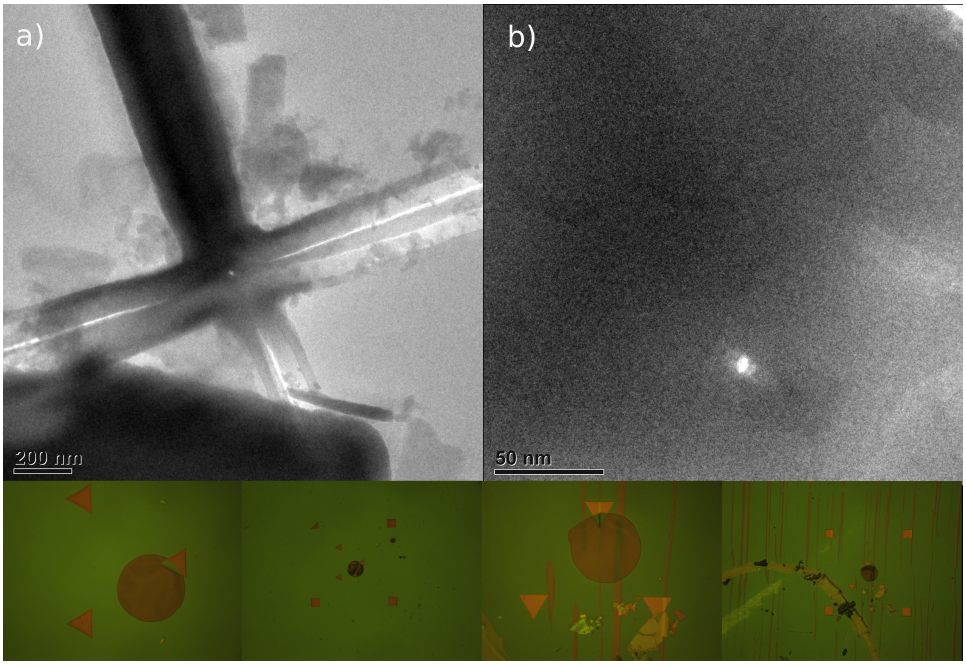


Figure 8.4: a) Through wafer TEM image of a top-down fabricated 5 nm diameter nano-pore. The cross-shaped outline is an alignment mark for ease of finding the pore in the TEM b) Close-up of 5 nm pore. Bottom: Optical micrographs of the topside of a free-standing silicon dioxide membrane (diameter of roughly 30 microns) under-cut from the backside of the wafer with a cryo etch and aligned to the single nano-pillar pore with photolithography. The squares and triangles are alignment marks.

Instead of relying on blockage current to parse base-pairs of the ssDNA I propose an inelastic tunneling detection scheme. Figure 8.5 shows a schematic of the device. The transverse field is applied to the ionic solution to drive the DNA through the nano-pore. The base pairs on the DNA are measured by looking at the change in tunneling current between the two metal layers that sandwich a thin dielectric layer, and surround the nano-pore. Inelastic tunneling measurement methods have been shown to accurately map out both defect energy and location in dielectric layers and could readily be applied to distinguishing ssDNA base pairs by treating them as 'defects' in the thin dielectric layer[97, 64]. Since we can choose the dielectric thickness quite accurately by using a well characterized deposition recipe we can specify the interaction volume we want between the electrodes and the DNA. With the recent interest in depositing thin dielectrics for gate oxides it would be possible to make this layer between 2-5nm thick allowing us to probe volumes approaching the size of a single DNA base pair.

Four such tunneling resistors would be fabricated in a "Wheatstone Bridge" configuration with one of the resistors aligned with the pore 8.6. By taking a differential measurement with respect to three other resistors, that do not contain pores, it should be possible to make very accurate measurements of the change in tunneling current as the DNA molecule moves through the pore, and thus read off the base-pairs.

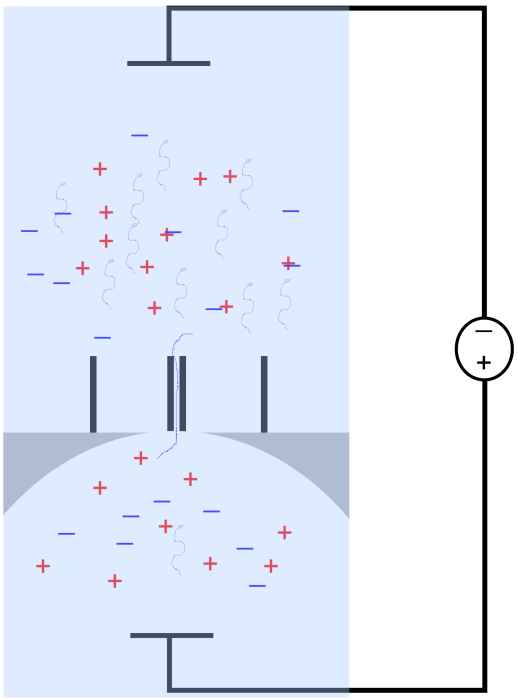


Figure 8.5: Schematic of DNA translocation. DNA is moved by the field set-up with the DC bias voltage. The presence of DNA in the pore blocks the ionic current induced by the voltage.

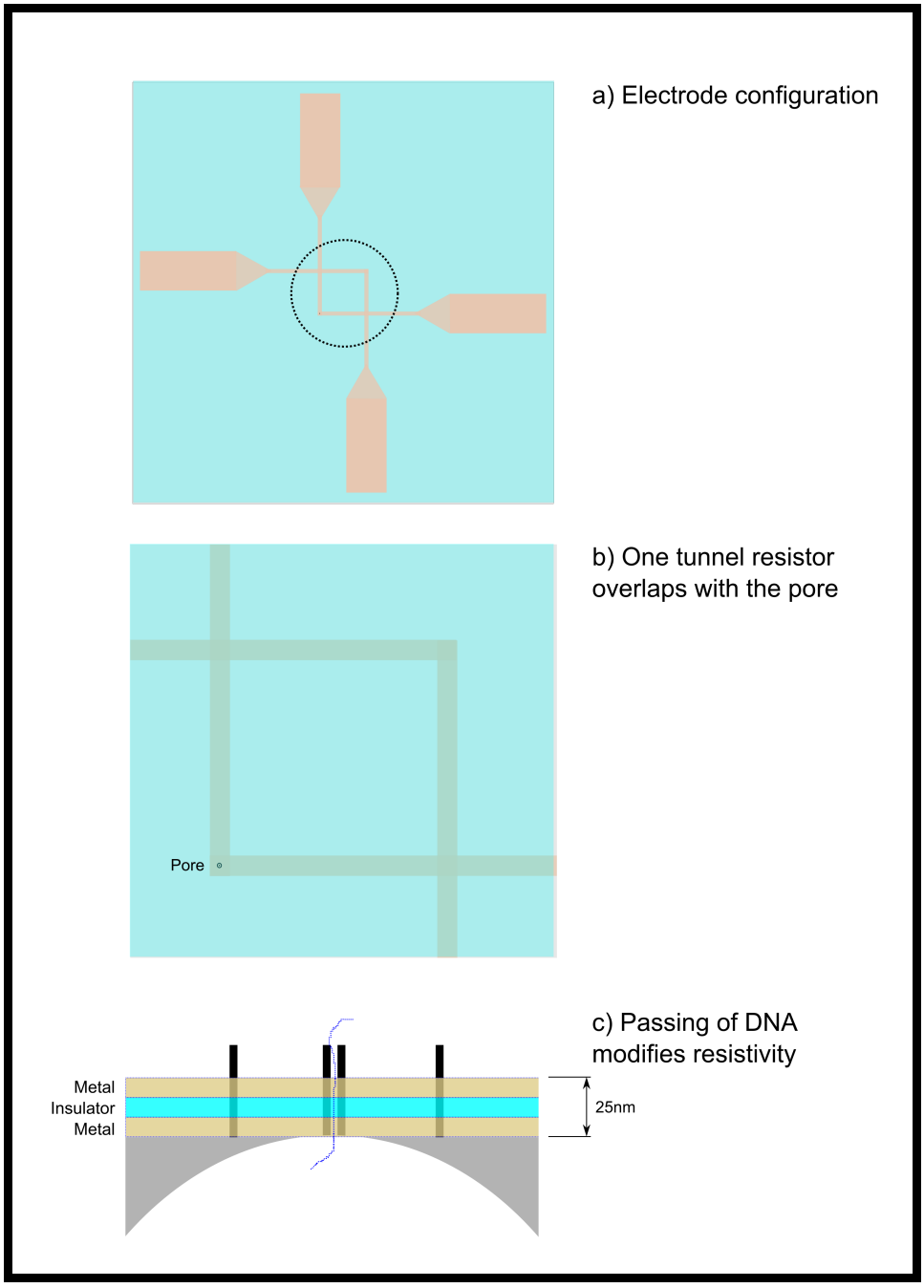


Figure 8.6: a) Cross-bar electrodes to read off DNA base pairs. Each crossing is a vertical tunnel current resistor. b) Note that one of the vertical reistors overlaps with the pore. c) The tunnel resistor is made up of a thin dielectric sandwiched between two metal layers.

Concluding remarks

This thesis has covered the fabrication, oxidation, and characterization of silicon nanopillars. Recipes for patterning and depositing the aluminum oxide hard-mask were also included. The 'pseudo-Bosch' etching technique was explained as the ideal way to etch the nanopillars including variations of the etch intended to form quantum dots and wine glass shaped pillars. Self-terminating oxidation was utilized to thin the silicon portion of the nanopillars down to 2 nanometer diameters while maintaining a silicon dioxide sheath around the silicon core for support.

Various properties of these nanopillars were examined. Initially un-oxidized nanopillars were tested for their mechanical flexibility by using PMMA as an electron beam activated, force mediating polymer. By examining the final bend angle of the pillar as it protruded from the PMMA it was possible to calculate the amount of strain present in the pillar; strains as high as 25% were found with bend angles up to 60^o. Furthermore, it was found that the pillars were undergoing, at least macroscopically, only elastic deformation, as they would snap back to their original orientation after they were released from the polymer.

The photoluminescent properties of thinned silicon 'whiskers' were measured as well. By utilizing the self-terminating oxidation it was possible to generate large arrays of nanowhiskers with uniform and predictable diameters. By examining the peak PL wavelength and comparing it to the TEM measured silicon core diameter it was possible to come up with a trend that described the blue-shift of the bandgap energy with decrease in whisker diameter. When constructing a TBM model of narrowed pillars it was found that it was necessary to take into account the strain fixed in the pillar by the oxidation in order to accurately model the behavior of the bandgap with decrease in whisker diameter. The importance of strain shown as the peak emission energies all red-shifted when the pillars were annealed at temperatures above the viscoelasctic flow temperature for glass and the silicon dioxide could reflow and neutralize the strain.

The quantum dots, etched with oscillating passivation conditions, were also luminescent after a round of oxidation. Depending on the initial size of the dots fabricated on a pillar, the decreasing post-oxidation diameter was shown to be correlated with the blue-shift in peak emission energy.

Finally the attempts at creating an electroluminescent, silicon device were explained. Current attempts at the fabrication of dual-gated, ambipolar, LEDs was explored, and the work completed was shown in a series of diagrams and SEM images. A theoretical and FEM model were created to estimate the future behavior of the device in action. The FEM model proved to produce more reasonable results and was used to calculate the expected current and diode-like behavior of the device. Current efforts are closing in on the successful fabrication of this type of device and will yield luminescent results.

Appendix A

Appendix A: Random musings on fabricaton

These are some recipes and tricks I have come up with while working in lab. This is meant to be an informal section; if things are unclear feel free to contact me at sameer.walavakar@gmail.com with the subject line 'Lithography'.

e-beam resist

This covered some of the tricks I use with PMMA.

- Always clean the wafer in the order: Acetone, IPA, N_2 Dry, Dichloromethane (DCM), IPA, N_2 Dry, 170 C^o bake on a hot-plate. The IPA and dry is needed between the acetone and DCM because those two chemicals are not miscible and result in a foggy solute that can stick to a wafer. Cleaning the wafer helps the PMMA spin on with fewer irregularities.

- If something goes wrong with the patterning or spinning always clean with DCM, acetone does not do a good enough job at removing PMMA. If thoroughness is needed run the cleaning process, then a 5 minute oxygen plasma, and then the cleaning process again before re-spinning the wafer.

- I use a high dose for PMMA due to some early fabrication difficulties with 75 nm thick PMMA. I use 1200 $\mu C/cm^2$ which over-doses the resist and ensures a good development. If there is residual resist left on the chip the alumina disks tend to have holes or peel-off entirely. In my case if my alumina disks are larger than expected due to overexposure/development my undercut etch can fix that problem. I try to keep my fabrication processes in the saturation range where there is always a little give in terms of precision while performing an etch/deposition/clean/exposure/development.

- When doing lift-off, as with cleaning the wafer, acetone is useful to help partially dissolve the PMMA, however to do a good job of stripping the PMMA DCM is needed. (remember that acetone and DCM don't mix!) Even with DCM there are occasions where a thicker mask is used and in those cases sonication or exfoliation via q-tip is required. The most reliable method of lift-off we have found is to invert and suspend the wafer in DCM and then sonicate it for 30 seconds. Inverting the wafer prevents flakes of alumina from re-depositing on the surface.

- If PMMA is being used as a spacer layer always over bake it. If there is any solvent left or play in the PMMA metals will not stick at all. If photoresist processing is done on the PMMA after baking ensure that the process is done via lift-off for some reason any baking of the PMMA once a metal layer is deposited causes the metal to buckle and bubble.

Photoresist

Some of my photoresist tricks.

- Be aware of the surface on which you are spinning the photoresist (PR). Silicon and silicon dioxide surfaces behave quite similarly for most PR. However if you are spinning onto a large quartz or glass wafer remember that your bake times are going to be completely different as the glass is quite a poor conductor. Furthermore, on some surfaces the PR just won't adhere, some of these include: Alumina, spin-on glass, and depending on the PR some metals provide poor adhesion.

- AZ 5214 is my photoresist of choice; like PMMA I tend to over-expose the resist. That it can undergo a reversal allows me to define all my masks as light-field masks letting me more easily align them.

- A rough positive process for AZ 5214 is: Spin at 3000RPM for 30 seconds, bake at 110 C^o for 70 seconds, expose on the 365 linewidth for 23 s with the machine with the lamp and 40 s with the machine with the LED, develop for 35 seconds in CD-26A– the pattern should be completely visible after 30 seconds, however there is still scum on the bottom.

- A rough reversal process for AZ 5214 is: A rough positive process for AZ 5214 is: Spin at 3000RPM for 30 seconds, bake at 110 C^o for 70 seconds, expose on the 365 linewidth for 23 s with the machine with the lamp and 40 s with the machine with the LED, bake at 115 C^o for 90 seconds to reverse, and flood expose for 60 seconds in the lamp aligner and 100 seconds in the LED aligner, develop in CD-26A for 35 seconds.

- When I am running a bi-layer process with PMMA under PR, IPA is good for removing the PR but leaving the PMMA alone. It may take a long soak in IPA but it should eventually

remove all the PR and leave the PMMA untouched. In order to reduce the time of removal one can decrease the temperature of the soft-bake to 100 C^o.

- If a thinner layer of PR is needed (typical AZ 5214 layers are between 1-2 μm) it can be cut with anisole. At about a 15:1 ratio of anisole to PR the PR begins to lose fidelity in terms of obtaining the mask pattern. The development time is much shorter based on the ratio of anisole to PR.

- AZ 5214 does stand up to XeF_2 for short periods of time however, fluorinating this polymer causes it to curl up quite a bit and it no longer sticks to the substrate well. This polymer can only be removed by a long oxygen plasma; it is fairly immune to acetone, IPA, and even DCM.

Pseudo-Bosch

- When doing characterization of etches it is quite helpful to have someone standing by on an SEM to do rapid prototyping so you can converge on a good etch quicker than etching several samples first and then SEMing them later to find the ideal etch.

- It is useful to run a hight forward power oxygen plasma in the ICP-RIE chamber at the end of the etch to strip whatever passivation polymer is left on your chip. A 10 second plasma should be sufficient.

- There are several knobs to turn to optimize an etch; go wild...just don't break the machine... In my opinion people are too scared of fabrication to really make full use of the technology

Copper

- Copper is a great material and adheres to just about any surface.

- Copper is only compatible for short periods of time with HF

- Copper does stand up to XeF_2.

- Sputtering copper, in my experience, tends to form a film with a larger grain-size while thermal evaporation tends to produce a denser more amorphous film. This is important when performing copper etches as the sputtered copper etches much faster than the evaporated copper.

- Copper etches quite well and fast in CR-7 chrome etch. When I do wet copper etches I dilute the CR-7 with 5 parts of water and etching through 100 nm of copper usually only takes 5 seconds.

- Copper has trouble remaining un-oxidized as it's being handled in subsequent processing steps, however when being used as a contact material it, like the statue of liberty, it only oxidizes on the exposed surface and can be pierced by probe tips quite easily.

Gold

- Evaporated or sputtered gold does not stick to glass or silicon well; titanium and chrome are good adhesion layers, although e-beam evaporation of chrome is quite finicky.
- Gold etches quite well and fairly quickly in Transene Gold Etch TFA, a mixture of potassium iodide and dissolved hydrogen iodide.
- Gold stands up to HF quite well, but peforms exceedingly poorly in XeF_2; more than 10 pulses on a gold subtrate will result in a tarnishing of the gold as well as sputtering the gold onto the sample holder plate. An example is shown in A.1.

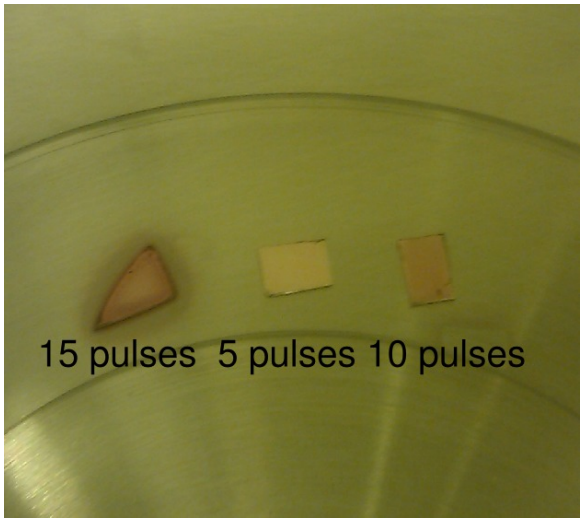


Figure A.1: Samples with the top surface covered with e-beam evaporated gold etched for various times in XeF_2. Note the greater number of pulses the more tarnished the gold becomes. By 15 pulses the gold has started sputter onto the sample holder as shown by the dark halo around the left-most sample.

Tungsten

- Tungsten is most easily deposited by sputtering; a relatively high power ($\sim$200 W) is required to obtain a decent deposition rate.
- Tungsten also etches with the same gas chemistry as silicon; SF_6 is a particularly good etchant for tungsten as WF_4 is volatile at room temperature.

- Like aluminum, tungsten compounds can be deposited with reactive ion sputtering. In the presence of oxygen tungsten forms tungsten oxide, a clear, slightly conductive dielectric that can mask chlorine based etches of III-V materials (as WCl_4 is not volatile at room temperature). It can be patterned via lift-off or by depositing the film, masking it with resist, and etching it with CF_4/O_2. Tungsten can also be deposited with methane to form tungsten carbide. The properties of this sputtered material are currently under study.

ITO

- Indium Tin Oxide is a great material for making transparent/translucent contacts. It is fairly resistive as, in order to retain clarity, the ITO must be deposited with excess oxygen.

- When depositing clear, conducting ITO I use the readily available 90:10 ratio of indium oxide to tin oxide sputtering target. I deposit the material with an RF sputtering gun as the target is only slightly conductive. ITO deposited with a pure argon gas chemistry produces a pink/purple colored, dim plasma. When oxygen is introduced with a ratio of 100 Ar: 1 O_2 the plasma becomes a vibrant pink/red color and is much brighter.

- The easiest way I found to etch ITO is HCl. Undiluted HCl (32-35% by weight) etches ITO very quickly, even the vapor coming off a 20 mL of the dissolved acid will etch off a 100 nm in less than 3 seconds. I use HCl diluted in DI water with a ratio of 1:20 and still etching off 100 nm takes less than 15 seconds. I am not aware of a gas-phase etch of ITO but it would be reasonable to assume that a chlorine based RIE would probably work.

Aluminum

- Buried aluminum layers, even when protected by PR/PMMA, will corrode within 15 seconds of exposure to BHF. Very frustrating.

- Aluminum etches quite well in Tetramethyl ammonium hydroxide (TMAH) and supposedly etches well with a chlorine chemistry in an RIE. Photoresist developer containing TMAH (MF/CD series) is a quick ever-present substitute for commercial aluminum etchant.

- Aluminum can be sputtered at quite a fast rate at 400 W, allowing for thick layers ($\sim$250 nm) to be deposited.

Al_2O_3

- I am partial to alumina as its use as a etch mask for nanostructures helped to open the field that this thesis is about. A great deal about its deposition and stoichiometry was covered in chapter 2.

- Alumina etches in BHF, KOH, and phosphoric acid at 60 C^o. In terms of a dry etch a chlorine chemistry is supposed to work but I haven't had an occasion to try it. Alumina's natural hardness allows it to stand up fairly well to high forward power argon ion beam or RIE etches.

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