Signal Integrity Issues in High-Speed Wireline Links: Analysis and Integrated System Solutions

Thesis by

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To

Yadollah Analui and Ashraf Kamali

for their unconditional love.

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Abstract

This work focuses on the basic signal integrity issues of high-speed wireline links. It bridges the gap between optimum system design and circuit design for such links by: (1) understanding the effects of the system parameters on the bit error rate (BER), (2) introducing circuit architectures for the realization of systems that minimize the BER, and (3) demonstrating integrated circuit prototypes that verify the solutions.

First, we develop a theory that analytically relates the data link BER to the system characteristics, *e.g.*, the channel response, the pre-amplifier bandwidth, and the transmitter clock jitter. We generate the BER contours to find the optimum receiver bandwidth as well as the optimum sampling point and its associated timing margin. We also develop the theory of the data-dependent jitter (DDJ), which is a significant component of the timing jitter in high-speed links. We provide an analytical distribution function for the DDJ of an arbitrary linear time-invariant system and include the impact of the DDJ on the BER.

Second, we propose a bandwidth enhancement method for wideband amplifiers. This is useful for the realization of high-speed links in technologies that suffer from large parasitic components. The method leverages two-port broadband matching to enable amplifier stages to achieve their maximum gain-bandwidth product. We demonstrate a 10Gb/s CMOS 0.18µm amplifier with this technique that has 2.4 times the bandwidth improvement over a design that does not apply the technique.

Third, we develop an eye-opening monitor (EOM) that enables full integration of adaptive equalizers. The EOM evaluates the signal eye diagram quality and reports a quantitative measure, which is correlated to the signal integrity. We demonstrate a prototype in 0.13µm standard CMOS that operates up to 12.5Gb/s and has 68dB error dynamic range.

Finally, we introduce an instantaneous clockless demultiplexer for burst-mode communication applications. We propose a clockless finite state machine that recovers and demultiplexes the received burst of data instantaneously. The architecture consists of a combinational logic structure and a bit-period-delayed feedback loop. We demonstrate a 1:2 clockless demultiplexer based on this concept in SiGe BiCMOS technology that operates at 7.5Gb/s.

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Chapter 1

Introduction

1.1 Information Technology: Desire for Higher Speed

Integrated systems are among the key technologies that have revolutionized the information era by enabling high-speed computation and communication technique as well as high-speed access to stored information. The commodities benefiting from this revolution, *e.g.*, internet, personal computer, and cellular wireless phone, have become commonplace. The evolution of such commodities has caused a dramatic growth in the amount of information generated and in the number of end users who access that information. A recent study estimates 0.5 million terabytes of original information was distributed over the internet in 2002, double the amount in 1999 [1]. The number of internet users worldwide has also increased by 146% from the year 2000 to the year 2005 [2]. The continuous growth of internet traffic necessitates an upgrade in the backbone infrastructure and local area networks to support even higher data transfer rates and larger numbers of end users. The Synchronous Optical NETwork (SONET) [3][4] and Ethernet [5] are evolving in response to this demand for communication at higher speed.

In addition to end users, there are two more types of network nodes that access information and will take advantage of higher data transfer rates: processor nodes and storage nodes. Today's microprocessors run at about 100 times faster than 15 years ago [6] due to device scaling and architecture design advances. As on-chip clock frequencies increase, I/O bus bandwidth becomes the speed bottleneck in a multi-chip environment. Developing high-speed chip-to-chip links allows increased processing power and faster networking with other chipsets. The impact of higher-speed links becomes increasingly significant in distributed computing networks and the so called “super computers” with multiple processing nodes, where the system's performance relies on fast, error-free communication between the processing nodes.

High-speed access to data storage devices for fast transfer of large volumes of information is another emerging application for high-speed data communication. An example is storage area networks (SAN) that, in contrast to a single large-capacity device, consist of a scalable network of storage nodes. The projected amount of data that will be stored using a SAN-based database is three million terabytes in 2005 [7]. Advancement of technology in various areas will accelerate the generation of more original information. For instance, sensor networks will be ubiquitous and will constantly sense and aggregate data from various environments. This data needs to be stored in sizable databases. Similarly, large databases will be necessary to store human genome sequences that occupy about 0.75 gigabytes per human being. The continuous increase in the size of databases is an additional incentive for developing high-speed mass-storage media networks.

In brief, high-speed reliable communication in various forms has to evolve inevitably to maintain efficient connectivity and information accessibility in a growing population of networks that consist of processors, storage nodes, and end users.

1.2 Scope of this Thesis

This thesis explores basic challenges in high-speed wireline communication, *i.e.*, at 10Gb/s and beyond, and provides silicon-based integrated circuits and systems as solutions. High-speed communication systems, also called high-speed links, typically use electrical or fiber optic channels for data transmission due to the large available bandwidth in such channels that allow higher transmission rate. Wireline links can be categorized based on the transmission distance and the transmission rate, as shown in Figure 1.1. Chip-to-chip links establish communication between chips on a single printed circuit board (PCB), such as the memory unit and the CPU. Backplane links refer to the communication between nodes on different expansion cards that are inserted on a single

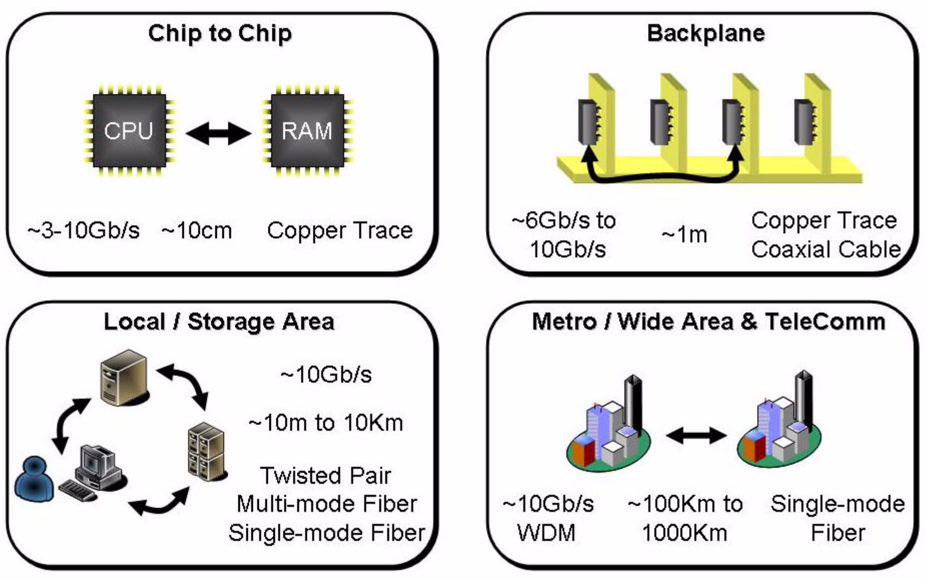


Figure 1.1: Categories of wireline communication applications

backplane board or a motherboard. An example is the link between several line cards on one backplane of a network router [8]. In a backplane link, the data rate is typically higher and the transmission distance is longer compared to a chip-to-chip link. However, the channel used is still electrical.

If the transmission distance is more than 100m and the data rate is above 10Gb/s, electrical transmission lines are not deployed anymore mainly due to the significant loss of the channel. In such cases, multi-mode fiber (MMF) or single-mode fiber (SMF) are used. While the copper attenuation easily reaches 10dB/m at 10Gb/s [9], typical loss of modern single-mode fiber remains below 0.5dB/Km in the 1200nm-1600nm wavelength range [10].

Although several applications exist in various categories discussed above, the front end architecture of the high-speed chip-to-chip, backplane or optical communication links is similar, as will be discussed in Chapter 2. The focus of this dissertation is on the basic challenges of high-speed link design resulting from channel impairments and hardware restrictions and thus the contributions that can be applied to any of the above categories of wireline communication links.

1.3 Why Silicon-Based Integrated Circuits?

Silicon-based integrated circuits (IC) play a central role in the evolution of the high-speed networks. The major advantage of silicon-based technologies is their ever-increasing capacity for integration that enables realization of complex ICs at very low cost. For example, one consequence of integration includes doubling the number of transistors in a microprocessor every 18 months [11][12], while dropping the price of each transistor by a factor of 100 over 15 years [12].

Besides cost advantage, integration has two other benefits. First, the parasitic impact of package and board on the interface between functions that are now integrated on the same die is eliminated. Therefore, the operation speed can be significantly higher as the speed is now only limited to the on-chip device and interconnect parasitic components. Second, the power consumption of the chip is lowered because the I/O drivers, required at the interface between chips in a multichip environment, will be eliminated.

The scaling trend of the silicon-based technologies, specifically the CMOS technologies, enables fabrication of devices with a higher frequency of operation. The latest International Technology Roadmap for Semiconductors (ITRS) projects the possibilities and challenges of integrated system design to year 2018 [13]. For instance, by 2009, the maximum unity current gain, f_t, and unity power gain, f_{max}, of a MOS device with 32nm gate length are expected to be 280GHz and 310GHz, respectively [14]. Scaling as well as development of advanced silicon technologies such as silicon germanium (SiGe) HBT transistors with germanium-doped base and silicon-on-insulator (SOI) technology with small device to substrate parasitics enables silicon technologies to meet the performance requirement of high-speed applications. Consequently, along with a remarkable integration advantage, silicon-based technologies seem to be capable of delivering more functionality for a lower price and are the perfect candidate for the implementation of low-cost high-speed integrated circuits.

1.4 Challenges

The main challenge in designing high-speed links is to understand and combat channel response restrictions. As the speed of link operation increases, the channel impacts that were primarily neglected will have a significant effect on the link reliability. For instance, frequency dependent loss and dispersion caused by channel degrade signal integrity and introduce inter-symbol interference (ISI) and data-dependent jitter (DDJ) that increase error probability. To optimize the link reliability, the ISI and jitter impact of the channel response should be quantified. Furthermore, the error probability should be related to the ISI and jitter, in addition to the channel noise.

If the channel response is known, Nyquist pulse shaping is used to eliminate the ISI [15]-[17]. However, pulse shaping is typically not applied to high-speed communication because the channel response is not necessarily known *a priori*. The alternative approach that is feasible for high-speed links is adaptive equalization. Equalizer is a filter that is designed to reshape the received pulse to minimize the overall effect of ISI and noise at the sampling point. Adaptive equalizer automatically adjusts filter parameters to accommodate unknown channel response and its variations over time. Adaptive equalization algorithms based on fast fourier transform have been efficiently realized by digital signal processors (DSP) at low frequency (multimega bits per second). However, the prohibitively large power consumption of the DSP and analog-to-digital converters at multigiga-bits-per-second speed makes such an approach impractical. Instead, realization of adaptive equalizers at 10Gb/s and beyond requires analog high-speed adaptive transversal filters and robust adaptation techniques with their associated circuitry.

The signal degradation induced by the channel is intensified by the nonidealities of the receiver circuit. Integrated circuits eliminate the bandwidth limitations imposed by the parasitic components of the packages and the wiring between the packages in a discrete design. However, intrinsic device and metal interconnect parasitics on the chip still restrict the maximum achievable bandwidth. Single-chip implementation of 10Gb/s systems requires an understanding of the factors that limit the on-chip operation speed and encourages development of circuit techniques and topologies for overcoming those limitations.

1.5 Contributions

This thesis focuses on the analysis, design, and hardware implementation of high-speed wireline integrated communication systems. The investigation of the challenges described in Section 1.4 has led to original contributions in this thesis that can be categorized into the following specific topics:

- Fundamental understanding of factors that affect signal integrity in high-speed data links, as the link data rate increases.
- Design of high frequency silicon-based circuit topologies for the receiver.
- Development of novel architectures and signal processing techniques for maintaining signal integrity in the high-speed links.

We will elaborate on these topics individually in the following and conclude the chapter with the thesis organization.

1.5.1 Fundamental Issues: Signal Integrity

This work provides a fundamental understanding of data-dependent jitter (DDJ) from a design perspective. Jitter is the deviation of the threshold-crossing times of data or clock transitions from a reference time. In a conventional communication system, the clock that is used to sample the signal and recover the data is derived from the received signal itself. Therefore, the clock inherits the phase uncertainty of the data transitions in the received signal. Understanding how data and clock jitter exacerbate bit error probability is fundamental to the design of a high-speed link. In our work, we focus on DDJ that is predominantly caused by system bandwidth limitation. The ISI resulting from the bandwidth limitation shifts the threshold-crossing times and translates to jitter. We provide a comprehensive analytical framework to model and predict DDJ caused by any linear time-invariant (LTI) system [18]–[22]. Associating the LTI system response to the DDJ provides insight for circuit and system designers for minimizing jitter and complements conventional measurement-based methods. In addition, we can predict the DDJ contribution of a system at any data rate from its step response. Experimental data verify our model predictions for various systems with less than 7.5% error.

1.5.2 High-Speed Integrated Circuit Topologies in Silicon

We propose a method for bandwidth enhancement of wideband amplifiers [23]. Using the bandwidth enhancement methodology, we demonstrate the first 10Gb/s 0.18µm CMOS trans-impedance amplifier [24][25]. This methodology is based on two-port broadband matching of multistage amplifiers. Passive components are introduced between stages and form wideband networks with controlled transfer impedance functions. Device parasitics are absorbed into the passive networks. As a result, the networks isolate cascaded stages and avoid loading. Therefore, in theory, each amplifier stage can achieve its maximum gain-bandwidth product set by the Bode-Fano limit [26][27]. The prototype we implemented shows 2.4 times the bandwidth improvement over a design that does not apply the technique.

1.5.3 Novel Architectures: High-Speed Signal Processing to Maintain Signal Integrity

The first contribution to this topic is the development of a novel eye-opening monitor that enables full integration of adaptive equalizers in the receiver high-speed front-end [28][29]. An eye-opening monitor (EOM) is a block that evaluates the quality of the received signal eye diagram and periodically reports a quantitative measure, which is directly correlated to the signal quality. This output is used as a cost function for automatic adjustment of the filter coefficients in an adaptive equalizer. Our proposed EOM can effectively capture a two-dimensional image of the eye diagram shape at the output of the equalizer. Its simple error detection mechanism allows implementation at very high speed. The prototype implemented in 0.13μm CMOS was successfully tested up to 12.5Gb/s [29]. It provides up to 68dB output error dynamic range that is sufficient for the optimization algorithm of the equalizer coefficients.

The other thesis contribution in this area is a novel architecture for instantaneous clockless demultiplexing [30]–[32]. Instantaneous data acquisition is required in burst-mode communication systems, where the data stream arrives at the receiver in asynchronous packets separated by unknown quiet intervals. Conventional narrowband phase-locked loops require a long preamble with a large acquisition time and are therefore not suitable. As an alternative to gated oscillators that require a full-rate clock for operation, we have proposed a clockless finite state machine that recovers and demultiplexes the received burst of data instantaneously. The architecture consists of a combinational logic structure with immediate response and a bit-period-delayed feedback loop. Therefore, every time a burst is received, the operation is initiated exactly in-phase with the first bit and continues synchronous to the stream. We implemented a 1:2 clockless demultiplexer based on this concept in a SiGe BiCMOS technology and verified its operation at 7.5Gb/s.

1.6 Thesis Organization

The dissertation consists of seven chapters. Chapter 2 covers the basic principles of the wireline communication systems. The objective of this chapter is to provide an introduction to wireline communication transceiver architecture and familiarize the reader with various channel impairments in high-speed applications that impact the link reliability, *i.e.*, probability of making an error. Each of the next four chapters, Chapters 3 to 6, cover one of the topics that was discussed in Section 1.5. The approach common to all the chapters is to, first, discuss the prior art and introduce the novel concept of the circuit topology or system architecture that is developed as part of the thesis. Then the design steps are discussed. Finally, each chapter concludes by demonstrating a hardware prototype and by providing experimental data from the measurements of the prototype that verify the concept. Chapter 3 describes the contributions to the understanding of data-dependent jitter from a circuit design perspective. Chapter 4 presents the methodology for bandwidth enhancement of wideband amplifiers. The eye-opening monitor technique is the subject of Chapter 5. Lastly, Chapter 6 discusses the development of the instantaneous demultiplexing architecture. We conclude with a summary in Chapter 7 that covers the achievements of the thesis as well as suggestions for future research to expand the results of the current work.

Chapter 2

Principles of High-Speed Communications

2.1 Trade-Offs in Link Design

The objective of the communication is to transfer information reliably from a transmitter to a receiver [33]. The measure of reliability is the probability of making an error in detecting the received information bit. A typical high-speed wireline link is designed to transfer data at a specified rate, *e.g.*, 10Gb/s, while maintaining a given level of reliability, *e.g.*, error probability of 10^{-12}. The physical medium that acts as the channel is selected based on the required bandwidth as well as the maximum amount of signal attenuation that can be tolerated due to channel loss. Once the channel is selected, the first step in link design is to derive the relationships between the error probability and the link specifications, *e.g.*, gain, bandwidth, sensitivity, jitter generation, and jitter tolerance. Then, the parameters of the transmitter and the receiver blocks are determined from such relationships as to minimize the error probability. Other parameters such as cost or power dissipation that affect the practicality of the design are also considered at this stage.

In this chapter, we introduce the underlying concepts of a high-speed wireline link and describe the first step mentioned above. We discuss the link design challenges caused by the inter-symbol interference (ISI) and jitter. Then, we analyze the relationship between the error probability, the ISI and jitter. We study the combined impact of the ISI and jitter on the link reliability and demonstrate the trade-offs between the ISI, jitter, and system parameters such as bandwidth. Finally, we provide a unified relationship that enables minimization of the link error probability in the presence of both the ISI and jitter. The assumptions and definitions of this chapter will be used throughout the dissertation.

2.2 Modulation Schemes

2.2.1 Modulation

The dominant modulation scheme that is used in high-speed links is two-level pulse-amplitude modulation (2-PAM). In the 2-PAM, the binary information is encoded to two signal levels. Typically, bipolar signals, *i.e.*, symmetrical levels around a well defined zero threshold, are selected. For instance, -1/2 represents binary “0” and +1/2 represents binary “1”. This way, if the information source generates “0” and “1” with equal probability, the data sequence will have a zero average. This is advantageous in reducing the wander jitter, which is the long term deviation of data transition time from a reference time and happens due to the drift or variation of the threshold.

The 2-PAM is also the dominant modulation method in optical communications. However, the physical phenomenon that transfers the information in optical communication is optical power or light intensity that can not take a negative value. The optical signal levels are switched between a high value and zero, *e.g.*, by modulating an optical source to *on* and *off* states. Therefore, the unipolar 2-PAM modulation in optical communication is typically referred to as the on-off keying (OOK) modulation.

The main reason for using 2-PAM in high-speed communication systems is its simplicity. The 2-PAM signal can be generated by simply turning a transistor or a laser source *on* and *off*. The detection mechanism is also simple, and it does not require accurate power-level control. A main reason to use more complex modulation techniques such as M-PAM or M-QAM is to achieve a higher data rate using the same channel bandwidth. However, because the channel in wireline links has abundant bandwidth, the designers tend to deploy simple 2-PAM modulation instead of a more complex technique and use a faster device technology to achieve the high data rates. Nevertheless, more recently, as data rates have hit the bandwidth limitations of copper transmission lines, it has become reasonable to design circuits for implementation of more complex modulations such as the

4-PAM [34][35]. In such a case, although a more complicated slicer, clock, and data recovery architecture is needed, the required bandwidth is only half of the bandwidth required for the 2-PAM because the symbol rate is half of the data rate. In this chapter, we assume that a 2-PAM modulation is used with amplitude 0 and 1 for information bits “0” and “1,” respectively.

2.2.2 Symbol Coding

The signal shapes in high-speed links typically take a nonreturn-to-zero (NRZ) format, which means that the pulses that represent each bit last for a full bit period, T_b. This is in contrast to the return-to-zero (RZ) signaling, where the pulses last only for half of the bit period. Figure 2.1 illustrates the NRZ and RZ representations of a “1011001” data sequence with unipolar pulses. RZ is typically preferred in the long-haul optical telecommunication networks, where the optical power is expensive, because the RZ format has relaxed signal-to-noise requirements compared to the NRZ format [36]. In other words, since the RZ pulses are *on* a shorter period of time, for a given average transmitted power, they have higher peak power compared to the NRZ pulses. This results in a lower bit-error probability because the optical receivers respond to the peak power.

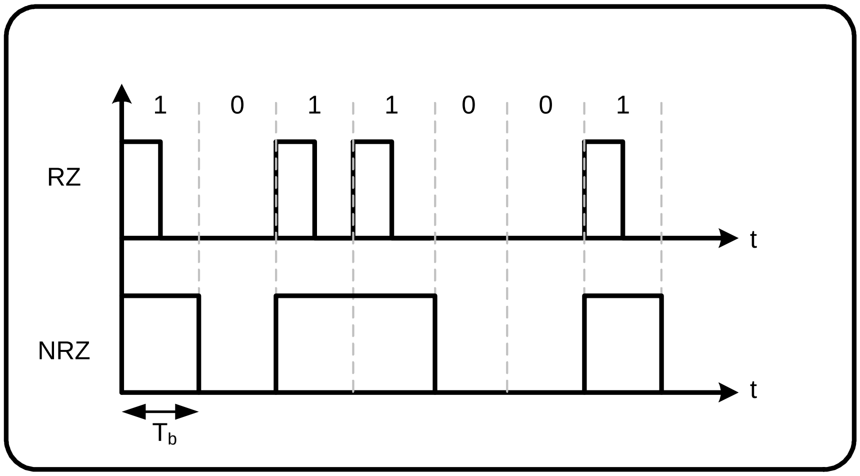


Figure 2.1: RZ and NRZ formats representing a “1011001” sequence

On the other hand, the RZ pulses have a larger transition density. They require a larger channel and receiver bandwidth, twice as much as the NRZ. Therefore, the NRZ pulses are the dominant format in high-speed wireline links due to their smaller bandwidth requirements and simpler implementation. In this dissertation, we assume that all the data sequences follow the NRZ format.

One potential problem with the NRZ format is the occurrence of long sequences of “0” or “1,” also referred to as consecutive identical digits (CID) [37]. When a long sequence of CID is transmitted, there is not any transition in the data for a long time. Consequently, the receiver that extracts the timing information from the spacing between received data transitions loses synchronization. To avoid the loss of synchronization, the data is encoded before the transmission using run-length-limited code words. Such code words guarantee a maximum number of CID bits. For instance the 8-bit/10-bit (8b/10b) encoding scheme that was proposed by IBM [38] is widely used in several high-speed wireline applications, such as Fibre Channel for storage networks and 10Gigabit Ethernet for local area networks. The 8b/10b coding replaces a byte of information with 10 transmission bits. It guarantees a maximum of five CID bits. In addition, it keeps dc balance of the signal by allowing an equal number of “1s” and “0s” for transmission. A disadvantage of the 8b/10b coding is the 25% increase in the data rate. Basically, to keep 10Gb/s data throughput, the signaling speed must be increased to 12.5Gb/s because of the 25% data overhead added by the encoding. This is undesirable in some applications such as SONET. Instead SONET standard recommends using data scrambling (no overhead) or very low overhead encoding. However, the link for SONET is required to tolerate up to 72 CID [36][39].

Coding techniques are also used for other purposes in data transmission such as error correction [36] and spectral shaping [40][41]. In this dissertation, we assume that the data sequence is a random binary sequence using 2-PAM NRZ signaling.

2.2.3 Power Spectral Density

A 2-PAM NRZ signal can be formulated as

$$x(t) = \sum_{k=-\infty}^{\infty} a_k \cdot p_i(t-kT_b) \qquad (a_k \in \{0, 1\}) \tag{2.1}$$

where $p_i(t)$ is the unit pulse function that is defined as

$$p_i(t) = \begin{cases} 1 & 0 \le t \le T_b \\ 0 & otherwise \end{cases} . \tag{2.2}$$

The coefficient a_k represents the kth transmitted bit which is “0” or “1” with known statistics. Because the transmitted bits are each a random variable, $x(t)$ is a stochastic process. We can show $x(t)$ is a cyclostationary process [17], which means that the mean and autocorrelation function of the process are time dependent and periodic. The average power spectral density, *i.e.*, the Fourier transform of the time-averaged autocorrelation function, demonstrates how the signal power is distributed in the frequency domain. It is an indication of the required bandwidth for transmission of a 2-PAM NRZ signal. The power spectral density can be calculated as

$$S(f) = \frac{1}{4}\delta(f) + \frac{1}{4}T_b \cdot [sinc(f \cdot T_b)]^2 \tag{2.3}$$

where the $sinc(x)$ function is defined as

$$sinc(x) = \frac{\sin(\pi x)}{\pi x} . \tag{2.4}$$

The first term on the right-hand side of (2.3) is the dc power that is caused by using unipolar signaling. The double-sided power spectrum is plotted in Figure 2.2. Due to the zeros of the *sinc* function, the spectrum experiences frequency nulls at integer multiple frequencies of the data rate, $1/T_b$. This indicates that the synchronization mechanism in the receiver should be a nonlinear process because the received signal itself does not have any information at the clock frequency. Figure 2.3 shows the same power spectral density on a

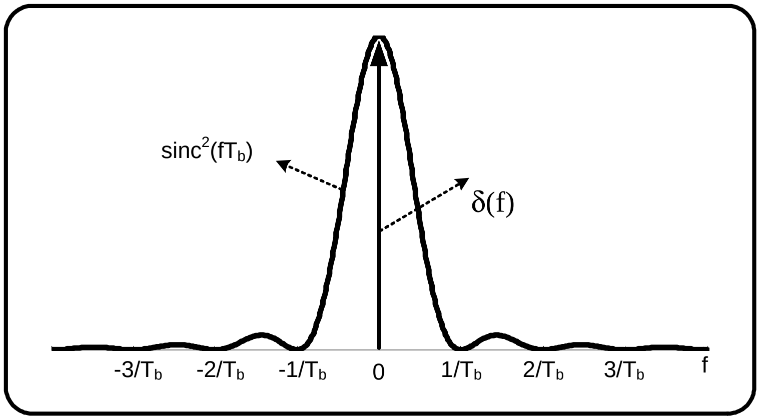


Figure 2.2: Power spectrum of 2PAM NRZ on linear axes

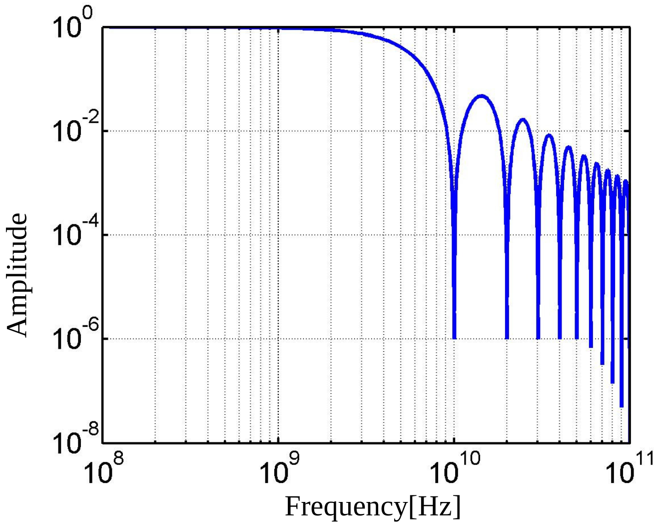


Figure 2.3: Power spectrum of 2-PAM NRZ on logarithmic axes

log-log scale. The gain is normalized to *one*, and the clock frequency is assumed to be 10GHz for a data rate of 10Gb/s. Evidently, the spectrum covers a broad frequency range from dc all the way to the clock frequency. All wireline communication systems require a wide bandwidth channel and circuit blocks to allow transmission of broadband NRZ signal with minimum distortion. Bandwidth restrictions of the channel and/or receiver circuits are the primary cause of signal impairment in high-speed communication, which limits the link reliability as we will discuss later.

Although the NRZ modulation scheme requires a broadband channel and receiver, excessive bandwidth in the receiver can be harmful to the receiver sensitivity because wider bandwidth results in a larger integrated noise power. Therefore, from a sensitivity standpoint, an optimum bandwidth exists that maximizes the sensitivity by balancing between performance degradation due to the inter-symbol interference (small bandwidth) and noise (large bandwidth). The conventional rule of thumb is to choose the receiver bandwidth equal to 70% of the data rate [36]. We will analytically demonstrate the validity of this rule and its underlying assumptions in Section 2.3. The receiver typically consists of several blocks such as the pre-amplifier, the main amplifier, and the equalizer. The individual bandwidth of each of these blocks should be larger than 70% of the data rate because when the blocks are cascaded the overall bandwidth is reduced. We will consider this in Chapter 4 when proposing bandwidth enhancement techniques for wideband amplifiers.

2.3 Link Reliability

2.3.1 Eye Diagram

The eye diagram of a data sequence is a form of representation of the signal that provides insight about the quality of the signal. As we will discuss in Section 2.3.2, Section 2.3.3, and Section 2.5.1, a received signal has several characteristics, such as amplitude noise, inter-symbol interference, or jitter, that affect the probability of extracting correct information from it. The eye diagram of a signal contains information about such characteristics of the signal. To generate the eye diagram, the signal is divided into frames where each has a length of an integer multiple of the symbol period (bit period, T_b, in the case of 2-PAM modulation). Then all the frames are overlapped to create a single diagram with one frame length that contains several traces of the signal. An example for a 2-PAM eye diagram with the length of $2.T_b$ is shown in Figure 2.4, which looks like an eye, hence the name.

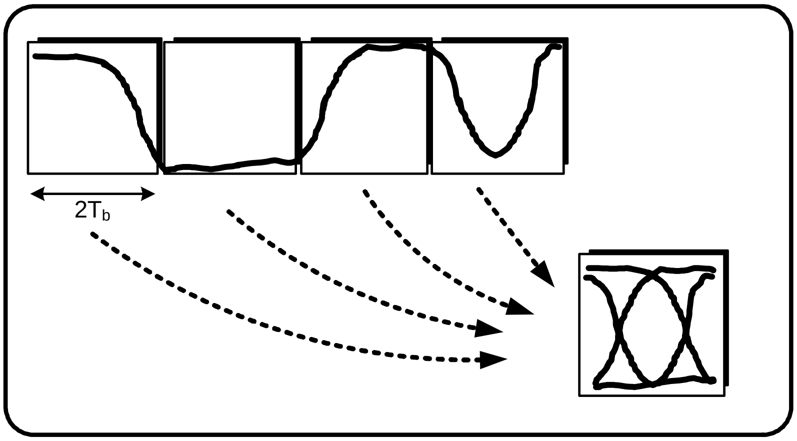


Figure 2.4: Creation of the eye diagram with the length of $2.T_b$ from signal

2.3.2 Bit Error Rate (BER)

A common performance measure for the reliability of a communication link is the probability of making an error in transmission of information. This parameter is estimated by the bit error rate (BER), which is defined as the ratio of the number of errors to the total number of bits transmitted. One of the primary impairments that causes errors in communication is noise. Noise is modeled as an additive component in the input of the receiver, as shown in Figure 2.5 for a simplified communication link. The distribution of the noise is assumed to be Gaussian with white (flat) power spectral density. Amplitude fluctuations at the sampling point due to noise can inject errors in the detection of the symbols, as illustrated in Figure 2.5 for a 2-PAM signal.

The error probability or BER for a simplified link as in Figure 2.5 can be calculated from the noise distribution at the sampling point. We have

$$BER = P(0) \cdot P(1|0) + P(1) \cdot P(0|1). \tag{2.5}$$

$P(0)$ and $P(1)$ are the probabilities that the transmitted bit is “0” and “1,” respectively. If we assume “0” and “1” are equiprobable, $P(0)=P(1)=0.5$. $P(0|1)$ is the probability of sampling a “0” if the transmitted bit is “1.” This is equal to the area under the tail of the noise distribution below the threshold level, as illustrated in Figure 2.6. Furthermore,

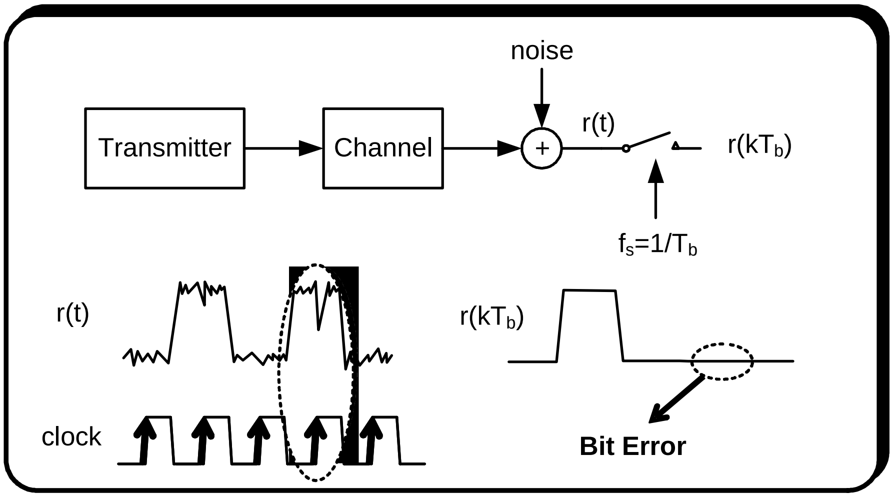


Figure 2.5: Bit error generation due to noise in a symbol detection-based receiver

$P(1|0)=P(0|1)$ if the noise distribution at the zero-amplitude level and the one-amplitude level are equal. Therefore, the BER is simplified to

$$BER = Q\left(\frac{1}{2\sigma}\right) \tag{2.6}$$

for a Gaussian noise source with cumulative distribution function of $Q(.)$ and standard deviation of σ. Equation (2.6) is not a very accurate approximation of BER in a real high-speed wireline link. Several other factors including inter-symbol interference (ISI), data timing jitter, and sampling clock uncertainty will affect the BER. We will introduce these issues in the following sections and study their effects on the link BER.

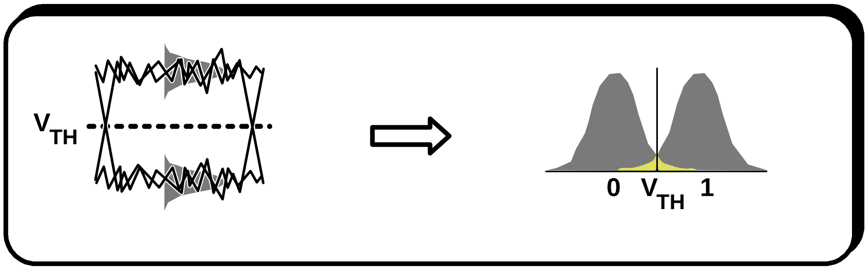


Figure 2.6: The BER calculation from the area under the tail of the noise distribution

2.3.3 Inter-Symbol Interference (ISI)

In reality the noise is not the only impairment of the communication channels. The tail of a received pulse shape associated with a symbol can last for longer than a symbol period, T_b, and therefore it can interfere with its neighboring symbols. This effect is called inter-symbol interference (ISI). The received signal for a 2-PAM NRZ, as $x(t)$ in (2.1), can be written as

$$r(t) = \sum_{k=-\infty}^{\infty} a_k \cdot p_o(t-kT_b) + n(t) \qquad (a_k \in \{0, 1\}) \tag{2.7}$$

where $n(t)$ is additive noise and $p_o(t)$ is the received pulse shape. The signal $r(t)$ is sampled at times $t=T_s+mT_b$ to regenerate the symbols, where m is an integer and $0<T_s<T_b$.

$$r(T_s + mT_b) = a_m p_o(T_s) + \sum_{k=-\infty,\, k \neq m}^{\infty} a_k \cdot p_o(T_s + (m-k)T_b) + n(T_s + mT_b) \,. \tag{2.8}$$

The second term on the right hand side is the ISI term that affects the decision of each symbol. Nyquist proposed conditions on the overall response as well as pulse shapes that completely null the ISI term [15]. Based on his works, the classical method to eliminate ISI is to design transmit and receive filters such that the overall received pulse shape is a Nyquist pulse, *i.e.*, $p_o(T_s+(m-k)T_b)=0$ for $m \neq k$, [16][17][40].

The channel bandwidth limitation is the primary cause of ISI. Consequently, it becomes an issue in high-speed communication, as faster data rates are required to be transmitted on the same channels. In electrical transmission line channels, the frequency-dependent loss is the main source of bandwidth limitation and thus the main cause for ISI. This frequency-dependent loss is mainly caused by the skin effect of the conductor and the dielectric absorption. Figure 2.7 shows an example transfer function of a stripline transmission line with FR4 dielectric [42]. In addition to the channel, the bandwidth

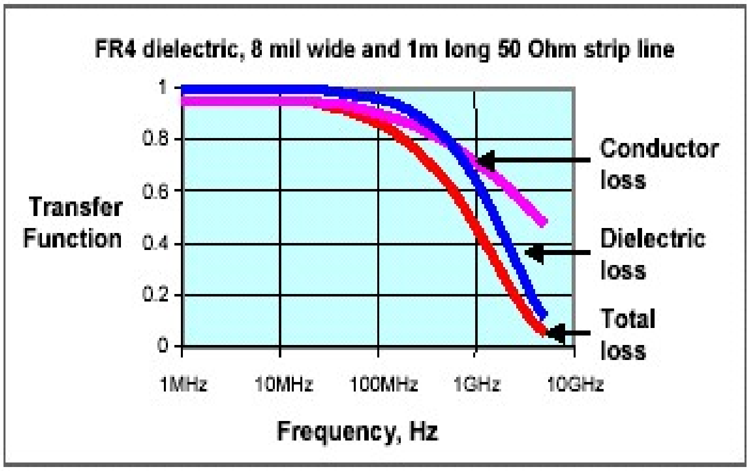


Figure 2.7: Loss contributions from conductor and dielectric in a FR4-based stripline [42]

limitation of the receiver blocks, and electromagnetic reflection due to impedance mismatch between connections or cables can exacerbate the overall ISI.

Dispersion is another significant source of the ISI. Dispersion occurs when the phase of the channel response transfer function is not a linear function of the frequency, and thus the group delay, which is the derivative of the phase, will be frequency dependent. Consequently, when a signal with broad spectrum travels in the channel, various frequency components get delayed by different amounts. The overall effect is to broaden the pulse shape of the signal in time domain and thus cause ISI. Both electrical and fiber optic channels are dispersive.

Dispersion is a major source of ISI in optical fiber [43]. In multi-mode fibers (MMF), modal dispersion is dominant. Modal dispersion is caused when various optical modes are excited on the fiber and travel at different speeds. Modal dispersion becomes more problematic at longer transmission distances because optical modes get separated more, and thus received pulse causes severe ISI. An example is shown in Figure 2.8 for 800m of MMF at 10Gb/s. In single-mode fibers (SMF), modal dispersion is absent and chromatic dispersion and polarization-mode dispersion are dominant [43]. Chromatic dispersion is mainly caused by the frequency-dependent refraction index of the fiber material. The

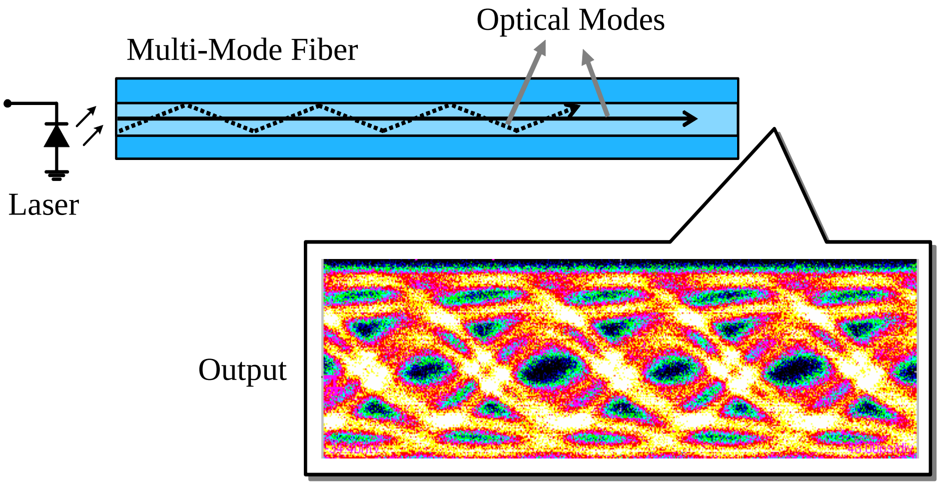


Figure 2.8: The output of an 800m MMF channel is severely distorted due to modal dispersion

fundamental optical mode that is excited on an SMF has nonzero spectral width and thus will disperse because various spectral contents will experience a different index of refraction. Polarization-mode dispersion is due to the group velocity difference of orthogonal polarization modes in an SMF that does not have a perfectly cylindrical shape. This is shown in Figure 2.9.

2.3.4 Equalization

Equalization refers to any technique used in link design to compensate for the impairments induced by ISI. For example, the equalizer can be a filter at the receiver that

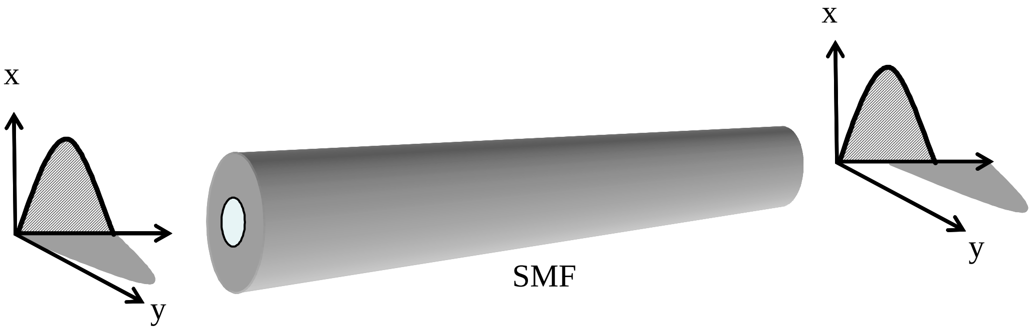


Figure 2.9: Polarization mode dispersion in a SMF with noncylindrical core

reshapes the channel's undesirable frequency response such that the final received pulses are ISI free. An example is a pulse that satisfies the Nyquist criterion [15][17] and is commonly called a Nyquist pulse shape. The Nyquist criterion was implicitly introduced in Section 2.3.3 for the received pulse shape $p_o(t)$. It can be stated as follows.

A received pulse shape $p_o(t)$ satisfies the Nyquist criterion and is called a Nyquist pulse shape if

$$p_o(t = kT_b) = \begin{cases} 1 & k = 0 \\ 0 & k \neq 0 \end{cases} . \tag{2.9}$$

If the equalizer filter is designed such that when cascaded with the channel the overall response satisfies (2.9), the link will be ISI free according to (2.8) and for T_s=0.

Equalization can be applied either in the transmitter or the receiver. The transmitter equalizer is sometimes referred to as the transmitter pre-emphasis. It amplifies the high frequency content of the signal at the transmitter to compensate for the high frequency attenuation of the channel after the signal travels through it. The advantage of the transmitter pre-emphasis is that it does not amplify the receiver noise because the compensation process takes place in the transmitter. Nevertheless, the transmitter pre-emphasis can cause large crosstalk between neighboring transmission lines in a parallel link due to the strength of the signal high frequency content. Receiver equalization is intended basically to add a filter at the receiver to minimize the overall effect of ISI and noise at the sampling point. It is typically preferred to the transmitter equalization because the equalizer can be made adaptive to accommodate the unknown channel response and its variations over time. In this work we focus on receiver equalization.

The straightforward equalization technique is to design the filter such that the overall response to the cascade of the channel and the filter satisfies the Nyquist criterion for zero ISI in (2.9). This technique is known as the zero-forcing (ZF) technique [44]. Essentially, the ZF algorithm forces the filter transfer function to be equal to the inverse of the channel's transfer function. Evidently, the ZF algorithm only accounts for the ISI impairment and neglects the noise. In band-limited channels, the equalizer filter transfer function with the ZF criterion becomes a highpass filter that amplifies the high frequency content of the signal to compensate for the channel's high frequency attenuation. However, the filter will also amplify the noise and will potentially degrade the received signal to noise ratio. An alternative approach to the ZF method is to use the mean square error (MSE) algorithm to design the filter. The MSE algorithm considers the noise and ISI together and avoids extensive noise amplification at the receiver by allowing occurrence of partial ISI. The MSE criterion minimizes the BER rather than the ISI. The filter parameters are designed to minimize the number of decision errors on the received symbols.

The previous equalization techniques are referred to as feedforward equalization (FFE), because the filter is inserted in the feedforward signal path, as shown in Figure 2.10(a). An alternative approach is decision feedback equalization (DFE), where the filter is inserted in the feedback path, as Figure 2.10(b) illustrates [16][17][40][44]. The filter input is the decision result of the previously received bits. Therefore, DFE is a nonlinear equalization. One way to design the filter in DFE is to match its transfer function to the transfer function of the channel. Assuming the receiver decisions are correct, the filter reproduces the ISI that would have been generated by the channel. This ISI is then subtracted from the current symbol. The advantage of the DFE architecture is

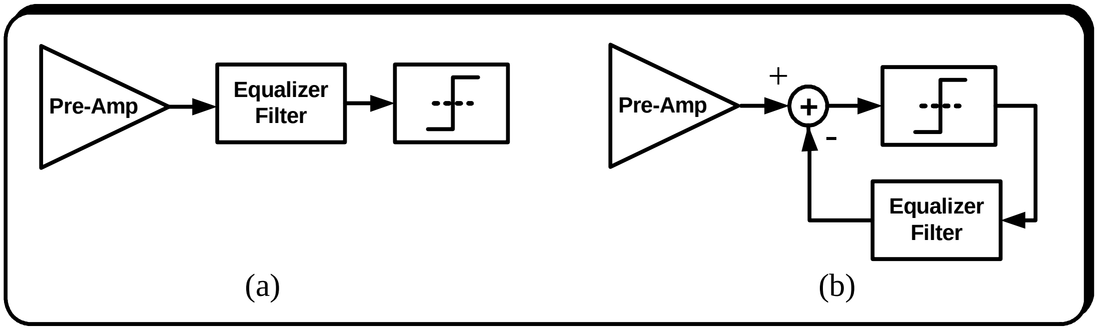


Figure 2.10: Equalizer filter in two topologies (a) FFE (b) DFE

that because it acts on the receiver decisions that are noise free, the DFE structure does not cause noise enhancement. However, the DFE architecture can potentially cause error propagation in cases where the BER is very large, when the assumption for correct receiver decisions is violated. A combination of FFE and DFE can be implemented to compensate linear and nonlinear ISI and to avoid significant noise enhancement.

In low-speed communication links, *e.g.*, voice channels, magnetic recording channels, and digital subscriber loop (xDSL) data channels, equalization is performed digitally as part of the baseband digital signal processing (DSP). The filtering process is done in frequency domain leveraging efficient Fast Fourier Transform (FFT) algorithms. Unfortunately, none of these luxuries are available at high-speed data rates, such as 10Gb/s. The required precision and clock-rate at such speeds for analog-to-digital conversion and the DSP processors drive the power consumption of such implementations to very unrealistic and impractical values. At such frequencies, analog implementation of the equalizer filter is more favorable.

The equalizer core in high-speed implementations is a finite impulse response (FIR) filter. The FIR filter components are shown in more detail in Figure 2.11. This form of implementation of the FIR filter is known as direct form FIR, transversal filter, or tapped-delay line [45]. In analog implementation, the delay cells can be realized with active [46][47] or passive elements [31][48] or a combination of those [49]. Passive delay cells are based on broadband inductor (L) capacitor (C) networks, or transmission line structures. For instance, Figure 2.12(b) shows a 3-section constant-*k* filter topology based on the *pi*-section LC ladder network of Figure 2.12(a) [50]. It consists of L and C elements that overall represent a lumped model of a transmission line. The transfer function of the structure, within its passband, resembles an ideal delay line with the delay value

$$T_D = n\sqrt{LC} \tag{2.10}$$

where n is the number of LC sections. The large layout area of the inductor elements is a disadvantage for this topology when implementing an integrated delay cell, especially

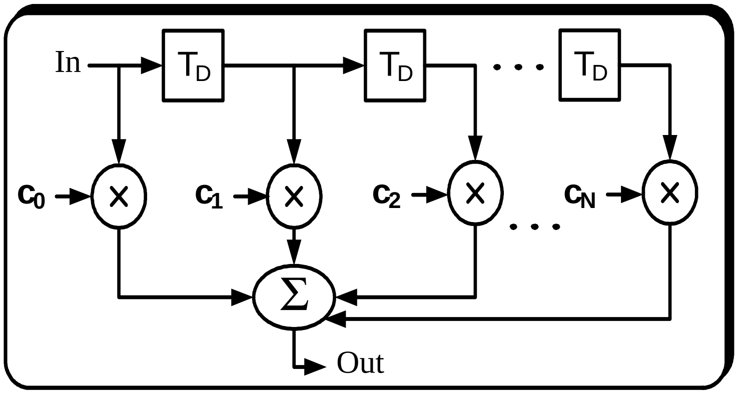


Figure 2.11: FIR filter with tapped-delay line topology and *N*+1 taps

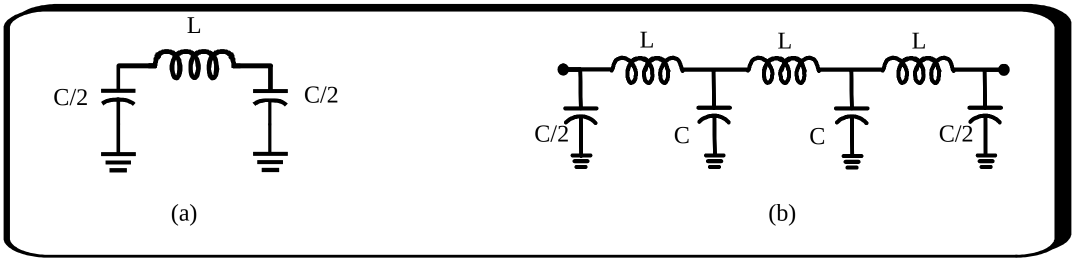


Figure 2.12: The constant-*k* filter-based LC delay line: (a) *pi*-section (b) 3-section

when *n* is large. However, because the passive delay cell is a linear system, it is desirable when a linear equalizer is needed to preserve the amplitude information of the signal as the signal travels in the delay line. An FFE equalizer that compensates linear ISI is an example of such a case.

Equalization is effective when the transversal filter coefficients are adjusted appropriately to compensate for the channel ISI. However, in most practical cases, the channel response is unknown at the link startup time and/or it is time-varying. For instance, in a chip-to-chip link, variations of the geometric shape of the interconnect during fabrication, the improper matching at the connections, or the via and stub loading make it practically impossible to predict the channel response. Another example is the MMF-based optical communication, where the channel response is usually unknown in startup because of the variations in the excitation condition of the laser, the geometrical shape of the MMF core, and the fiber length. Furthermore, factors such as changes in the environmental condition or aging may result in a time-varying channel response. Adaptive equalization, which was first proposed by Lucky [16][51] for communication systems, remedies these issues by automatically adjusting filter coefficients and constantly tracking any time variations in the channel response.

Adaptive equalization can be implemented with or without a training sequence. In the former case, a set of known symbols is transmitted over the channel to the receiver. The equalizer has *a priori* knowledge of these symbols and determines filter coefficients to minimize the ISI for them. A similar approach for equalization using training sequence is to perform channel estimation based on the received training sequence. The coefficients of the filter can be calculated based on the estimated channel response, *e.g.*, with the ZF criterion. Training sequence-based equalization is not used in high-speed communication, mainly because it requires complex signal processing with power hungry implementation that is simply not yet practical at 10Gb/s or beyond.

An effective adaptive equalization algorithm that has received more attention for high-speed implementation recently is the least mean square (LMS) algorithm (*e.g.*, [52]). This is due to its ease of implementation. The LMS algorithm is an MSE-based algorithm, in which the optimization criteria is defined in order to minimize the mean square of the difference between the filter output and the receiver's decision. The equation for updating the coefficient of tap *m* can be simplified to [17]

$$C_m(k) = C_m(k-1) + \Delta \cdot \varepsilon_{k-1} \cdot x_m(k-1) \tag{2.11}$$

where ε_{k-1} is the difference between filter output and receiver decision and Δ is a scaling parameter that affects the convergence speed. The hardware structure of the adaptive equalizer filter with the LMS algorithm can be implemented as illustrated in Figure 2.13. The architecture only requires the implementation of high-speed summation and multiplication to add the LMS algorithm to the transversal filter structure of Figure 2.11, which is feasible in today's advanced integrated technologies. As can be seen from Figure 2.13, the

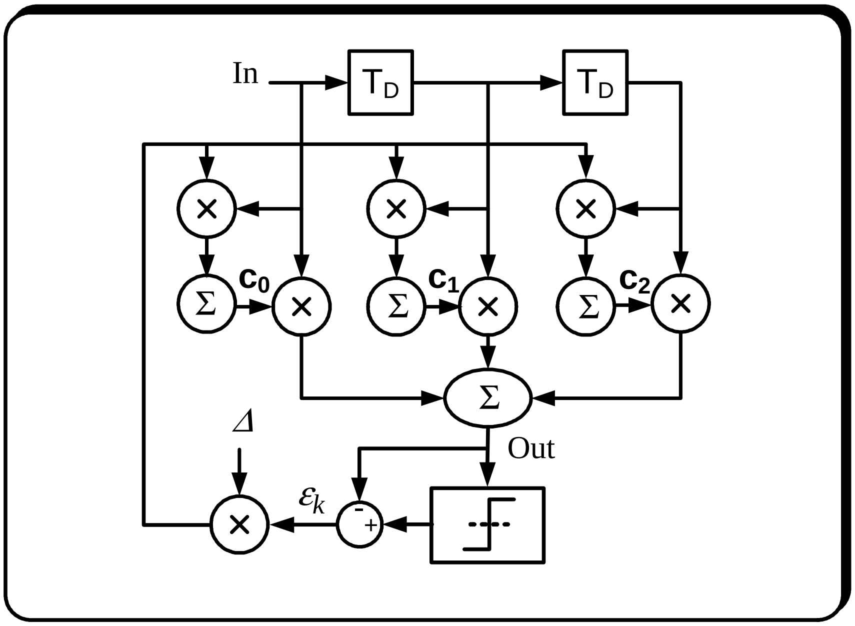


Figure 2.13: The implementation of the LMS algorithm for adaptive equalization

LMS algorithm is a decision-based optimization algorithm, *i.e.*, the parameter that is minimized depends on the decision of the receiver. In blind equalization algorithms that do not use any training sequence, this can be a potential disadvantage for the LMS algorithm. In high BER conditions many of the receiver decisions may be incorrect, which will result in a slow convergence of the algorithm. In Chapter 5 we discuss one of the contributions of this thesis, *i.e.*, an alternative technique for adaptive equalization.

2.3.5 ISI Impact on BER

The calculations in Section 2.3.2 assume the ISI is zero at the sampling instance. In practice, the noise margin at the sampling point is reduced because of the ISI, and thus the probability of error is increased. Using (2.5) and (2.8) and assuming equiprobable data bits, the condition for finding probability of error can be rewritten as

$$P_e = P\left(\left[\sum_{k=-\infty,\, k\neq m}^{\infty} a_k \cdot p_o(T_s + (m-k)T_b) + n(T_s + mT_b)\right] > \frac{1}{2}\right) \tag{2.12}$$

and can be calculated from the joint probability distribution of the noise and ISI. However, finding this joint probability distribution is very complicated for an arbitrary system [16]. Lucky *et al.* provide a solution for P_e in the form of a finite sum [16]. They assume that only a finite number of ISI terms in (2.8) affect the joint probability distribution of the noise and ISI. The suggested solution requires tedious numerical computation for finding the P_e for any system and does not provide an insight to correlate the P_e to the system parameters. An alternative approach for finding the impact of the ISI on P_e is to find an accurate bound on the P_e in the presence of the ISI. For example, Saltzberg provided a tight bound on P_e that depends only on the noise variance and the samples of the received pulse shape [53]. Therefore, the complexity of the bound grows linearly with the number of ISI terms. Excellent tutorials on several computationally efficient methods to calculate P_e for the ISI channels can be found in [54]–[57].

In this section we estimate the error probability by providing a simple relationship between the BER and the system bandwidth that is also helpful in understanding the trade-off between noise and the ISI for various system bandwidths. We perform our calculations based on a first-order linear time-invariant (LTI) system and leverage the results to estimate the P_e based on the practical system parameters such as bandwidth.

2.3.5.1 First-Order LTI System

If the link has a first-order system response with an associated time constant, τ, the received pulse shape can be written as

$$p_o(t) = \begin{cases} 0 & t \le 0 \\ 1 - e^{-\frac{t}{\tau}} & 0 \le t \le T_b \\ \left(\frac{1}{\alpha} - 1\right) \cdot e^{-\frac{t}{\tau}} & T_b \le t \end{cases} \tag{2.13}$$

where we define $\alpha \equiv e^{-T_b/\tau}$ that relates the system time constant and the bit period. The ISI term for a_0 can be calculated by replacing (2.13) in (2.8) for m=0 as

$$ISI = \sum_{k=-\infty}^{-1} a_k \cdot p_o(T_s - kT_b) = \alpha^{\frac{T_s}{T_b}} \sum_{k=-\infty}^{-1} a_k \cdot (1-\alpha) \cdot \alpha^{-k-1} \tag{2.14}$$

where the sum goes only to k=-1 because we assume the system is causal. T_s is the sampling time offset from t=0 and $0 \le T_s \le T_b$. The sampled value of the current symbol, *i.e.*, a_0, can be calculated from the first term on the right in (2.8) as

$$p(T_s) = 1 - \alpha^{\frac{T_s}{T_b}}. \tag{2.15}$$

The optimum sampling point for the first-order system is at T_s=T_b because (2.15) reaches its maximum at this sampling point. Equation (2.14) demonstrates that the interference impact of the prior bits decreases exponentially. When the impact of only one prior bit, *i.e.*, a_{-1}, is significant, ISI terms will be concentrated around two mean values, ISI_0 and ISI_1. The two mean values can be calculated from the expected value of ISI in (2.14) when it is conditioned on the value of a_{-1}. We have

$$ISI_0 = E\{ISI|a_{-1} = 0\} = \frac{1}{2}\alpha^{\frac{T_s}{T_b}+1} \tag{2.16}$$

$$ISI_1 = E\{ISI|a_{-1} = 1\} = \alpha^{\frac{T_s}{T_b}}\left(1 - \frac{\alpha}{2}\right) \tag{2.17}$$

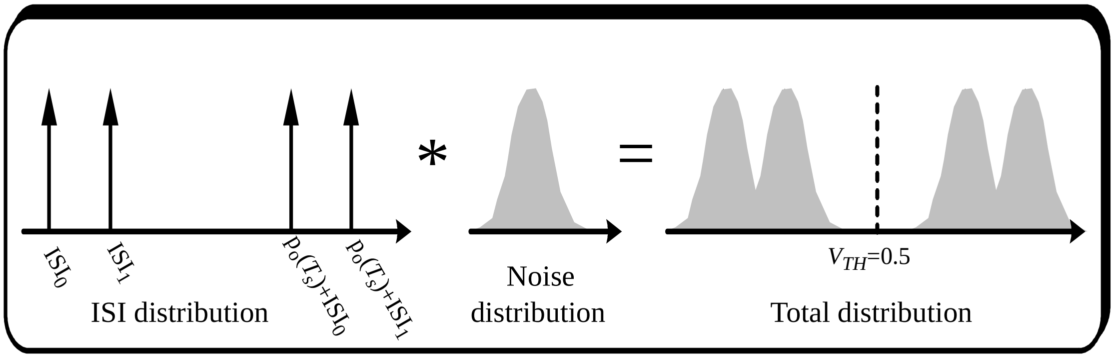


Figure 2.14: Total amplitude distribution at the sampling point when ISI impact of one bit is taken into account

where *E{.}* is the expected value. The two mean ISI terms perturb the amplitude at the sampling point. Because of the stochastic nature of the data, the ISI at any point can be modeled by a random variable. Then, the ISI distribution can be represented by two probability mass functions, *i.e.*, two delta functions at the values ISI_0 and ISI_1, with probability weight p and $(1-p)$, respectively, where p is the probability of $a_{-1}=0$. The overall amplitude distribution can be found by the convolution of the ISI distribution and the Gaussian noise distribution as shown in Figure 2.14.

The optimum slicing threshold, V_{TH}, can be calculated from the average of the four possible mean signal levels in Figure 2.14, which simplifies to V_{TH}=0.5 independent of T_s. If the receiver input noise is white with double-sided power spectral density $\frac{N_0}{2}$, the amplitude noise variance at the sampling point is reshaped by the first-order system transfer function. The total noise power can be calculated from

$$\sigma^2 = \int_{-\infty}^{\infty} \frac{\frac{N_0}{2}}{1 + \tau^2\omega^2} df = \frac{N_0}{4\tau}. \tag{2.18}$$

Similar to Section 2.3.2, we can now calculate the total BER as

$$
\begin{aligned}
BER &= \frac{1}{4}\left(Q\left(\frac{0.5 - ISI_0}{\sigma}\right) + Q\left(\frac{0.5 - ISI_1}{\sigma}\right)\right. \\
&\quad \left. + Q\left(\frac{p_o(T_s) + ISI_0 - 0.5}{\sigma}\right) + Q\left(\frac{p_o(T_s) + ISI_1 - 0.5}{\sigma}\right)\right)
\end{aligned} \tag{2.19}
$$

which can be evaluated for different sampling time by using (2.15)–(2.18). Figure 2.15 compares the BER at various signal-to-noise ratios (SNR) in the zero-ISI case in equation (2.6) with the BER in the ISI channels from equation (2.19), when the systems have the same noise bandwidth, *i.e.*, equal σ. The BER curves are plotted for various 3dB bandwidth-to-bit rate ratios (BW/BR) for the ISI channel. The figure shows that the ISI degrades the performance of the link at large SNR values when the ISI dominates over noise. Also, as the bandwidth-to-bit rate ratio decreases, the BER degrades more.

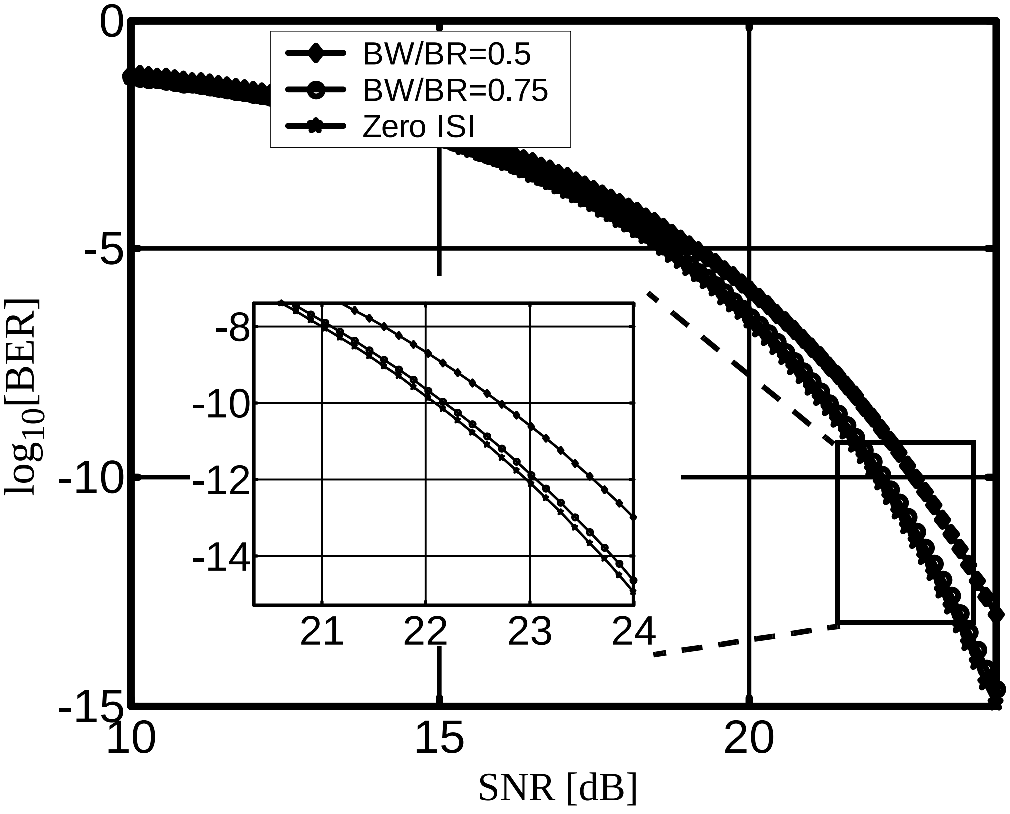


Figure 2.15: The BER vs. SNR for various normalized bandwidths compared to the zero-ISI BER of equation (2.19), sampled at optimum point, *i.e.*, $T_s = T_b$

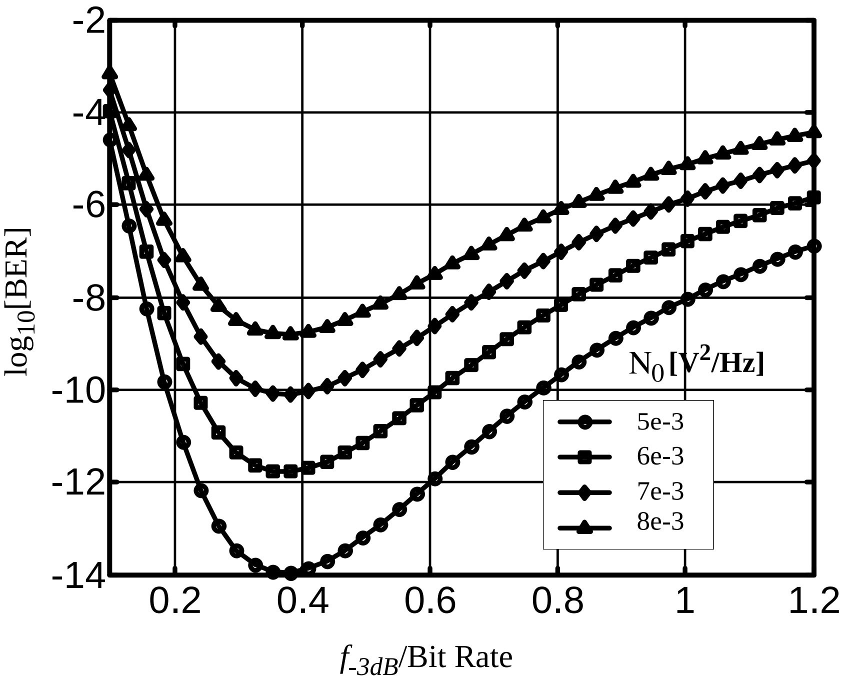


Figure 2.16: ISI and noise trade-off as normalized bandwidth variations justifies existence of a minimum for BER

Figure 2.16 relates the BER to the system 3dB bandwidth, f_{-3dB}, for various noise power spectral density, when the signal is sampled at the optimum point, *i.e.*, $T_s = T_b$. Evidently, at very small f_{-3dB}, the ISI is severe and limits the BER. However as bandwidth gets excessively large, the noise power that is injected into the receiver is the dominant contributor to the link-quality degradation and causes higher BER. Consequently, there is a trade-off between the system noise and the ISI impact. There exists an optimum bandwidth that minimizes BER. The optimum bandwidth in the case of the first-order system is around 40% of the bit rate when $T_s = T_b$. In typical wireline link architectures the sampling clock is in the middle of the eye at $T_b/2$. Although this results in simple hardware implementations, $T_b/2$ is not necessarily the optimum sampling point. The BER for when sampling occurs in the middle of the eye, *i.e.*, $T_s = T_b/2$, is plotted in Figure 2.17. The same trade-off exists between the noise and the ISI. However, the optimum

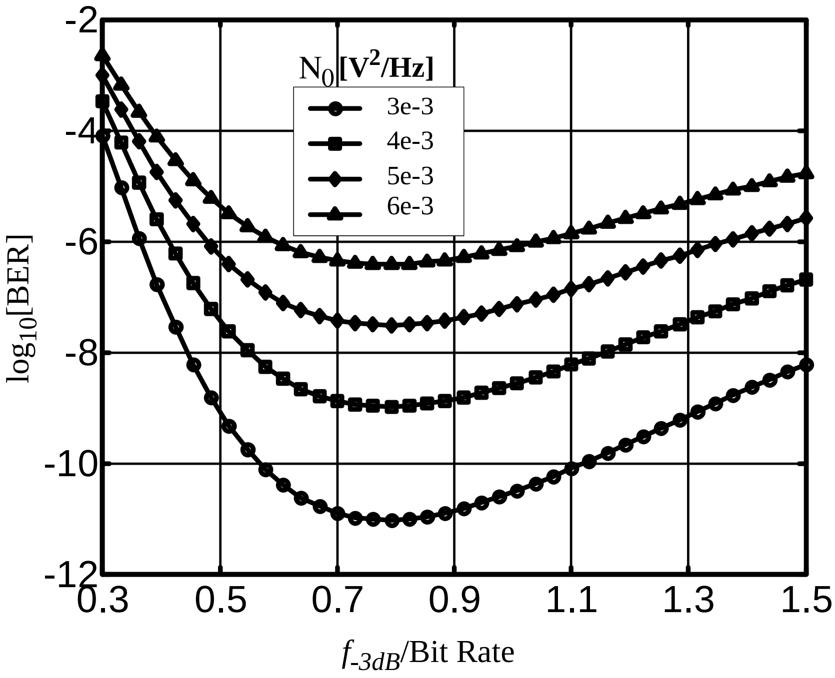


Figure 2.17: The optimum bandwidth for minimum BER when sampling point is in the middle of the eye at $T_b/2$

bandwidth is now at around 70% of the bit rate which agrees with the well-known optimum bandwidth-to-bit rate ratio for best sensitivity in broadband receivers [36].

We also notice by comparing Figure 2.16 and Figure 2.17 that for equal input noise, the location of the sampling point affects the minimum achievable BER. In fact, the plot in Figure 2.16 can be reproduced for all possible sampling points, and the optimum sampling point can be determined from the plot that results in the smallest minimum-achievable BER. The optimum receiver bandwidth is also determined from the same plot. We will elaborate on this topic for the link design when we add the effect of jitter to the BER. We will analytically derive the two-dimensional BER contours that allow the designer to simultaneously determine the optimum bandwidth and the optimum sampling point to minimize the BER.

2.3.5.2 Second-Order LTI System

One characteristic of a first-order system is the monotonic step response. In real systems the step response can have oscillatory tail, *e.g.*, because of multiple electromagnetic reflections. The relationship between the response of such a system and the the BER can be modelled by studying the link BER of an under-damped second-order LTI system. The transfer function of an all-pole second-order LTI system can be written as

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.20}$$

where ζ is the damping factor and ω_n is the natural frequency. The step response of an under-damped system, *i.e.*, when $\zeta<1$ is

$$s(t) = \left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin\left(\omega_n\sqrt{1-\zeta^2}\,t + \cos^{-1}\zeta\right)\right] \tag{2.21}$$

and the system 3dB bandwidth is

$$f_{-3dB} = \frac{\omega_n}{2\pi}\sqrt{1 - 2\zeta^2 + \sqrt{1 + (1-2\zeta^2)^2}}\,. \tag{2.22}$$

Figure 2.18 shows the pulse response of a second-order system for two different values of ζ. For each value, the pulse response is plotted for four different f_{-3dB}. We can carry out the same procedure as in Section 2.3.5.1 to find the BER equation. All of the ISI terms that have significant impact on the BER from (2.12) are included in the calculations. In addition, for every given pair of ζ and f_{-3dB}, the BER can be calculated at several sampling points in the unit interval. The trade-off between the noise and the ISI is also present in the second-order system. This trade-off, and hence the existence of an optimum system bandwidth to minimize the BER, can be seen by plotting the BER vs. f_{-3dB}. In Figure 2.19, we have plotted the BER contours that show the BER values vs. f_{-3dB} at various sampling points, for three different values of ζ. The cross section of the contours for a constant T_s that are in parallel to the y-axis show the noise-ISI trade-off. The optimum f_{-3dB} that

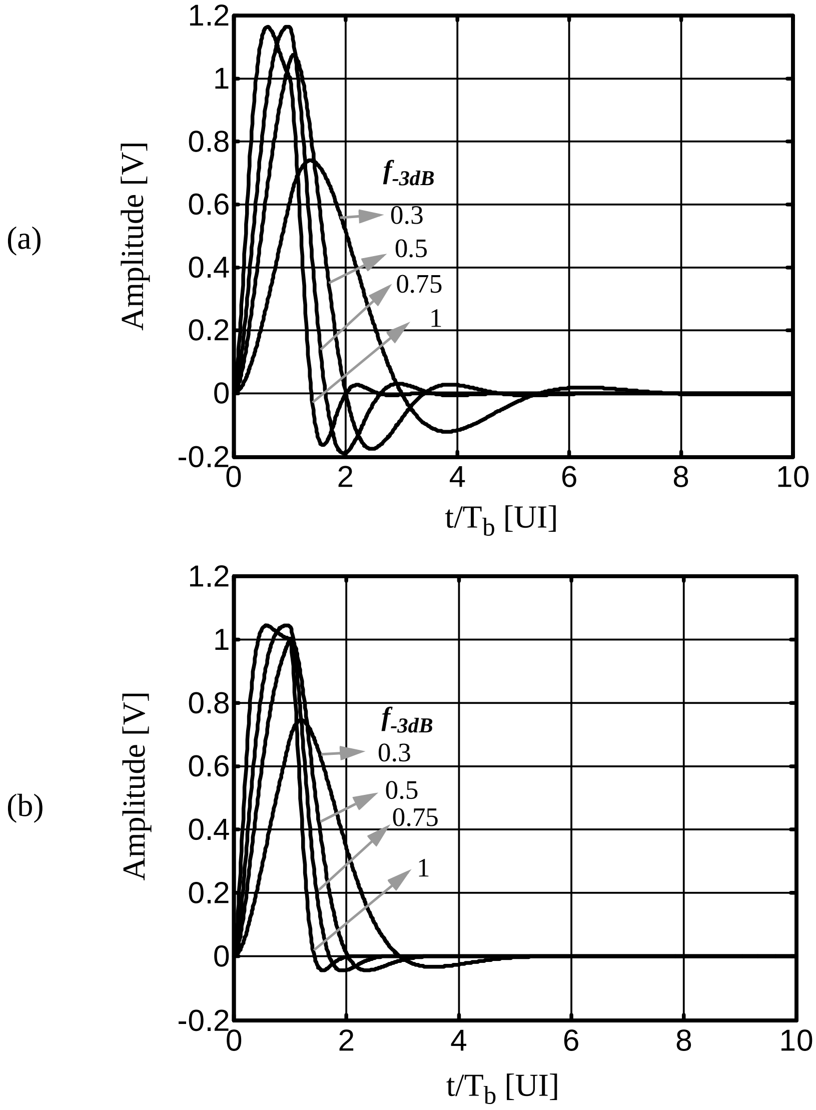
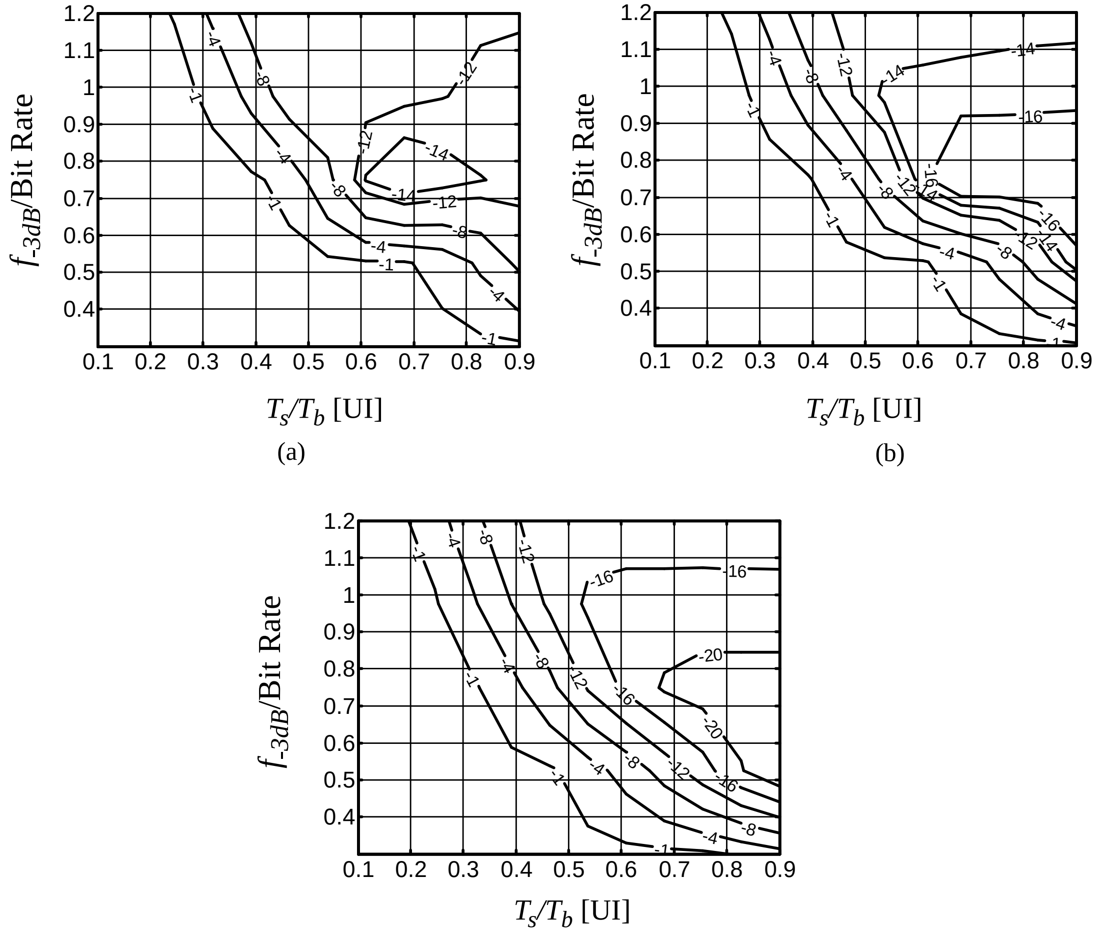


Figure 2.18: Pulse response of a second-order system at various normalized 3dB bandwidths: (a) ζ=0.5 (b)$\zeta = \sqrt{2}/2$

results in the minimum BER occurs around 70% of the bit rate. Furthermore, the contours can be used to select the sampling point that results in the minimum achievable BER.

Similar calculations can be performed for any linear time-invariant (LTI) system, when the system pulse response is available. The BER relationship that includes the ISI impact can be derived as in (2.19), which provides insight about the relationship of the response of the system and the BER. One contribution of this thesis is to use a similar



(a)

(b)

(c)

Figure 2.19: The contours of $\log_{10}$[BER] for N_0=4e-3 v^2/Hz: (a) ζ=0.4 (b) ζ=0.5 (c) $\zeta=\sqrt{2}/2$

approach in Chapter 3 to find a general relationship between the system response and the data-dependent jitter (DDJ) to minimize DDJ and improve link reliability.

2.4 Wireline Communication Transceiver

2.4.1 General Architecture

Although there exist several applications for wireline communication, as it was discussed in Section 1.2, the general transceiver architecture that is used in their implementation is more or less the same. Table 2.1 lists some of the wireline standards developed for 10Gb/s communication with various applications. Differences such as transmission distance or power consumption impact the design parameters such as channel type, number of repeaters, gain budget, and jitter budget. Figure 2.20 illustrates the general architecture of a wireline communication transceiver, also known as a serial link, that can be applied to any of the standards in Table 2.1.

Table 2.1: Various high-speed wireline communication standards

Standard	Bit Rate	BER	Application	Channel
10Gigabit Ethernet Family	10Gb/s	10^{-12}	LAN Backplane	Copper or MMF/SMF*
10Gigabit Fibre Channel	10Gb/s	10^{-12}	SAN	MMF/SMF
SONET OC-192, OC-768	10/40Gb/s	10^{-12}	Long Haul Telecomm.	SMF

*MMF: multi-mode fiber SMF: single-mode fiber

On the transmit side, low-speed data arrives at the multiplexer that serializes the parallel data into a single high-speed serial data sequence synchronous to the transmitter clock. The driver either directly sources the data to the electrical transmission line or drives an optical modulator that modulates the data onto optical pulses, which then get transmitted over the fiber optic channel. In both cases, several channel impairments degrade the quality of the high-speed signal until it arrives at the receiver. The degraded

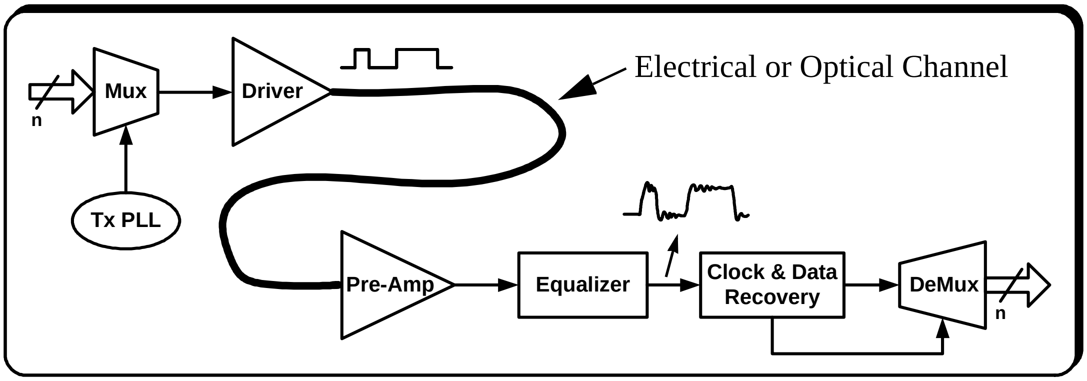


Figure 2.20: General architecture of a serial link

signal is amplified with a low noise wideband pre-amplifier. Then, the equalizer filter partially revives the signal by reducing the ISI and increasing the signal-to-noise ratio. Next, a sampling clock is extracted from the signal by a clock recovery phase-locked loop (PLL). The clock is used to sample the received signal to retime and recover the data. The clock is also used in a demultiplexer to deserialize the single data sequence back to the original data in parallel lines.

If the channel is formed by an optical fiber, the driver is connected to an optical modulator that modulates a laser source with the input data. On the receive side of an optical link, the light is shed on a photodetector that generates an output electrical current proportional to the received optical power. Therefore, the pre-amplifier will be a trans-impedance amplifier with small input impedance. The focus of this thesis is on the receiver side of the architecture.

2.4.2 Channel

The channel can be electrical or optical. The simplest electrical channel is unshielded twisted-pair copper wire such as the ones used in Category 5 (CAT5) that consists of 4 pairs of twisted pair and is commonly used in 10/100Mb/s Ethernet LAN. Chip-to-chip and backplane communication at multi-Gb/s require channels with less loss at high frequencies. They use coaxial cable or controlled impedance PCB microstrip transmission line or stripline. However, the loss of such channels is not tolerable either, when the transmission distance is above hundreds of meters. Multi-mode fiber (MMF) is deployed for longer than 100m transmission. The dominant impairment of the MMF is modal dispersion that is caused by the difference in the propagation velocity of the various excited optical modes, as was discussed in Section 2.3.3. Since the MMF and the electrical channels discussed above mainly induce linear distortion on the signal, they can be modeled with a linear system. We will make this assumption throughout the dissertation that the channel can be modeled with a linear time-invariant (LTI) system. Therefore, all the analysis results from the thesis contributions can be generally applied to all of the channels above.

2.4.3 Pre-Amplifier

The main function of the pre-amplifier is to amplify the received weak signal to the sensitivity level of the next stage in the receiver. The stages following the pre-amplifier often require fixed-minimum swing at their input, *e.g.*, in emitter-coupled logic (ECL). While the required output swing of the pre-amplifier is constant, the amplitude of the input signal can take a wide range of values depending on the transmitted power and the channel attenuation. Therefore, the pre-amplifier needs to have a wide dynamic range and high gain. In addition, the pre-amplifier should be low noise to have minimum impact on the signal-to-noise ratio. Figure 2.21 shows an example schematic of a pre-amplifier for an optical link with a second main-amplifier stage. The main amplifier is in the form of a limiting amplifier (LA) or automatic gain-controlled (AGC) amplifier for maintaining a constant output amplitude. In this example, the pre-amplifier is a trans-impedance

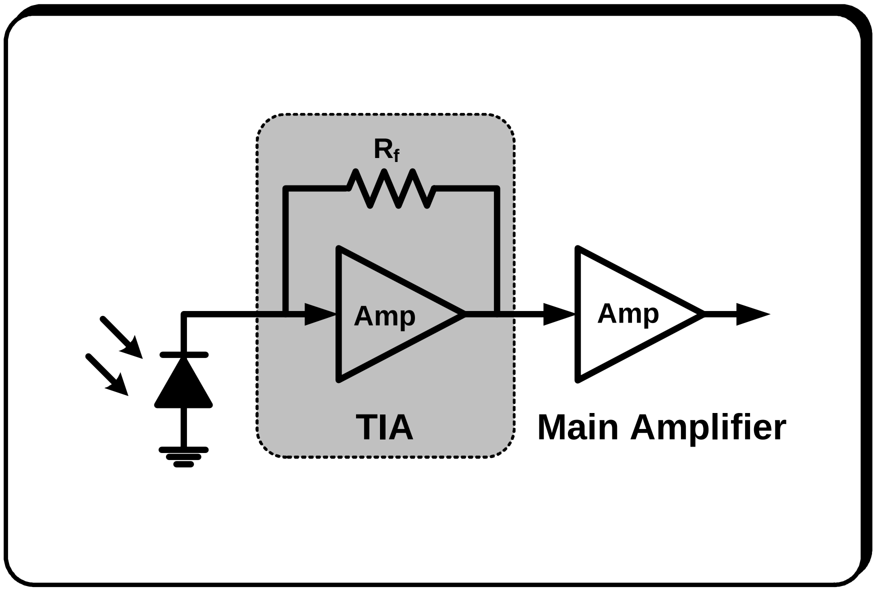


Figure 2.21: The front end of an optical communication receiver with the photo detector and a shunt-feedback trans-impedance amplifier (TIA)

amplifier (TIA) with shunt-feedback configuration. The low input impedance of the TIA absorbs most of the current generated by the photodetector. Also, it avoids bandwidth limitation that can be caused by the large photodetector capacitance. Designing a TIA with large gain and bandwidth and reasonable sensitivity is challenging particularly in CMOS technologies due to their poor device parasitic components or low-current unity-gain frequency, f_t. Chapter 4 discusses this issue and provides a methodology for overcoming these challenges.

2.4.4 Adaptive Equalizer

We elaborated on the need for adaptive equalization in high-speed links in Section 2.3.4. The channels we consider in this dissertation, such as the electrical transmission line or the MMF only impose linear distortion and can be modeled with an LTI system. Therefore, in most implementations, a feedforward adaptive equalizer suffices to minimize the ISI imposed by the channel. In Chapter 5 we discuss a contribution of the thesis that proposes a new architecture for adaptive equalization based on an eye-opening monitor system.

2.4.5 Clock Recovery

As can be seen from Figure 2.3, the 2-PAM NRZ data sequence has zero energy at the data rate frequency and its integer multiples. Therefore, the received signal does not contain any direct component of the timing information from the transmitter clock. In addition, the signal has travelled over a channel with an arbitrary length that causes an unknown delay or phase for the signal at the receiver. In a symbol detection-based scheme, a synchronous clock is required to sample each signal at an optimum sampling point to recover the data. Therefore, in such systems, a synchronization technique or clock recovery is needed.

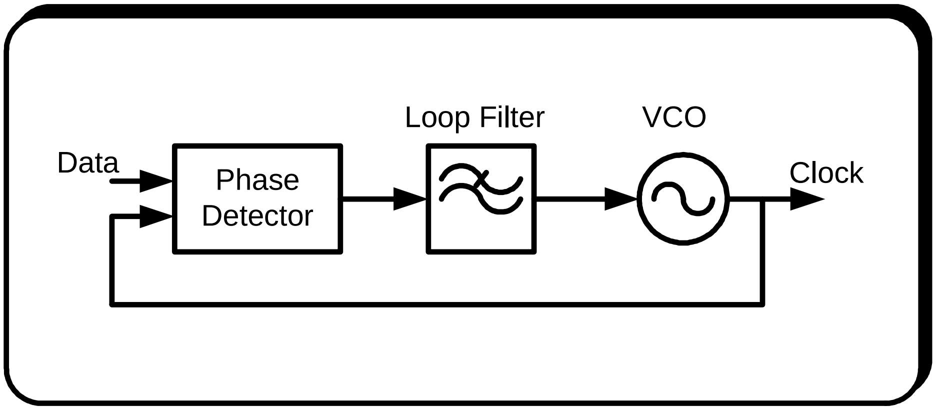


Figure 2.22: PLL-based clock recovery architecture

Clock recovery methods for communication applications can be categorized into two groups: Feedforward and feedback clock recovery [41]. Feedforward methods generally comprise of a nonlinear element in front of the signal for generations of the spectral lines at the clock frequency followed by a very high-quality bandpass filter to extract the clock. The nonlinearity can take many forms, *e.g.*, derivative [58][60] or square law [59]. It is very costly to integrate a high-quality bandpass filter at 10Gb/s [60]. Therefore feedforward techniques are rarely deployed in high-speed wireline communication.

Feedback clock recovery is based on a phase-locked loop (PLL) structure. A simplified architecture is shown in Figure 2.22. A voltage-controlled oscillator (VCO) generates the required sampling clock. The frequency and phase of the VCO are controlled by the output of the loop filter to track and minimize the error between the data transition phase and the clock. Although the PLL-based clock recovery acquires input data phase and locks to it to always keep the sampling phase at the optimum point, it partially filters high-frequency timing variations of data transitions by retiming the data. This feature is desirable in data repeaters and regenerators, *e.g.*, in a SONET architecture because it avoids accumulation of timing jitter, *i.e.*, excessive timing deviation from ideal threshold-crossing points. We will discuss the problems arising from the timing jitter and its impact on link reliability next.

2.5 Timing Jitter

2.5.1 Timing Jitter Definition

In a perfect transmission using 2-PAM NRZ, the data transitions, *i.e*, “01” or “10” occurrences, cross the decision threshold at integer multiples of the bit period, T_b. Because of several causes, *e.g.*, random noise and ISI, the actual threshold-crossing times of data transitions deviate from their ideal values, as shown in Figure 2.23. The timing jitter of the data is deviations from a reference time at a defined threshold [61]. We will show in the next section how the data timing jitter impacts the link reliability and increases the BER. Because of the random nature of the sources of jitter, the timing jitter is modelled by a random variable and is thus characterized by a distribution. The jitter distribution is then used to find its impact on the BER. Figure 2.24 shows an accumulated eye diagram of a data sequence measured with an oscilloscope, superimposed onto the jitter histogram. The histogram is generated by capturing and accumulating the time of all of the threshold-crossing events. This histogram approximates the jitter distribution.

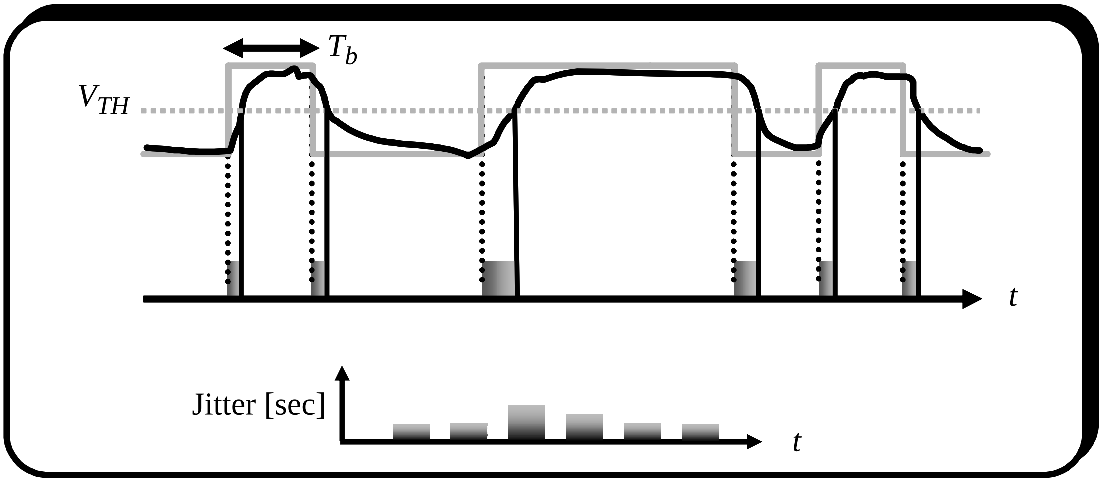


Figure 2.23: Jitter is deviation of the threshold-crossing time from a reference time

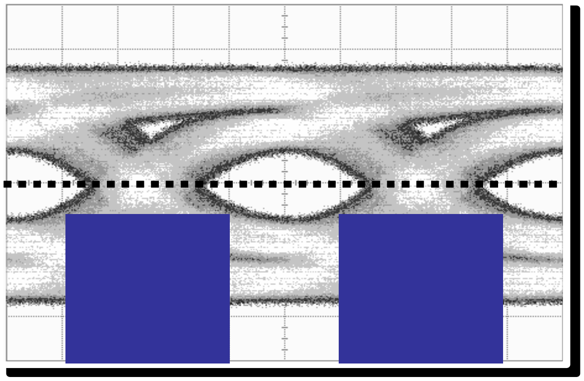


Figure 2.24: Accumulated eye diagram with data jitter histogram

2.5.2 Jitter Impact on the BER

In calculations of Section 2.3.2 and Section 2.3.5, we had two implicit assumptions. First, we assumed the sampling clock is ideal, *i.e.*, all clock periods equal T_b and the clock does not have any timing jitter that randomly moves the sampling point. Second, we assumed that all the transmitted bits are sampled and bits are never lost or sampled twice. Existence of data jitter violates these two assumptions and increases BER.

Figure 2.25 shows the clock and data recovery stage of the high-speed receiver front end right before sampling. Data jitter at the input of clock and data recovery impacts the BER in two ways. First, the data jitter decreases the horizontal eye diagram opening of the signal, which means for a given BER, larger data jitter leaves a smaller sampling window in the eye diagram that achieves that target BER. In other words, for a fixed sampling point, the BER increases as the data jitter increases because of the error induced by the jitter.

The BER from jitter can be calculated from the area under the tail of the jitter distribution, as illustrated in Figure 2.26. This area corresponds to the data transitions that happen on the wrong side of the sampling clock. Therefore, such an event is called bit slipping. The errors due to jitter are independent of errors caused by amplitude noise or

ISI. If we assume an ideal sampling clock, zero amplitude noise, and zero ISI, we can calculate the BER only caused by jitter as

$$BER(T_s) = \frac{1}{2}\left[\int_{T_s}^{\infty} f_{TJ}(t) \cdot dt\right] + \frac{1}{2}\left[\int_{-\infty}^{-T_b + T_s} f_{TJ}(t) \cdot dt\right] \tag{2.23}$$

where $f_{TJ}(t)$ is the probability distribution function of the total jitter from all sources and T_s is the location of the sampling clock in the eye. We assume the sampling point varies within a unit interval (UI), *i.e.*, $0 \le T_s \le T_b$. The 1/2 factor represents the probability of a transition event. If the sampling point is in the middle of the eye at $T_s = T_b/2$, (2.23) simplifies to

$$BER = \int_{\frac{T_b}{2}}^{\infty} f_{TJ}(t) \cdot dt. \tag{2.24}$$

Although the probability of a data transition event on each side of the eye diagram in Figure 2.26 is half, both sides of the eye can independently contribute to BER by adding an error, as indicated by the area under the tail of both distributions.

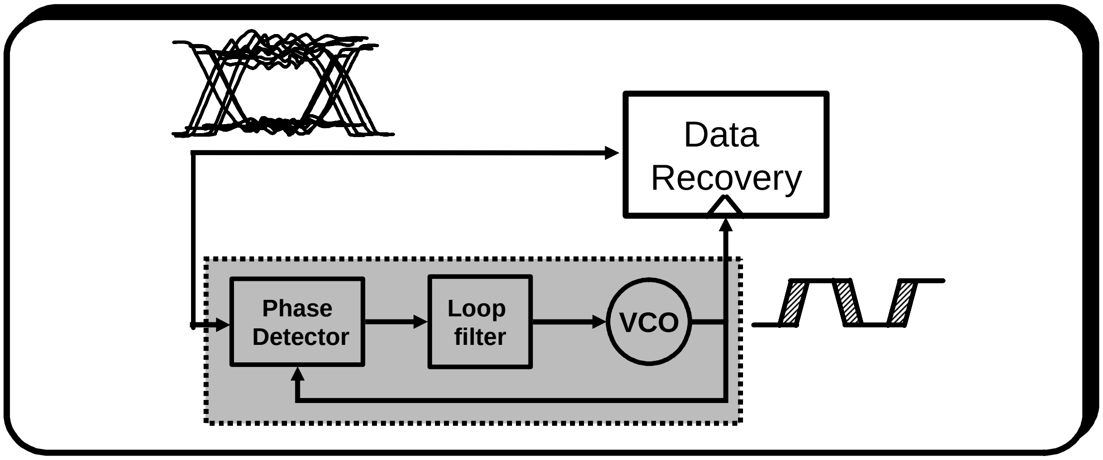


Figure 2.25: Impact of data jitter on BER from data path and clock path

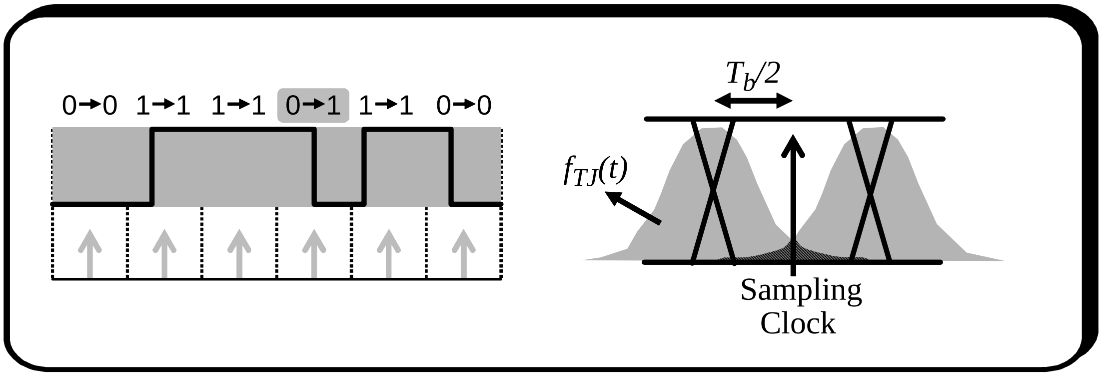


Figure 2.26: Impact of the data jitter on the BER by causing bit slipping

The second impact of jitter on the BER comes from the uncertainty of the sampling clock. Data jitter acts as a reference noise for the clock recovery PLL, and therefore it creates clock jitter at the output of the clock recovery. Because of the inherently slow response of the clock recovery to the input fluctuations, the clock jitter at the time of sampling is uncorrelated to the data that it samples. Therefore, the clock jitter degrades the BER further. In the next section, we combine the results of this section with Section 2.3.5 to find the overall impact of impairments such as noise, ISI, and jitter on the link BER. In the next chapter we break down the total jitter to its components and show an analytical model for data-dependent jitter that is caused by ISI. We also highlight the impact of data-dependent jitter on the BER.

2.6 Overall Impact of Jitter and ISI on the BER

In Section 2.3.5 and Section 2.5.2 we studied the impact of noise, ISI, and jitter on the BER independently. In a real implementation of a high-speed link all of these impairments exist and degrade the BER simultaneously. We combine the impact of all those effects in this section.

2.6.1 Ideal Sampling Clock

When the sampling clock is ideal, *i.e.*, all the clock cycles are exactly one bit period, a detection error may occur due to the combination of noise and ISI. We calculated the BER for such a case in (2.19). This BER is a function of the sampling time. The minimum BER is achieved when sampling at the optimum point, which is not necessarily at $T_b/2$. If the sampling point is moved from the optimum sampling point, the ISI contribution changes from (2.16) and (2.17) and thus the BER increases. However, the general form of the BER remains the same as in (2.19). We denote the BER that is caused from the amplitude noise and the ISI by $BER_{ISI}(T_s)$ as it is a function of the sampling point, T_s. We can rewrite (2.19) as

$$BER_{ISI}(T_s) = \frac{1}{2}[BER(ISI_0(T_s)) + BER(ISI_1(T_s))] \tag{2.25}$$

where we have defined

$$BER(ISI_0(T_s)) \equiv Q\left(\frac{0.5 - ISI_0}{\sigma}\right) = Q\left(\frac{p_o(T_s) + ISI_1 - 0.5}{\sigma}\right) \tag{2.26}$$

$$BER(ISI_1(T_s)) \equiv Q\left(\frac{0.5 - ISI_1}{\sigma}\right) = Q\left(\frac{p_o(T_s) + ISI_0 - 0.5}{\sigma}\right). \tag{2.27}$$

In the presence of the timing jitter, the relative location of the sampling point and the threshold crossing of the data is changing randomly. In other words, if we assume that the timing jitter, Δt, is a random variable with zero mean, the sampling point for the bit that is sampled right after a transition is T_s-Δt. Therefore, the BER for such a bit for a given Δt is $BER_{ISI}(T_s - \Delta t)$. The overall BER for such bits is found by integrating the BER over all possible values of Δt weighted by the probability distribution function. For instance, for a “01” transition, the overall BER from the combined effect of the noise, the ISI, and the timing jitter is

$$BER(T_s|''01'') = \frac{1}{2}\int_{-\infty}^{\infty} f_{TJ}(t) \cdot BER_{ISI}(T_s - t)dt + \frac{1}{2}\int_{-\infty}^{\infty} f_{TJ}(t) \cdot BER_{ISI}(T_b - T_s + t)dt\,. \tag{2.28}$$

The two terms on the right in (2.28) correspond to when bit “1” and bit “0” in the “01” pair are in error, respectively. Notice that when the ISI and noise are absent and only the timing jitter is present we have

$$BER_{ISI}(t) = \begin{cases} 0 & t \geq 0 \\ 1 & t < 0 \end{cases} . \tag{2.29}$$

Therefore, (2.28) simplifies to (2.23). Furthermore, if the timing jitter is absent, the jitter distribution is a delta function concentrated at t=0, and if it is replaced in (2.28), the equation is simplified to $BER_{ISI}(T_s)$.

We have calculated the approximate overall BER caused by the combined effects of the ISI, noise, and jitter in Appendix A, equation (A.9), which is rewritten here as

$$BER(T_s)= \frac{1}{4}\left[\left(Q\left(\frac{0.5 - ISI_0(T_s)}{\sigma_n}\right) + \int_{-\infty}^{T_s} f_t(t) \cdot Q\left(\frac{0.5 - ISI_1(T_s - t)}{\sigma_n}\right)dt\right) \cdot \left(1 + Q\left(\frac{T_s - T_b}{\sigma_j}\right)\right) + Q\left(\frac{T_s}{\sigma_j}\right) + Q\left(\frac{T_b - T_s}{\sigma_j}\right)\right] . \tag{2.30}$$

Equation (2.30) provides the overall BER as a function of the sampling time and the system response, *i.e.*, ISI_0 and ISI_1, for the given noise and timing jitter standard deviations.

2.6.2 Non-Ideal Sampling Clock

In reality the sampling clock has some uncertainty or jitter associated with it that can be modeled by a probability distribution function, $pdf_{clk}(T_s)$, where T_s is now a random variable. Then, the total BER can be found by using the continuous total probability theorem [62] as

$$BER = \int_0^{T_b} pdf_{clk}(T_s) \cdot BER(T_s) dT_s \tag{2.31}$$

that simplifies to (2.30) if the clock is ideal with a delta probability distribution function. We have neglected the contributions of the tails of the clock and have bounded the clock distribution to one bit period. Although (2.31) does not have a closed form for an arbitrary clock distribution, we can use it to numerically compute or simulate the BER and compare the impacts of jitter and ISI. In the rest of this chapter we assume that the sampling clock is ideal and $pdf_{clk}(T_s)$ is a Dirac delta distribution function.

2.6.3 ISI and Jitter Trade-off

2.6.3.1 The Bathtub Curve

If the BER caused by the timing jitter in equation (2.23) is plotted vs. the sampling point in a unit interval, *i.e.*, when $0 \le T_s \le T_b$, a curve is achieved that resembles the shape of a bathtub and is thus called a bathtub curve. It graphically demonstrates that as the sampling point approaches the edges of the data eye diagram, the BER significantly increases. An example bathtub curve is shown in Figure 2.27, when the total jitter distribution is Gaussian with zero mean and standard deviation, σ_j=0.05 UI. A unit interval (UI) is a unit of time that equals the time normalized to a bit period. The bathtub curve is a useful tool for characterization of high-speed links. It is used to define an eye diagram opening for a given BER. For instance, in Figure 2.27, the eye diagram opening at the BER=10^{-12} is about 0.3 UI. The eye diagram opening corresponds to the available timing margin for the location of the sampling clock in the eye diagram that can achieve

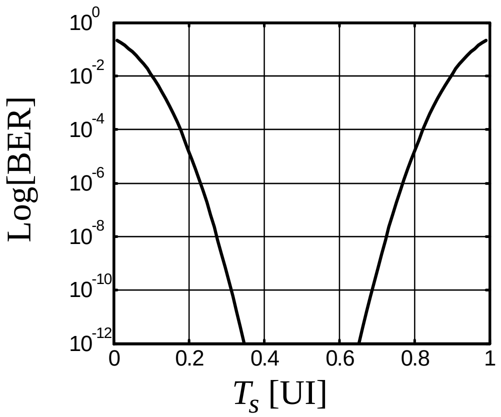


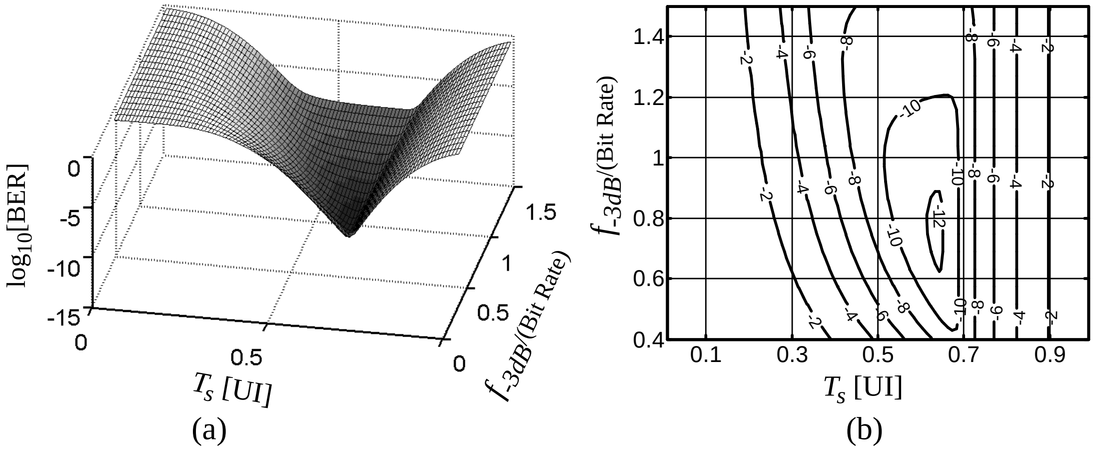
Figure 2.27: Bathtub curve for σ_j=0.05 UI

the target BER. Therefore, the bathtub curve can be used as a measure for the trade-off between the link data jitter budget, σ_j, and the clock jitter budget, the eye opening.

2.6.3.2 The BER Contours: 3D Bathtub Curve

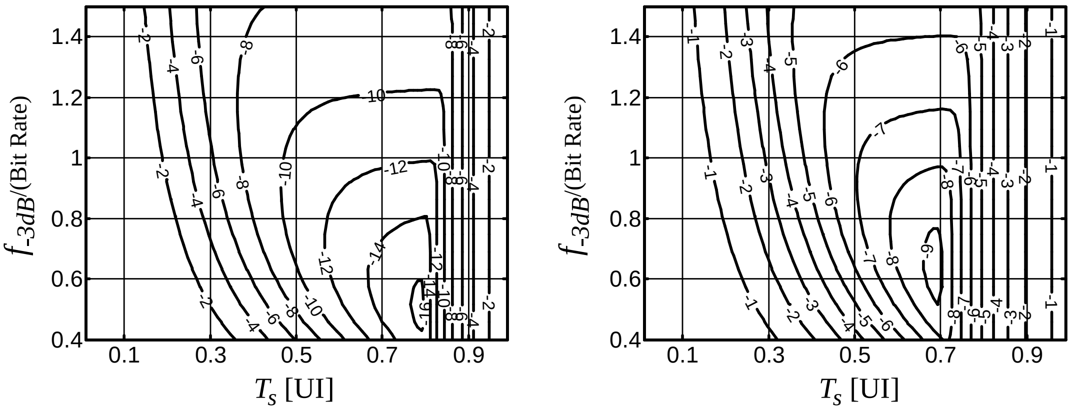
We can generalize the concept of the bathtub curve to a data link with noise and ISI. If we use (2.30) to calculate the BER, we can plot a three-dimensional bathtub curve as a function of the sampling time and the system bandwidth that represents the ISI in the case of a first-order system. Consequently, we obtain an insight about the trade-offs between the data link's jitter and ISI budget and the sampling clock timing margin. Such trade-offs are important in determining the specifications of the pre-amplifier response and the clock and data recovery characteristics for achieving minimum BER.

Figure 2.28(a) shows the 3D bathtub curve when the link is modeled with a first-order system. The BER is calculated for various sampling points and normalized 3dB bandwidths, when σ_j=0.05UI and N_0=4e-3V/Hz^2. If N_0=0, the cross section of the plot, when bandwidth approaches infinity, becomes the conventional bathtub curve. Figure 2.28(b) shows the contours of the BER as a function of the sampling point and the bandwidth, which is equivalent to the top view of the 3D bathtub curve. The contours



(a) (b)

Figure 2.28: (a) Three dimensional bathtub curve for a first-order system for various normalized bandwidths; σ_j=0.05UI and N_0=4e-3v^2/Hz (b) Contours of BER from top view of plot (a)



(a)

(b)

Figure 2.29: BER contours (a) σ_j=0.025UI and N_0=4e-3V^2/Hz (b)σ_j=0.05UI and N_0=5e-3V^2/Hz

show that the BER is independent of bandwidth as the sampling point approaches the data edges because the timing jitter dominates the BER. Moreover, the optimum bandwidth that minimizes BER is about 75% of the bit rate. At this bandwidth, the optimum sampling point is neither in the center of the eye nor at T_s=T_b as we saw in a first-order system. Finally, we can see that the timing margin for the sampling clock reduces drastically at smaller system bandwidths.

We can use (2.30) to find the contours of the BER for any given σ_j and N_0. The noise standard deviation, σ_n, is a function of the bandwidth and N_0. Figure 2.29 shows the BER contours for two more cases. In Figure 2.29(a), the BER is plotted when the σ_j=0.025 UI, half the value in Figure 2.28(b)'s plot. All the other parameters are the same. The jitter reduction lowers the minimum achievable BER. It also moves the optimum sampling point to the left, closer to T_s=T_b, which is the optimum sampling point for first-order response in the absence of jitter. The optimum bandwidth is shifted to lower values, as the sampling point is closer to T_s=T_b. This is because the ISI terms from (2.16) and (2.17) decrease, and amplitude noise dominates BER_{ISI}. Therefore, a smaller system bandwidth that filters more of the noise power can achieve a lower BER. Figure 2.29(b) shows the

BER contours when N_0=5e-3V/Hz^2 and all the other parameters are the same as Figure 2.28(b). The increase in amplitude noise degrades the overall BER by 3-4 orders of magnitude. The optimum system bandwidth-to-bit rate ratio is smaller compared to Figure 2.28(b), as we discussed above. The sampling timing margin for achieving BER of 10^{-12} has significantly decreased.

The y-axis in Figure 2.29 is the normalized bandwidth only for a first-order system. For a general LTI system the y-axis is related to the size of the pulse response at each subsequent sampling point, which is in turn associated with the received pulse response as a result of the combination of the channel response and pre-amplifier transfer function. Therefore, the designer can use the BER contours to determine the optimum front end time response shape for achieving a target BER. In addition, the optimum sampling point and its associated timing margin can be obtained from the BER contours with a target BER and is used to design the parameters for the clock recovery circuit.

In the next chapter, we introduce the data-dependent jitter (DDJ) phenomenon that is the impact of the ISI on the threshold-crossing time of the data. The DDJ modifies the jitter distribution by effectively increasing the jitter variance. In this case, (2.30) is not sufficient for finding the total BER. We complete the equation for computing the BER by including the impact of DDJ in our calculations.

2.7 Summary

In this chapter we introduced the principles of wireline communication systems. We discussed the system level challenges for designing a reliable high-speed communication link. We studied the impacts of the noise, the ISI, and the timing jitter on the link bit-error probability and provided the relationships between the system parameters, *e.g.,* bandwidth and sampling point, and the BER. These relationships are the first step in designing the system for minimizing the BER. Finally, we combined the effects of the ISI, noise, and jitter and calculated the overall BER when all of these impairments are present. We used the result to demonstrate some of the existing trade-offs between system parameters. We showed how the analytical formulation for the BER can be used to find the system level specifications for the blocks of the receiver, such as the pre-amplifier and the clock recovery. In the next chapter we analyze data-dependent jitter (DDJ) and provide an analytical probability distribution function for it that modifies the timing jitter distribution we discussed in this chapter. We add the DDJ component to the BER and demonstrate its remarkable impact on the performance of high-speed serial links.

Chapter 3

Data-Dependent Jitter in Wireline Communications

3.1 Introduction

As we discussed in Chapter 2, the reliability of high-speed serial communication links depends upon timing jitter. The timing jitter of data transition is deviations of the threshold-crossing time, *i.e.*, time at which data crosses a decision threshold, compared to a reference clock. The transmitter, the channel, and the receiver contribute to the timing jitter of the data sequence. In addition, at least a part of the timing jitter of the data is inherited as phase uncertainty of the recovered sampling clock in the clock recovery system. The bit error rate (BER) of the regenerated data sequence in the receiver is degraded by the timing jitter of the data and sampling clock. Nonidealities such as bandwidth limitation and medium dispersion exacerbate jitter effects.

Data timing jitter is separated into two main categories, namely, random jitter (RJ) and deterministic jitter (DJ) [61]. RJ is random variations of threshold-crossing time due to amplitude fluctuations around the crossing time or phase noise of the transmitter clock [63]. DJ is further categorized into data-dependent jitter (DDJ), duty cycle distortion jitter, and bounded uncorrelated to data jitter (*e.g.*, crosstalk jitter or sinusoidal jitter) [61]. DDJ is threshold-crossing time deviations correlated to the previous bits on the current data bit. It is also known as pattern jitter. DDJ is often caused by bandwidth limitations of the system or electromagnetic reflections of the signal. Therefore, DDJ has a larger impact on high-speed transmission systems with restricted bandwidth. In this chapter, we propose methods for characterizing DDJ theoretically based on system parameters and study its impact on BER.

The impact of timing jitter on the performance of different communication links has been studied extensively [59],[64]–[69]. However, these works have focused on the effect of digital pattern on the output jitter of the extracted clock. They have neglected the limitations of all other blocks in the communication link. For instance, Byrne *et al.* have investigated the accumulation effect of timing jitter in a series of regenerators with special attention to the effect of pattern jitter [65]. However, the analysis is limited to a simple second-order tank as the timing extraction block. Saltzberg has estimated the aggregate effect of RJ and DDJ using Taylor series expansion and has calculated the jitter of the extracted sampling clock [66]. Similarly, Gardner has compared the effect of pattern jitter on different clock recovery schemes [67]. He has presented a relation between DDJ and the sampling clock phase variation with qualitative explanations. Huang has proposed pulse shapes that result in DDJ-free data streams [68]. But, he has emphasized the peak-to-peak data-dependent jitter and has calculated it from the two data sequences that result in the maximum shift of the threshold-crossing time. He has assumed a given form for the received data stream, namely an ideal non-causal Nyquist pulse. All these works condition the system that generates DDJ to several assumptions. A model for the DDJ generated from a general LTI system is still lacking.

In a different context, jitter modelling techniques are developed for separating and measuring jitter performance of devices in communication links [61],[70]–[72]. Reliable jitter measurement methods are more important in high-speed devices, where bandwidth limitations aggravate DDJ. Therefore, predicting DDJ contribution is essential to accurate measurement systems. For instance, Shimanouchi has related the bandwidth of an automatic test equipment (ATE) system and the DDJ [70]. However his analysis was based on the previous data transition *only.* In addition, he limits the model to first-order system response.

Although the significance of DDJ has been realized in the aforementioned literature, theoretical analysis of DDJ and study of its relation to system parameters such as bandwidth has been neglected. The main contribution of this chapter is to propose a method for predicting data-dependent jitter for a general LTI system in a context suitable for circuits and system designers. The dependence of DDJ on system parameters provides additional insights for minimizing jitter and highlights that increasing the bandwidth does not necessarily minimize DDJ. In addition, the method reduces the simulation or measurement time remarkably by relating DDJ characterization linearly to the number of prior bits considered. The conventional computation grows exponentially with the number of bits because it requires passing all possible sequences through the system. The theoretical results are matched with jitter histogram measurements.

In the rest of this chapter, we first define data-dependent jitter formally. Then we derive an analytical expression for DDJ of first-order LTI systems. The expressions are associated to conventional approximations of the distribution of data-dependent jitter, and the results are experimentally verified. Next, we generalize the analysis for any LTI system with known step response. A perturbation method is introduced that approximates DDJ by separating the jitter contributions of the previous bits. We compare the measured deterministic jitter of real communication media with analytical expressions that we derive for DDJ and demonstrate that the presented analytical results estimate DDJ accurately and are reliable for predicting jitter. Finally, we update the BER calculation from the previous chapter by accounting for the correlation between DDJ and ISI.

3.2 Framework

3.2.1 Data Jitter

A typical serial communication receiver regenerates data by sampling the received signal. Sampling occurs synchronously to a clock extracted from the received signal. Ideally, the sampling clock should occur between adjacent data transitions to optimize the BER. For a given symbol rate, each threshold-crossing time occurs ideally at integer multiples of symbol period. However, it deviates from the ideal value due to several factors in the link (*e.g.*, noise, limited channel bandwidth, or limited receiver front-end bandwidth). Consequently, the knowledge of the effect of the system on data threshold-crossing times and the sampling clock timing is essential for optimizing BER.

As we discussed in Section 2.5.1, data jitter is the deviation of the data threshold-crossing times from a reference time. The total jitter is modeled as the sum of two independent random variables, random jitter (RJ), Δt_{rj}, and deterministic jitter (DJ), Δt_{dj} [61];

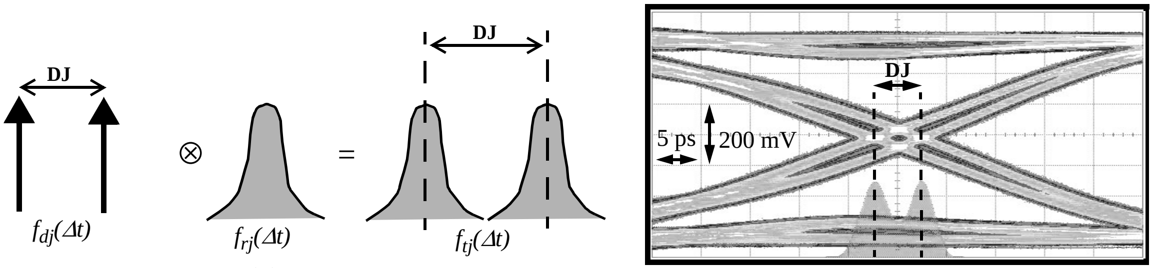
$$\Delta t_{tj} = \Delta t_{rj} + \Delta t_{dj} . \tag{3.1}$$

Hence, the total jitter probability distribution function (PDF) is the convolution of the PDF of RJ and DJ,

$$f_{tj}(\Delta t) = f_{rj}(\Delta t) \otimes f_{dj}(\Delta t) \tag{3.2}$$

where $f(\Delta t)$ is the PDF of each jitter term.

Random jitter is modeled by a Gaussian random variable. Deterministic jitter has systematic origins such as bandwidth limitation, crosstalk, or power supply noise. In general, it can be modeled as a stochastic process because transmitted data or data in neighboring channels is random. Efforts for modelling the probability distribution function of deterministic jitter are typically based on results from measurement techniques and numerical computation algorithms [72]–[75]. The distribution function of the DJ has been previously modeled as two impulses [61][73]. DJ is characterized by the distance between the two impulses [75]. Figure 3.1(a) illustrates how the total jitter distribution results from the combination of the RJ and the DJ. Figure 3.1(b) shows a typical measurement result for the eye diagram of a received data sequence around threshold-crossing time. The measured jitter histogram approximates data jitter distribution in Figure 3.1(a). In this chapter, we study analytically data-dependent jitter, one of the major components of deterministic jitter. We propose methods for



(a) (b)

Figure 3.1: (a) Distribution of total jitter from the convolution of RJ and DJ PDF (b) Eye diagram and jitter histogram measurement for a data sequence passed through a microstrip transmission line on FR4 PCB

characterizing DDJ theoretically, based on system parameters. Analytical studies on other sources of deterministic jitter can be found in [21].

3.2.2 Data-Dependent Jitter

Data-dependent jitter (DDJ) is the deviation of each data threshold-crossing time from a reference time due to the residual signal of the previous data bits delayed due to the memory of the system. Limited bandwidth of the transmission medium (*e.g.,* PCB traces), receiver front-end (*e.g.,* TIA), or electromagnetic reflections cause prior symbols to interfere with the current transition. While the effect of inter-symbol interference (ISI) on the amplitude of the received symbols has been studied (*e.g.,* [15][17]), its effect on the timing needs further analysis. The effect of ISI on timing is to change the threshold-crossing time of a data transition and cause DDJ, as shown by an example in Figure 3.2. Here, depending on the value of the bit prior to the “01” transition, the transition can occur earlier or later at the output of the system, as shown on the right.

To analyze DDJ, the data link with ISI is modeled as an LTI system. A sequence of random 2-PAM NRZ data is passed through the LTI system. The last two bits of the sequence are either “01” or “10” to model a rising edge transition or falling edge transition, respectively. The variation of the crossing time of the transition can be related to the data statistics to calculate DDJ. The process is illustrated in Figure 3.3, for a “01”

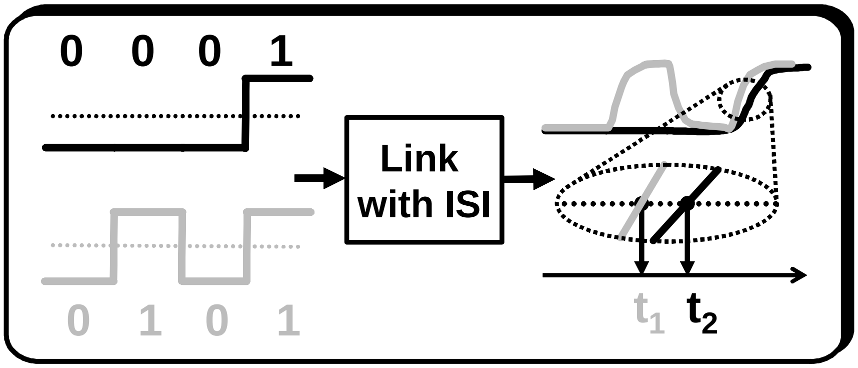


Figure 3.2: Data-dependent jitter is caused by ISI impact of prior bits

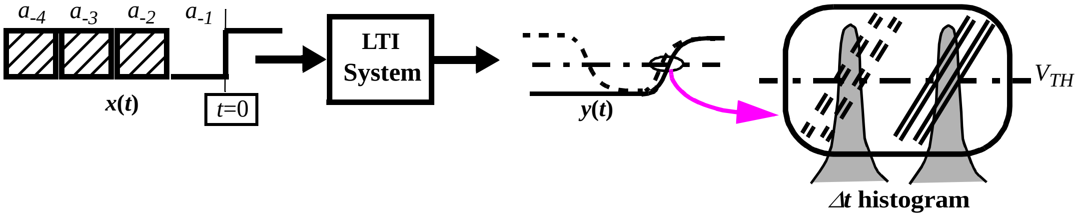


Figure 3.3: Response of a general LTI system to a random bit sequence and generation of DDJ

transition. For symmetric input rising and falling transitions and a threshold of half-signal swing, the jitter distributions for rising and falling transitions are identical and calculation of one is sufficient.

A random data sequence arriving at the input can be represented by

$$x(t) = u(t) + \sum_{k=-\infty}^{-2} a_k \cdot p_i(t - kT_b) \qquad (a_k \in \{0, 1\}) \tag{3.3}$$

$$p_i(t) = \begin{cases} 1 & 0 \le t \le T_b \\ 0 & otherwise \end{cases} \tag{3.4}$$

where $u(t)$ is the unit step function and models the rising edge, $p_i(t)$ is the unit pulse signal, as described in (3.4) with duration of bit period, T_b, and the a_ks are the random bits that are either "*1*" or "*0*" with a given probability. The sum in (3.3) starts from k=-2, *i.e.*, a_{-1}=0, to guarantee a rising edge at $t=0$. One can write a similar equation for a falling edge in which case $a_{-1}=1$, $a_0=0$, and the rest of the equation is the same as (3.3). Because the system is linear, we can use superposition theorem to find the output as

$$y(t) = s(t) + \sum_{k=-\infty}^{-2} a_k \cdot p_o(t - kT_b) \ , \tag{3.5}$$

where $s(t)$ and $p_o(t)$ are, respectively, the system step response and unit pulse response. The solution to

$$y(t_c) = v_{th} = 0.5 \tag{3.6}$$

for t_c determines the time of the threshold-crossing event as a function of data statistics and system parameters. We compare t_c to the time of the threshold-crossing event when all the a_ks are zero, and we denote it by t_0. We can calculate t_0 by solving $s(t_0) = V_{TH} = 0.5$.

Then, DDJ is defined as

$$\Delta t \equiv t_0 - t_c . \tag{3.7}$$

We will solve (3.6) for the first-order system as an example in Section 3.3 and analyze the general LTI system in Section 3.4.

3.3 An Analytical Expression for DDJ: First-Order System

3.3.1 Analytical Expression for Threshold-Crossing Time

In this section we analyze the DDJ of a first-order system, as described by the transfer function

$$H(s) = \frac{1}{1 + \tau s} . \tag{3.8}$$

Here, τ is the system time constant and the associated 3dB bandwidth is $1/(2\pi\tau)$. From (3.6) and (3.7), we can find a closed-form solution for the DDJ random variable of a first-order system as

$$\Delta t = -\tau \cdot \ln\left(1-\left(\frac{1-\alpha}{\alpha}\right)\sum_{k=-\infty}^{-2} a_k \cdot \alpha^{-k}\right) \tag{3.9}$$

where we define $\alpha \equiv e^{-T_b/\tau}$ similar to Chapter 2. In a system with a large bandwidth compared to the input data rate, α approaches zero. On the other hand, if the bandwidth is small the data transitions take longer. The upper limit on α for this calculation is set if we assume the rising transition crosses the threshold within a bit period. This bounds α to values smaller than 0.5. At α=0.5 the bandwidth is *only* 11% of the bit rate.

Equation (3.9) relates the impact of each prior bit and the threshold-crossing time deviation. For any data transition the prior bits are random sequences that overall result in an ensemble of Δt values. As $\alpha \leq 0.5$, the more recent bits have a dominant effect on jitter and a_{-2} has the largest impact. Also, the residual effect of the bits vanishes exponentially for a larger system bandwidth to bit rate ratio, *i.e.*, when α approaches zero. Figure 3.4 captures these effects by plotting Δt in unit intervals (UI) for different values of α. For each α, all the possible values of Δt are plotted. We include the impact of four prior bits and neglect the effect of more distant bits. A larger α corresponds to smaller

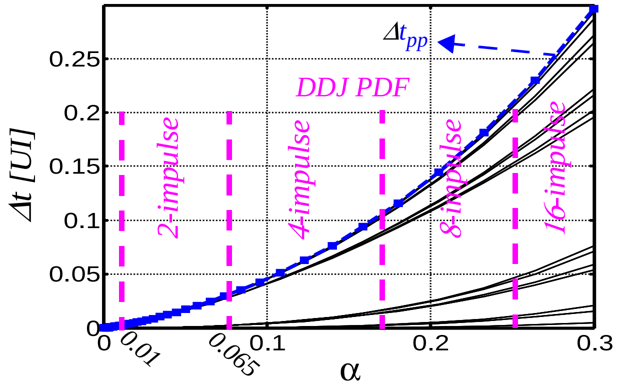


Figure 3.4: Ensemble of normalized DDJ values for different ratios of bandwidth to bit rate along with the appropriate model to use for data-dependent jitter PDF

bandwidth-to-bit rate ratio causing divergence in Δt values and larger data-dependent jitter. If we change the scale on the x-axis and plot DDJ for small values of α we will observe similar DDJ characteristics on a different scale of Δt. In fact it can be seen from (3.9) that for each data sequence, Δt takes a unique value. Therefore, on a smaller scale for α the same divergence characteristics would be observed for Δt values. The parameter Δt has a self-similar behavior for different scales of α.

For $0.01 \le \alpha \le 0.065$ Δt is concentrated around two values. In this range of system bandwidth, the DDJ distribution can be modeled with two impulses that carry the probability weight expressed in section Figure 3.2 However, for larger α the distribution should be extended to four or more impulses, as can be seen from Figure 3.4. In a first-order system, the concentration of data jitter around two values corresponds to bandwidth range, where only the penultimate bit, a_{-2}, has a remarkable effect on jitter. Since a_{-2} is “1” or “0,” the data jitter is divided into two mean probability masses, modeled by the two impulse functions. This is exactly the same as the conventional model for DDJ distribution based on the double Dirac delta function. We can also observe the behavior of DDJ similar to predictions of Figure 3.4. The threshold-crossing time and related histogram in the output of a first-order system is shown in Figure 3.5 for two different α values and demonstrates bifurcation of DDJ distribution from two delta functions to four delta functions as α increases.

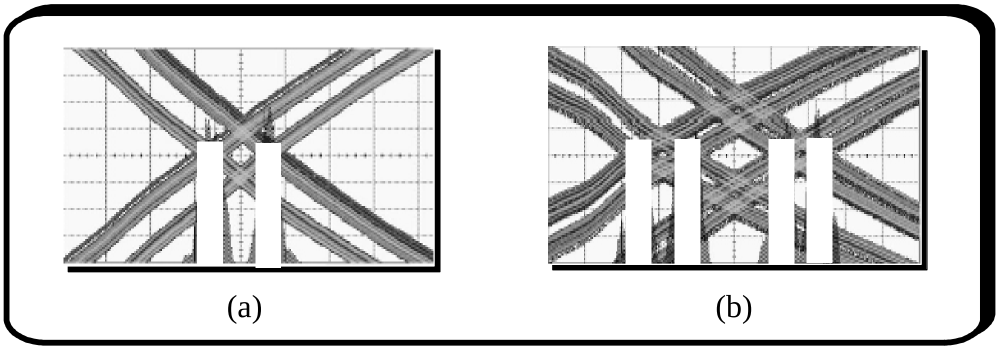

(a)
(b)

Figure 3.5: Threshold-crossing histogram and DDJ distribution: (a) α=0.1 (b) α=0.3

Similar behavior for data-dependent jitter distribution is generalized to higher-order systems as will be seen in Section 3.4. A dominant prior bit (not necessarily a_{-2}) will be identified that shapes data-dependent jitter distribution as two impulse functions.

3.3.2 Peak-to-Peak Jitter

Data-dependent jitter is bounded. It can be characterized by its peak-to-peak jitter value, Δt_{pp}. From (3.9), the maximum and minimum of Δt are obtained for "all one" and "all zero" sequence of a_k's. The "all zero" sequence corresponds to the latest threshold-crossing time, which is also selected as the reference time, t_0. Therefore, we can calculate peak-to-peak data-dependent jitter as

$$\Delta t_{pp} = -\tau \cdot \ln(1-\alpha) \tag{3.10}$$

which is overlaid with a dashed line on the plot in Figure 3.4. Since the latest crossing time is referenced, the plot shows that Δt_{pp} sets an upper bound on Δt.

3.3.3 Scale-One DDJ

In modern serial communication links, measured total jitter distributions resemble the jitter histogram in Figure 3.1(b). In such systems, a useful measure of data-dependent jitter is the distance between the two impulse functions in Figure 3.1(a) or the separation between the means of the two Gaussian distributions. According to discussions in Section 3.3.1, the two impulse distribution results when the impact of only one prior bit, a_{-2}, on jitter is included. Therefore we define the separation of the impulses as follows and call it the scale-one data-dependent jitter, DDJ_1, because only the impact of one prior bit is included.

$$DDJ_1 = E\{\Delta t | a_{-2} = 0\} - E\{\Delta t | a_{-2} = 1\} \tag{3.11}$$

where $E\{.\}$ is the expected value of Δt conditioned on a_{-2}. For equal probabilities of "1" and "0" we can show

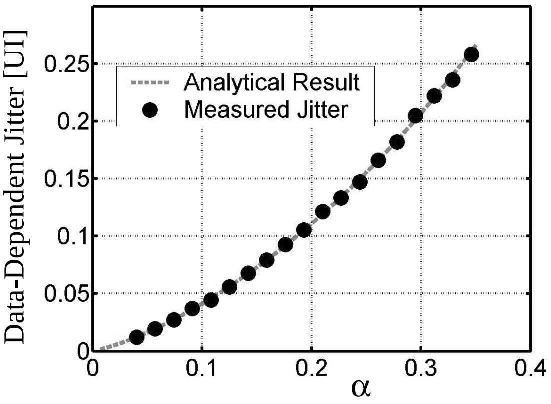


Figure 3.6: Comparison of the measurement results for DDJ_1 and the analytical expression in (3.12) for a first-order system

$$DDJ_1 = \frac{\tau}{2}\ln\frac{1+\alpha}{1-\alpha+\alpha^2}. \tag{3.12}$$

We verified the expression in (3.12) experimentally by testing an RC filter that serves as the first-order system. A $2^7 - 1$ pseudo-random bit sequence was applied to the filter and the jitter histogram was measured using Agilent's 86100 communication analyzer. The input bit rate was scanned over a wide range of observable DDJ_1 values. The separation of the jitter mean of the two Gaussians in the histogram was measured. Figure 3.6 demonstrates the excellent agreement between (3.12) and the measurement results. For $\alpha<0.02$ random jitter dominated DDJ_1.

3.4 An Analytical Expression for DDJ: General LTI System

3.4.1 Perturbation Method

For a general LTI system, equation (3.6) may not be solvable analytically. We propose a technique that approximates DDJ for a general LTI system based only on its step

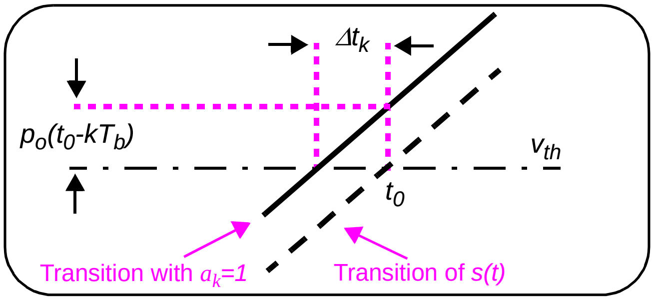


Figure 3.7: Deviation of the threshold-crossing time due to the effect of the *k*th bit

response. The method can be exploited easily in simulation or measurement to characterize DDJ and optimize jitter performance.

Data-dependent jitter occurs because the tails of prior bits *perturb* the time that the data transition crosses the threshold level. In the absence of any prior bit, threshold-crossing time is t_0 as discussed in Section 3.3.1. However, if a_k is "1" the *k*th prior bit changes $s(t)$ by $p_o(t_0\text{-}kT_b)$, in (3.5). This amplitude perturbation shifts the threshold-crossing time from t_0 and causes jitter. Assuming $p_o(t_0 - kT_b) \ll s(t_0)$, the shift in threshold-crossing time from the contribution of the *k*th bit can be calculated from the slope of $s(t)$ at t_0 and the shift in the amplitude of $s(t)$. This process is shown graphically in Figure 3.7. The threshold-crossing time shift due to the *k*th bit is denoted by Δt_k. We have

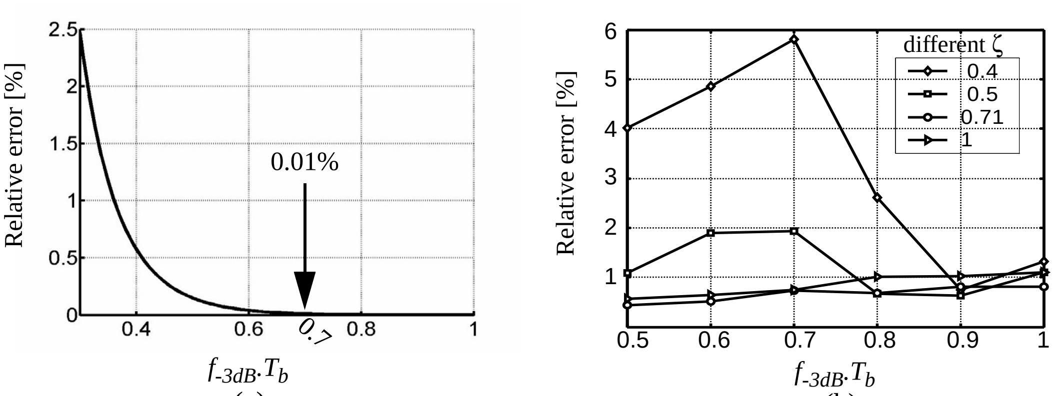
$$\Delta t_k \cong -\frac{p_o(t_0 - kT_b)}{\left.\dfrac{ds(t)}{dt}\right|_{t = t_0}} \qquad (3.13)$$

and the overall perturbation effect, DDJ, is

$$\Delta t \equiv \sum_{k=-\infty}^{-2} a_k \Delta t_k = \frac{-1}{\left.\dfrac{ds(t)}{dt}\right|_{t = t_0}} \cdot \sum_{k=-\infty}^{-2} a_k p_o(t_0 - kT_b). \qquad (3.14)$$

This technique is based on classical perturbation theory (*e.g.*, [76]). The assumption made above on the amount of perturbation bounds the accuracy of the method. In a practical system the bandwidth is chosen such that unit pulse response fall time is within T_b. Therefore, $p_o(t_0\text{-}kT_b)$ is much smaller than v_{th} and (3.14) is a good approximation. If the link is designed such that the received pulse has the shape of a Nyquist pulse, the approximation still holds. For such pulses the residual memory of prior bits changes slowly around the threshold-crossing [40]. Therefore, the perturbation of the step response is $p_o(t_0\text{-}kT_b)$. A similar methodology was used to calculate the reference jitter in a clock recovery system [66][77][78].

We evaluated the results in (3.14) for all possible bit sequences and compared them against the accurate DDJ in (3.9) for a first-order system. We limit k to $-10 \le k \le -2$ to account for the 11 most recent bits only because the effect of the bits exponentially decreases. Error in DDJ prediction is calculated for each bit sequence at different ratios of bandwidth ($1/2\pi\tau$) to bit rate ($1/T_b$), and for each ratio the worst case relative error is plotted in Figure 3.8(a). The perturbation method approximation has worst case accuracy of better than 2.5% in a practical range of bandwidth. Moreover, at the nominally optimum bandwidth-to-bit rate ratio of 0.7, the error is only 0.01%. For a first-order system, the error in approximation is identical even if $-3 \le k \le -2$.Therefore, (3.14) introduces a basis for a very efficient technique of calculating data-dependent jitter.



(a) (b)

Figure 3.8: Worst case accuracy of the perturbation method in predicting DDJ: (a) for a first-order system. (b) for a second-order system

A further verification of the perturbation technique is done for an all-pole second-order system with transfer function

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.15}$$

where ω_n is the natural frequency and ζ is the damping factor. The exact DDJ value for this system is computed from MATLAB simulations of system output for all possible bit sequences. Then, the approximated DDJ is calculated using (3.14). The results are compared and the worst case relative error is plotted in Figure 3.8(b) for different damping factors over a practical range of bandwidth normalized to bit rate. Again, small relative errors verify that (3.14) is an accurate expression for predicting the DDJ of a general LTI system based on its step response.

3.4.2 Peak-to-Peak Jitter and Scale-One DDJ

We can use (3.14) to estimate the peak-to-peak data-dependent jitter for a general LTI system. We have

$$\Delta t_{pp} = max\{\Delta t\} - min\{\Delta t\}. \tag{3.16}$$

The maximum of Δt is achieved for the data sequence in which $a_k = 1$ if $p_o(t_0 - kT_b) \le 0$ and $a_k = 0$ otherwise. Similarly, the minimum of Δt is achieved for the data sequence, where $a_k = 1$ if $p_o(t_0 - kT_b) \ge 0$ and $a_k = 0$ otherwise. Therefore, (3.16) is simplified to

$$\Delta t_{pp} = \frac{1}{\left.\frac{ds(t)}{dt}\right|_{t = t_0}} \cdot \sum_{k = -\infty}^{-2} \left|p_o(t_0 - kT_b)\right|. \tag{3.17}$$

Scale-one DDJ can also be defined for a general LTI system similar to (3.11). However, the predominant impact on jitter is not necessarily related to a_{-2}, as discussed in Section 3.3.3. The pulse response of the system and the bit rate determine the effect of prior bits. The effect of each prior bit can be estimated separately from (3.13) and the bit with most prominent impact can be distinguished. Then, using the same definition as in (3.11) and assuming that a_m has the largest impact on DDJ, we can write

$$\begin{aligned} DDJ_1 &= \left|E\{\Delta t|a_m = 0\} - E\{\Delta t|a_m = 1\}\right| \\ &= \left|E\left\{\sum_{\substack{k=-\infty \\ k\neq m}}^{-2} a_k\Delta t_k\right\} - E\left\{\Delta t_m + \sum_{\substack{k=-\infty \\ k\neq m}}^{-2} a_k\Delta t_k\right\}\right| = |\Delta t_m| \end{aligned} . \qquad (3.18)$$

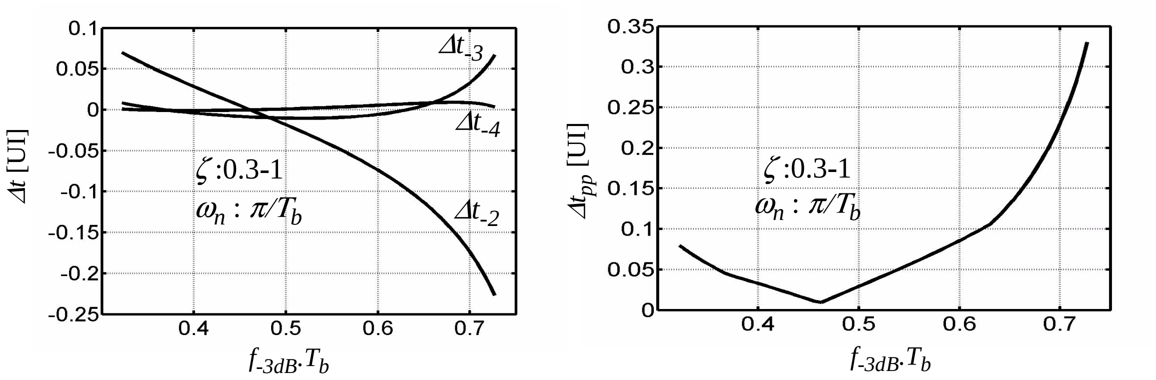
Therefore, we conclude

$$DDJ_1 = \left|\frac{p_o(t_0 - mT_b)}{\left.\frac{ds(t)}{dt}\right|_{t=t_0}}\right|, \qquad (3.19)$$

which is an important expression that determines the separation of the two impulses in the probability distribution function of DDJ as in Figure 3.1(a) for a general LTI system. It can be integrated into any communication link design or circuit design simulation software to predict the data-dependent jitter contribution of the corresponding component in the system. In addition, DDJ_1 can be easily measured using a general purpose high speed oscilloscope. We will verify equation (3.19) experimentally in Section 3.5. A significant advantage of the perturbation method is the remarkable reduction of the simulation or measurement time of DDJ. In fact, simulation time for peak-to-peak DDJ is now linearly related to k, while direct calculation from (3.6) requires passing all the 2^k possible sequences through the system, which increases exponentially with k.

3.4.3 Data-Dependent Jitter Minimization

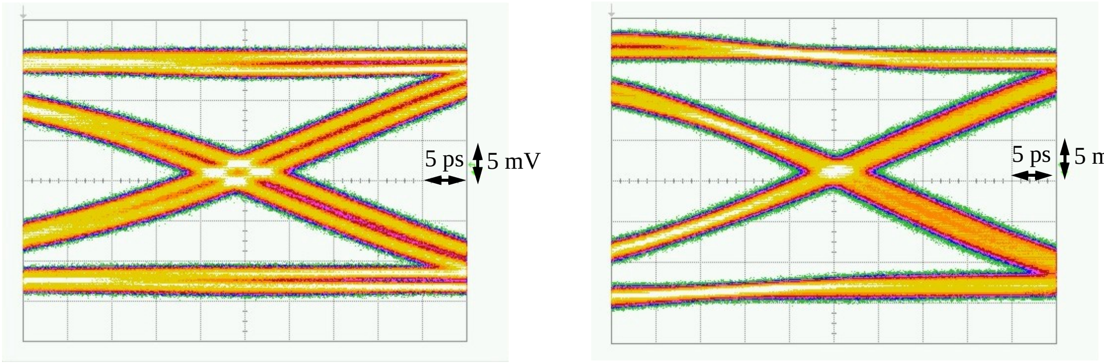
In a first-order system, any $a_k=1$ will increase the absolute value of DDJ. Furthermore, the closer the bit to the data transition, the stronger its impact on data jitter. However, this



(a) (b)

Figure 3.9: (a) Variation of the impacts of the last three prior bits on DDJ in a second-order system. (b) Existence of a minimum in the peak-to-peak data-dependent jitter

is not generally true for all LTI systems. It can be seen from (3.13) that the sign and value of Δt_k depends on $p_o(t_0 - kT_b)$, and based on the response of the system the effect of each prior bit can dramatically vary independent of the other bits. Particularly, the pulse response in (3.13) is sampled at integer multiples of bit period. Therefore, for a given bit rate, the system can be designed such that its pulse response reduces dominant DDJ terms and minimizes overall jitter. Pulse shapes that result in minimum jitter in addition to minimum ISI in the receiver have been studied [68][79]. As an example, the variations of the first three DDJ terms from (3.13) are plotted in Figure 3.9(a) for a second-order system with different bandwidth-to-bit rate ratios. The selected range covers under-damped, over-damped, and critically damped systems. In the range of *0.46-0.48* for the normalized bandwidth, Δt_{-3} has a larger impact on DDJ than Δt_{-2}. In addition, there exists a minimum in the peak-to-peak data-dependent jitter as illustrated in Figure 3.9(b). This jitter minimization behavior can be observed in higher-order systems as well. An experimental example is shown in Figure 3.10, where the output eye diagram of a 4” copper microstrip transmission line on conventional FR4 board is plotted at two different bit rates. The



(a) (b)

Figure 3.10: The output eye diagram of a 4” microstrip line on FR4 PCB at (a) 5 Gb/s and (b) 6.5 Gb/s demonstrates larger peak-to-peak deterministic jitter at lower bit rate

peak-to-peak jitter is clearly larger at the lower bit rate. As will be shown in Section 3.5, increasing the bandwidth blindly does not necessarily reduce the DDJ.

3.5 Experimental Verification

Equation (3.19) provides a simple means for finding the DDJ contributions of any LTI system for any bit rate based only on the step response. The pulse response can be stated in terms of step response as $p(t)=s(t)-s(t-T_b)$. We will verify the validity of the results experimentally by comparing the predictions of (3.19) with measured DDJ_1 of several high-frequency systems including an integrated CMOS trans-impedance amplifier. We associate DDJ_1 to the separation of the means of two Gaussian distributions, as in Figure 3.1(b) when the jitter histogram at the output of the device under test (DUT) is measured. We use Anritsu’s MP1763C pulse pattern generator to provide the step input and pseudo random bit sequence (PRBS) input of the length 2^7-1. We also use Agilent’s 86100 communication analyzer to measure the step response and jitter histogram at the output. For each system, we first measure and record the step response. Then, we apply a PRBS at the input with varying bit rate. We measure DDJ_1 at a bit rate where the system shows significant amount of data-dependent jitter. The bit rate is always such that the data spectrum does not exceed the system bandwidth. This fact demonstrates that while the system bandwidth is large enough to minimize amplitude distortion, DDJ still persists. The jitter histogram is measured after at least 500,000 crossing events are captured by the oscilloscope. At the same time, we compute the pulse response from the measured step response and the current bit rate and calculate DDJ_1 from (3.19). Finally, we compare the measured and analytically-calculated DDJ_1.

A. Discrete systems. In one set of experiments we carry out the procedure for various off-the-bench systems available in the lab. They include a Mini Circuit ZFL 1000-LN driver amplifier with 1GHz bandwidth, a 9” long 50Ω copper microstrip on standard FR4 printed circuit board, a 10.5’ long standard BNC coaxial cable, and an HP 11688A microwave high-order lowpass filter with cut-off frequency of f_c=2.8 GHz. None of these systems has a simple first-order response. Therefore the DDJ_1 should be estimated from (3.19). The measurement results are summarized in Table 3.1. Small relative errors in the last column verify the validity of the analytical results for predicting data-dependent jitter. For the microstrip line, a_{-3} rather than a_{-2} has the most dominant effect on DDJ and causes the scale-one separation of the threshold-crossing times.

Table 3.1: Comparing measured DDJ_1 and predictions of analytical expression in (3.19)

DUT	Bit Rate Measured	Measured DDJ_1 [psec]	Dominant Bit	Corresponding dominant Δt_k [psec]	Error
Mini Circuit ZFL-1000	1.3 Gb/s	7.665	a_{-2}	7.15	-6.7%
microstrip on FR4 PCB	10 Gb/s	5.35	a_{-3}	5.23	-2.3%
HP 11688A Lowpass Filter	1.2 Gb/s	20.5	a_{-2}	18.96	-7.5%
coaxial cable	3 Gb/s	4.6	a_{-2}	4.72	2.5%

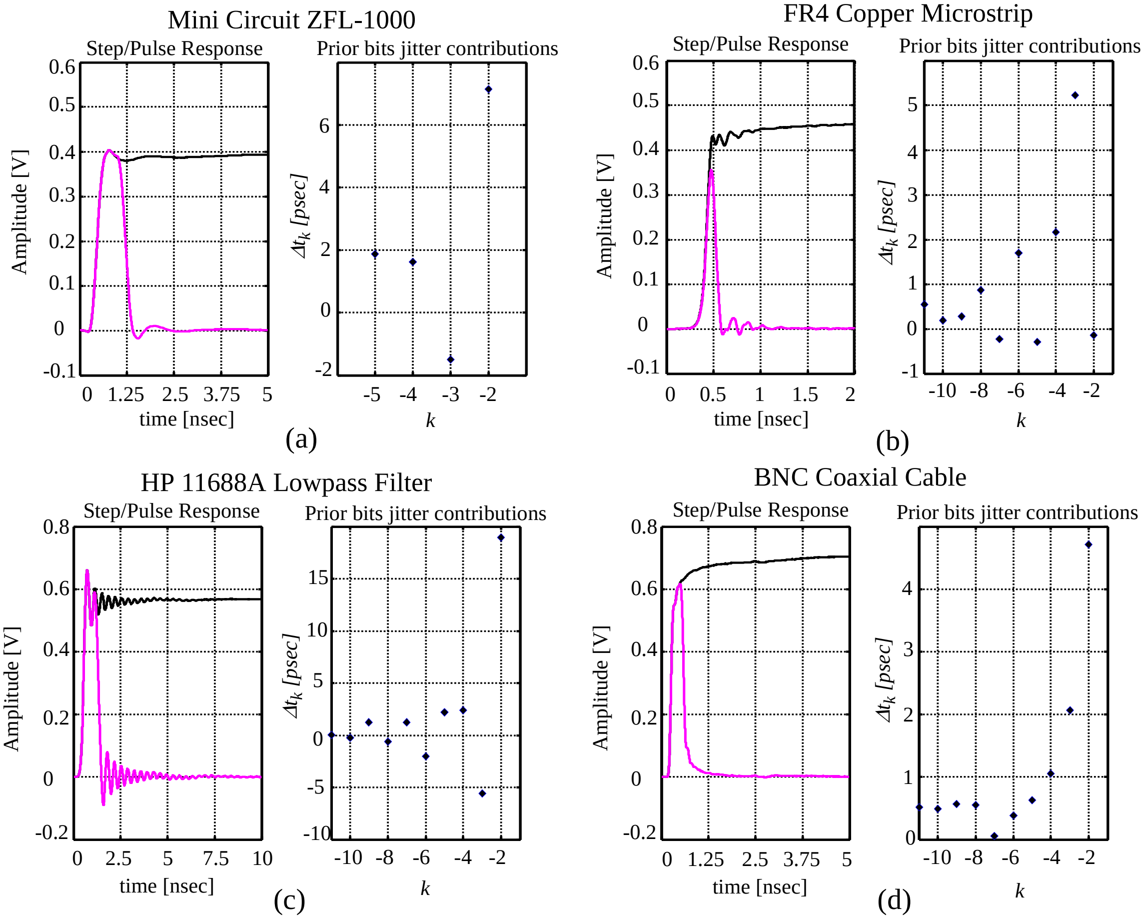


Figure 3.11: Step response, pulse response, and the individual jitter contributions of prior bits as calculated from (3.13) for the systems under test: (a) Mini Circuit ZFL-1000 amplifier (b) Copper microstrip line on FR4 PCB (c) HP 11688A lowpass filter (d) BNC coaxial cable

Step response, pulse response, and the jitter contributions of some prior bits are plotted in Figure 3.11 for the systems we tested. Δt_k is calculated from pulse response using (3.13). An important observation is the significance of the time response of the system and its impact on data-dependent jitter at the output. HP 11688A is a lowpass filter with the 3dB cut-off frequency at 2.8GHz. Compared to ZFL-1000, an amplifier with 3dB bandwidth of 1GHz, one may suspect that the data-dependent jitter contribution to overall jitter is larger for the amplifier due to smaller bandwidth. However, around the same bit rate (1.2-1.3 Gb/s), the filter has significantly larger DDJ. This can be associated to the pulse response characteristics of the two systems as illustrated in Figure 3.11(a) and (c). Pulse response of the filter has larger ringing in its damping tail that dramatically increases the jitter from (3.13) because the samples of the pulse response at the measurement bit rate (1.2 Gb/s) coincide with the maxima and minima of the oscillating tail. Consequently, the contributions of prior bits are all significant and oscillate between negative and positive values, as can be seen from Figure 3.11(c). However, the amplifier has smaller ringing, and the ringing oscillation frequency is not constant and is not related to the measurement bit rate.

In summary, we must emphasize that bandwidth alone cannot be a complete measure to characterize the DDJ contributions of an LTI system. Although systems with small bandwidth tend to increase DDJ, step response or pulse response of the system is required to analyze the exact characteristics of output data-dependent jitter. Particularly, the system can be designed such that the samples of its pulse response are negligible at integer multiples of bit period to minimize DDJ. Along the same line of arguments and similar to Nyquist’s zero-ISI pulse shaping [15], Huang *et al.* [68] and Gibby *et al.* [79] have proposed channel pulse shapes that result in minimum jitter contributions from prior bits and hence optimize data-dependent jitter performance of the link.

In a communication link, if the channel response is not known or is time varying, zero-ISI pulse shaping is not possible. In such cases, an adaptive equalizer is utilized in the receiver to minimize ISI. Similarly, if pulse shaping for the transmitted data sequence is not feasible due to channel unpredictability, a data-dependent jitter equalizer can be used in front of the clock recovery circuit [80].

B. Integrated Trans-Impedance Amplifier. To verify the validity of the DDJ prediction theory we tested an integrated trans-impedance amplifier (TIA). The TIA was implemented in a 0.18μm BiCMOS technology using only CMOS transistors and demonstrated a 9.2 GHz 3dB bandwidth [23][24]. We mounted the amplifier on a brass substrate and built the additional circuitry around it on the same substrate using a low-loss

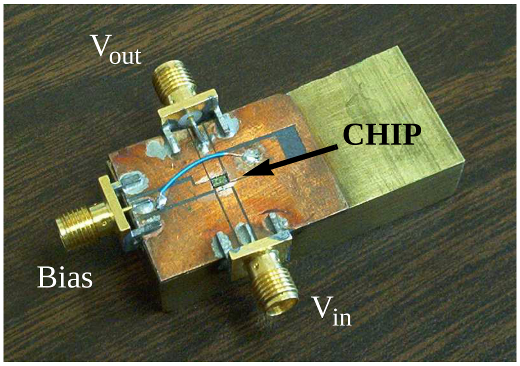


Figure 3.12: TIA test board setup for the 10 Gb/s TIA

duroid PCB. The chip is wire bonded to microstrip transmission lines that then transfer the signal to SMA connectors on the brass substrate. The test board setup is shown in Figure 3.12. Although this TIA has enough bandwidth to operate at 10 Gb/s, the reflections from connectors and wirebond mismatches in addition to the amplifier response cause the whole system to have a ringing step response as the measurement shows in Figure 3.13. In spite of having enough bandwidth, the TIA, along with the measurement setup, exhibits a large amount of DDJ.

We measured the DDJ of the TIA at two bit rates, 1.65 Gb/s and 3.3 Gb/s, using the same procedure previously discussed. While the bit rates are within the bandwidth range of the TIA, we observed significant amounts of DDJ. The eye diagram at 1.65 Gb/s is

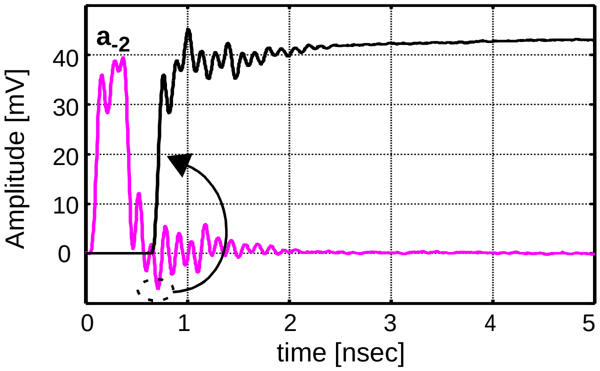


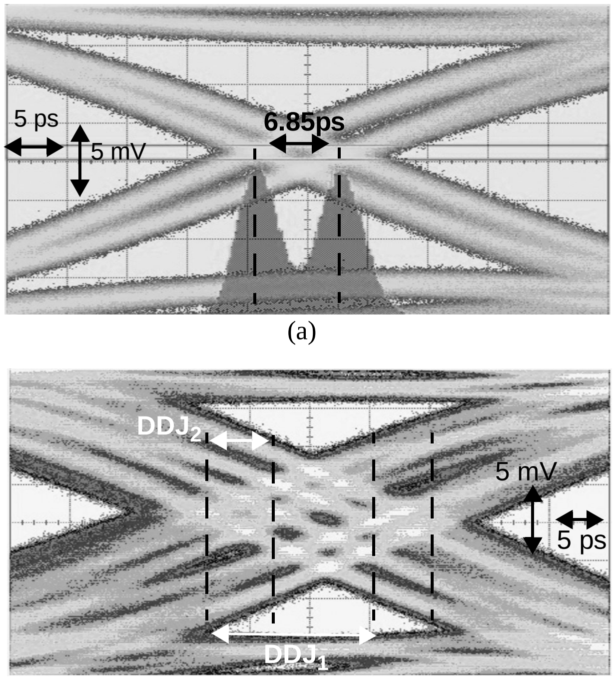
Figure 3.13: TIA step response and impact of a_{-2} pulse on t_0 in a “101” sequence at 3.3Gb/s

shown in Figure 3.14(a). The measurement results are summarized in Table 3.2. We should stress that the prediction of DDJ at several bit rates can be done by measuring the step response only once.

Table 3.2: Comparing measured DDJ_1 and predictions of analytical expression for the 10GB/s CMOS TIA

Bit Rate	**Measured DDJ_1[psec]**	**Dominant Bit**	**Predicted Δt_k [psec]**	**Error**
1.65 Gb/s	6.85	a_{-2}	6.8	0.85%
3.3 Gb/s	13.6	a_{-2}	12.7	6.6%
3.37 Gb/s	14.1	a_{-2}	12.4	12%
3.37 Gb/s	**DDJ_2=5.85**	a_{-3}	5.7	2.5%

In the case of 1.65 Gb/s, DDJ prediction using the perturbation method has only 0.85% error. Larger scales of data-dependent jitter that are associated with prior bits with less-dominant jitter contributions are often smaller than rms of random jitter. Therefore, they are hard to measure or observe and are thus neglected. However, the perturbation method can still predict the DDJ of larger scales. We measured the DDJ scale-one (DDJ_1) and scale-two (DDJ_2) of the TIA at 3.37 Gb/s, where both were observable, as Figure 3.14 illustrates. The measurement results are compared with the calculations in Table 3.2. The perturbation method predicts scale-two DDJ with an accuracy of 2.5%. The measured values of DDJ_1 and DDJ_2 are respectively related to Δt_{-2} and Δt_{-3} as calculated from (3.13). The negative value of Δt_{-2} corresponds to a negative shift in the zero crossing. In other words, all the sequences in which Δt_{-2} is *"1"* will split from the zero crossings that occur at t_0 and will move to $t_0 -|\Delta t_{-2}|$. On the other hand, positive Δt_{-3} will split each crossing group to two groups, one remaining in the same position and one moving Δt_{-3} to the right. Therefore, overall, four crossing groups can be observed, as in Figure 3.14(b).



(a)

(b)

Figure 3.14: TIA eye diagram when DDJ$_1$ and DDJ$_2$ are observable (a)1.65 Gb/s (b)3.37Gb/s

3.6 DDJ Impact on the BER

In the previous chapter, we studied the combined effect of ISI and jitter on the BER. However, we saw in this chapter that the jitter distribution should be modified in the presence of inter-symbol interference because ISI causes DDJ. The impact of DDJ is to change the distribution of the total jitter distribution. The effect of jitter on the BER is formulated in (2.23), which is rewritten here as

$$BER_j(T_s) = \frac{1}{2}\left[\int_{T_s}^{\infty} f_{TJ}(t)\cdot dt\right] + \frac{1}{2}\left[\int_{-\infty}^{-T_b+T_s} f_{TJ}(t)\cdot dt\right]. \tag{3.20}$$

Let’s assume that the DDJ is modeled with a double Dirac delta function distribution and the dominant prior bit that causes this distribution is a_{-2}. $f_{TJ}(.)$ is the convolution of the

RJ Gaussian distribution and the DDJ distribution as in (3.2). Equivalently, we can split (3.20) to two terms where each is the BER caused by random jitter conditioned on the value of a_{-2}. We have

$$BER_j(T_s) = p \cdot BER_j(T_s, a_{-2} = 0) + (1-p) \cdot BER_j(T_s, a_{-2} = 1) \tag{3.21}$$

where p is the probability that a_{-2}=0. Each of the BER_j terms on the right can be calculated from (3.20) by replacing $f_{TJ}(.)$ with a Gaussian distribution, while noting that the value of the a_{-2} determines the mean value of the Gaussian distribution. The mean value of the Gaussian distribution is the same as the mean of the threshold-crossing times and can be found from (3.7)

$$t_{c,0} = E\{t_c | a_{-2} = 0\} = t_0 - E\{\Delta t | a_{-2} = 0\} \tag{3.22}$$

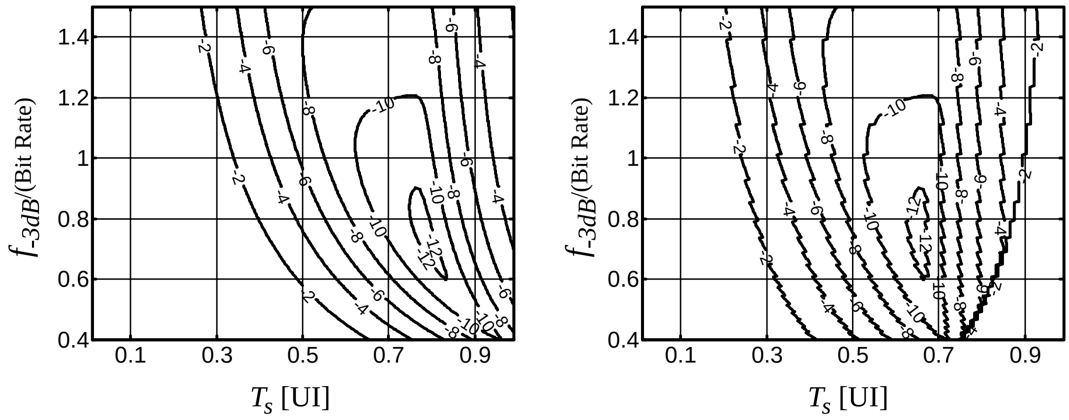
$$t_{c,1} = E\{t_c | a_{-2} = 1\} = t_0 - E\{\Delta t | a_{-2} = 1\}. \tag{3.23}$$

We find the values of $t_{c,0}$ and $t_{c,1}$ in Appendix B. We can write the BER caused by jitter, conditioned on a_{-2}, as

$$BER_j(T_s, a_{-2} = 0) = BER_j(T_s, t_{c,0}) = \left[Q\left(\frac{T_s - t_{c,0}}{\sigma_j}\right) + Q\left(\frac{T_b - (T_s - t_{c,0})}{\sigma_j}\right)\right] \tag{3.24}$$

$$BER_j(T_s, a_{-2} = 1) = BER_j(T_s, t_{c,1}) = \left[Q\left(\frac{T_s - t_{c,1}}{\sigma_j}\right) + Q\left(\frac{T_b - (T_s - t_{c,1})}{\sigma_j}\right)\right]. \tag{3.25}$$

The impact of DDJ on the overall BER can also be calculated by modifying the distribution of the timing jitter. We have carried out this analysis in Appendix A, equation (A.10). We can use (A.10) to generate the BER contours similar to Section 2.6.3.2. We have plotted the BER contours for a first-order system in Figure 3.15(a) for when σ_j=0.05UI and N_0=4e-3V/Hz^2. Because the DDJ is related to the system response and it decreases with larger bandwidth in a first-order system, the BER contours depend on the bandwidth at all of the sampling points. This is in contrast to Figure 2.28(b), where DDJ was neglected and the BER becomes independent of bandwidth when jitter dominates the BER.



(a)

(b)

Figure 3.15: BER contours for σ_j=0.05UI and N_0=4e-3V^2/Hz for two reference times for the sampling point (a) t=0 (b) bandwidth-dependent threshold-crossing time

The values of $t_{c,0}$ and $t_{c,1}$ are functions of the system response. For instance, for a first-order system, both $t_{c,0}$ and $t_{c,1}$ increase. In practice, this results in an offset in the eye diagram of the data. This is because the threshold-crossing times that determine the start and stop time of the eye diagram shift. Therefore, the absolute value of the optimum sampling time that is achieved from the BER contours such as the one in Figure 3.15(a) must also be offset by the same amount. Equivalently, we can replot the BER contours and change the reference time for the sampling time from t=0 to the threshold-crossing time for each bandwidth. This will result in the contours in Figure 3.15(b). Figure 3.15(b) demonstrates that for all of the bandwidths, the optimum sampling point is at 0.65UI, which is 0.15UI offset from the middle of the eye. The optimum system bandwidth for minimum BER is again around 70% of the data rate.

We showed in Section 3.4 how to estimate the DDJ impact of a general LTI system from its response that can be used to calculate $t_{c,0}$ and $t_{c,1}$ in (3.22) and (3.23). Therefore, the BER contours can be easily obtained for any LTI system based on its response.

3.7 Summary

The data-dependent jitter is one type of deterministic jitter that results from residual effects of prior bits on a data threshold-crossing time. It degrades the BER and the data link performance as the data rates increase, while the system bandwidth budget is restricted. We proposed a methodology to analytically estimate a general LTI system's data-dependent jitter based on its step response. The method reduces the complexity remarkably because computation time grows linearly with the number of prior bits. Whereas, in conventional methods, the complexity grows exponentially with the number of bits.

We verified the validity of the analytical results with simulations and demonstrated experimentally that this approximation is reasonably accurate for several systems. In addition, we showed that certain pulse response shapes can result in a minimum peak-to-peak data-dependent jitter. Finally, we highlighted that 3dB bandwidth does not characterize DDJ of the system completely, and the shape of the system step response is the important and essential element that determines DDJ characteristics. We provided the relationship between the overall BER of a data link and the link response by considering the effect of DDJ that complemented our calculations in Chapter 2. By analytically relating the impact of the data link impairments to the BER we can design the system response and link specifications to optimize the link reliability.

Chapter 4

Bandwidth Enhancement for Wideband Amplifiers

4.1 Introduction

Wideband amplifiers are one of the most critical building blocks at the front-end of a high-speed link receiver. As we discussed in Chapter 2, any baseband communication system needs a wide bandwidth receiver due to the signal's low-frequency spectral content. Particularly, all amplifiers in the signal path, such as the trans-impedance amplifier (TIA) in Figure 2.21, should have enough bandwidth with minimum variations in the passband and near constant group-delay to avoid distortion in the signal. We studied the impact of restricted bandwidth, in the form of ISI and jitter. In this chapter, we provide conditions to maximize the bandwidth of amplifiers in the front-end of high-speed receivers. We are mainly interested in integrated amplifiers that are implemented by a silicon-based technology.

Silicon integrated circuits are the only candidates that can achieve the required level of integration with reasonable speed, cost, and yield and have thus been pursued to a great degree in recent years. In particular, full integration of silicon-based optical-fiber communication systems at 10Gb/s and 40Gb/s is of great interest. However, silicon-based integrated circuits implementing such systems face serious challenges due to the inferior parasitic characteristics in silicon-based technologies, complicating the procedure for a wideband design.

The inherent parasitic capacitors of devices are the main cause of bandwidth limitation in wideband amplifiers. Several bandwidth enhancement methods have been proposed in the past that can be utilized to overcome this issue in silicon technologies. First-order shunt peaking has historically been used to introduce a resonant peaking at the output as the amplitude starts to roll off at high frequencies [81]–[83][1]. It improves the bandwidth by adding an inductor in series with the output load to increase the effective load impedance as the capacitive reactance drops at high frequencies. Neuhauser *et al.* studied the effect of bondwire inductors and used an active peaking network to enhance the bandwidth [84][85]. Capacitive peaking uses an explicit capacitor to control the pole locations of a feedback amplifier and thus potentially improves the bandwidth [86].

A more exotic approach to solving the problem that was proposed by Ginzton *et al.* is using distributed amplification [87]. Here, the gain stages are separated with transmission lines. Although the gain contributions of several stages are added together, the artificial transmission line isolates the parasitic capacitors of several stages. In the absence of loss, we can improve the gain-bandwidth product without limit by increasing the number of stages. In practice, the improvement is limited by the loss of the transmission line. Hence, the design of distributed amplifiers requires careful electromagnetic simulations and very accurate modeling of transistor parasitics. For instance, a CMOS distributed amplifier was presented in [88] with a unity gain frequency of 8.5 GHz.

The work presented in this chapter applies a multi-pole bandwidth enhancement technique to wideband amplifier design. It is based on turning the entire amplifier into a low-pass filter with a well-defined passband characteristic and cut-off frequency. The inevitable parasitic capacitances of the devices are absorbed as part of the low-pass filter and, hence, affect the bandwidth of the amplifier in a controlled fashion. Theoretical limits of the gain-bandwidth product of lumped amplifiers have been known for over half a century [26], [27], [89]–[91]. Broadband filter synthesis techniques for bandwidth enhancement have been used for wideband amplifiers [93][94] and interconnect [95] design. Applying proper matching networks between amplifier stages to approach those limits is the key step in improving wideband amplifiers' bandwidth with this method.

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[1] For more references on traditional techniques for wideband amplifier design look at the bibliography of [89].

Section 4.2 reviews these theoretical limitations. Section 4.3 presents a technique to improve the bandwidth of wideband amplifiers. A design example using this technique follows in Section 4.4 to demonstrate the practicality of the method, whose validity is shown with experimental results in Section 4.5.

4.2 Wideband-Amplifier Limits

A wideband amplifier should retain near-constant gain and linear phase over its passband. The bandwidth requirements of such amplifiers continuously increase following the drive for higher-speed systems. While device scaling continues to provide faster transistors with higher cut-off frequencies, it is still desirable to improve the bandwidth of amplifiers using circuit techniques that enable us to do so for a given process technology.

Over the last few decades, many techniques have been developed to improve the bandwidth of amplifiers [36]. An improvement in the bandwidth of the amplifier is often accompanied by a corresponding drop in its low frequency voltage gain. As such, the gain-bandwidth product (*GBW*) can serve as a first-order figure of merit for an amplifier topology in a given device technology [89][90]. For the purposes of this discussion, the bandwidth is defined as the lowest frequency at which the voltage gain drops by $\sqrt{2}$ or 3dB. Accordingly, this bandwidth is often called the *3dB bandwidth*. In Section 4.2.1, we discuss the GBW limits of single-stage amplifiers for one- and two-port passive load networks. Section 4.2.2 is dedicated to GBW limits of multi-stage amplifiers.

4.2.1 Single-Stage Amplifiers

4.2.1.1 One-port (two-terminal) load network

Figure 4.1(a) shows the simplest model for a linear single-stage amplifier, where R and C are, respectively, the aggregate parasitic resistance and capacitance of the transistor and the input of the following stage. The gain-bandwidth product of this amplifier is given by:

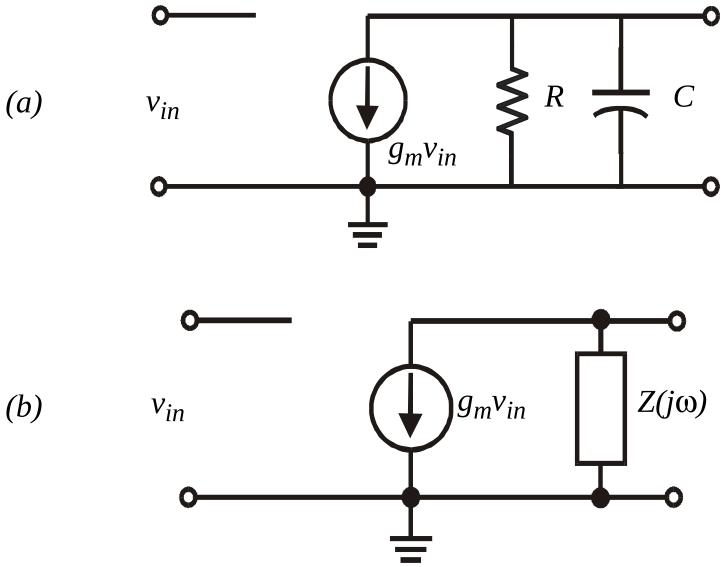

Figure 4.1: Single-stage amplifier: (a) First-order load (b) General passive impedance load

$$GBW = g_m R \cdot \frac{1}{2\pi \cdot RC} = \frac{g_m}{2\pi \cdot C} \tag{4.1}$$

As can be seen, the parasitic capacitance directly limits the bandwidth by reducing the output impedance of the amplifier as the frequency grows. Consequently, retaining a uniform output impedance over a wider frequency range will increase the GBW. In general, it is possible to introduce a more elaborate passive load network $Z(j\omega)$ to do so. Figure 4.1(b) shows the generic load network, $Z(j\omega)$, that should look like a constant resistor over as wide a frequency range as possible. Wheeler [89] and Hansen [90] have derived an intuitive upper bound for such a range. Bode [26] has mathematically proven the existence of a bandwidth limit for a class of load impedances. Fano [27] and Youla [91] have further generalized the theory for a larger class. This theoretical limit (a.k.a. Bode-Fano Limit) for the amplifier in Figure 4.1(b) is [96]:

$$GBW_{max} = \frac{g_m}{\pi \cdot \overline{C}} \tag{4.2}$$

where $\overline{C}$ is defined as:

$$\bar{C} = \lim_{\omega \to \infty}\left(\frac{1}{j\omega Z}\right) \tag{4.3}$$

and *Z(jω)* is an impedance function, as defined in Appendix C. *Z(jω)* includes the aggregate output capacitance *C*, shown in Figure 4.1(a). It is easy to show that for a one-port load network, $\bar{C}$ is greater than or equal to *C*. Thus, according to (4.2), *any* one-port passive network added in parallel to *C* can improve the GBW by at most a factor of two over that of the amplifier in Figure 4.1(a). As a result, the maximum achievable bandwidth enhancement ratio (*BWER*) for a one-port load is *two*. Shunt-peaking is an example of this case. Shunt peaking results in BWER of 1.6 and 1.72 when designed for optimum group delay or maximally flat responses, respectively [83].

4.2.1.2 Two-port (four-terminal) matching network

Figure 4.2(a) shows a single-stage amplifier, where the intrinsic output resistance and capacitance of the transistor, *i.e.*, R_1 and C_1 are separated from those of the load, namely, R_2 and C_2. The combination of capacitors C_1 and C_2 limits the bandwidth of the amplifier, *i.e.*,

$$GBW = \frac{g_m}{2\pi \cdot (C_1 + C_2)}. \tag{4.4}$$

In this case, a passive two-port network can be inserted between the transistor's intrinsic components (R_1 and C_1) and load (R_2 and C_2) to increase the bandwidth, as shown in Figure 4.2(b). This two-port passive network can be designed to maintain the impedance constant over a wider frequency range, as it separates and isolates C_1 and C_2. Therefore, C_1 is the only capacitor that affects the gain-bandwidth product at the input port of the network. Based on the argument in Section 4.2.1.1, the maximum gain-bandwidth product at the input port of *N(jω)* is:

$$GBW_{max} = \frac{g_m}{\pi \cdot C_1}. \tag{4.5}$$

Bode has shown that for $C_1 = C_2 = C/2$[1] it is possible to design *N(jω)* in such a way that the gain-bandwidth product at the output port is the same as that of the input [26]. Thus, for a single stage-amplifier with a two-port passive load network:

$$GBW_{max} = \frac{2g_m}{\pi \cdot C}. \tag{4.6}$$

This can be done by using a constant-*k* LC-ladder filter [26][50][89] terminated to its image impedance. A constant-*k* LC-ladder filter that is terminated in its image impedance

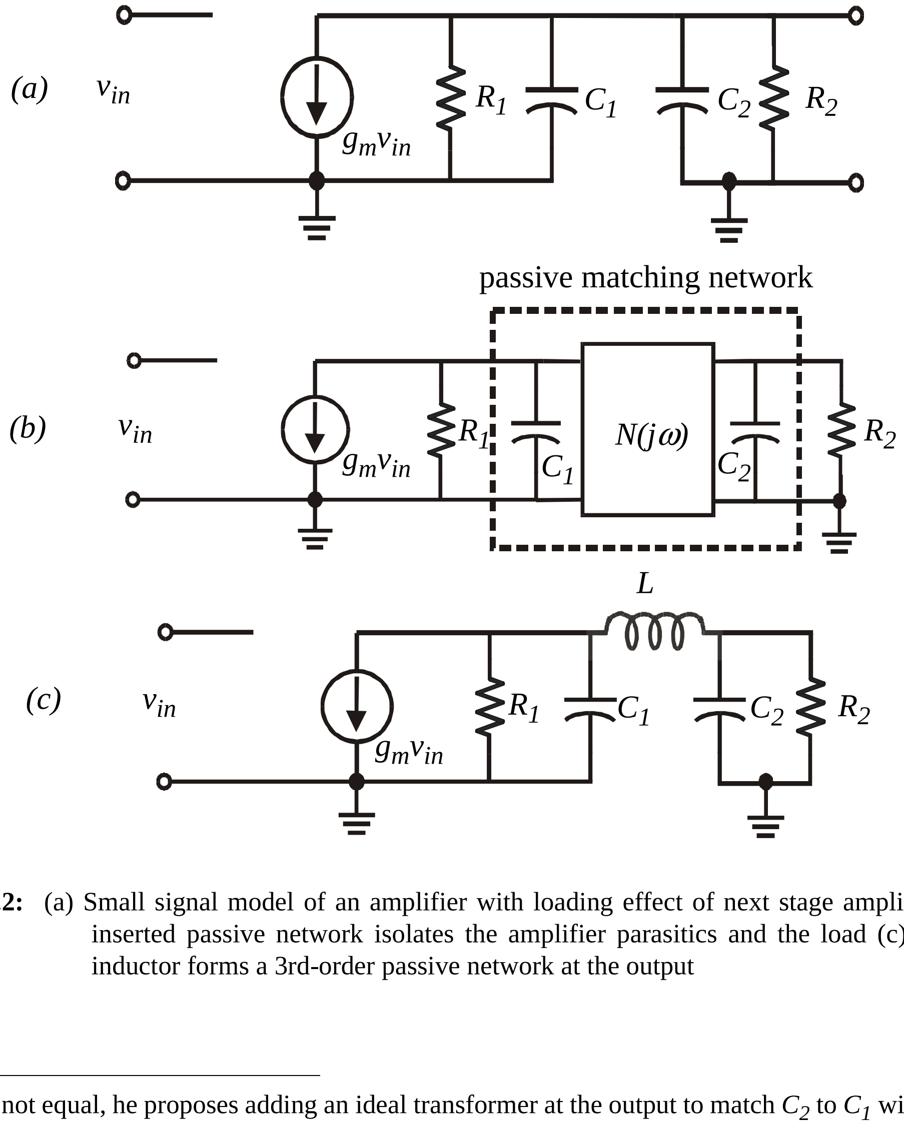

Figure 4.2: (a) Small signal model of an amplifier with loading effect of next stage amplifier (b) The inserted passive network isolates the amplifier parasitics and the load (c) Additional inductor forms a 3rd-order passive network at the output

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[1] If not equal, he proposes adding an ideal transformer at the output to match C_2 to C_1 with the proper ratio.

has a *constant* transfer function over the frequencies less than its cut-off frequency. Compared to (4.4) with $C_1 = C_2 = C/2$, (4.6) is four-times larger than the gain-bandwidth product of a single-stage amplifier without an additional coupling network. As a result, for equal low-frequency gain, the maximum achievable *BWER* for a two-port load is *four*.

In general, it is computationally difficult to calculate the component values for the optimizing two-port network directly. Even in the case of a third-order system, with only an additional inductor between the device and the load as in Figure 4.2(c), the equation for the value of the inductor that maximizes the bandwidth is quite complicated. Instead, graphical or numerical methods can be used. Figure 4.3 shows a normalized gain of a single-stage amplifier with a passive network load similar to Figure 4.2(c), where a single inductor isolates C_1 and C_2. The component values are normalized to achieve *0dB* gain at low frequency and a *1 rad/s* 3dB bandwidth. Figure 4.3(a) corresponds to when the output impedance of the amplifier is equal to the load ($R_1 = R_2 = 1\Omega$ and $C_1 = C_2 = 1F$). Figure 4.3(b) shows the case for $R_1 = 0.5\Omega$ and $R_2 = \infty$. This may occur when the output of the amplifier is connected to the next stage with capacitive input. Values for the bandwidth enhancement ratio *(BWER)*, defined as the ratio of the 3dB bandwidth of the amplifier to the 3dB bandwidth when *L=0*, in both cases is summarized in Table 4.1. It is noteworthy that even with a simple third-order passive network, BWER is significant compared to its theoretical limit. Bandwidth optimization assumes no gain peaking constraints.

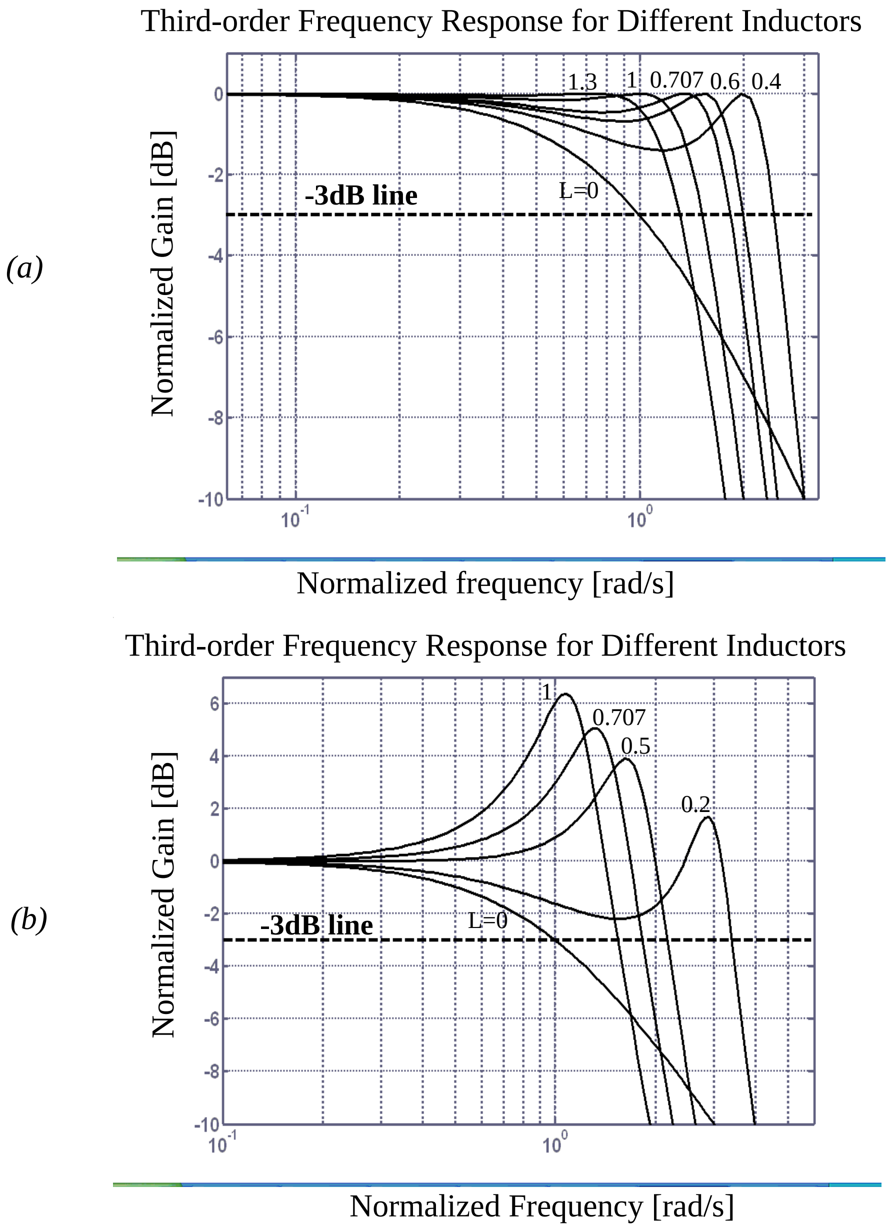

Figure 4.3: Normalized gain of the amplifier with 3rd-order network load and different inductor values: (a)$R_1 = R_2 = 1\Omega, C_1 = C_2 = 1F$ (b)$R_1 = 0.5\Omega, R_2 = \infty, C_1 = C_2 = 1F$

An alternative method to design the passive network is to look up the component values in standard tables for low-pass filter design [97] or compute them from corresponding equations [23][24][98]. Essentially, the additional passive networks are low-pass structures that control the frequency response of the amplifier. After choosing the desired frequency response for the amplifier, such as maximally flat gain or maximally flat group delay, the component values can be chosen directly from standard tables. This will be discussed thoroughly in Section 4.3.

Table 4.1: Bandwidth enhancement ratios for the two 3rd-order passive networks in Figure 4.3

L Value [H]	Case 1 $R_1=R_2=1\Omega$	Case 2 $R_1=0.5\Omega$ $R_2=\infty$
0	1	1
0.2	1.44	3.4
0.4	2.46	2.42
0.5	2.2	2.17
0.6	2	1.99
0.707	1.83	1.83
1	1.52	1.55
1.3	1.31	1.36

4.2.2 Multi-Stage Amplifiers

Often it is hard to achieve a desirable gain-bandwidth product with a single-stage amplifier. Then, several stages can be cascaded. The total gain is the product of the gain of each stage. However, the overall bandwidth is less than the bandwidth of each stage, because the gain drop in the passband of each amplifier will accumulate. For instance, the overall 3dB bandwidth and the GBW of an amplifier made by cascading *N* similar single-pole amplifiers with gain A_v and bandwidth $\omega_\circ$ with no mutual loading is:

$$\omega_{overall} = \omega_\circ \cdot \sqrt{\sqrt[N]{2} - 1} \tag{4.7}$$

$$GBW = A_v^N \cdot \omega_{overall} . \tag{4.8}$$

Compared to the single-stage gain-bandwidth product, $A_v\omega_\circ$, there is a gain-bandwidth improvement of[1]:

$$\frac{GBW_{multi-stage}}{GBW_{one-stage}} = A_v^{N-1} \cdot \sqrt{\sqrt[N]{2}-1}\,. \tag{4.9}$$

For instance, $N=2$ and A_v=10 correspond to a factor of *6.4* improvement in GBW. For larger A_v, GBW will increase dramatically by introducing additional single stages at the price of increasing overall power consumption.

In practice, each stage has a loading effect on its previous stage, which reduces its bandwidth, hence reducing the overall bandwidth. The matching networks introduced in Section 4.2.1.2 can reduce the loading effect by separating the output of an amplifier from the input of its next stage. One disadvantage of multi-stage amplifiers, in general, and multi-stage amplifiers with two-port matching networks between each stage, in particular, is excessive phase shift that each amplifier stage or each network adds to the signal path, which can result in instability in *feedback* amplifiers.

4.3 Design Methodology

Based on the discussions in the previous section, for a given wideband amplifier one can add passive matching networks at the input and output, as well as between the gain stages of the amplifier to enhance the bandwidth. This method brings each stage of the amplifier closer to its theoretical limit discussed in Section 4.2. The networks absorb the capacitive parasitic components of the gain stages (transistors) and/or the source and load into their structure. Each network can be designed as a *low-pass filter* structure with standard response [23][89]. To achieve a particular response shape for each network (*e.g.*, maximally flat group delay) the components in the passive network take the same values as their corresponding element in the filter.

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[1] The overall GBW will actually improve if $A_v > (\sqrt[N]{2}-1)^{\frac{-1}{2N-2}}$.

In this approach one can resort to passive networks with *low sensitivity* to component values such as ladder structure [99]. Figure 4.4 shows a general low-pass ladder structure inserted between two gain stages in an amplifier. The component values are generated using standard look-up tables [97] or network synthesis methods [98]. The network order, N, is an additional design parameter. Using higher-order networks will provide wider bandwidth and sharper transition from passband to stopband. However, it may cause some practical issues, such as unreasonable component values, large numbers of passive components (large die area), and additional signal loss due to passive components (primarily inductors). Typically these issues limit the order of the network to *five*, *i.e.*, only three additional passive components.

Design Example: Here, we show the procedure for designing a maximally flat response 3rd-order passive network as an example. Figure 4.5(a) illustrates the two stages of a given amplifier with an inductor inserted between them. Figure 4.5(b) demonstrates that the inductor forms a 3rd-order ladder structure with C_1 and C_3, transistor parasitic capacitances. The values for R_1, R_2, C_1, and C_3 are known for the amplifier. To achieve a maximally flat frequency response at the output of the ladder, components values should be equal to their corresponding 3rd-order Butterworth filter elements as follows [98]:

$$C_1 = \frac{1}{R_1(1-\delta)\omega_c} \tag{4.10}$$

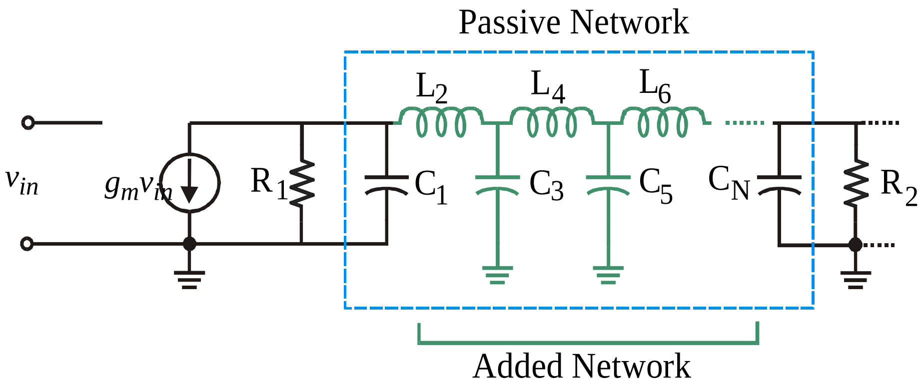


Figure 4.4: Passive ladder structure of order N, inserted between the gain stages

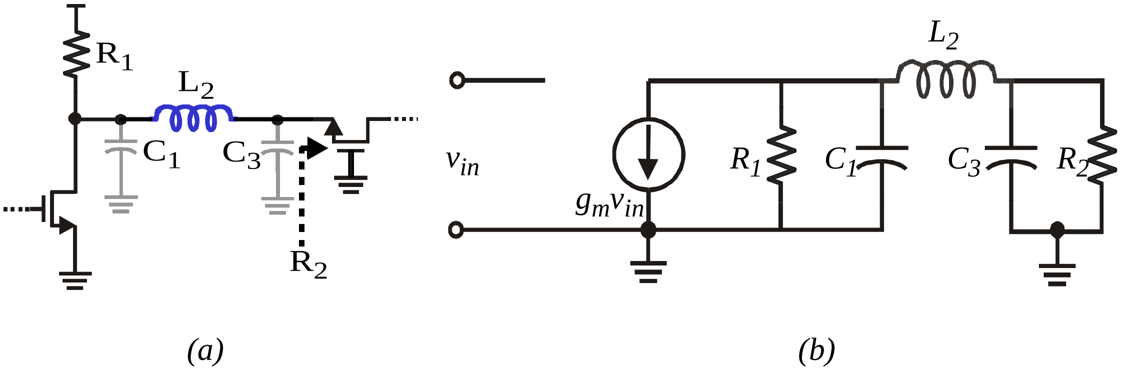


Figure 4.5: (a) An inductor is inserted between two gain stages. (b) The small signal model shows formation of a 3rd-order ladder network

$$L_2 = \frac{2}{(1-\delta+\delta^2)\cdot\omega_c^2\cdot C_1} \tag{4.11}$$

$$C_3 = \frac{1}{R_2(1+\delta)\omega_c} \tag{4.12}$$

where δ is an indication of impedance transformation between R_1 and R_2 and is defined as

$$\delta = \sqrt[3]{\frac{R_1-R_2}{R_1+R_2}} \tag{4.13}$$

and ω_c is the 3dB cut-off frequency of the network. From (4.10) the new amplifier bandwidth at the output of the ladder structure is

$$\omega_{c,\,new} = \frac{1}{(1-\delta)\cdot R_1\cdot C_1}\,. \tag{4.14}$$

The inductor value can be calculated from (4.11) and (4.14). C_3 for the original amplifier may not be equal to the value with the new cut-off frequency, calculated from (4.12). Some explicit capacitance should be added to adjust for this. If we define the bandwidth enhancement ratio (*BWER*) as the ratio between the new 3dB bandwidth and the old one (without adding the inductor) of the single-stage amplifier, we can show:

$$BWER \equiv \frac{\omega_{c,\,new}}{\omega_{c,\,old}} = \frac{1}{1-\delta} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{C_1 + C_3}{C_1}. \tag{4.15}$$

Equations (4.10), (4.12), and (4.13) simplify (4.15) to an expression based on the ratio of R_1 and R_2. BWER decreases monotonically when R_2/R_1 increases. For a given amplifier with $R_2<R_1$, adding the inductor always enhances the bandwidth by BWER. When $R_2=R_1$, BWER=1 and there is no bandwidth enhancement with adding the inductor. However, a maximally flat pass band and sharp cut-off response is still achieved.

The same analysis can be applied to the input stage of a trans-impedance amplifier (TIA) as shown in Figure 2.21. The photodiode is modelled by a current input in parallel with a capacitance, C_{PD}, as shown in Figure 4.6. Although R_1 is eliminated from the model, design calculations using (4.10)–(4.14) can use an arbitrary value for R_1. An optimum value for R_1 can be computed from (4.14) with fixed C_1 (C_{PD} in this case) and R_2, to maximize the 3dB bandwidth. It results in $R_1 = 2.05R_2$ with $\delta = 0.7$. After designing the inductor and adjusting for C_3, R_1 can be eliminated. Essentially, the trans-impedance gain will increase as no portion of the input current is absorbed by R_1 anymore. The enhancement ratio should also be modified for the input passive structure as:

$$BWER = \frac{1}{1-\delta} \cdot \frac{R_2}{R_1} \cdot \frac{C_{PD} + C_3}{C_{PD}} = 1.63 \cdot \left(1 + \frac{C_3}{C_{PD}}\right). \tag{4.16}$$

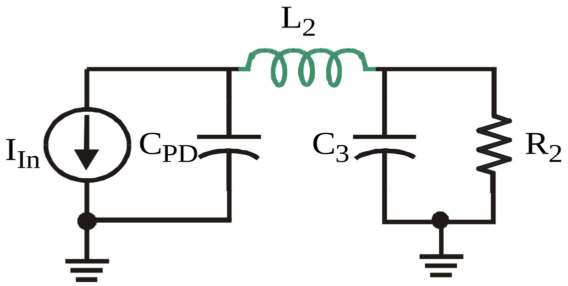


Figure 4.6: The inductor at the input forms a 3rd-order ladder network with the photodiode capacitance

The preceding example can be generalized to any response shape when (4.10)-(4.12) are replaced with their corresponding filter component equation. (4.15) and (4.16) should also be modified to correspond to the new component values.

4.4 Example Design

To demonstrate the effectiveness of the developed methodology, a CMOS trans-impedance amplifier (TIA) is designed. It is a single-ended design consisting of three gain stages. The first stage is a shunt-shunt feedback trans-impedance stage as Figure 4.7 shows. The input resistance of the amplifier is approximated by $R_f/(A+1)$, where A is the inverting voltage gain. Thus, the stage can provide a low input impedance and reduce the dominant effect of the input pole due to the large photodiode junction capacitance, C_{PD}. The input pole frequency can be written as:

$$P_{in} \approx \frac{1}{R_{in} \cdot (C_{PD} + C_{in})} \approx \frac{A}{R_f \cdot (C_{PD} + C_{in})} \tag{4.17}$$

where R_{in} and C_{in} are the input resistance and input capacitance, respectively. For the circuit in Figure 4.7, if the transistors are in short channel region, both C_{in} and A are proportional to the input transistor width, W_{in}:

$$A \approx g_m \cdot R_L \approx v_{sat} C_{ox} W_{in} \cdot R_L \tag{4.18}$$

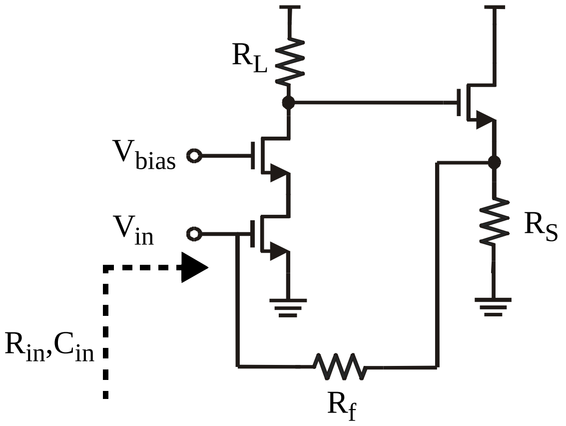


Figure 4.7: Schematic of the input stage of the TIA

$$C_{in} \propto C_{ox} L_{in} W_{in} \tag{4.19}$$

where C_{ox} is the gate oxide capacitance, v_{sat} is the carrier saturation velocity, and L_{in} is the input transistor channel length. When the input width increases there is a bound for the input pole dominated by C_{in}. However, additional constraints such as power consumption or input noise set an optimum width for the input transistor [101]. Adding the additional inductor to isolate C_{in} and C_{PD} enhances the bandwidth according to (4.16). In this design we match the input resistance to our electrical measurement setup, which had a 50Ω input resistance.

The complete schematic of the circuit including the added passive components is shown in Figure 4.8. The second and third stages of the amplifier are designed as cascode configuration with intermediate inductors and are isolated using a source follower buffer. Adding the source follower avoids the large input capacitance of the 3rd-stage amplifier to load the 2nd stage as well as providing a low impedance node at its output and increasing its pole frequency.

Four passive networks are inserted between the stages of the amplifier to enhance the bandwidth. The input network separates the photodiode capacitance and the parasitic capacitance of the input stage. Adding one inductor will transform it to a 3rd-order ladder structure. The next two networks are also 3rd-order and are placed between the cascode

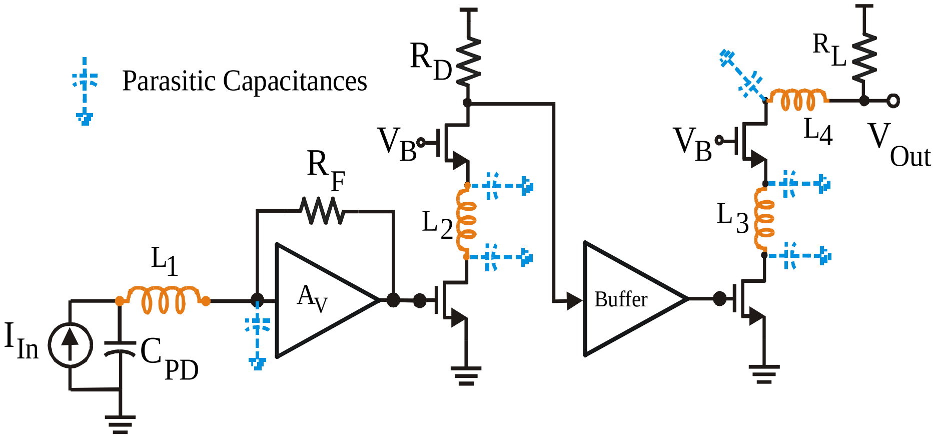


Figure 4.8: Schematic of the TIA with parasitic capacitances and additional inductors

transistors. The load capacitance in conjunction with the output capacitance (including bonding pad) and output bondwire inductor form the output 3rd-order network.

The capacitors, as shown with a dotted line in Figure 4.8, are the parasitics from the devices and only four inductors are added to the original circuit. The input and output inductors are bondwire inductors and the inter-stage ones are on-chip spiral inductors. A final optimization step in simulation is performed to include the bilateral effects of the devices. Note that the output network is different from a conventional shunt-peaking approach. For a photodiode capacitance of 0.5pF, the circuit achieves over 9GHz 3dB bandwidth in simulation. This is *2.4 times* larger than the bandwidth achieved using the same circuit without the inductors. The individual effect of each passive network and the effect of a combination of them are summarized in Table 4.2 from simulation results.

Table 4.2: Comparison of the individual effects of the inductors on BWER

Additional Inductors	**BWER**
no inductor	1
L_1 only	1.48
L_2 only	1.42
L_3 only	1.62
L_4 only	1.17
L_1, L_3	2
L_1, L_2, L_3	2.3
All	2.4

L_3 causes the largest improvement in bandwidth because the device sizes of the second cascode amplifier are large to drive 50Ω with a minimum loss of gain. L_1 is separating the two large capacitances that form the input pole frequency. In our design, this pole is the dominant bandwidth limiting factor of the core TIA without a driver. L_4 is not remarkably enhancing the bandwidth because the output pole is not dominant. However, L_4 will exist in the circuit as the bondwire and should be modeled. All four passive networks have a ladder structure for lower sensitivity to process variations.

Both on-chip inductors were implemented as spiral inductors in the top metal layer. Accurate electromagnetic modeling of the inductors was done using ASITIC [102] and SONNET [103] E&M simulators and gave similar results. The parasitic capacitances of the inductors are not negligible, and their impact is considered in addition to device parasitics.

4.5 Experimental Results

The trans-impedance amplifier was implemented in a 0.18μm BiCMOS process technology using *only* CMOS transistors. It draws 55mA from a 2.5V power supply. The scattering parameters were measured with a 20 GHz HP8720B network analyzer. Assuming matched output, it can be shown that the complex TIA trans-impedance, $Z(j\omega)$, can be extracted from this measurement using:

$$Z(j\omega) = \frac{Z_\circ \cdot S_{21}}{1 - S_{11} + Z_\circ \cdot j\omega C_{PD}(1 + S_{11})} \tag{4.20}$$

where $Z_\circ = 50\Omega$ is the reference impedance and C_{PD} is the photodiode capacitance. The amplitude and group delay response of the implemented TIA, extracted from measurement data, are shown in Figure 4.9(a) and Figure 4.9(b), respectively, when $C_{PD}=0.5pF$. Matched output will cause a 6dB drop in the gain, which is adjusted for in the reported result. Group delay is calculated from the phase response of the amplifier and logarithmic frequency steps of the network analyzer.

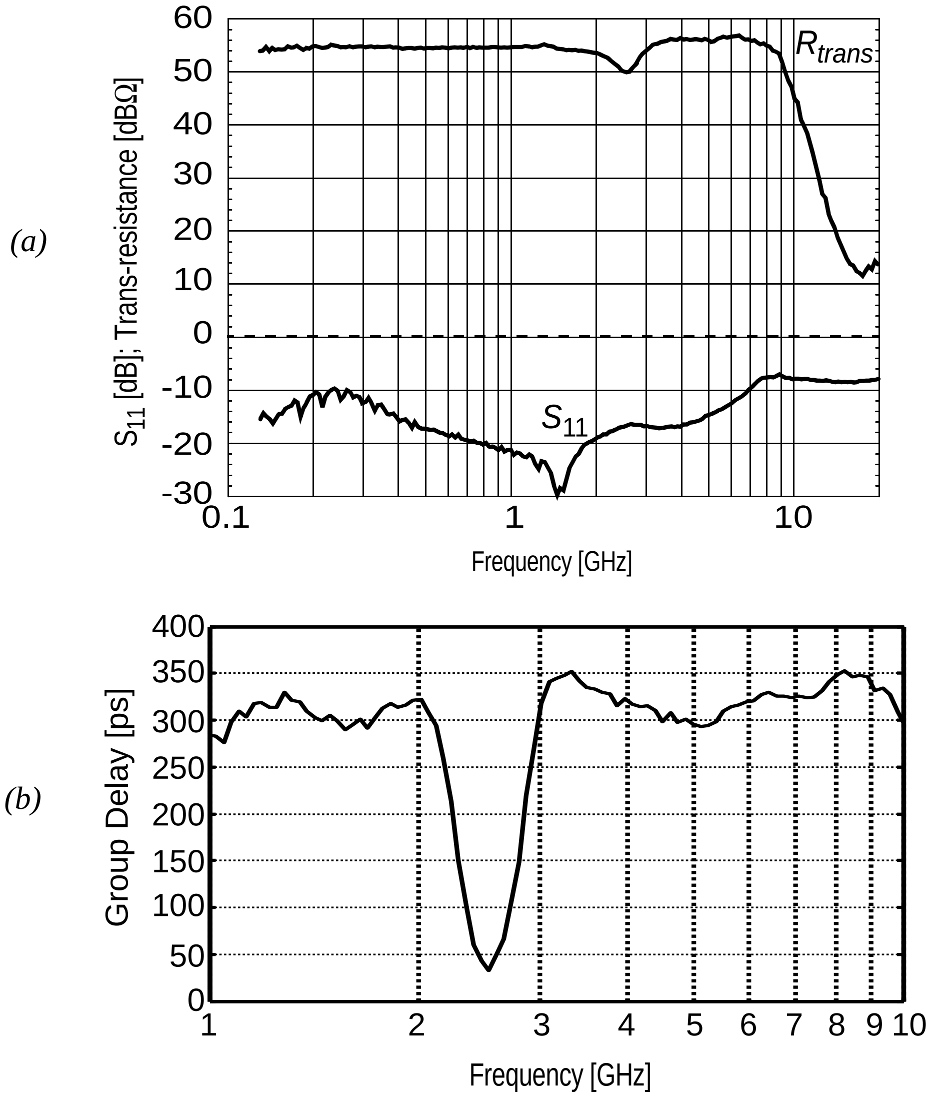


Figure 4.9: (a) Trans-resistance gain of the TIA with 0.5 pF photodiode capacitance and the input matching. (b) Group delay response of the TIA

The 3dB bandwidth is 9.2 GHz, which is in good agreement with the simulations, and the trans-impedance gain is 54 dBΩ. The input reflection coefficient, S_{11}, remains below -10 dB up to 7 GHz. Although we did not design for flat group delay, the group delay ripples are $\pm 25ps$. The dip in the frequency response of the trans-impedance at 2.5 GHz can be correlated to a resonance mode between the on-chip supply by-pass capacitor and bondwire and supply line inductances. Changing these parameters changes its depth and

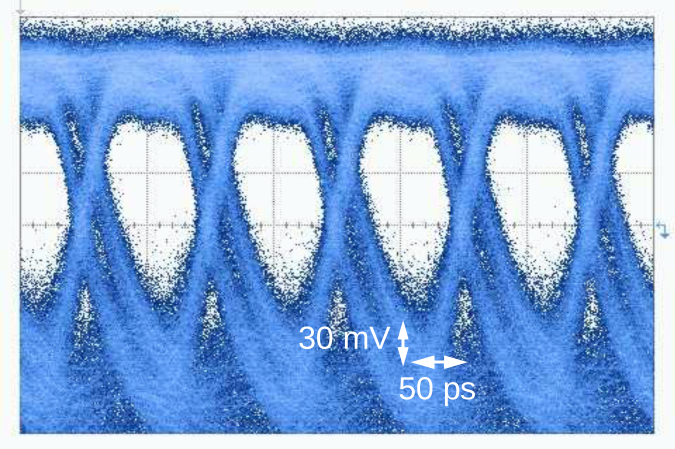


Figure 4.10: Eye diagram of the TIA output with 10GB/s 2^{31}-1 PRBS at the input

frequency during the measurement and can be removed by using a different supply by-passing technique in a revised version of the design. The design has low sensitivity to inductor values. The simulated values for L_1 and L_4 are 0.5–0.6nH. L_2 and L_3 are 1nH 100x100 μm^2 spiral inductors.

Figure 4.10 shows the eye diagram when a 2^{31}-1 pseudo random bit sequence is applied to the input at 10GB/s. The ringing is partly due to the resonance mode at 2.5 GHz and partly due to the absence of the photodiode capacitance that will cause peaking in the overall transfer function. This peaking translates to a ringing response in the time domain and will increase the ISI penalty and close the eye vertically. However, the TIA still achieves the overall sensitivity of -18dBm for BER, which is better than 10^{-12} as we discuss next.

The electrical sensitivity of the amplifier for different bit error rates (BER) is measured using Antrisu’s MP1763C and MP1764C BERT system. A 2^{31}-1 pseudo random bit sequence is applied to the input at 10GB/s, and the BER is measured for different electrical input powers at 500-second intervals. The results are depicted in Figure 4.11. For a data communication link, the required BER is typically 10^{-12}. The TIA achieves a sensitivity of -18dBm or 15.8μW for this BER when photodiode capacitance is not present. At very low power inputs we were limited to the sensitivity of the BERT system.

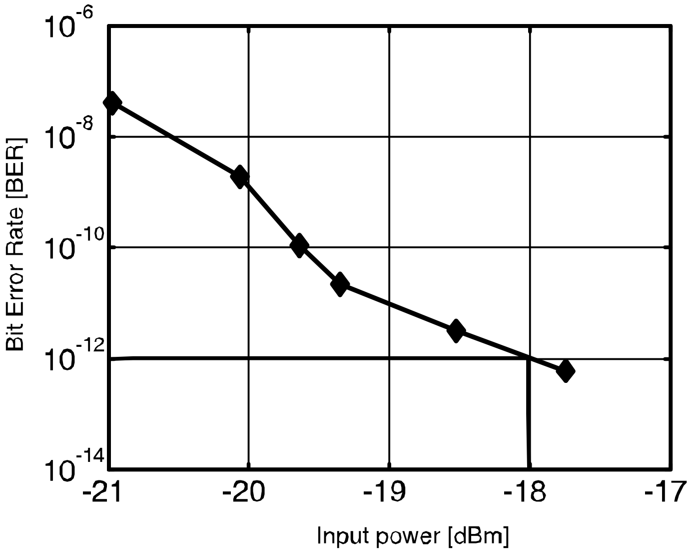


Figure 4.11: The BER of the TIA for different input powers at 10GB/s

The TIA output swing was not large enough to meet the minimum requirement of the BERT input.

Simulated total input noise current of the TIA, integrated over the bandwidth, equals 1.6μA. In an optical receiver, there are two other noise sources that contribute to increase the minimum-detectable optical power. One is the intensity noise of the transmitted signal originating mainly from spontaneous emission of the laser source [43]. Resulting current noise at the receiver input can be quantified as

$$i_{t,\,rms} = R \cdot P_{in} \cdot RIN \tag{4.21}$$

where R is the responsivity of the detector, P_{in} is the input optical power, and RIN is the relative intensity noise of the laser integrated over the bandwidth. Second noise source is the shot noise of the photodetector that is generated proportionally to the optical power given by [43]

$$i_{s,\,rms} = \sqrt{2q(R \cdot P_{in} + I_{dark}) \cdot \Delta f} \tag{4.22}$$

where q is the electron charge, I_{dark} is the dark current of the detector, and Δf is the system bandwidth. From (4.21) and (4.22) we can compare the injected noise currents and deter-

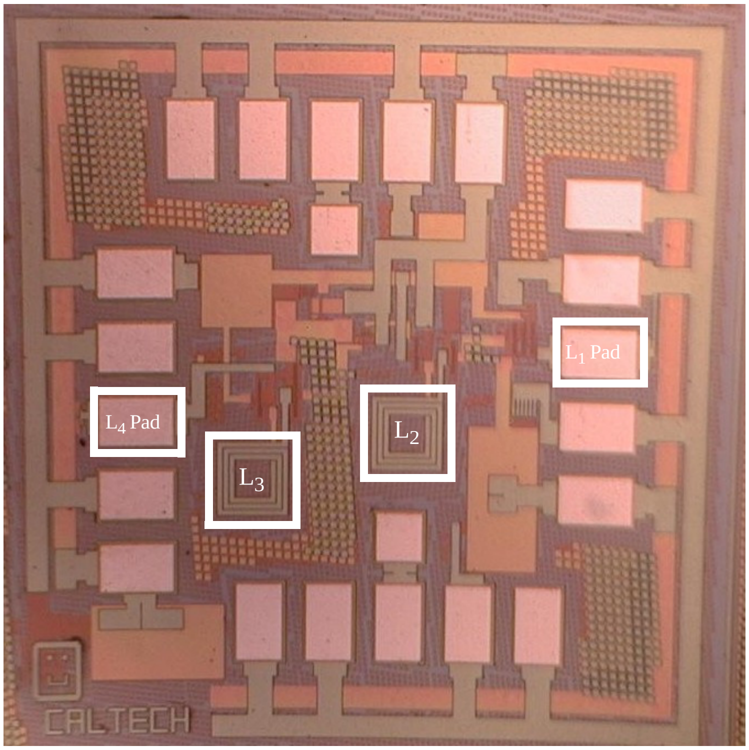


Figure 4.12: The die photograph of the 9.2 GHz TIA

mine the dominant noise source. Assuming peak $RIN/\Delta f = -130 dB/Hz$ for a typical laser and a detector with $R=0.8A/W$ and $I_{dark}=10nA$, minimum input optical power of $P_{in}=20\mu W$ will result in $i_{t,rms}=0.014\mu A$ and $i_{s,rms}=0.22\mu A$ ($\Delta f=9.2GHz$). Therefore, the thermal noise of the TIA is the dominant noise source of the receiver, and we expect that the optical sensitivity and the electrical sensitivity of the TIA are comparable. The amplifier core occupies $0.8 \times 0.8mm^2$ of area, as shown in Figure 4.12.

4.6 Summary

In this chapter, we studied wideband amplifier design for the front-end of high-speed wireline links. We addressed the gain-bandwidth product (GBW) limits of amplifiers and introduced a methodology that can be used to enhance the bandwidth of wideband amplifiers with specified characteristics for their transfer functions. In a simple design procedure, parasitic capacitances of transistors can be absorbed into passive networks, inserted between the gain stages. The component values can be calculated based on standard low-pass filter structures. A prototype CMOS TIA implemented using the developed technique achieves over 9 GHz bandwidth and 54dBΩ trans-impedance gain in the presence of a 0.5pF photodiode capacitance.

Chapter 5

Eye-Opening Monitor for Adaptive Equalization

5.1 Introduction

In Chapters 2 and 3, we discussed how the channel and receiver front ends of a high-speed wireline communication system degrade received signal quality by adding ISI and jitter. In Chapter 4, we provided a bandwidth enhancement method that can be utilized in the design of the receiver front-end. To minimize the ISI caused by the channel response we can use an equalizer (Section 2.3.4*)*. For instance, Wu *et al.* [48][104] and Reynolds *et al.* [49] have demonstrated significant bit error rate (BER) reduction by using transversal filter equalizers in the receiver front-end of multi-mode fiber links to compensate for modal dispersion.

When the channel response is initially unknown or if it may vary over time, an adaptive equalizer is used in which the transversal filter coefficients are adjusted automatically and continuously to track channel response variations. Since the adaptation is an iterative process, a feedback mechanism is required to measure and report the signal quality at the equalizer output. In this chapter, we propose an eye-opening monitor (EOM), which is a circuit block that reports a quantitative measure of the quality of the signal eye diagram and thus can be used as such feedback.

Figure 5.1 shows the block diagram of a transversal filter adaptive equalizer that uses an EOM circuit. The EOM evaluates signal quality by making periodic observations of the filter output and providing information about the filter performance to an optimization algorithm. The algorithm updates all of the filter coefficients accordingly. This architecture is desirable if the transversal filter is implemented using broadband passive

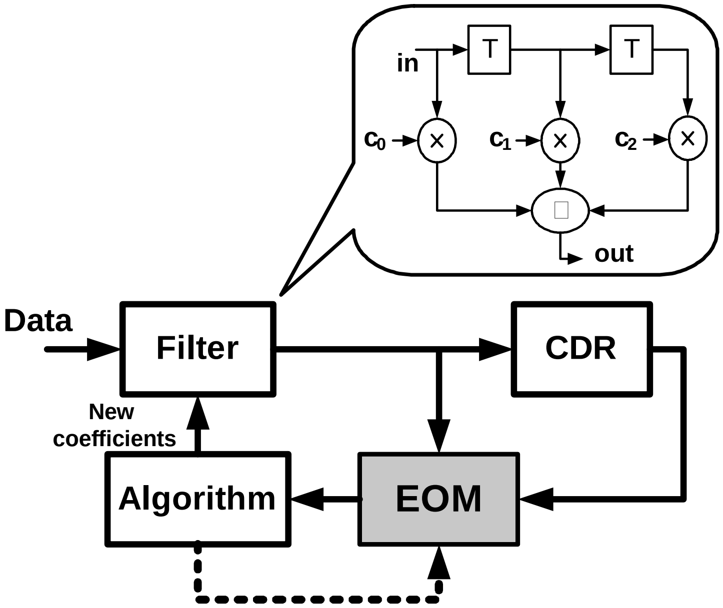


Figure 5.1: Adaptive transversal filter equalizer with an eye-opening monitor (EOM)

delay lines, *i.e.*, LC networks [48][49][104] or active delay elements [80]. At multi-Gb/s data rates, the passive or active delay cells become more sensitive to on-chip parasitic components. In contrast to conventional LMS adaptive equalization (Section 2.3.4), when an EOM-based adaptive equalizer is used, the nodes of the delay cells of the filter are not loaded by additional hardware for adaptation circuitry. Therefore, the filter can be designed as a separate module and its response remains intact. The other advantage of the EOM-based architecture is that the cost function for the coefficient optimization is only based on the filter output and is independent of the receiver decision on the symbols. This is specially beneficial in links where training sequences are not used for adaptation and most decisions are erroneous at the startup when BER is high. The EOM can also be utilized as a standalone measurement system to verify the quality of the eye.

5.2 Prior Art

The received signal quality in a communication link and the shape of its eye diagram are strongly correlated [16][17]. Therefore, eye diagram monitoring has been proposed as a technique for extracting information about the received signal [105]–[108] and is used in various applications including adaptive equalizers. George [109] and Hogge [110] both introduced eye monitor hardware that are used as pseudo-error detectors [105][111] for rapid estimation of low BER. The estimation is based on evaluating the eye diagrams by comparing them against a fixed rectangular eye-opening mask. Shin *et al.* [112] use an eye monitor to perform a pass/fail test on fiber optic channels. They also use a fixed rectangular mask overlapped with the eye diagram and count the number of eye traces inside it. If it is more than a given threshold the channel has failed and another stand-by fiber channel is selected. Various signal performance monitors have been proposed [113]–[116] to adaptively adjust the decision threshold level of the receiver. For instance, in [114] and [115] the approach is to fit a rectangular mask with a fixed width to the eye and to adaptively adjust its height to keep the number of eye traces occurring inside the mask constant. The traces above and below threshold (representing “1” and “0” bits) are counted separately to capture unbalanced eye shapes. The threshold is set to the center of the rectangular mask.

Eye-opening monitor circuits have also been utilized as part of adaptive equalizers [117]-[125] mainly to mitigate various dispersion issues in optical fibers. In [120] the eye monitor estimates the vertical eye opening at the sampling point. The receiver includes a path parallel to the main path that embraces a decision circuit with a variable decision threshold. The threshold is varied to sweep the eye vertically. The decision of the two paths are compared and an error is recorded if they differ. When the error is integrated over time for various thresholds, the eye vertical opening for a given error rate can be estimated from the separation of the thresholds that resulted in that error rate. Ellermeyer suggests a circuit for estimating the horizontal eye opening of the input signal [118][119].

A rectangular mask with fixed height is overlapped with the input eye. The width of the mask is increased as long as eye traces do not occur inside it and is decreased otherwise. In steady state, the mask width indicates the horizontal eye opening.

We propose an EOM circuit architecture that has a unique feature of mapping *both* the vertical (amplitude) and horizontal (temporal) opening of the received eye to a two-dimensional error diagram [28]. The error diagram is directly correlated to the eye opening in both dimensions and is essentially the captured image of the signal eye diagram. The output error rate is recorded with a digital counter as opposed to an accumulated or integrated format. This is advantageous when the eye monitor is in a feedback loop with a microcontroller that runs the optimization algorithm because error is recorded in finer resolution and potentially has larger dynamic range. We have implemented a prototype of this 2D EOM circuit in 0.13µm standard CMOS technology, and we have verified its operation up to 12.5Gb/s.

In the following sections, the operation principle of the EOM is discussed first. Then, the architecture and details of the associated circuit blocks are presented. Finally, the experimental techniques for verifying the operation of the prototype and the measurement results are described.

5.3 EOM Principle of Operation

The EOM characterizes the opening of an eye diagram by an eye mask. The eye is overlapped by several rectangular masks with various sizes and aspect ratios. Any eye trace, *i.e.*, data transition, that passes inside a mask is counted as an error. For a given mask, if the EOM runs for a sufficiently long time, some data transitions will eventually fall inside the mask and create an error even for an apparently good eye diagram. This is because random jitter and amplitude noise often have unbounded distributions. A *mask error rate* (MER) can be defined as the number of data transitions that fall inside a given

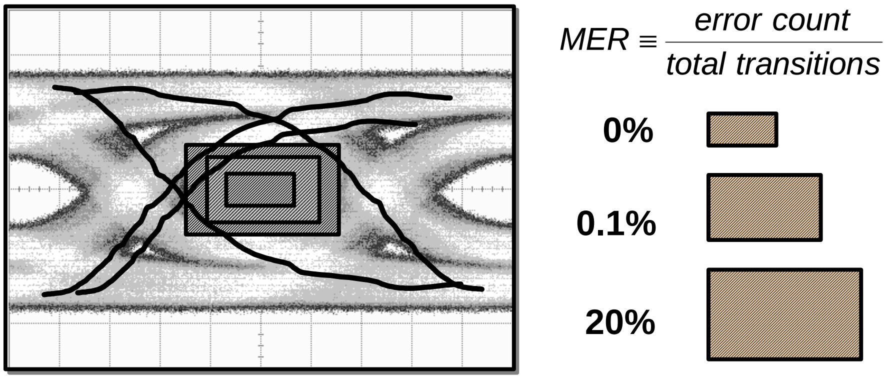


Figure 5.2: The mask error rate (MER) varies for different mask shapes in a given eye diagram

mask normalized by the total transitions during the same time period. Figure 5.2 illustrates an example where MER is obtained for three different masks in a given eye diagram. Any given mask is associated with a MER that increases as the quality of the monitored eye degrades. The horizontal and vertical opening of an eye can be determined from the mask size for a specific MER. Moreover, different eye diagrams can be quantitatively compared by comparing their associated mask sizes at a given MER. The eye that can fit a larger mask for the given MER is more desirable.

A significant feature of a 2D eye-opening monitor is that it can capture eye diagram shapes with irregular and non-rectangular openings that are common in high-speed links. In such a case a rectangular mask shape might not be the optimum choice for comparing eye openings because the non-zero rise time and fall time of data transitions constitute a large portion of the bit period and form a rounded diamond eye opening. A 2D EOM can generate rectangular masks of different size in both horizontal and vertical dimensions. For a given eye diagram, a group of masks with different aspect ratio can have the same MER. Figure 5.3 demonstrates an example of a typical eye diagram shape overlapped with three masks. All the masks result in MER=0. The combined area inside the eye that covers all the masks with the same MER is defined as the *effective eye opening* at that MER. This effective eye opening is not necessarily rectangular and contains more realistic

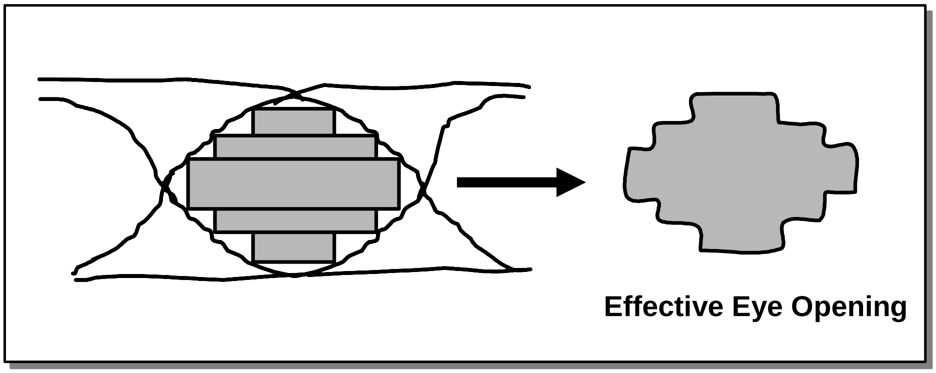


Figure 5.3: The *effective eye opening* formed by combining the mask areas that have the same MER

information about the shape of the eye. The EOM architecture in this design can measure the effective eye opening for different MER values. The aggregate of effective eye openings is a 2D error map that covers the eye diagram completely and is a representation of the shape of the eye as Figure 5.4 illustrates hypothetically.

The MER for a given mask is found from counting the errors, *i.e.*, the number of data transitions that cross either of the two vertical sides of the mask. The operation is demonstrated in Figure 5.5. Two reference voltages, V_H and V_L, define the vertical opening of the mask, and the two phases of the sampling clock, ϕ_{early} and ϕ_{late}, determine its horizontal opening. Data is continuously compared with V_H and V_L, and these results

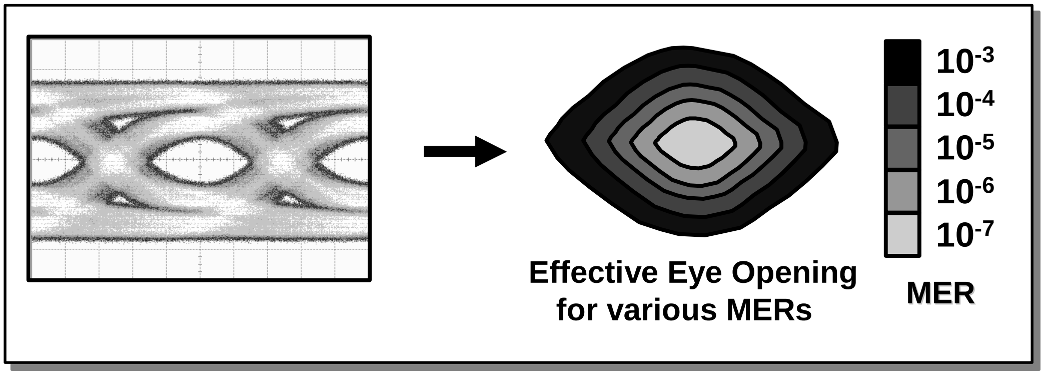


Figure 5.4: The combination of effective eye openings is a 2D error map that is correlated to the shape of the eye diagram

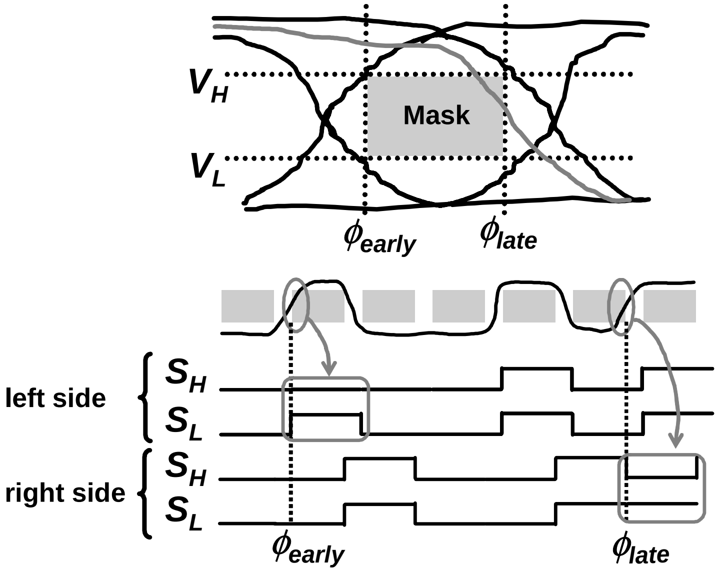


Figure 5.5: Operation principle of the EOM for one mask

are sampled at both early and late phases. At each phase, if the sampled values differ, a mask violation has occurred and an error is flagged. The error detection logic is $error = S_H \oplus S_L$, where S_H and S_L are sampled comparison results for either of the phases, *i.e.*, either side of the mask, and the operator is XOR. The timing diagram in Figure 5.5 illustrates one violation for each side of the mask. If the errors of the left (from ϕ_{early}) and the right (from ϕ_{late}) sides of the mask are counted separately, horizontally assymetrical eye diagrams can be captured effectively. We have added this capability to the architecture by providing two independent error detector blocks for two sides of the mask.

5.4 EOM Architecture

Figure 5.6 shows the proposed architecture of the EOM circuit. Differential input data is compared with differential reference levels in two comparators. The lower comparator reference is generated by swapping V_H and V_L [118][126]. The reference levels can be adjusted either through an on-chip DAC or externally. The DAC sets $V_H = V_{cm} + n\Delta V$

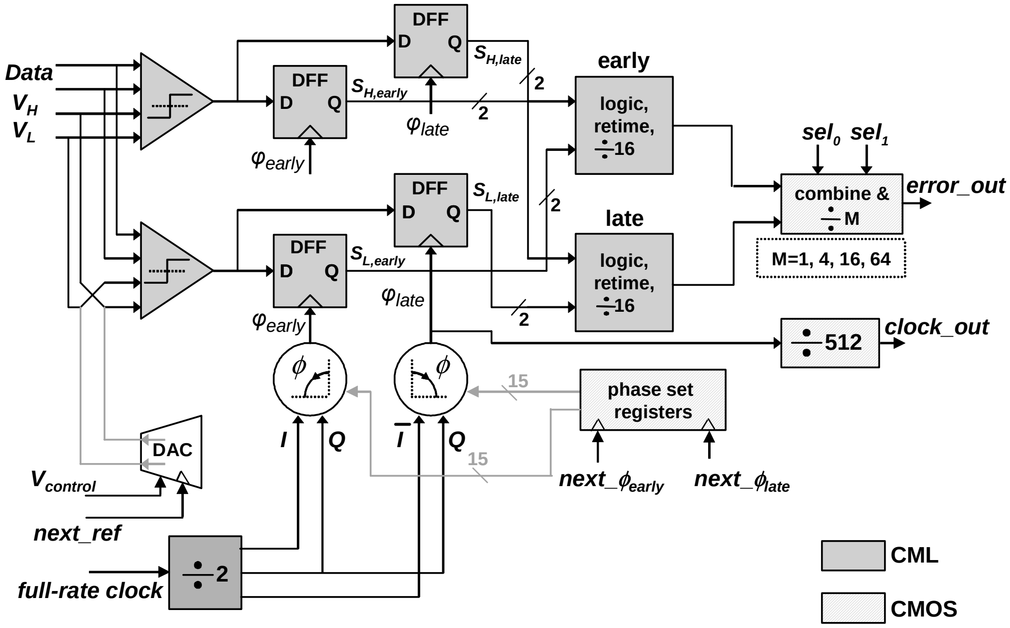


Figure 5.6: The EOM architecture

and $V_L = V_{cm} - n\Delta V$, where V_{cm} is the input common mode and $1 \le n \le 7$. Every positive edge on *next_ref* triggers a reference-set shift register that increases *n* by one. The eighth edge resets *n* to 1. The step size, ΔV, is adjustable externally. The comparators' outputs are sampled at both early and late phases by the D-flip flops (DFF) that follow the comparators. The sampling clocks are half-rate and thus each DFF block consists of two master-slave DFFs to sample at both rising and falling edges of the clocks. This avoids skipping any data transitions. The samples from early and late phases are processed separately in two independent logic blocks. From discussions in Section 5.3, this allows the EOM to differentiate data transitions that cross the left side of the eye mask from those that cross the right side and enable it to capture asymmetrical eye diagrams. In our prototype implementation we have combined the early and late errors to only one *error_out* signal due to test equipment limitations. However, asymmetric eye shapes can still be captured by triggering the early or late sampling phases one at a time.

In each logic block for early or late phases, the errors due to rising and falling edge samples are detected, retimed, and merged. The errors are detected for the edges separately by independent XOR gates. Then the error signals from the falling sampling edge are re-sampled at the next rising edge to align the two error signals in time. Then, they are merged by a logic OR function. The merged error signal is divided down by a factor of 16 using CML logic. This allows the use of low power CMOS logic for the dividers in the subsequent stages. Finally, the two error signals from the ϕ_{early} and ϕ_{late} are retimed by the early sampling phase and are combined. The error output passes through a digital divider with four selectable divide ratios. A larger divide ratio is selected in order to measure cases with high-error counts. The chip output, *error_out* signal, is a toggling output. MER for a fixed mask size can be calculated from the frequency of *error_out* signal, f_{error}, as

$$MER = \frac{N \cdot f_{error}}{BR}, \qquad (5.1)$$

where N is the total divide ratio in the chain and BR is the input bit rate. A separate divider chain is used to divide the late sampling clock, ϕ_{late}, by 512. The output is used to monitor the clock divider and phase rotator functionality and is also applied as a trigger signal during the chip test and characterization.

The sampling clocks are generated from an external full-rate clock that is divided by two with an on-chip divider to create half-rate I and Q phases. Two single-quadrant phase rotators interpolate between I and Q and between $\bar{I}$ and Q to create, respectively, ϕ_{early} and ϕ_{late}. Therefore, the output phase of each rotator covers a range of 90^{o} or half of the bit period as can be seen from the timing chart in Figure 5.7. Each rotator has a 15-bit thermometer-encoded control line that sets the phase interpolation weights and results in a phase step of 6^{o}. The control-line value for each rotator is determined by a phase-set shift register. The trigger signals of the shift registers that increment the control lines for ϕ_{early} and ϕ_{late} are *next_*ϕ_{early} and *next_*ϕ_{late}, respectively. When both control lines are set to zero, ϕ_{early} and ϕ_{late} have the same phase as Q and overlap in the center of the eye. Every positive edge on *next_*ϕ_{early} moves ϕ_{early} one step to the left. Similarly, every positive edge

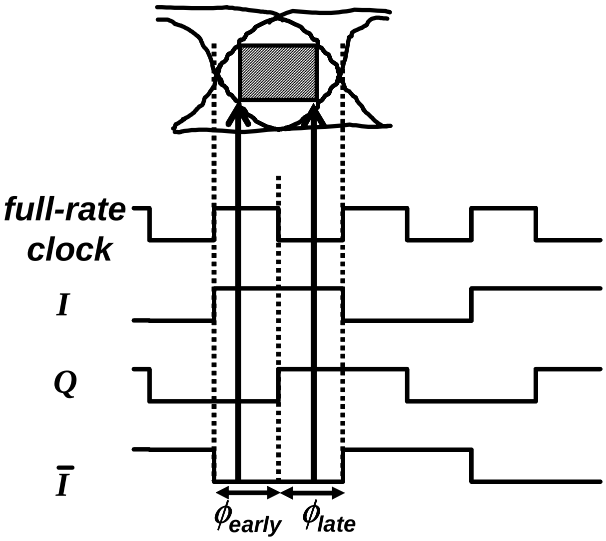


Figure 5.7: Generation of ϕ_{early} and ϕ_{late} by phase interpolation

on the *next_*ϕ_{late} moves ϕ_{late} one step to the right. The 16th positive edge on either *next_*ϕ_{early} or *next_*ϕ_{late} automatically resets the phase to the center (Q) position.

By separately stepping the *next_*ϕ_{early}, *next_*ϕ_{late}, and *next_ref* trigger signals, the architecture provides three degrees of freedom for obtaining several rectangular mask sizes in both horizontal and vertical dimensions. Seven settings for the differential reference voltage DAC and 15 for each phase rotator provide 210 different masks. The number of masks can be increased by applying reference voltages externally with a smaller step size. The MER increases as the mask size expands in either dimension. The EOM can be utilized in two ways. Mask expansion can be stopped at a threshold MER to report the eye opening or all masks can be swept to capture the full error map that represents the effective shape of the eye diagram.

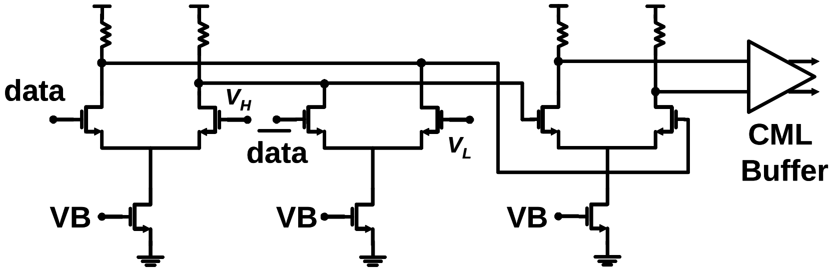


Figure 5.8: The differential comparator circuit

5.5 Circuit Implementation

The comparator circuits use a two-stage differential topology followed by a current-mode logic (CML) buffer, as in Figure 5.8. The first stage consists of two parallel source-coupled pairs [126]. The overall output of the stage is

$$v_o = g_m \cdot R \cdot [(v_i - V_H) - (\overline{v_i} - V_L)] \tag{5.2}$$

that can be rewritten as

$$v_o = g_m \cdot R \cdot [(v_i - \overline{v_i}) - (V_H - V_L)]\,. \tag{5.3}$$

The latter is the desired output for a differential comparator with differential reference voltage. The parameters g_m and R in both Chapter (5.2) and (5.3) are, respectively, the transconductance of one MOS transistor and the load resistor. Since the reference voltages V_H and V_L are stepped such that all the input swing range is covered by the vertical mask opening, each source-coupled pair must tolerate a wide range of common-mode input and thus needs a large CMRR. The second stage is also added to enhance the CMRR of the comparator and to increase its sensitivity. The tail current devices are designed longer than the minimum feature size to improve their output impedance and further enhance CMRR. The comparator is optimized to achieve maximum gain-bandwidth product. This maximizes the comparators' sensitivity and thus minimizes the degradation of the input eye diagram shape due to the EOM non-idealities. We will discuss the impact of EOM non-idealities on the eye opening in Section 5.6.

The comparator's offset is another limitation that affects the EOM operation by shifting the rectangular mask vertically. The input offset for each input source-coupled pair can be modelled by a shift in either of V_H or V_L in (5.2). Equivalently, the overall offset can be modelled as a constant term on the right-hand side of (5.3). In the absence of offset, the comparator maximum sensitivity is when $V_H = V_L$, and both are equal to the input common mode. With offset, the maximum sensitivity is when $V_H - V_L$ equals the amount of offset. This interpretation is used to de-embed the offset impact on MER measurements as will be shown in Section 5.6. In the implementation of the prototype we minimized offset by careful layout techniques to increase matching between transistors. We also avoided using low-V_t (MOS threshold voltage) devices for the input stage transistors of the comparator due to their poor V_t-matching property. Monte-carlo simulation of the comparator shows a mean output offset voltage of 6.4mV with worst-case value of 25mV. A CML buffer follows the second stage of the comparator to convert the output swing to proper levels for CML DFF blocks in the subsequent stages. The DFFs use standard master-slave topology with conventional CML latches and resistive loads. The clock divider is a static divider based on similar CML latches. We used low-V_t transistors in the latch circuit to enhance the latch switching speed.

The phase rotator circuit consists of a phase interpolator and a phase-set register that adjusts the proper interpolation weight. The phase interpolator is formed by two parallel differential stages, as Figure 5.9 shows. The differential input of each stage is connected to

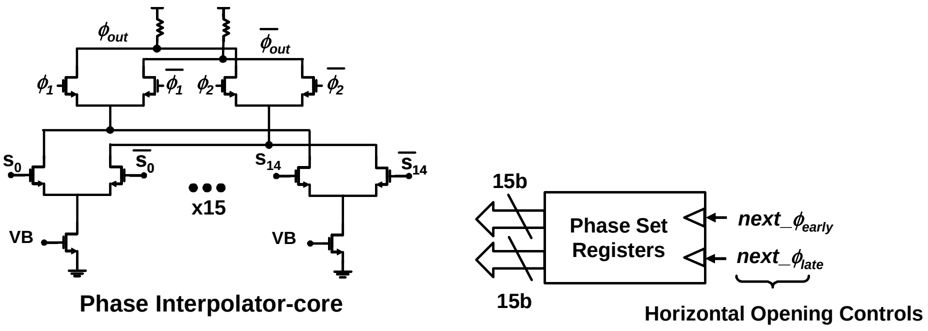


Figure 5.9: The phase interpolator and phase-set register

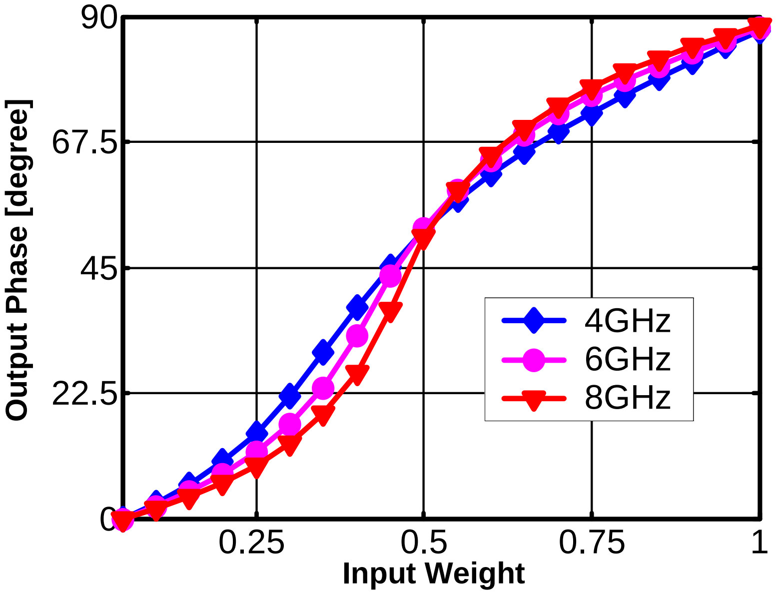


Figure 5.10: Simulated phase interpolator transfer function for different bandwidth

one of the two input phases. By properly adjusting the differential control lines, s_0-s_{15}, the tail current is steered between the two stages to set the input phases weights and obtain the desired interpolated phase. To generate uniform phase steps and thus uniformly sweep the mask horizontal opening, the transfer characteristic of the phase interpolator, *i.e.*, the relationship between output phase and input weight, should be linear. This characteristic can be controlled by the input signal transition slope and the bandwidth of the interpolator. Figure 5.10 illustrates the transfer function for three different bandwidths that is achieved by generalizing the approach in [127]. The phase interpolator is modelled by a bandlimited system that performs a weighted sum operation on two input signals. Although smaller bandwidths linearize the transfer function, they cause increased jitter because they reduce output signal transition slope and thus create more timing uncertainty due to amplitude fluctuation at the signal threshold-crossing point.

The reference-set register for the DAC, the phase-set registers for the phase rotators, and all the back-end dividers and the error combiner are implemented using CMOS standard cells in the technology to achieve lower power consumption.

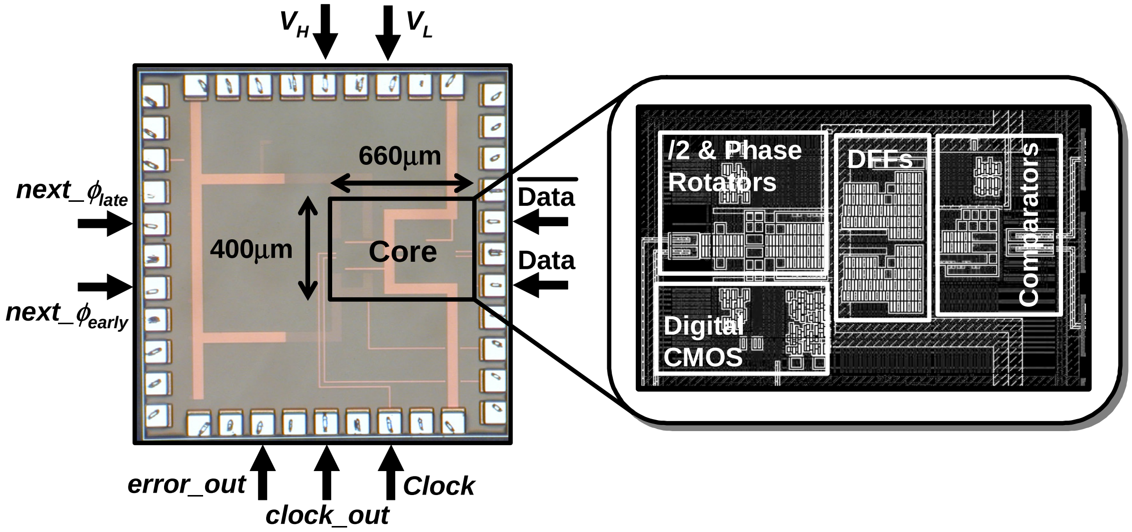


Figure 5.11: The die photograph of the EOM with magnified active core

5.6 Experimental Results

The EOM circuit was implemented in a 0.13µm standard CMOS technology. The die photograph, along with the layout of the active core, is shown in Figure 5.11. The chip is designed for a customized pad frame that enabled us to perform on-wafer testing. As a result, the die size is bounded to the pad frame and is 1.7x1.7mm^2. However, the active area of the EOM circuit that is highlighted on the die photograph is only 400x660µm^2. On-wafer measurements at up to a 12.5Gb/s input data rate with a 2^{31}-1 PRBS source and 1.2V power supply showed successful error diagram measurement. Tested input amplitude was from 50mVp to 400mVp. The chip consumes about 275mA from a 1.2V supply. It is functional at 10Gb/s with a supply voltage as low as 1V. It operates reliably even at severe input conditions when a closed eye with 10^{-2} BER is applied to the input. In the following, we elaborate on the test setup and experimental results.

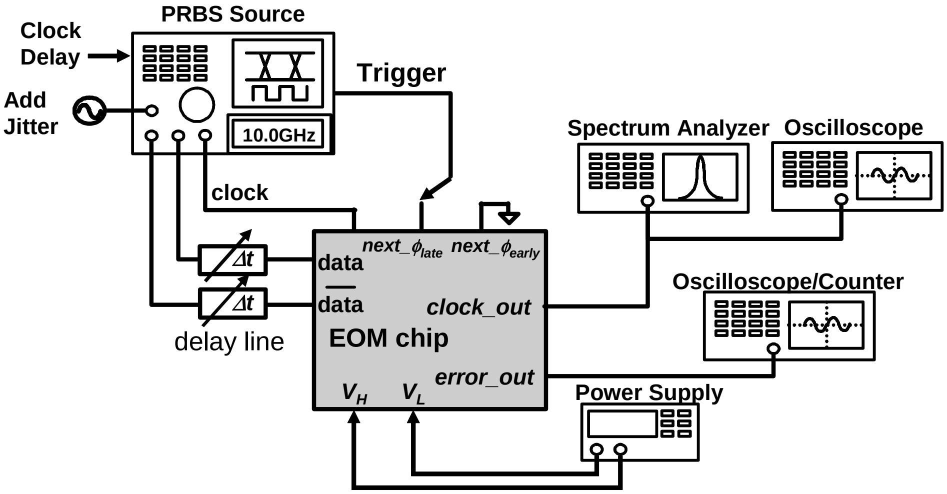


Figure 5.12: Measurement setup

5.6.1 Test Setup

The block diagram of our test setup is shown in Figure 5.12. A PRBS source provides the data and clock for a wide range of data rates up to 12.5Gb/s. The data source has an additional port that controls the amount of jitter added to the data artificially. Although the full rate clock phase is primarily phase-locked to data when applied to the EOM, the on-chip path difference does not preserve the phase relationship. In our measurements, we compensated the path delay mismatch by an external delay line. We adjusted the external delay to minimize the MER for the minimum size mask to guarantee that the mask is centered with respect to the eye. In the adaptive equalizer loop this calibration can be done once at start up, as the delay mismatch is a systematic effect. In addition, two external delay lines were used at the input path to compensate external cable mismatches and insure a 180^{o} phase difference between differential inputs.

The trigger signal for $next\_\phi_{early}$ and $next\_\phi_{late}$ are applied externally, and step horizontal opening of the mask. Similarly, vertical opening is controlled by varying V_H and V_L externally. A frequency counter records the average frequency of the *error_out* signal, from which MER can be calculated using (5.1).

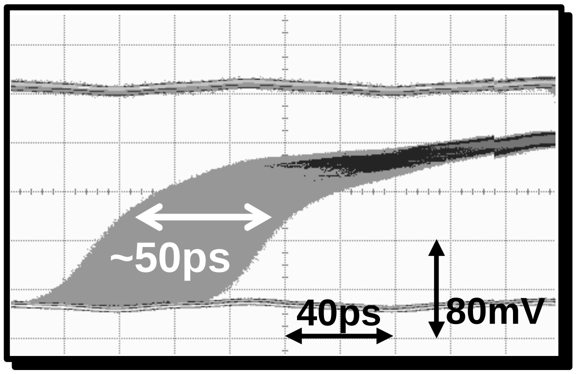


Figure 5.13: Accumulated phase of the *clock_out* signal that verifies functionality of the divider and phase rotator with 10GHz input clock

5.6.2 Clock Path

We first tested the functionality of the divider and the phase rotators by observing the *clock_out* output signal on the oscilloscope. Figure 5.13 shows the accumulated phases of the *clock_out* when a 10GHz clock is applied to the clock input. We trigger the $next\_\phi_{late}$ signal by applying a 3MHz square wave pulse. Although the standard-cell CMOS dividers slow down the clock transition, the accumulated phases correctly cover 50ps, which is equivalent to half of the bit period of a 10GB/s signal.

5.6.3 Qualitative Eye-Opening Measurement

The objective of this test is to verify the functionality of the main blocks in the data path of the EOM. We apply a 10Gb/s PRBS input signal and add a 41ps peak-to-peak sinusoidal jitter (SJ) to it to degrade the eye quality, as in Figure 5.14(a). The $next\_\phi_{early}$ and $next\_\phi_{late}$ signals are stepped simultaneously. The vertical opening of the mask is constant and is set to 120mV with external references. Figure 5.14(b) shows the measured *error_out* signal. There is an error-free region (no toggle) for a small mask opening that corresponds to when ϕ_{early} and ϕ_{late} are close to their initial positions in the center of the

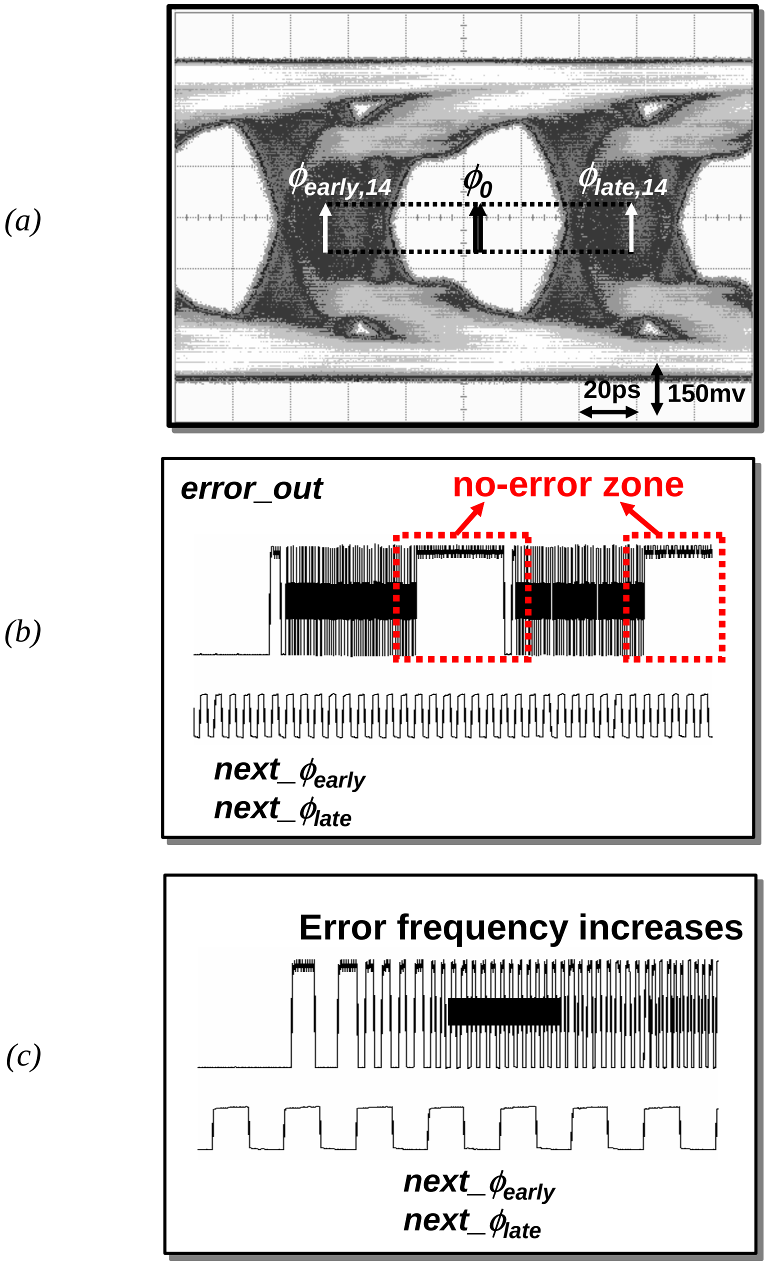


Figure 5.14: Qualitative eye-opening measurement. (a)10Gb/s input eye diagram (b) *error_out* signal demonstrates an error-free region (c) magnified *error_out* signal shows MER increase for wider mask

eye. But as the trigger signals step the sampling phases toward the edges of the eye and thus the mask gets wider, the error frequency gradually increases. This can be seen in Figure 5.14(c), which is the magnified *error_out* signal around regions with error and

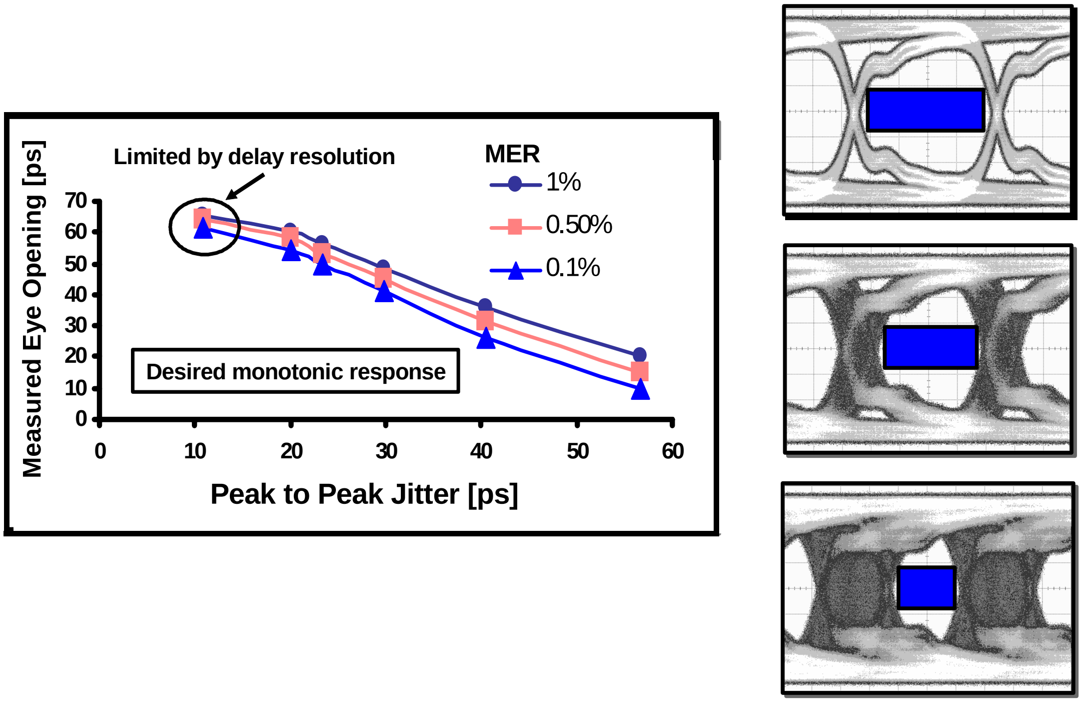


Figure 5.15: Measured eye opening for various input eye diagrams with different peak-to-peak jitter

shows the frequency of *error_out* signal increases after each positive trigger edge. The periodic behavior of the *error_out* signal is due to the self-resetting mechanism of the phases.

5.6.4 Eye-Opening Measurement Variations

Ultimately, the EOM will be used in an adaptive equalizer as shown in Figure 5.1. In such a setting, the EOM output should track variations of the eye opening and provide a correct gradient to assist the optimization algorithm in adjusting the filter coefficients. We verified the behavior of the EOM in this scenario by measuring the eye opening when various amounts of peak-to-peak SJ are added to the 10Gb/s, 2^{31}-1 PRBS input. The vertical opening of the mask is constant. Figure 5.15 shows the measurement result with three sample input eye diagrams that demonstrate the gradual closing of the eye. As expected, the measured eye opening monotonically decreases as additional jitter closes the eye. At low input jitter, the transition from small to large measured MER is abrupt and thus the plot loses accuracy, because the resolution of the horizontal eye-opening step becomes comparable to the peak-to-peak input jitter. Therefore, when the sampling clocks approach the data edge, one horizontal opening step can increase the number of transitions falling inside the mask from zero to all the transitions.

5.6.5 Complete System Test

This experiment demonstrates the EOM capability in generating the two-dimensional error diagram that corresponds to the input eye shape. A pair of 5-foot coaxial cables were used to add ISI to the input data. A computer program controls a pulse generator and two external power sources through a GPIB port. The program steps through several mask horizontal and vertical openings. A frequency counter records the *error_out* frequency, as the number of transition errors, for each mask. In each mask sweep only one half of the eye is covered by triggering only one of the $next\_\phi_{early}$ or $next\_\phi_{late}$ signals. The other phase is held in the center of the eye in phase with Q. Once one half of the eye is swept completely, the other *next* signal will be stepped through to cover the other half. This way any horizontal asymmetry in the eye is captured.

Ideally, when V_H and V_L are both equal to the input data common mode the mask error rate should be minimal because the comparators have the highest sensitivity. Therefore, the vertical mask is swept for $V_H = V_{cm} + n\Delta V$ and $V_L = V_{cm} - n\Delta V$, where V_{cm} is data common mode and $1 \le n \le N$. N is seven if on-chip DAC is used but can be larger with external reference adjustment. However, due to the comparators' offset, the minimum error count may occur when $V_H \le V_{cm}$ or $V_L \ge V_{cm}$. To guarantee that all the horizontal range is covered, the horizontal sweep is done for $-N \le n \le N$. We measured three sample chips and we observed that the minimum mask error rate occurs at n=1 or 2 corresponding to 5mV to 10mV differential offset.

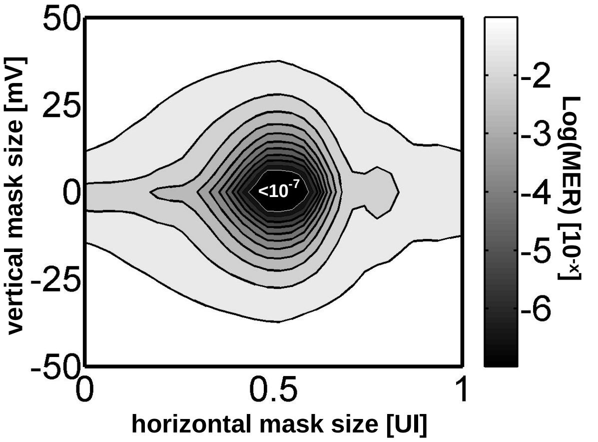


Figure 5.16: Measured 2D error map with 68dB dynamic range

Figure 5.16 illustrates the two-dimensional error diagram that is generated as the result of the measurement for the input eye in Figure 5.14(a). It demonstrates that the asymmetrical input eye shape is captured. Furthermore, the diagram has 68dB dynamic range for MER. The dynamic range is a function of the time period for MER measurement per one mask. A longer period of error-free measurement corresponds to a smaller MER.

It can be shown that MER is bounded by the input noise. We show in Appendix D that the MER measured by an ideal EOM can be expressed as

$$MER \cong Q\left(\frac{1-(V_H - V_L)}{2\sigma}\right) \tag{5.4}$$

for a signal amplitude of “1” and a noise standard deviation of σ. Equation (5.4) simplifies to conventional BER expression when $V_H = V_L$. Amplitude noise is assumed to have Gaussian distribution, and $Q(.)$ is its cumulative distribution function. Due to the exponential nature of the $Q(.)$, expected MER is about four orders of magnitude larger than BER for BER about 10^{-12}.

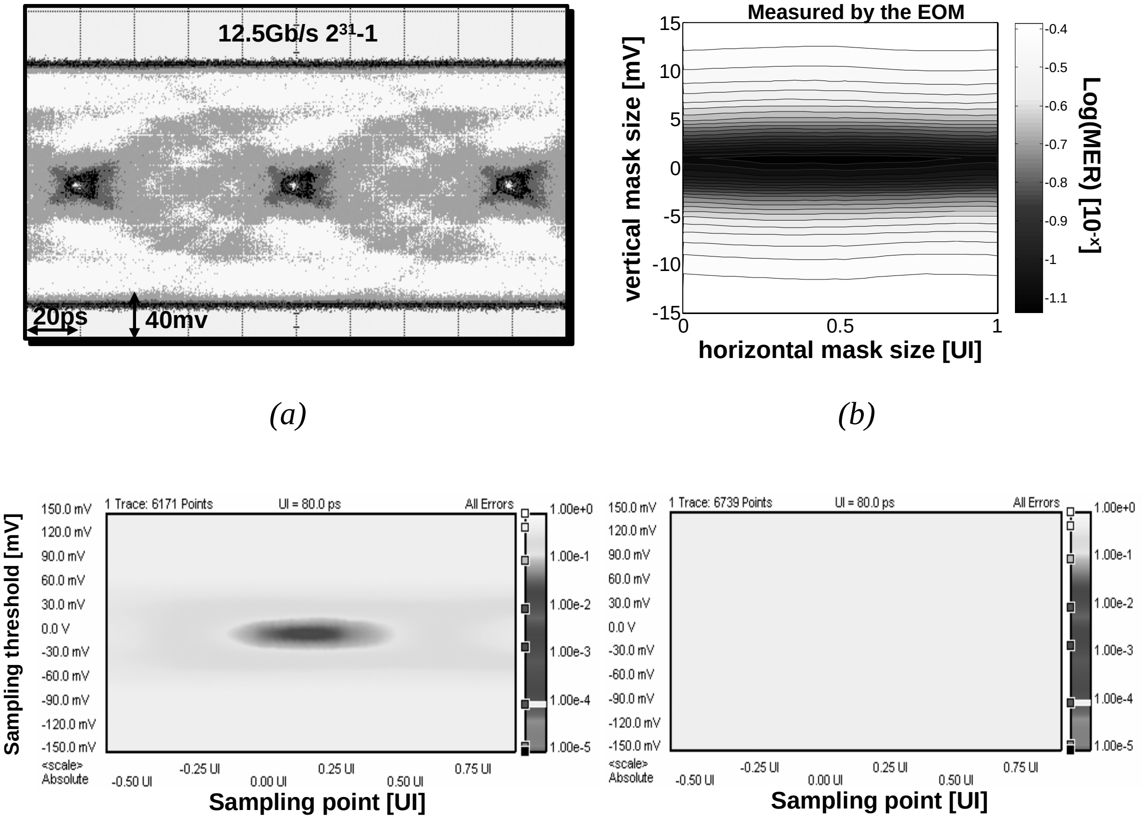
The non-idealities of the EOM, specifically the bandwidth limitations of the comparators further degrade the measured MER. It is shown in Appendix D that (5.4) can be modified to

$$MER \cong Q\left(\frac{A(t) - (V_H - V_L)}{2\sigma}\right) \cdot \left(1 - Q\left(\frac{A(t) + (V_H - V_L)}{2\sigma}\right)\right) \tag{5.5}$$

to take the impact of the EOM into account. $A(t)$ is the response of the comparator to the input sequence at the time of sampling, t. As the sampling clocks, ϕ_{early} or ϕ_{late} are stepped toward the edges of the eye diagram, $A(t)$ approaches the threshold level and MER increases as a consequence. A two-dimensional MER map can be obtained from (5.5) for different sampling times and V_H-V_L based on the input and comparator response. We generated this error map using the simulation results of the comparator in our design and compared it with the measured 2D error map in Figure 5.16. A two-dimensional cross-correlation of the two maps resulted in a 0.9 correlation coefficient that verifies that our measurement is closely following the expected result from the simulation.

5.7 EOM vs. BERT

The EOM has two main features that distinguish it from a conventional bit error rate test (BERT) system. First, the EOM detects errors based on two samples at the same sampling phase. It does not require pattern matching. Thus, unlike a BERT that requires a PRBS sequence for proper operation, the EOM can operate with truly random sequences and does not need the *a priori* knowledge of the transmitted sequence. This simplifies the error detection computation and hardware remarkably well. Second, a BERT treats a channel's deterministic impacts, amplitude noise, random jitter, and digital errors induced from imperfect digital circuit blocks, *e.g.*, multiplexer and demultiplexer, equally. Therefore, the effect of individual impairments on the number of detected errors can not be separated. On the other hand, the EOM is more sensitive to deterministic impairments of the channel, *e.g.*, deterministic jitter and ISI because the random effects are averaged when the error number is divided down in the counter. Furthermore, the digital errors are ignored by the EOM as it does not compare received data with a pre-determined sequence. Consequently, the error count is mainly correlated to the impact of the channel response. Figure 5.17 compares the response of the EOM and a commercial BERT in the presence



(a) *(b)*

(c) *(d)*

Figure 5.17: Comparing EOM and BERT operations: (a) 12.5Gb/s input eye (b) MER measurement with EOM in presence of 10% digital error (c) BER measured with commercial BERT (d) BER measured with commercial BERT in presence of 10% digital error

of digital errors intentionally added to the input. A 12.5Gb/s 2^{31}-1 PRBS is passed through 5 feet of lossy coaxial cable to introduce ISI and is then applied to the input of the EOM or BERT. The eye diagram is closed and is shown in Figure 5.17(a). Figure 5.17(c) is the response of the BERT with about 18dB BER dynamic range. However, when 10% digital error is added to the input, the BERT cannot capture the eye diagram shape although the channel has not changed. Evidently, from Figure 5.17(d) the BERT has lost its error dynamic range completely. Figure 5.17(b) is the response of the EOM in the presence of the digital errors and demonstrates that the EOM successfully captures the shape of the eye diagram as in Figure 5.17(c). The MER dynamic range is reduced to about 8dB due to the reasons discussed in Section 5.6.5.

5.8 Summary

We have developed an architecture that can essentially capture a two-dimensional map of the eye diagram of a high-speed data signal. The error map can be used to extract various features of the received signal. Specifically, it can be used in an adaptive equalizer to generate the cost function for coefficient optimization. The cost function will solely depend on the quality of the received signal and not on the decision of the receiver.

The architecture is based on comparing two samples of the signal at one sampling point and therefore does not require *a priori* knowledge of data sequence or pattern matching, which remarkably simplifies the architecture. A prototype was implemented in 0.13μm standard CMOS technology that was successfully tested up to 12.5Gb/s input data rate. It consumes about 275mA from a 1.2V supply that is significantly lower than prior art.

Chapter 6

Instantaneous Demultiplexing for Burst-Mode Links

6.1 Introduction

The wireline communication link has either continuous transmission or burst-mode transmission. In burst-mode communication, data is transmitted in asynchronous packets (a.k.a. bursts), and there are long variable-length intervals between packet transmissions when the transmitter is off [36]. An example application for burst-mode links is in passive optical networks, *e.g.*, fiber-to-the-home, where multiple end users (EU) share an optical channel to the central office (CO). The CO assigns a time slot to each EU and allows each EU to upload burst-mode data in a designated time slot.

Burst-mode communication relies on very fast acquisition circuitry to achieve low network latency. If the data stream is bursty, the receiver must be able to synchronize with the data instantaneously to maintain reliable communication. For Burst-mode communication, conventional clock recovery (CR) methods based on narrowband phase-locked loops (PLLs), such as the ones designed for SONET applications, are not applicable. PLL-based CR circuits in SONET have stringent jitter transfer specifications to avoid jitter accumulation. In addition, they are required to tolerate long sequences of identical bits (Section 2.2.2). These constraints impose a narrowband PLL that will have a long acquisition time. For instance, [37] reports a minimum of 50μs acquisition time for a 155MHz CR circuit. In this case, approximately the first 8000 bits of data will be lost. Although designing a wideband PLL reduces the number of lost bits, it still requires preamble bits to enable synchronization prior to the arrival of the data payload.

Gated-oscillator clock recovery provides instantaneous lock to the first data transition. Such circuits have been reported at several hundred Mb/s [128]–[132]. Gated-oscillator clock recovery relies on two oscillators that are activated with the rising and falling edges of the input signal and are, hence, resynchronized with every transition. The frequency of the gated oscillators are equal to the bit rates and the right value is typically maintained via another replica oscillator in a PLL.

In this chapter we introduce an alternative method for instantaneous data recovery and demultiplexing based on a finite state machine (FSM). The FSM receives the data and decides on the output values based on the current input data and the previous state. The previous state is provided to the FSM input with a bit-period delay. While decisions are synchronized with every incoming data transition, no oscillator is required. Although the jitter transfer function is flat similar to the gated oscillator-based approach, there is a reduction by a factor of n, the demultiplexing ratio, in output jitter due to the integrated demultiplexer function.

We first introduce the new general architecture for an 1:n clockless demultiplexer and discuss the complexity of the FSM for different demultiplexing ratios, n. Then, we describe the design procedure for a 1:2 demultiplexer and discuss different possibilities for implementing the delay cells. We perform a comprehensive statistical study on process variations of passive delay cells and explore their feasibility for this application. Lastly, we demonstrate the experimental results of the fabricated 1:2 demultiplexer prototype.

6.2 Instantaneous 1:*n* Demultiplexer

6.2.1 General Architecture

Figure 6.1 shows the general block diagram of the proposed clockless data recovery and the 1:n demultiplexer. The FSM consists of a combinational-states logic block and bit-period delay cells. It maps the combination of the input and previous state to a current state. The previous state is the output of the FSM at the last bit period, T_b, and is fed back to the input of the states logic block with a delay of T_b. The output logic block generates

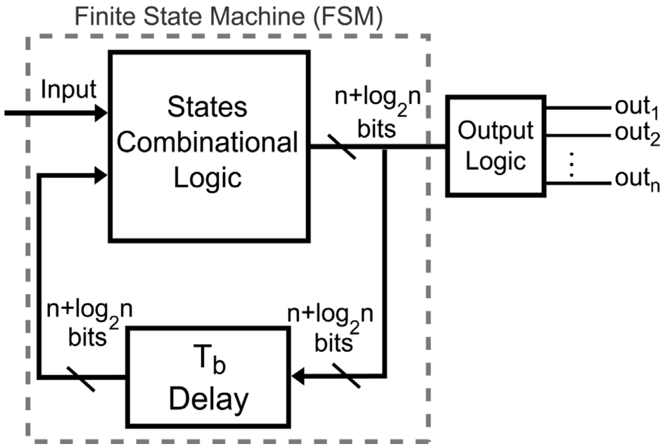


Figure 6.1: Instantaneous 1:n demultiplexer

the demultiplexed outputs based on the current state. Both logic blocks respond to their inputs instantaneously. Therefore, each data transition at the input immediately affects the outputs of the demultiplexer, if the logic gate propagation delay is neglected.

In a conventional 1:n demultiplexer, each output changes based on its corresponding bit at the input and then keeps its value for nT_b periods. The combination of the FSM and output logic operates similarly. Each input bit is directed to the proper output, and the value of the other outputs are kept constant in the memory of the FSM state. Therefore, the information stored in one state of the FSM consists of the value of current bit (1 bit), the values of the unaffected bits ($n-1$ bits), and the binary address of the affected output (log_2n bits). As a result, for a 1:n demultiplexer a $n+log_2n$ bit FSM is required, as Figure 6.1 demonstrates. Consequently, the number of states in the FSM is $n.2^n$.

The delay cell in Figure 6.1 guarantees that the information of the previous state is available whenever a data transition occurs, *i.e.*, every bit period. The output is updated for every data transition, and thus there is no explicit jitter rejection. However, the input data jitter at any transition impacts only one of the n outputs. Moreover, each output has 1/n the data rate of the input. Therefore, effective output data jitter in unit intervals (UI), *i.e.*, normalized to nT_b, is reduced to 1/n of the input data jitter.

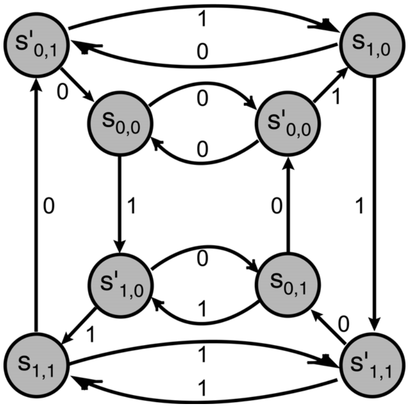


Figure 6.2: State diagram for a FSM-based 1:2 demultiplexer

Next, we demonstrate the design of a 1:2 demultiplexer based on the clockless data recovery method.

6.2.2 Design of a 1:2 Demultiplexer

The major advantage of the clockless demultiplexer is that it responds to data transitions instantaneously. After a long quiet period with zero input and zero outputs, the first data transition initiates the state transitions of the FSM. Thereafter, the FSM state is updated every period, T_b, synchronous to data transitions. If the delay is not exactly T_b, any incoming data transition resynchronizes the FSM. The output of FSM will be valid as soon as the data transition arrives at the input provided that the logic propagation delay is negligible.

Figure 6.2 illustrates the states and state transitions of the 1:2 clockless demultiplexer. Each arrow corresponds to a state transition in FSM. The binary value on the arrow represents the current value of the input. For the 1:2 demultiplexer, the FSM has a total of eight states, as shown in (b). The FSM stays in each state for a period of T_b. Then it transitions to the next state based on the input bit. The prime superscript in the state name is equivalent to the *select* line of a conventional demultiplexer. States with prime superscript correspond to the ones for which the input bit affects out_2. The first subscript in the state name is the current input bit, and the second subscript is the previous input bit stored to hold the unaffected output. For example, when FSM is in $s_{1,0}$ it corresponds to the state when the input bit, “1,” is transferred to out_1 and stored previous bit, “0,” is transferred to out_2. If after T_b, a data transition occurs and the input bit is “0,” FSM transitions to $s'_{0,1}$, for which the input bit, “0,” is now transferred to out_2 and stored previous bit, “1,” is transferred to out_1. Table 6.1 summarizes the two output values for all the eight states.

Table 6.1: 1:2 Demultiplexer output in each state

Current State	**out$_1$**	**out$_2$**	**Current State**	**out$_1$**	**out$_2$**
$s_{0,0}$	0	0	$s_{0,1}$	0	1
$s'_{0,0}$	0	0	$s'_{0,1}$	1	0
$s_{1,0}$	1	0	$s_{1,1}$	1	1
$s'_{1,0}$	0	1	$s'_{1,1}$	1	1

A 3-bit FSM represents the state diagram in Figure 6.2. Each state is assigned a 3-bit code word. To avoid races, *i.e.*, erroneous transitions to other states, the codes are assigned such that only one bit changes in every state transition. Therefore, delay mismatches in the implementation cannot cause errors, and the FSM is race free. The code words are presented in Table 6.2.

Table 6.2: Race-free code assignment for the states of the FSM

State	**Code ($y_0 y_1 y_2$)**	**State**	**Code ($y_0 y_1 y_2$)**
$s_{0,0}$	001	$s_{0,1}$	100
$s'_{0,0}$	000	$s'_{0,1}$	011
$s_{1,0}$	010	$s_{1,1}$	111
$s'_{1,0}$	101	$s'_{1,1}$	110

We associate the binary variables y_0, y_1, and y_2 to the three bits that code the FSM states. Therefore, when y_0, y_1, and y_2 are updated every T_b, we say FSM has transitioned to the next state. The updated binary values for each of y_0, y_1, or y_2 is determined from the state diagram and the code word table based on the current values of y_0, y_1, or y_2 and the input bit. The next value of each of the three binary variables is described as

$$y_i^* = f_i(y_0, y_1, y_2, x) \qquad (i = 0, 1, 2) \tag{6.1}$$

where "*" signifies the updated value of y_i. Function f_i is a logic function, and the arguments are the current values of the binary variables. Variable x corresponds to the current input bit. The logic functions are designed based on standard methods such as the sum of products (SOP) using Karnaugh maps [133].

Similarly, out_1 and out_2 can be represented as functions of y_0, y_1, y_2, and x. Based on the concept of a conventional 1:2 demultiplexer we predict the logic function for the two outputs as

$$out_1^* = out_1 \cdot S + x \cdot \bar{S} \tag{6.2}$$

$$out_2^* = out_2 \cdot \bar{S} + x \cdot S \tag{6.3}$$

where S is a binary function representing which output should change and is equivalent to the select line of an ordinary demultiplexer. The "." and "+" are logical AND and OR functions, respectively. For instance, in (6.2), the next value for out_1 is the current value of out_1 if S=1 and is the input if S=0. The change is synchronous with x.

From the Figure 6.2 and Table 6.2 we can show that

$$S = y_0 \cdot (y_1 \oplus y_2) + \overline{y_0} \cdot \overline{(y_1 \oplus y_2)} \tag{6.4}$$

where $\oplus$ is the "*exclusive or*" function. Additionally, we can show $out_1 = y_1$ and $out_2 = y_0$. Therefore, the output logic block in Figure 6.1 is omitted and the outputs are tapped directly from the FSM output variables. Hence, the simplified output functions are

$$out_1 = y_0 \cdot (y_1 \oplus y_2) + x \cdot (y_0 + y_1 \oplus y_2) \tag{6.5}$$

$$out_2 = y_1 \cdot \overline{(y_0 \oplus y_2)} + x \cdot (y_1 + \overline{y_0 \oplus y_2}) . \qquad (6.6)$$

Equations (6.5) and (6.6) are computed directly from digital maps of Table 6.2 code words. However, they have the form as in (6.2) and (6.3) and can be obtained directly by replacing (6.4) in (6.2) or (6.3).

6.2.3 Cascade Architecture

For *n*>2, one approach to design the demultiplexer is to follow the same procedure as in Section 6.2.2. The number of states increases exponentially with *n*. The state transition table should also be updated. Furthermore, the number of binary variables that encode the state increases. For instance, for n=4, the FSM has 64 states that needs 6 bits for encoding the states. Consequently, the SOP terms require implementation of 6-input gates that are all working at the speed of data rate. An alternative approach is to use a cascaded chain of 1:2 demultiplexers to implement the 1:*n* demultiplexer. For example, if n=4 each output of the first 1:2 demultiplexer is used as the input to a second 1:2 demultiplexer. Therefore, a total of three 1:2 demultiplexers is used. The latter approach has a total of nine delay cells in contrast to six delay cells in the former approach. Therefore, if the delay cells are implemented using passive elements, the latter approach will have area disadvantage. However, the combinational logic design is much simpler because of fewer number of variables. In addition, the required speed of operation for the 1:2 demultiplexers decreases monotonically as they are placed closer to the outputs in the chain because the data rate at the output of each stage is divided by two. Therefore, alternative digital gate circuit topologies such as complementary-MOS can be used for 1:2 demultiplexers at the end of the chain that can reduce the power consumption significantly.

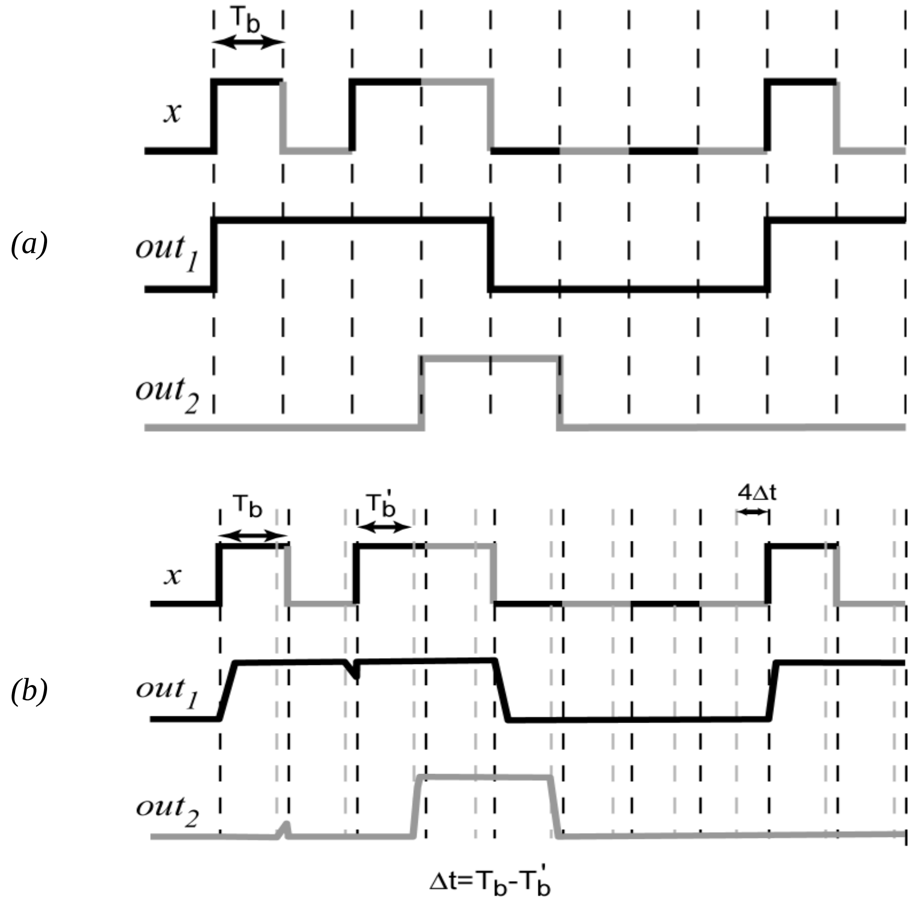


Figure 6.3: Demultiplexer outputs for 1011000010 input sequence (a) Ideal case (b) Delay cell has smaller delay than bit period

6.3 Delay Mismatch

The delay cell in Figure 6.1 is the synchronizing block in the demultiplexer that controls how long the FSM stays in one state. When the first data transition initiates the demultiplexer, FSM binary outputs, *i.e.*, y_0, y_1, y_2 in a 1:2 demultiplexer, are fed back to the input of FSM every T_b and generate the next state and next outputs based on (6.1), (6.5), and (6.6). Ideally, the delay must be equal to the input bit period T_b. Figure 6.3(a) demonstrates how the demultiplexer operates for a sample input data. When one output is following the input, the other output is holding its own previous value.

If the delay cell has a delay T_b', different from T_b, the outputs might experience glitches. However, any input transition will immediately correct those glitches and avoid any unwanted output transition. Figure 6.3(b) illustrates an example where $T_b' < T_b$. As can be seen, out_1 in the second bit period is holding its previous value, "1." After T_b' new values for y_0, y_1, y_2 are ready at the FSM input while the correct input, x, corresponding to out_1 has not arrived yet. out_1 starts to follow the incorrect x. However, after $\Delta t = T_b - T_b'$, the next data transition arrives and out_1, out_2, y_0, y_1, and y_2 are immediately corrected because they relate to x with a combinational-logic relation such as (6.5) or (6.6). Although glitches are observed at the outputs as a consequence, delay mismatch is corrected every cycle and does not accumulate when data transitions occur.

A behavioral simulation of the demultiplexer in HSPICE confirms the above argument. T_b' is chosen 125ps while input data is 7.5Gb/s, which corresponds to T_b=133ps. In Figure 6.4, the marked bumps on out_1 and out_2 correspond to the same glitches discussed in Figure 6.3(b). As predicted, the next data transition immediately

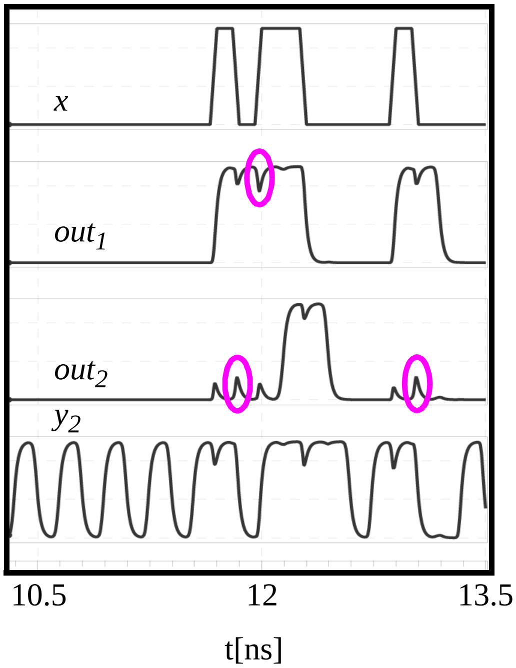


Figure 6.4: Outputs of the 1:2 demultiplexer when $T_b' < T_b$ simulated with HSPICE

corrects such errors. The other weaker bumps in the outputs are related to hazards that occur when two or more terms in the SOP of output function are changing simultaneously, while the overall output function remains at the same logic level.

The delay mismatch bounds the maximum number of consecutive identical bits (CIB) at the input. If delay mismatch is Δt, as in Figure 6.3(b), the number of CIB's should be fewer than $n = T_b / \Delta t$. Otherwise, the FSM will swap the outputs, and the $(n+1)$th bit will be resolved at the incorrect output.

Δt can be made very small by using a delay control circuit that forces Δt to zero. A ring oscillator is formed by closing a positive feedback loop around a replica of the delay cells. The period of oscillation equals twice the delay of the delay cells, $2T_b'$. A PLL locks the frequency of the ring oscillator to an accurate reference clock by tuning the replica delay cell. The same control voltage is used to adjust the delays in the FSM. In practice, the logic circuits in the FSM have propagation delays that contribute to the total delay around the feedback loop of the FSM. Furthermore, process variations could significantly impact the propagation delay of the gates. Therefore, a delay control loop that adjusts the delay cells alone would be inconsequential. The replica ring oscillator must include all the blocks that contribute to the delay.

For the 1:2 demultiplexer, it can be shown that in the absence of input transitions, f_2 from (6.1) is simplified to

$$y_2^* = \overline{y_2}. \tag{6.7}$$

Equation (6.7) shows the y_2 output inverts for every period delay around the FSM loop, T_b'. In other words, the y_2 output oscillates with the period of $2T_b'$ when the input is constant. In fact, y_2 acts as the internal timer of the FSM in the absence of input transitions. The y_2 output in Figure 6.4 demonstrates this. When input is zero, y_2 oscillates for four cycles. As soon as the data transition arrives in the fifth cycle, the y_2 phase is aligned and the oscillation stops. If there were no additional input transitions y_2 would oscillate again with corrected phase. Now, the replica of the 1:2 demultiplexer with y_2 as the output forms

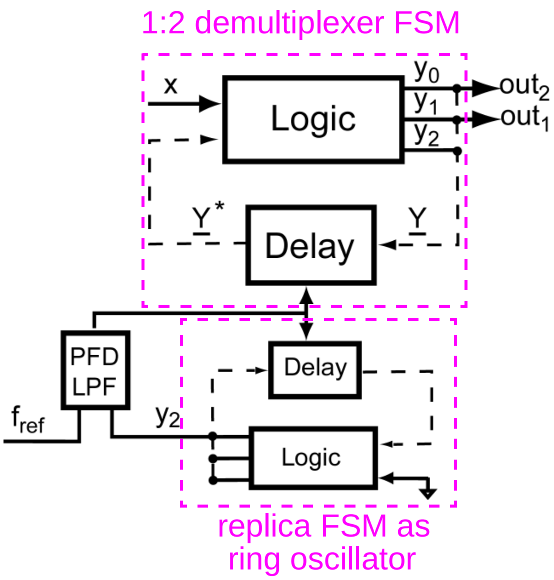


Figure 6.5: Demultiplexer with delay control loop

the ring oscillator in the delay control loop. This ring oscillator includes all the digital blocks that contribute to the delay. Figure 6.5 illustrates the architecture. The same architecture could be used to design a variable bit rate demultiplexer by adjusting the delay around the loop based on the input bit rate.

6.4 Delay Implementation

6.4.1 Passive Delay

The delay block can be implemented using active or passive delay elements. If the delay control loop is not used, passive delay cells based on LC ladder structures can be used, as shown in Figure 6.6 (also in Section 2.3.4). The delay is determined by the value of the passive components from $T_D = n\sqrt{LC}$ where L and C are the inductance and capacitance, respectively, and n is the number of sections in the ladder. Integrated LC delay lines have practically no sensitivity to the supply voltage while maintaining a low sensitivity to process variations and temperature. This is because the L and C component

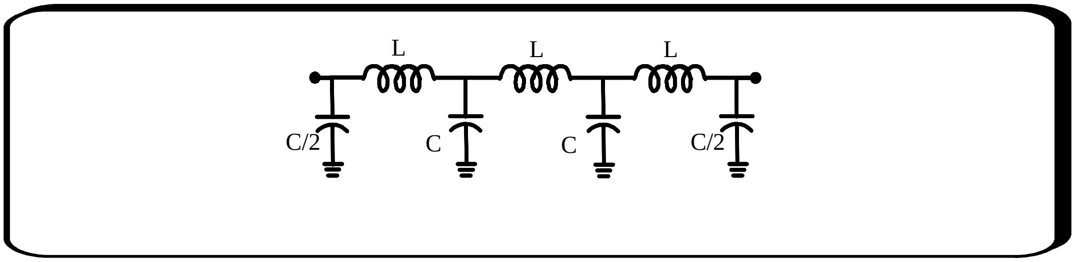


Figure 6.6: 3-section constant-*k* filter-based passive LC delay line

values are primarily determined by high-accuracy fabrication processes, and they will not vary after fabrication is complete. In contrast the delay of active delay cells is a strong function of temperature.

In addition, it has been shown [134] that using building blocks that depend only on the lateral dimensions, such as vertical parallel plate (VPP) capacitors, one can achieve even a tighter tolerance and better matching across the chip, wafer, and process lots for the capacitance value. If VPP capacitors and spiral inductors are used to implement the delay cell, the delay value will only depend on lateral dimensions of components. Lateral dimensions are defined by lithography and etching processes that have inherently higher accuracy than process steps such as deposition and planarization that control the vertical dimensions. We will present a statistical analysis of passive delay lines that were used to implement the 1:2 demultiplexer prototype.

Constant-*k* LC ladder structures consist of identical interconnected inductors and capacitors in a ladder form, as shown in Figure 6.6. The ladder is a lumped approximation of transmission line and, hence, can be used as a delay line. It can be shown that the delay of the structure is approximately

$$T_D = n\sqrt{LC} \tag{6.8}$$

where n is the number of LC sections. Using spiral inductors and high-density VPP or MIM capacitors one can obtain large delay values. Using the image impedance techniques, we can calculate the impedance of the line to be

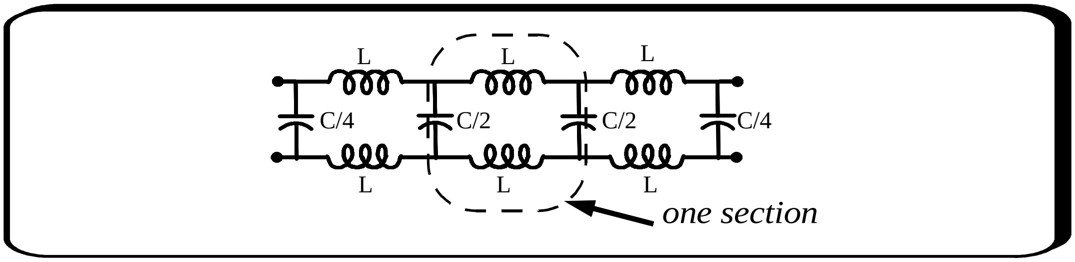


Figure 6.7: 3-section differential constant-*k* filter-based delay line

$$Z(\omega) = \sqrt{\frac{L}{C}} \cdot \sqrt{1 - \frac{LC\omega^2}{4}} = Z_0 \cdot \sqrt{1 - \frac{LC\omega^2}{4}} \tag{6.9}$$

where $Z_0 = \sqrt{L/C}$ is the characteristic impedance of the line [50]. As can be seen, the impedance becomes imaginary for frequencies above a critical frequency given by

$$\omega_c = \frac{2}{\sqrt{LC}}. \tag{6.10}$$

The LC delay line can be designed in a differential form as shown in Figure 6.7. In such circuits, the differential inductors can be interwound in order to benefit from the mutual inductance of the two inductors. Therefore, larger value inductances will be achievable with the same (or even smaller) area/size. It can be shown that if two equal differential inductors with value L are interwound with mutual inductance of k (with proper sign), the effective inductance value for each will be $(1+k)L$. We have taken advantage of this fact in our implementation of the delay lines. In the next two sections we measure several integrated passive delay lines and analyze the experimental results to study the process variation of passive delay lines

6.4.2 LC Delay Line Implementation

Two sets of LC delay lines are implemented in the form of differential constant-*k* filters in a 5-metal SiGe BiCMOS process in two different process runs. We will refer to these two process runs by PR1 and PR2. The differential inductors are implemented using coupled inductors and have 1.25 interwound turns in the top metal. Figure 6.8 shows the

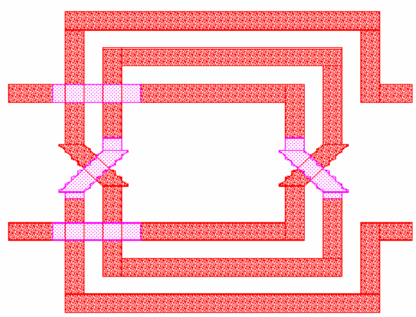


Figure 6.8: Differential symmetric interwound inductors for one section of the delay line

symmetric layout of the inductors. Inductors are simulated using a 2.5D electromagnetic simulator.

The first set of delay lines use MIM capacitors and consist of 24 LC sections in PR1. In the second set, the VPP capacitors are used instead of the MIMs. It has 19 LC sections and was fabricated in PR2. Based on our earlier discussion, we expect this VPP-based delay line to show smaller delay variations compared to its MIM-based counterpart. In VPP capacitors, the distance of the adjacent parallel plates of the capacitors are chosen to be larger than the minimum allowable spacing between adjacent metals to reduce the effect of lateral surface roughness on the capacitor value. The increased fringe capacitance is modelled accurately with electromagnetic simulations. Table 6.3 summarizes the delay line parameters.

Table 6.3: Summary of the delay line parameters

Delay Line Parameter	**Value**
Effective Inductance per section	0.58 nH
Total Capacitance per section	230 fF
Characteristic Impedance	50 Ω (100 Ω differential)
Total Simulated Passive Delay per section	11.5 ps
Ideal Critical Frequency ($\omega_c/2\pi$ from (6.10))	28 GHz

6.4.3 Experimental Results and Analysis

Standalone delay structures using MIMs and VPPs with direct on-wafer probing were tested. The results are summarized in the following sub-sections.

6.4.3.1 Measurement Accuracy and Repeatability

Twenty-seven MIM-based delay lines in PR1 and 47 VPP-based delay lines in PR2 were characterized using an Agilent Technologies E8364A network analyzer. To ensure constant environmental conditions (including temperature and measurement setup variations) during the measurement of all 74 sites, a set of preliminary experiments was performed. Six random sites were selected as witness cases and were measured three times each at different times during the measurement. Then, the results for each site were compared. The observed variations were always less than 0.05% indicating the measurement error and the degree of its repeatability. This very high repeatability of results indicates minimum changes in the conditions of the experiments.

6.4.3.2 S-parameters

Magnitude of S_{11} and S_{21} parameters of MIM-based and VPP-based delay lines were measured. A sample result for a MIM-based delay line, plotted in Figure 6.9, shows $S_{11} <$ -12dB (upto 30 GHz). Similar measurements for VPP-based delay lines show $S_{11} <$ -16dB

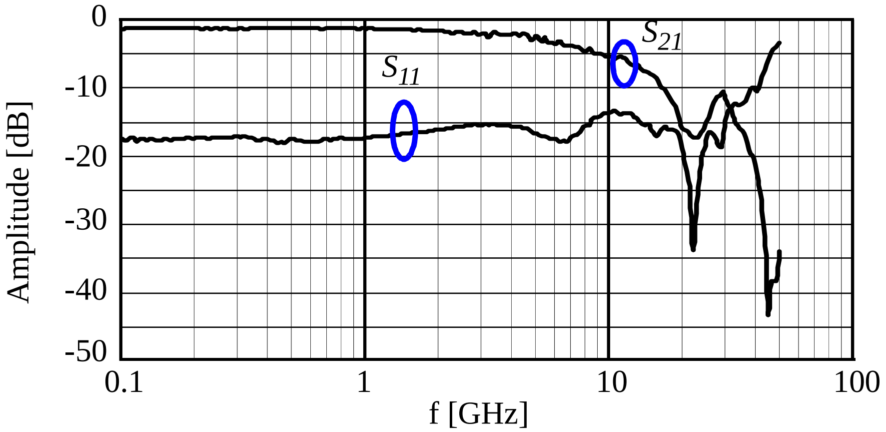


Figure 6.9: Magnitude of the *S*-parameters of one MIM-based standalone delay line

($.5GHz \leq f \leq 20GH$). They indicate that the delay line characteristic impedances are very close to 50 Ω over that wide range of frequencies. The low frequency loss of MIM-based delay line is 1.2 dB and its 3dB bandwidth is 7.5 GHz.

6.4.3.3 Standalone Delay Lines: Group Delay

The group delay is an indication of the delay value of the delay line at different frequencies. The group delays of the whole ensemble for both MIM-based and VPP-based lines are plotted in Figure 6.10 and Figure 6.11, respectively. The dominant source of variations over different wafer sites for samples in MIM-based lines is the tolerance of MIM capacitors. The reported MIM tolerance in this process technology is $:0.15 fF/\mu m'$. It translates to a total tolerance of ΔC=18.8 fF for the MIMs that we used. The time delay variations per section can be approximated from (6.8)

$$\Delta T_D = \frac{\partial T_D}{\partial C} \cdot \Delta C \tag{6.11}$$

$$\frac{\Delta T_D}{T_D} = \frac{1}{2} \cdot \frac{\Delta C}{C} = 0.04\,. \tag{6.12}$$

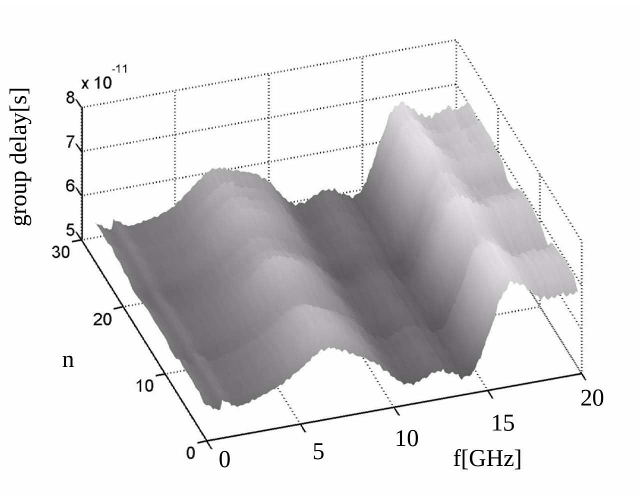


Figure 6.10: Collective group delays of 27 standalone MIM-based delay lines

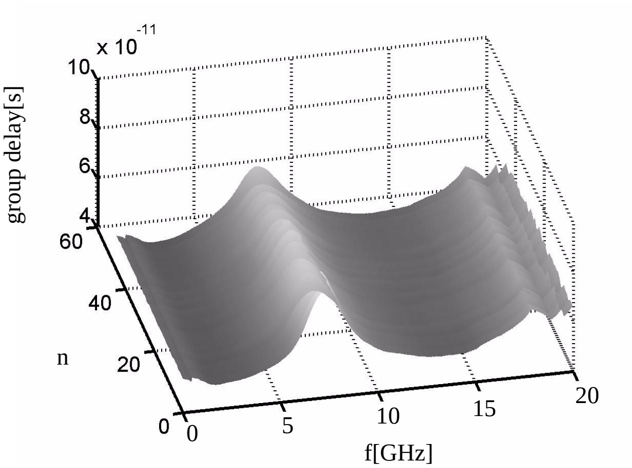


Figure 6.11: Collective group delays of 47 standalone VPP-based delay lines

The normalized standard deviations of group delay (normalized to the mean group delay at corresponding frequency) for MIM-based and VPP-based lines are plotted in Figure 6.12. The variations for MIM-based lines are within the tolerance of the MIM capacitors in (6.12). The delay lines with VPP capacitors are almost twice as accurate across most of the frequency range. This corresponds to a factor of 3.3 improved tolerance for the VPPs in agreement with [134]. Table 6.4 compares the average low-frequency

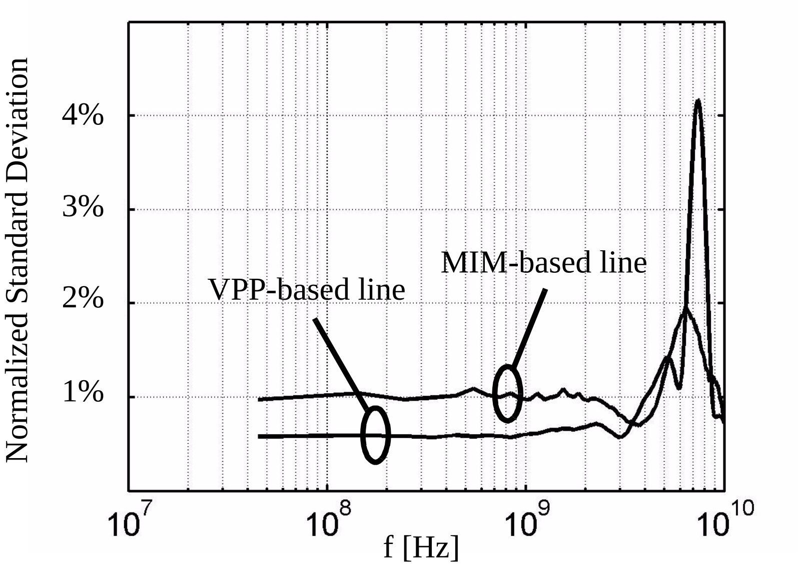


Figure 6.12: Normalized standard deviations for group delays of standalone delay lines

group delays and the average normalized standard deviations of that in both cases. Again, it can be seen that the VPP-based delay lines are almost twice as accurate. Figure 6.13 shows the distribution of normalized delay at 1 GHz for both MIM- and VPP-based delay lines. Passive LC delay lines are low sensitivity to process variations and no sensitivity to supply variations.

Table 6.4: Statistical comparison for MIM and VPP-based lines

Parameter	**Mean (η)**	**Standard Deviation (σ)**	σ/η
MIM *low freq. group delay*	56.7 ps	0.572 ps	1.01%
VPP *low freq. group delay*	52.14 ps	0.306 ps	0.59%

The die photos of the VPP-based line and MIM-based line are shown in Figure 6.14 and Figure 6.15, respectively. The passive delay lines are dominating the area. The spiral inductors are formed in a loop in the oscillator to avoid long interconnect lines. The capacitors are located in between the inductors. Inductor size is $150\mu m \times 150\mu m$.

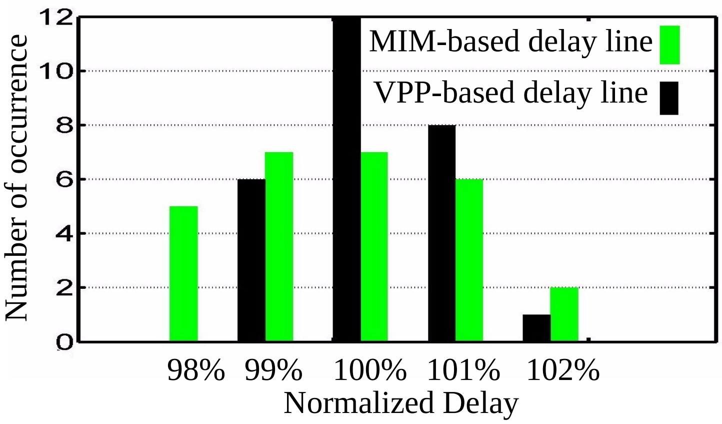


Figure 6.13: Distributions of normalized delay at 1GHz for both MIM and VPP-based delay lines

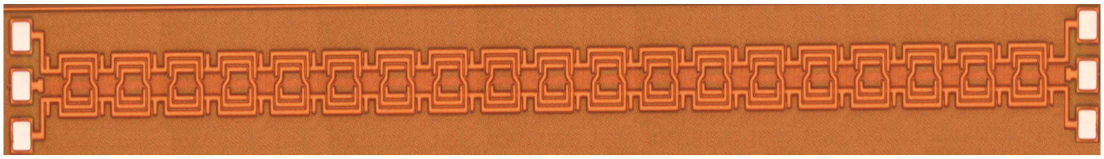


Figure 6.14: Die photo of 19-section VPP-based LC delay line

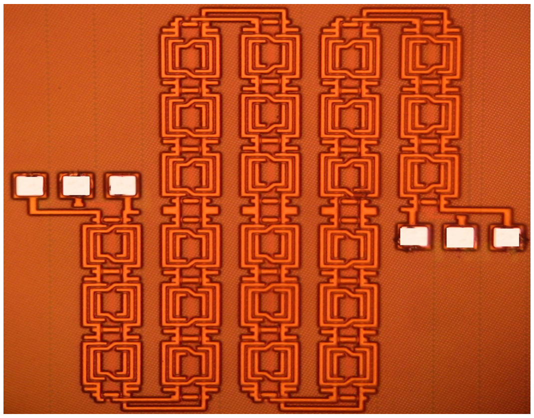


Figure 6.15: Die photo of 24-section MIM-based LC delay line

6.5 Prototype Measurement Results

We fabricated an integrated 1:2 demultiplexer based on the instantaneous clockless architecture in the SiGe BiCMOS process technology, which is the same technology we used to analyze process variations of the delay lines. SOP logic functions form the FSM as described in Section 6.2.2. The logic functions are realized by emitter-coupled logic (ECL) gates. Figure 6.16 shows a 3-input *OR* gate. When any one of the three inputs is at high logic level, all the tail current, I_t, runs in the left branch of the emitter-coupled stage,

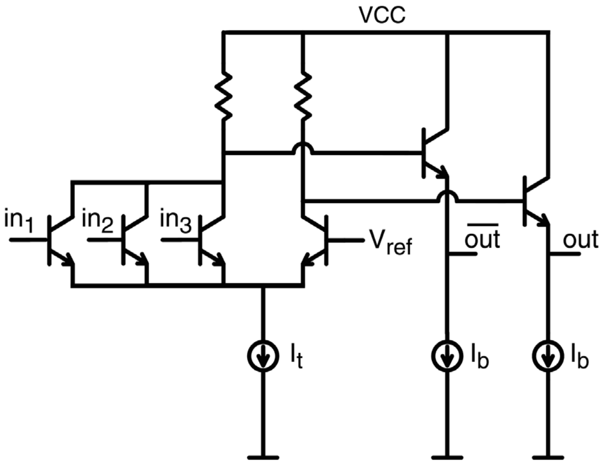


Figure 6.16: A three-input ECL OR gate

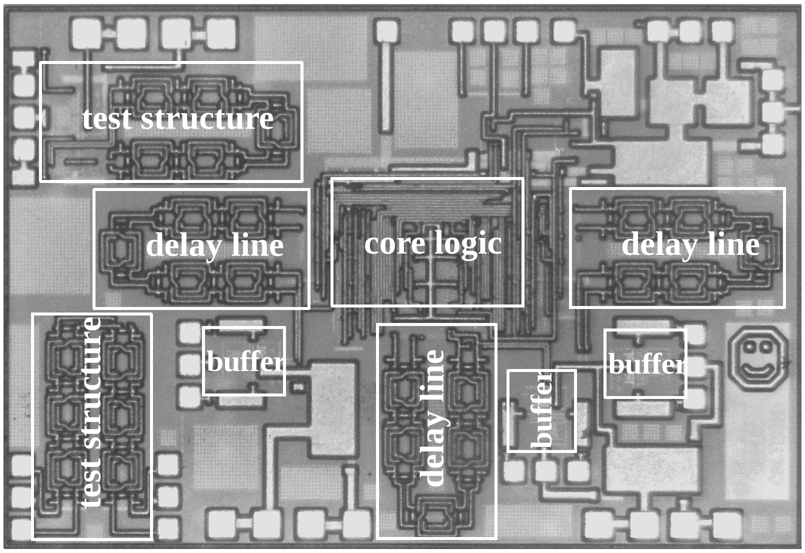


Figure 6.17: Die microphotograph of the 1:2 demultiplexer with three 5-section differential LC delay line

which forces the *out* to high logic level. The *AND* gates are implemented using *OR* gates by inverting the inputs and output. A 5-section differential LC delay line is implemented for each of the delay cells in the feedback loop of binary functions y_0, y_1, and y_2. The die photograph is shown in Figure 6.17. Chip dimensions are $2.5mm \times 1.7mm$.The core logic occupies only 11% of the total die area.

Figure 6.18 is the y_2 output of the demultiplexer when the input is a constant “1.” As mentioned, y_2 oscillates with a period equal to twice the total delay around the FSM feedback loop, 266ps. Therefore, the delay (bit period) is 133ps, and the demultiplexer

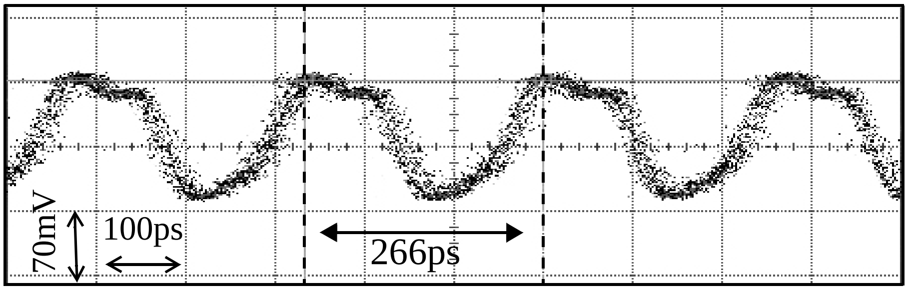


Figure 6.18: The y_2 output in the oscillator mode

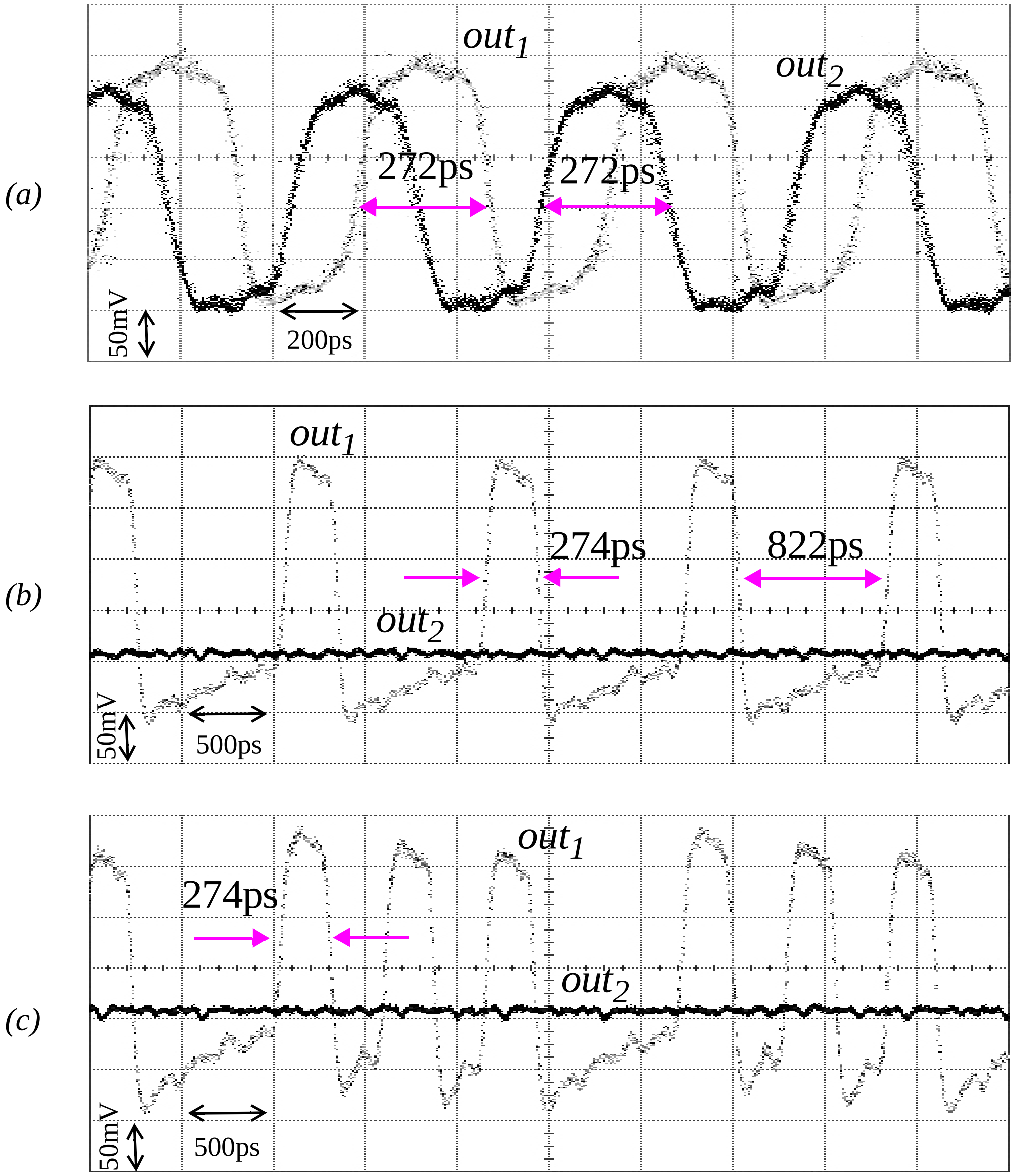


Figure 6.19: Demultiplexer outputs out_1 and out_2 for 3 input sequences (a)1100 (b)10000000 (c) 1000000010001000

works at input bit rate of 7.5 Gb/s. About 55% of the total delay is generated by the passive delay lines and the rest is from the ECL gates and interconnect parasitics.

The two outputs of the demultiplexer, out_1 and out_2, are measured for three different input sequences, as shown in Figure 6.19. The “sync” signal from the input signal source is used to trigger the sampling oscilloscope for viewing the outputs and justifies that the outputs are synchronized with the input. When the input is a repeating “1100” sequence, the demultiplexed outputs should both be “10” sequence repeating at half the bit rate, *i.e.*, twice the bit period, of the input. In addition, out_2 is one input bit period delayed with respect to out_1. Figure 6.19(a) shows these outputs.

A data transition can experience different delays when propagating through an LC-ladder delay cell, based on previous data bits [18]. Delay is defined as the time difference of the threshold-crossing times of the data transition, *e.g.*, a “10” falling transition, at the input and output. The threshold-crossing time is affected by the bits arriving at the delay cell prior to the transition due to the memory of the delay cell [18][20]. For example, “010” and “110” sequences will have different threshold-crossing times at the output of the delay cell. In the latter sequence the residue of the last bit before the falling transition impacts the threshold-crossing time. This data-dependent delay affects the overall delay in the FSM feedback loop. There are three delay cells for y_0, y_1, and y_2 in the FSM and the input to each depends on the FSM input sequence. Thus each of the individual delay values may vary based on the input sequence. Furthermore, the sequences to the input of the delay cells are not necessarily the same. We define the FSM loop delay as the average of the three delays, while this average depends on the FSM input sequence. For instance, when the FSM input is a constant “1,” the three delay cells for y_0, y_1, and y_2 respectively see a constant “1,” a constant “1,” and “10” sequences at their input; whereas for a “1100” at the input the delay cells respectively experience “1100,” “1100,” and “10” sequences. The inputs to the y_0 and y_1 have changed. Consequently, the average loop delay changes. The two cases are shown in Figure 6.18 and Figure 6.19(a), where average loop delay is changing from 133ps (half of 266ps) in the former to 136ps (half of 272ps) in the latter. One way to avoid data-dependent delay values is to use nonlinear (digital) delay cells as opposed to linear LC-delay cells.

Figure 6.19(b) shows the outputs when the input sequence is “10000000,” which has seven consecutive zeros. The two outputs are respectively “1000” at half bit rate and all-zero. The droop for long sequences of one is due to ac-coupled outputs, which will not be present in a dc-coupled version. A longer sequence, *i.e.*, 16 bit, is tested in Figure 6.19(c). The input sequence, “1000000010001000,” results in the outputs “10001010” at half the bit rate and all-zero. The demultiplexer is locking to the input phase and correctly demultiplexes to two outputs without using a synchronous clock. The chip is using a 3.3V power supply and draws 316mA of current, of which 110mA is flowing in the output buffers and bias circuits.

6.6 Summary

We introduced a new architecture that instantaneously recovers and demultiplexes data without explicit clock recovery. The architecture is based on a finite state machine (FSM) that assigns input to a proper output and maintains the value of other outputs. State transitions are synchronized with the arrival of input-data transitions. Binary logic functions map the current state along with the input bit to the next state. Analog delay cells with bit-period delay feedback the value of the binary functions to the input and synchronize FSM with the input data.

One approach to implement the delay cells in the architecture is to use passive delay cells that are low sensitive to process and temperature variations. We performed an experimental statistical analysis on passive delay lines to demonstrate this fact. We then showed the measurement results of a prototype 1:2 demultiplexer based on integrated passive LC delay lines that operates at 7.5Gb/s without using a clock signal.

Chapter 7

Conclusion

7.1 Thesis Highlights

In this work we explored the analysis and design of wireline communication systems and focused on the basic challenges of high-speed wireline links. We bridged the gap between system design and circuit design by: (1) understanding the relationship between the wireline link reliability and the system parameters, (2) introducing practical circuit architectures that enable realization of such systems with the required parameters, and (3) demonstrating implementation of hardware prototypes using silicon-based integrated circuit technologies that verify our solutions.

First, we provided the principles of today's high-speed communication links. We developed a theory that analytically relates the data link reliability, *i.e.*, the BER, to the system level characteristics, *e.g.*, the channel response, the pre-amplifier bandwidth, the amplitude noise, and the transmitter clock jitter. In particular, we used the BER contours to find the optimum system bandwidth that is a crucial specification for the pre-amplifier in the receiver architecture. In addition, we determined the optimum sampling point and its associated timing margin that is an important design specification for the clock recovery circuit. We also developed the theory of the data-dependent jitter (DDJ), which is a significant component of the timing jitter in high-speed links because of the system bandwidth limitations. We provided an analytical distribution function for the DDJ of an arbitrary linear time-invariant system and included the impact of the DDJ in the data link's overall BER.

Second, we proposed a method for bandwidth enhancement of wideband amplifiers. This is useful for the pre-amplifier design in the high-speed links using technologies that suffer from large parasitic components and thus small maximum frequency of operation. This methodology was based on two-port broadband matching of multistage amplifiers. We absorbed the device parasitics into the passive matching networks in order to allow each amplifier stage to achieve its theoretical maximum gain-bandwidth product set by the Bode-Fano limit [26][27]. We demonstrated a CMOS 0.18μm amplifier that operates at 10Gb/s and achieves 2.4 times the bandwidth improvement over a design that does not apply our technique.

Third, we developed a novel eye-opening monitor architecture that enables full integration of adaptive equalizers, for compensation of channel-induced impairments such as the inter-symbol interference. The eye-opening monitor circuit (EOM) is a block that evaluates the quality of the received signal eye diagram and periodically reports a quantitative measure that is correlated to the signal quality. This output can be used as a cost function for automatic adjustment of the filter coefficients in an adaptive equalizer. Our proposed EOM can effectively capture a two-dimensional image of the eye diagram shape and thus can be used for general signal integrity evaluation. The simple error detection mechanism of the EOM can be implemented at very high speed. We demonstrated a prototype implemented in 0.13μm CMOS that was successfully tested up to 12.5Gb/s and provides up to 68dB output error dynamic range.

Finally, we introduced a novel architecture for instantaneous clockless demultiplexing. Instantaneous data acquisition is required in burst-mode communication systems, where the data stream arrives at the receiver in asynchronous packets separated by unknown quiet intervals. The conventional narrowband phase-locked loops require a long preamble with large acquisition time and are therefore not suitable. As an alternative to gated oscillators that require a full-rate clock for operation, we proposed a clockless finite state machine that recovers and demultiplexes the received burst of data instantaneously. The architecture consists of a combinational logic structure with immediate response and a bit-period-delayed feedback loop. Therefore, every time a burst is received, the operation is initiated exactly in-phase with the first bit and continues synchronously to the stream. We implemented a 1:2 clockless demultiplexer based on this concept in SiGe BiCMOS technology and verified its operation at 7.5Gb/s.

7.2 Directions for Future Work

We have investigated the underlying principles of high-speed wireline communications and have developed a general relationship between the data link reliability and the system parameters. One direction that can be pursued for future research to expand this work is to include other impairments in high-speed link and to complete the model for calculation of the BER. The most significant effect that we neglect in this thesis is nonlinearity of the channel or the transceiver. For instance, in long-haul optical communication, the deployment of optical amplifiers for boosting the optical power may force the fiber into its nonlinear regime that will affect the signal integrity. Furthermore, some of the receiver blocks, and particularly the main amplifier that succeeds the pre-amplifier, is typically a high-gain nonlinear block for limiting the signal amplitude. Therefore, it should be modelled by a slew rate-limited system as opposed to an LTI system. The impact of such systems on the ISI and timing jitter and ultimately the way they affect the BER is an important and interesting subject for future research that expands the results of this thesis.

This work relates the time response of an arbitrary LTI system to the ISI that results from that system. Therefore, the analytical results for calculating the BER, in general, and the data-dependent jitter, in particular, are based on the time response of the system. From a circuit design perspective, it is also interesting and useful to derive such analytical results for the frequency response, *i.e.*, both the amplitude response and the phase response, of the system. The relationship between the circuit parameters and the frequency response are conventionally studied more rigorously and are better documented, *e.g.*, the theory of poles and zeros or the tables of filter design. For instance, the design of an amplifier is more straightforward if the specifications are presented in terms of the maximum ripple in the amplitude and group delay response, as opposed to specifying the maximum values for the samples of the pulse response.

Two important topics related to the proposed eye-opening monitor (EOM) circuit that require further investigations are the optimization algorithm and the loop dynamics of an adaptive equalizer that uses the EOM. The algorithm can be chosen freely because it is separate from the hardware of the filter. However, convergence speed is a practical constraint that may eliminate probabilistic algorithms such as the genetic algorithm or the simulated annealing algorithm. On the other hand, the cost function, *i.e*, the EOM output, does not have a known direct relationship with the optimizing parameters, *i.e.*, the filter coefficients. Therefore, application of gradient descent-based algorithms is not straight forward. As a result, understanding the trade-offs for the choice of the algorithm is a topic of interest for future research in this area.

Understanding the loop dynamics of the adaptive equalizer is important for guaranteeing convergence and controlling the speed of convergence. The EOM is a nonlinear system and its impact on the loop dynamics should be studied carefully. Particularly, the required mask error rate dynamic range, which determines the integration time for each mask, and the number of masks, which determines the resolution of the mask error rate, are among the parameters whose relationships to the loop dynamics should be investigated.

Possible future directions for enhancing the design of the proposed instantaneous demultiplexer include targeting accurate delay implementation and low-power design. Absolute value of the feedback loop delay is the only parameter that determines the operating bit rate of the demultiplexer. The loop delay includes the delay of the feedback delay cells, the propagation delay of the combinational logic, and the delay of the interconnect parasitic components. The optimum way to adjust the loop delay and accurately control the delay value is to form a delay reference loop by a replica of the demultiplexer that is configured as a ring oscillator. The oscillating frequency of this ring oscillator is determined by the same parameters that set the delay value of the loop. Consequently, if the frequency is adjusted accurately in the delay reference loop, the feedback delay will be determined with the same accuracy. Finally, the demultiplexer design was not optimized for minimum power consumption. The power consumption also affects the heat generated by the demultiplexer chip that sets the local temperature around the active devices and impacts their propagation delay. Therefore, controlling the power consumption can improve the operation of the block.

All in all, the thesis provides insight and develops useful tools and techniques for designing high-speed wireline communication systems using integrated circuit technologies.

Appendix A

Overall BER Calculation

In this appendix we calculate the overall BER when both timing jitter and ISI are present. To calculate the probability of error for the current bit that is being sampled, we have to take into account the value of the next bit and the previous bit. This is in order to add the impact of the timing jitter of the transitions before or after the current sampling on the BER. Therefore, we should consider 3-bit sequences, where the middle bit is the one being sampled. Out of the eight possibilities, we only need to calculate the BER for four sequences of “000,” “001,” “100,” and “101.” Each of the other four cases, where the middle bit is “1,” equals one of the sequences with “0” as the middle bit because of the symmetry and is thus found automatically. Therefore, we have

$$BER(T_s) = \frac{1}{4}[BER(T_s|''000'') + BER(T_s|''001'') + BER(T_s|''100'') + BER(T_s|''101'')] . \tag{A.1}$$

The error for the first term on the right is caused only by the ISI and noise because there is no transition. Hence, we can write

$$BER(T_s|''000'') = BER(ISI_0(T_s)) . \tag{A.2}$$

In the second sequence, “001,” one transition occurs to the next bit. Because of the timing jitter the transition can occur before or after the sampling point, T_s. If the transition occurs after the sampling point, the BER is not affected by it because we assume the system is causal. On the other hand, if the transition takes place before the sampling point, the receiver samples $ISI_0(T_s)+s(T_s-t_R)$. The random variable t_R denotes the location of the transition on the right of the current bit. It has a mean value equal to T_b. Therefore, the overall BER for the “001” sequence can be found as a conditional probability conditioned on t_R as

$$BER(T_s|''001'') = \begin{cases} BER(ISI_0(T_s)) & t_R \ge T_s \\ BER(ISI_0(T_s) + s(T_s - t_R)) & t_R < T_s \end{cases} . \tag{A.3}$$

If we assume t_R has the probability distribution function $f_t(t_R)$, we have

$$BER(T_s|''001'') = BER(ISI_0(T_s))\int_{T_s}^{\infty} f_t(t_R)dt_R + \int_{-\infty}^{T_s} f_t(t_R) \cdot BER(ISI_0(T_s) + s(T_s - t_R))dt_R . \tag{A.4}$$

We can calculate the BER for the "100" sequence similarly. However, the location of the transition only affects the BER if it occurs before the sampling point, because it changes the amount of the ISI_1 at the sampling point. We have

$$BER(T_s|''100'') = \begin{cases} BER(ISI_1(T_s - t_L)) & t_L < T_s \\ BER(ISI_1(T_s) + s(T_s)) & t_L \ge T_s \end{cases} \tag{A.5}$$

$$BER(T_s|''100'') = BER(ISI_1(T_s) + s(T_s))\int_{T_s}^{\infty} f_t(t_L)dt_L + \int_{-\infty}^{T_s} f_t(t_L) \cdot BER(ISI_1(T_s - t_L))dt . \tag{A.6}$$

For the "101" sequence we have both the left and right transitions. However, the right transition does not impact the BER if $t_R > T_s$ because the system is causal. In that case, the BER is equivalent to the BER for the "100" sequence. On the other hand, if $t_R < T_s$, we also implicitly know that $t_L < T_s$. We can write

$$BER(T_s|''101'') = \begin{cases} BER(T_s|''100'') & t_R > T_s \\ BER(T_s|''100'', t_L < t_R < T_s) & t_R < T_s \end{cases} . \tag{A.7}$$

Therefore, we have

$$BER(T_s|''101'') = BER(T_s|''100'')\int_{T_s}^{\infty} f_t(t_R)dt_R + \int_{-\infty}^{T_s} f_t(t_R) \cdot \left(\int_{-\infty}^{T_s} f_t(t_L) \cdot BER(ISI_1(T_s - t_L) + s(T_s - t_R))dt_L \right) dt_R \tag{A.8}$$

We assume the timing jitter distribution is Gaussian with means of zero and T_b, for t_L and t_R, respectively, and standard deviation of σ_j. In addition, we assume the noise distribution is Gaussian with zero mean and standard deviation σ_n. Therefore, all the BER terms in the above equations will be in the form of a $Q(.)$ function, where $Q(.)$ is the cumulative distribution function of the Gaussian distribution. We can approximate some of the BER terms in (A.4), (A.6), and (A.8) by *one*. This applies to all the terms where the argument of the BER, *i.e.*, the argument of the $Q(.)$, is large due to the effect of the step response, *e.g.*, in $BER(ISI_0(T_s)+s(T_s\text{-}t_R))$. Then, we estimate the overall BER by replacing (A.2), (A.4), (A.6), and (A.8) in (A.1). We get

$$BER(T_s)=$$

$$\frac{1}{4}\left[\left(Q\left(\frac{0.5-ISI_0(T_s)}{\sigma_n}\right)+\int_{-\infty}^{T_s} f_t(t_L)\cdot Q\left(\frac{0.5\text{–}ISI_1(T_s-t_L)}{\sigma_n}\right)dt_L\right)\cdot\left(1+Q\left(\frac{T_s-T_b}{\sigma_j}\right)\right)+Q\left(\frac{T_s}{\sigma_j}\right)+Q\left(\frac{T_b-T_s}{\sigma_j}\right)\right] \quad . \tag{A.9}$$

We have also neglected all the second-order terms that include products of two $Q(.)$ functions.

In reality, the total jitter distribution should also include the effect of the DDJ, as we discussed in Chapter 3. Here, we investigate how the DDJ affects each of the terms in (A.1). The DDJ does not have any impact on the $BER(T_s|$ “000”) because “000” has no transitions. In the “001” sequence, there is a “01” transition with a “0” as the penultimate bit. Therefore, $f_t(t_R)$ should be modified to a Gaussian with the mean of $T_b+t_{c,0}$. The $t_{c,0}$ is defined in (3.22) and is calculated in Appendix B.

We do not have the knowledge of the penultimate bit for the transition in “100,” in contrast to the “001” case. Therefore, to calculate $BER(T_s|$ “100”), the previously Gaussian distribution for $f_t(t_L)$ should be modified by convolving it with a double Dirac delta function DDJ distribution. Finally, both the $f_t(t_R)$ and $f_t(t_L)$ should be modified to calculate $BER(T_s|$ “101”). The $f_t(t_R)$ distribution becomes a Gaussian with the mean of $T_b+t_{c,1}$, because the penultimate bit to the “01” transition is now “1.” The $t_{c,1}$ is defined in (3.23) and is calculated in Appendix B. The $f_t(t_L)$ distribution convolves with a double Dirac delta function DDJ distribution. Therefore, the resulting overall BER is

$$
\begin{aligned}
&BER(T_s)= \\
&\frac{1}{4}\left\{\left(Q\left(\frac{0.5-ISI_0(T_s)}{\sigma_n}\right)\cdot\left(1+Q\left(\frac{T_s-T_b-t_{c,0}}{\sigma_j}\right)\right)+Q\left(\frac{T_b+t_{c,0}-T_s}{\sigma_j}\right)\right.\right. \\
&\left.+\left[\int_{-\infty}^{T_s} f_t(t_L)\cdot Q\left(\frac{0.5-ISI_1(T_s-t_L)}{\sigma_n}\right)dt_L\right]\cdot\left(1+Q\left(\frac{T_s-T_b-t_{c,1}}{\sigma_j}\right)\right)+\frac{1}{2}Q\left(\frac{T_s-t_{c,0}}{\sigma_j}\right)+\frac{1}{2}Q\left(\frac{T_s-t_{c,1}}{\sigma_j}\right)\right\}
\end{aligned}
\quad .\text{(A.10)}
$$

Appendix B

Threshold-Crossing Time

In this appendix we calculate $t_{c,0}$ and $t_{c,1}$, defined in (3.22) and (3.23), for a first-order system. We can show

$$t_0 = \tau \cdot \ln 2 . \tag{B.1}$$

We also have

$$\Delta t\big|_{a_{-2} = 0} = -\tau \cdot \ln\left(1 - (1-\alpha)\sum_{k' = -\infty}^{-2} a_{k'} \cdot \alpha^{-k}\right) \tag{B.2}$$

$$\begin{aligned}\Delta t\big|_{a_{-2} = 1} &= -\tau \cdot \ln\left(1 - \frac{(1-\alpha)}{\alpha}\left[\alpha^2 + \alpha\sum_{k' = -\infty}^{-2} a_{k'} \cdot \alpha^{-k}\right]\right) \\ &= -\tau \cdot \ln\left(1 - \alpha + \alpha^2 - (1-\alpha)\sum_{k' = -\infty}^{-2} a_{k'} \cdot \alpha^{-k}\right) \\ &= -\tau \cdot \ln(1 - \alpha + \alpha^2) + (-\tau) \cdot \ln\left(1 - \left(\frac{1-\alpha}{1-\alpha+\alpha^2}\right)\sum_{k' = -\infty}^{-2} a_{k'} \cdot \alpha^{-k}\right) .\end{aligned} \tag{B.3}$$

We define a new discrete random variable Φ as follows

$$\Phi \equiv \sum_{k = -\infty}^{-2} a_k \cdot \alpha^{-k} = a_{-2} \cdot \alpha^2 + \sum_{k = -\infty}^{-3} a_k \cdot \alpha^{-k} . \tag{B.4}$$

After reorganizing the terms in the sum and renumbering the indices we have

$$\Phi = a_{-2} \cdot \alpha^2 + \alpha \sum_{k' = -\infty}^{-2} a_{k'} \cdot \alpha^{-k} \tag{B.5}$$

where $k' = k + 1$. As the a_k's are independent identically distributed (iid) random variables, the sum in the second term on the right is, by definition in (B.4), a random variable with identical statistical properties to *Φ*. Specifically, all the statistical moments are equal for the two random variables. If we denote this new random variable by Φ', we have

$$\Phi = a_{-2} \cdot \alpha^2 + \alpha\Phi' . \tag{B.6}$$

Also, note that Φ' and a_{-2} are independent random variables. Now we can write

$$E\{\Phi\} = E\left\{a_{-2} \cdot \alpha^2 + \alpha\Phi'\right\} = \alpha^2 E\{a_{-2}\} + \alpha E\{\Phi'\} . \tag{B.7}$$

We know that $E\{\Phi\} = E\{\Phi'\}$. We also assume

$$p(a_k = 1) = p(a_k = 0) = 0.5 . \tag{B.8}$$

Then, we have

$$E\{a_{-2}\} = 1/2 \times 0 + 1/2 \times 1 = 1/2. \tag{B.9}$$

Replacing into (B.7) we will get

$$E\{\Phi\} = \frac{1}{2} \cdot \frac{\alpha^2}{1 - \alpha} . \tag{B.10}$$

The second-order moment can be calculated from (B.6) as follows

$$E\{\Phi^2\} = \alpha^4 \cdot m_2 + 2\alpha^3 m_1 E\{\Phi\} + \alpha^2 E\{\Phi^2\} \tag{B.11}$$

$$E\{\Phi^2\} = \frac{1}{1 - \alpha^2}(\alpha^4 \cdot m_2 + 2\alpha^3 m_1 E\{\Phi\}) = \frac{0.5\alpha^4}{(1 - \alpha)(1 - \alpha^2)} \tag{B.12}$$

in which m_i is the *i*th order moment of a_{-2} and *E{Φ}* is known from (B.10). It is easy to show m_i=1/2 for all *i*. Similarly, the *k*th order moment can be written as follows

$$E\{\Phi^k\} = \frac{0.5}{1-\alpha^k}\sum_{i=0}^{k-1}\binom{k}{i}\alpha^{2k-i}E\{\Phi^i\}. \tag{B.13}$$

This gives a recursive expression based on lower-order moments. Now, we can calculate

$$E\left\{\Delta t\big|_{a_{-2}=0}\right\} = E\{-\tau\cdot\ln(1-(1-\alpha)\Phi)\} \tag{B.14}$$

$$E\left\{\Delta t\big|_{a_{-2}=1}\right\} = -\tau\cdot\ln(1-\alpha+\alpha^2) + E\left\{\ln\left(1-\left(\frac{1-\alpha}{1-\alpha+\alpha^2}\right)\Phi\right)\right\}. \tag{B.15}$$

From (B.4) we know $\Phi \le \frac{\alpha^2}{1-\alpha}$ where the maximum occurs when all a_k's are "1." In addition, T_b/τ is positive and so $\alpha \le 1$. Therefore,

$$|(1-\alpha)\Phi| \le \frac{\alpha^2}{1-\alpha}\cdot(1-\alpha) = \alpha^2 \le 1. \tag{B.16}$$

Similarly,

$$\left|\left(\frac{1-\alpha}{1-\alpha+\alpha^2}\right)\Phi\right| \le \frac{\alpha^2}{1-\alpha}\cdot\left(\frac{1-\alpha}{1-\alpha+\alpha^2}\right) = \frac{\alpha^2}{1-\alpha+\alpha^2} \le 1. \tag{B.17}$$

Hence, we can use the Taylor series expansion of the natural logarithm to estimate (B.14) and (B.15). We have

$$\ln(1-x) \cong -\sum_{k=1}^{\infty}\frac{x^k}{k}. \tag{B.18}$$

Therefore,

$$E\left\{\Delta t\big|_{a_{-2}=0}\right\} = \tau\cdot\sum_{k=1}^{\infty}\frac{1}{k}(1-\alpha)^k E\{\Phi^k\} \tag{B.19}$$

$$E\left\{\Delta t|_{a_{-2}=1}\right\} = -\tau\cdot\ln(1-\alpha+\alpha^2) + \tau\cdot\sum_{k=1}^{\infty}\frac{1}{k}\left(\frac{1-\alpha}{1-\alpha+\alpha^2}\right)^k E\{\Phi^k\}\,. \qquad \text{(B.20)}$$

We can approximate (B.19) and (B.20) by neglecting all the moments of *Φ* for $k>2$ because we can show that the kth moment is proportional to the kth power of α and thus shrinks exponentially. Then we have

$$E\left\{\Delta t|_{a_{-2}=0}\right\} \cong \tau\cdot\left[(1-\alpha)E\{\Phi\} + \frac{1}{2}(1-\alpha)^2 E\{\Phi^2\}\right] = \frac{\tau}{2}\cdot\left[\alpha^2 + \frac{0.5\alpha^4}{1+\alpha}\right] \qquad \text{(B.21)}$$

$$\begin{aligned} E\left\{\Delta t|_{a_{-2}=0}\right\} &\cong \tau\cdot\left[\left(\frac{1-\alpha}{1-\alpha+\alpha^2}\right)E\{\Phi\} + \frac{1}{2}\left(\frac{1-\alpha}{1-\alpha+\alpha^2}\right)^2 E\{\Phi^2\}\right] - \tau\cdot\ln(1-\alpha+\alpha^2) \\ &= \frac{\tau}{2}\cdot\frac{\alpha^2+0.5\alpha^4+\alpha^5}{(1+\alpha^3)\cdot(1-\alpha+\alpha^2)} - \tau\cdot\ln(1-\alpha+\alpha^2)\ \cdot \end{aligned} \qquad \text{(B.22)}$$

Finally, $t_{c,0}$ and $t_{c,1}$ can be found by replacing (B.1), (B.21), and (B.22) in (3.22) and (3.23).

Appendix C

Impedance Function

An impedance function is a rational function (ratio of two polynomials with real coefficients) of frequency with no right half-plane poles. Additionally, the numerator polynomial should be of at most one degree higher than the denominator one. The conditions for an impedance function can be found in [26][96]. The upper-bound in (4.2) is not valid if the load does not satisfy the conditions of an impedance function. In other words, if the overall transfer function of an amplifier is of the form:

$$A_v(j\omega) = g_m \cdot Z(j\omega) \tag{C.1}$$

and $Z(j\omega)$ is *not* an impedance function, then the Bode-Fano limit need not be satisfied. Distributing passive structures between gain stages can result in overall transfer functions that are *not* impedance functions *per se* [23]. Therefore, the GBW product can potentially be higher than the limit in (4.2). One design approach for such a structure is stagger tuning of the frequency responses. An early amplitude roll-off due to a low-frequency pole in one stage can be compensated for with a peaking in the next stage. Similarly, the overall phase response of passive structures can be properly controlled.

Appendix D

Mask Error Rate

We assume that the amplitude noise cumulative distribution function is $Q(.)$. The probability of occurring a mask error is

$$MER = Pr\{S_H \neq S_L\}, \tag{D.1}$$

where $Pr\{.\}$ denotes probability and S_H and S_L are defined in Section 5.3. S_H and S_L take binary values and thus there are two combinations that contribute to (D.1). The conditional probability of each of the combinations can be calculated, given the input bit to the EOM. Therefore we have

$$MER = \frac{1}{2}\cdot\left(Pr\left\{ S_H = 0\ S_L = 1 \;\middle|\; in = 1+z\right\} + Pr\left\{ S_H = 0\ S_L = 1 \;\middle|\; in = z\right\}\right., \tag{D.2}$$
$$\left. + Pr\left\{ S_H = 1\ S_L = 0 \;\middle|\; in = z\right\} + Pr\left\{ S_H = 1\ S_L = 0 \;\middle|\; in = 1+z\right\}\right)$$

where z is the input noise at the sampling point. When the EOM is ideal, only input noise impacts S_H and S_L values. The last two terms in (D.2) will be identically zero because they both imply $V_H < V_L$. The first two terms both equal the probability that

$$\frac{1-(V_H - V_L)}{2} < z < \frac{1+(V_H - V_L)}{2}. \tag{D.3}$$

Hence, we can write

$$MER = Q\left(\frac{1-(V_H - V_L)}{2\sigma}\right) - Q\left(\frac{1+(V_H - V_L)}{2\sigma}\right) \cong Q\left(\frac{1-(V_H - V_L)}{2\sigma}\right). \tag{D.4}$$

When the impact of EOM is considered, the last two terms in (D.2) are not identical to zero anymore because S_H and S_L are the output of two comparators with different noise contribution. However, we can still neglect them in MER calculation for reasonable noise levels in the comparators. The first term in (D.2) can be written as

$$Pr\left\{ S_H = 0\ S_L = 1 \middle| in = 1 + z \right\} = Pr\left\{ S_H = 0 \middle| 1 + z \right\} \cdot Pr\left\{ S_L = 1 \middle| 1 + z \right\}. \quad \text{(D.5)}$$

Because of the bandwidth limitations of the comparators, the probabilities on the right side of (D.5) are functions of the sampling time and are smaller when sampling time is closer to the data edge. If the response of the comparators to the input is denoted by $y(t)$ we have

$$y(t) = \sum_i A_i(t) . \quad \text{(D.6)}$$

We define $A_i(t)$ as the response of the comparators to the input in a unit interval, $(i-1) \cdot T_b < t < i \cdot T_b$, where T_b is the bit period. Several $A_i(t)$ exist due to various combinations of symbols that cause ISI. The overlap of $A_i(t)$'s for all i when transformed to $0 < t < T_b$ is the eye diagram. If we limit ISI to the last n symbols only 2^n distinct $A_i(t)$ could be achieved for a binary modulation. Then from (D.5) we can write

$$MER \cong \frac{1}{2^n} \sum_{i=1}^{2^n} Q\left(\frac{A_i(t) - (V_H - V_L)}{2\sigma}\right) \cdot \left(1 - Q\left(\frac{A_i(t) + (V_H - V_L)}{2\sigma}\right)\right). \quad \text{(D.7)}$$

For simplicity we rewrite (D.7) as

$$MER \cong Q\left(\frac{A(t) - (V_H - V_L)}{2\sigma}\right) \cdot \left(1 - Q\left(\frac{A(t) + (V_H - V_L)}{2\sigma}\right)\right), \quad \text{(D.8)}$$

where the sum is implicit in the notation. Equation (D.7) can be used to generate a 2D map of the MER.

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