SILICON NANOWIRES AND SILICON/MOLECULAR INTERFACES FOR NANOSCALE ELECTRONICS

Thesis by

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In Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy

CALIFORNIA INSTITUTE OF TECHNOLOGY

Pasadena, California

2009

(Defended June 11, 2008)

To my best friend and husband,

Bryan

Acknowledgements

I am so grateful to the many people who enriched my experiences at Caltech. First, I would like to thank my advisor, Professor Jim Heath, whose dedication to the pursuit of scientific understanding has been truly inspirational. I am indebted to his support and guidance over the last 5 years. I also would like to thank my thesis committee for their support and insights into my graduate research: Prof. Mitchio Okumura, Prof. Pat Collier, and Prof. Bill Goddard.

I was blessed to be surrounded by many excellent colleagues. I would like to acknowledge the support and assistance of several current and past Heath group members: Dunwei Wang, whom I learned so much from; Yi Luo, a true mentor for so many; and Johnny Green, Erica DeIonno, Gabe Kwong, Rosemary Rohde, Heather Agnew Akram Boukai, Habib Ahmad, Kris Beverly, Ryan Bailey, Mike McAlpine, and John Nagarah, for their friendship, guidance, and for making going to work so much fun. I also would like to thank Rosemary Rohde and Heather Agnew for their help with surface chemistry techniques and acknowledge Will Dichtel, Jason Spruell, and Dorota Rozkiewicz for their contributions with the microcontact printing project. Thanks to Ruo-Gu Huang, Peigen Cao, and Clara Ji-Hyun Cho for continuing the logic and microcontacting printing projects. I owe a big thanks to Diane Clark-Robinson for running the group efficiently and for keeping things interesting, and Kevin Kan, the guardian of the cleanroom and its equipment.

When I was an intern at Intel, I had the pleasure of working with several friendly and extremely helpful colleagues. In particular, I would like to thank Juanita Kurtin,

Janice Lee, Keith Bowman, Ravi Pillarisetty, and Tanay Karnik. I would also like to acknowledge the Intel Foundation for providing financial support during the last two years here in the form of a Ph.D. Fellowship.

I would like to acknowledge my friends at Caltech who made my experiences here so much better. In particular, I would like to thank Heather Wiencko, Christina Vizcarra, and Amie Boal for their support and friendship.

Finally, I would like to thank my husband, Bryan, who has been a source of unlimited love, friendship, laughter, support, and motivation.

Abstract of the thesis

The thesis describes the realization of high-performance silicon nanowire (Si NW) logic circuits and a novel surface modification technique for nanoscale electronics applications. First, doped Si NWs were generated via the superlattice nanowire pattern transfer (SNAP) process, forming aligned, uniform, ultra-dense NW arrays. The NWs served as the channel material for field-effect transistors. NWs could be doped n- or p-type using a diffusion doping process and both n-FETs and p-FETs could be fabricated simultaneously on the same substrate.

Individual p-FETs exhibited excellent performance metrics compared to other NW and carbon nanotube (CNT) transistors, including high on/off ratios, low off currents, high mobilities, and low subthreshold swings. The n-type devices also had good characteristics, although they did not perform as well as the p-FETs. A comparison of nanowire and microwire device performance revealed that the NW FET performance was dominated by the high surface-area-to-volume ratio. These devices were integrated into complementary symmetry (CS) inverter circuits, which showed a consistent performance and a gain (a measure of performance) of ~ 5.

Circuit performance was optimized by utilizing a methodology that combined prototype devices with circuit simulations. First, prototype devices were fabricated and their DC and AC characteristics were tabulated into a look-up-table model. This model was accessed by a circuit simulator, which could predict the performance of arbitrary circuits utilizing these devices and provide feedback into the device design. Circuits could then be fabricated from the optimized devices resulting in increased performance.

This methodology was demonstrated by optimizing the gain of the CS inverter circuit from an initially measured value of 8 to a gain of 45.

A novel microcontact printing method was developed to functionalize gold and silicon surfaces. The copper^{I}-catalyzed azide-alkyne cycloaddition (CuAAC) reaction was used to covalently attach molecules containing an alkyne functional group to azide-terminated monolayers on gold or silicon. The copper^{I} catalyst in the ink solution (homogeneous catalyst) was replaced by coating the elastomer stamp with copper metal (heterogeneous catalyst). The copper-coated stamp was shown to catalyze the reaction to completion within 1 hour with a zero-order reaction rate. In comparison, the homogeneous catalyzed stamp reaction took ~ 30 minutes to complete with a pseudo first-order reaction rate. No pattern diffusion was observed, suggesting that free copper ions are not responsible for the catalysis. It is proposed that this method can be used to sequentially synthesize electronically active molecules directly onto gold or silicon electrodes.

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Chapter 1

Thesis Overview

1.1 Introduction to nanoelectronics

Nanoelectronics is an emerging field whose goal is to surpass existing ultra-large-scale integration (ULSI) technology in device size, density, and performance. This is indeed a challenge, as current silicon ULSI technology has been improving at an aggressive rate since the manufacture of the first integrated circuit (IC) in 1959.[1, 2] In 1965, the co-founder of Intel, Gordon Moore, made the famous prediction that the number of transistors in an IC would double approximately every 24 months.[3] This prediction has astonishingly held true for the past 40 years. IC technology has rapidly progressed from small scale integration (SSI) in the 1960s, with less than 30 transistors per chip, to the current technology, ULSI, with over 1,000,000 transistors per chip.

The success of Moore's law has been due to three factors.[4] First, the size of the transistor, the active element in ICs, has steadily decreased. The Intel Corporation's

current 45 nm technology contains transistors with a physical gate length of ~ 22 nm. In contrast, the gate length of the state-of-the-art transistors in 2001 was ~ 5.5 times larger. Also, the area on which the transistor sits has decreased by a factor of 30.[5] Second, the size of ICs has also increased. This has been due to both increasing the size of Si wafers and improving the capabilities of the fabrication tools. Lastly, the architecture of ICs has improved and fewer transistors are required to perform a specific function.

However, the conventional lithography techniques used to produce modern ICs will not be able to indefinitely shrink transistor size or increase density. The United States Semiconductor Industry Association, a nonprofit organization that assesses the future semiconductor industry's technology requirements and publishes the International Technology Roadmap for Semiconductors (ITRS), has stated it will be a "difficult challenge" to progress complementary metal oxide semiconductor (CMOS) technology beyond the 22 nm technology generation.[6] This challenge has stimulated intense research for alternatives to conventional, planar Si transistors.

The next-generation devices will most likely be based on non-planar structures such as double-gate FETs[7, 8] and fin-FETs,[9, 10] as well as on non-Si electronic materials, such as III-V compound semiconductors.[11–13] However, both of these technologies rely on an enhancement of individual device performance (such as increased mobility, lower leakage current, or higher drive current)[9, 14] and do not solve the issues of the size and density limitations.

To directly address these challenges, novel nanoscale transistor channel materials, such as semiconducting nanowires (NWs)[15–18] and carbon nanotubes (CNTs)[19–25] are also being explored. These materials are attractive because they have very narrow diameters

and have no density limitations since they are not fabricated using conventional lithography techniques. NWs and CNTs can also exhibit enhanced electronic behavior due to their highly confined nature, such as a high intrinsic mobility[17, 26] and enhanced phonon drag.[27] Additionally, these materials possess other interesting properties due to quantum confinement effects and their high surface area-to-volume ratios, which can be exploited in other fields, such as chemical and biological sensing,[28, 29] superconductivity,[30] and thermoelectrics.[27, 31]

Another class of nano-materials that will become increasingly more important for electronics applications are molecules. Individual molecules represent the ultimate scaling of electronic components and are fabricated using a bottom-up approach. Single molecules and monolayers can be used as the active electronic element or they can be used to enhance the properties of other nanoscale materials. For instance, molecules have been exploited as an active element for high-density logic and memory circuits.[32, 33] Examples of ways that molecular films can enhance other devices include passivating NW surfaces,[34] acting as gate dielectrics,[35, 36] and being the capture agents in sensors.[28, 37]

NWs, CNTs, and molecular films for electronics are still in the development stage and have not yet been fully utilized for any commercial application. The major problems associated with using these materials include difficulty in placing and aligning devices, controlling surface properties, and reducing variability in performance. For instance, the synthesis of single-walled CNTs will produce a distribution of diameters and chirality, which has profound affects on their electrical properties.[26, 38] Even if a synthetic approach yielded identical tubes, it is still prohibitively difficult to align these devices into a working circuit that is competitive, in terms of density or number of devices, with

CMOS technology. To fully utilize these nanoscale materials, the ITRS has summarized several challenges that must be addressed (Table 1.1):[6]

Table 1.1. Summary of nanoscale material challenges. Table adapted from Ref [6], Table ITWG6. Issues highlighted in blue are specifically addressed in this thesis.

Difficult Challenges ≤ 22 nm	*Summary of Issues*
Control of nanostructures and properties	Ability to pattern sub-20-nm structures in resist or other manufacturing related patterning materials (resist, imprint, self-assembled materials, etc.) (Chapter 2) Control of surfaces and interfaces (Chapter 2) Control of CNT properties, bandgap distribution, and metallic fraction Control of stoichiometry and vacancy composition in complex metal oxides Control and identification of nanoscale phase segregation in spin materials Control of growth and heterointerface strain Ability to predict nanocomposite properties based on a "rule of mixtures" Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability (Chapter 4) Control of interface properties (e.g., electromigration)
Control of self assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components (Chapter 3) Control of line width of self-assembled patterning materials (Chapter 5) Control of registration and defects in self-assembled materials
Compatibility with CMOS processing	Integration for device extensibility (Chapter 2) Material compatibility and process temperature compatibility (Chapters 2, 3)
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures (Chapter 5) Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability (Chapters 2, 3)

The goal of this thesis is to provide solutions to several of the challenges associated with working with nanoscale materials. The specific challenges that were addressed in this work are highlighted in blue in Table 1.1. In Chapter 2, a method is described that generates silicon nanowires (Si NWs) with a high control over their

placement, alignment, and doping and surface properties. Field-effect transistors (FETs) utilizing the NWs as the channel material were found to have high performance metrics and consistent behavior. In Chapter 3, the NW FETs were utilized for complementary symmetry logic circuits, which required precise alignment of devices and interconnects. In Chapter 4, these circuits were optimized by utilizing a strategy that coupled prototype devices with device and circuit simulations. Lastly, in Chapter 5, the silicon/molecular interface was manipulated by microcontact printing methods for molecular electronics applications. These advancements show that nanoscale materials *can* be highly controllable and that nanoscale electronics is a realizable technology.

1.2 Organization of the thesis

This thesis is organized into four main chapters. Each chapter was written to be largely self-contained and complete. To avoid excessive redundancy, lengthy information that is required in a later chapter of the thesis was occasionally referenced to an earlier chapter.

Inverters with Gain. *Small* **2006**, 2, 1153–1158.

1.2.1 Summary of Chapter 2

Chapter 2, titled "High-performance nanowire field-effect transistors", discusses the development of high-performance n- and p-type field effect transistors (FETs) from Si NWs generated from the superlattice nanowire pattern transfer (SNAP) process.[17, 18] The SNAP process produces ultra-dense arrays of metal or Si NWs at 33 nm pitch with virtually no defects using a template-mediated approach.[39] The NWs are doped by using conventional diffusion doping on the substrates prior to the NW formation.[40] The development of the SNAP process and the diffusion doping technique are introduced in the chapter. These technologies were the key behind the fabrication of NW FETs with consistent behavior and strong performance metrics, such as high on/off ratios, high mobilities, and small subthreshold swings.

Another important aspect to generating successful NW FETs was exploring methods to control the properties of the NW surface. A comparison of NW and microwire (μW) FET performance revealed that the NW FET performance is dominated by the properties of the surface. Reducing the amount of surface states increased the performance of the NW FETs significantly. This laid the foundation for developing complementary symmetry (CS) logic circuits from these devices.

1.2.2 Summary of Chapter 3

Once NW FETs were developed, their integration into CS circuits was explored in Chapter 3, titled "Fabrication and characterization of complementary nanowire logic circuits".[18] To achieve side-by-side p- and n-FETs on a single substrate, two technologies were developed: a patterned doping technique that allowed for spatial control of doped regions, and a SNAP master alignment system that facilitated the precise placement of NWs on the substrate. These technologies allowed the n- and p-FETs to be fabricated with precise control over location and alignment on a single substrate. The pattern doping technique was characterized using electrostatic force microscopy and by testing fabricated pn diodes. The inverter circuit, which represents the most basic Boolean logic function and consists of 1 p-FET and 1 n-FET,[41] was fabricated and tested. A gain of ~ 5 was consistently measured from 7 working inverter circuits. This demonstration provided the foundation for the eventual fabrication and characterization of the other Boolean logic functions.

1.2.3 Summary of Chapter 4

In Chapter 4, "In silico design optimization of nanowire circuits", a methodology is described that optimizes the design of high-performance logic circuits constructed from Si NW p- and n-type FETs.[42] Although NW circuits were demonstrated in the previous chapter, improving their performance is difficult and time consuming. In this methodology, circuit performance can be predicted from individual fabricated NW FETs before prototype circuits are manufactured, resulting in a faster and more efficient design process. NW FETs are fabricated and electrically characterized, the results of which are

placed into a circuit simulation environment. Next, a variety of DC and transient analyses can be performed for various circuit designs, and various circuit metrics can be optimized in silico. These results suggest design options for fabricating high performance NW circuits, which can then be implemented experimentally. The effectiveness of this methodology is shown by optimizing the gain of Si NW complementary symmetry inverter from an initially measured value of 8 to a gain of 45.

1.2.4 Summary of Chapter 5

Chapter 5, "Microcontact printing methods for molecular electronic applications", discusses efforts to develop methods to covalently attach electronically interesting molecules onto gold and silicon substrates. These methods utilized an elastomer stamp coated with reactive molecules. Pressing the stamp to a monolayer-covered substrate encourages the covalent attachment of the reactive molecules to the monolayer due to the highly concentrated environment. In these studies, the Cu^{I}-catalyzed azide-alkyne cycloaddition (CuAAC) reaction was used to form the covalent attachment. It was observed that the reaction would proceed readily by replacing the Cu catalyst in the stamp ink (the homogeneous catalyst) by a Cu coating on the stamp directly (the heterogeneous catalyst). Kinetics were monitored using ferrocene as the attached species and electrochemical measurements, and it was shown that the heterogeneous catalyst proceeded almost as quickly as the homogeneous catalyst (30 minutes versus 60 minutes). This reaction proceeded quickly on both azide-terminated monolayers on Au and Si(111) substrates.

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Chapter 2

High-performance nanowire field-effect transistors

2.1 Introduction

Semiconductor nanowires (NWs)[1, 2] have attracted significant interest because of their potential for a variety of different applications, including logic and memory circuitry, photonics devices, and chemical and biomolecular sensors.[3–6] Although many different types of semiconductor NW have been investigated, silicon NWs have become prototypical nanowires because they can be readily prepared, the Si/SiO_2 interface is chemically stable, and Si NWs are utilized in a number of device demonstrations that have well-known silicon-technology-based counterparts.[3, 7, 8] Various techniques have been developed to synthesize semiconductor NWs, including the materials method known as vapor-liquid-solid (VLS) growth,[3, 7] and the templating method known as superlattice nanowire pattern transfer (SNAP).[9, 10] Each method has its advantages. The VLS technique can produce bulk quantities of semiconductor NWs, but those NWs are

characterized by a distribution of lengths and diameters, and they also must be assembled into the appropriate device structure (or the device structure must be constructed around the nanowire[11]). However, VLS NWs may be prepared with various doping configurations,[12] and they may be studied on a variety of different substrates.[13]

The SNAP process, which will be described in detail in the next section, can be applied to the production of both metal and semiconductor NWs. Those NWs are characterized by extremely narrow width distributions, they can possess aspect ratios of up to 10^6, and they are prepared as highly defined arrays with near atomic control over NW width and pitch.[9, 10] In addition, the growth of VLS Si NWs relies upon a metal particle to seed the growth, and that particle can also serve as an impurity dopant.[7] SNAP Si NWs, by contrast, are prepared from thin film materials, and so the purity of the NW is limited only by the purity of the thin film. In any case, the ultimate test of the quality of a NW is based upon its electronic properties. For VLS Si NWs, field effect transistors (FETs) with high mobilities and low subthreshold swings have been reported.[8, 13] The DC transport characteristics of heavily doped SNAP Si NWs have been reported, and those wires exhibited bulk-like conductivity characteristics.[14] A key toward achieving that result was the use of spin-on-dopants (SODs). SODs, which have found uses in devices such as thin film transistors,[15, 16] provides a means for controlling doping levels while avoiding the damage that can occur through alternative methods, such as ion implantation.

In this chapter, the doping and fabrication processes were optimized for the production of SNAP Si NW FETs. P-type FETs exhibited high carrier mobilities, high on-current, excellent on/off ratios, and a low subthreshold swing of hole carriers. N-type

FETs showed consistent performance and also exhibited good performance metrics. These results reveal that the SNAP Si NWs have low defects, low surface and interface states, and can operate as high-performance FETs.

2.1.1 The SNAP technique

The key enabling technology for high-performance nanowire logic is the superlattice nanowire pattern transfer (SNAP) technique developed by Melosh et al. in 2003.[9] In this technique, Si NWs are formed from silicon-on-insulator (SOI) substrates using a template-mediated, top-down fabrication process. In this section, the process for generating SNAP NWs is qualitatively described and the full experimental details appear in Section 2.2.2.

First, superlattices (SLs) consisting of alternating GaAs and $Al_xGa_{(1-x)}As$ layers are grown via molecular-beam epitaxy (MBE). The SL wafer is carefully cleaved to form an atomically flat edge. The SLs are then diced into small pieces called "masters" (Figure 2.1A). Each master is carefully cleaned to remove any dust particles from the cleaved edge and then immersed in an etch solution that selectively etches back the $Al_xGa_{(1-x)}As$ layers, leaving behind GaAs ridges (Figures 2.1B, 2.2A, and 2.2B). Metal is then anisotropically deposited onto the cleaved edge of the master, forming metal NWs along the GaAs ridges (Figure 2.1C). The SL containing the metal NWs are transferred onto the SOI substrate and adhered via an epoxy layer (Figure 2.1D). The SL is removed using a chemical etch process, leaving behind the metal NWs on the substrate (Figure 2.1E). The metal NWs act as a physical etch mask and the pattern is transferred into the Si epilayer using a reaction-ion-etching process (Figure 2.1F). Lastly, the metal NWs are

removed by dissolving them in acid. The resulting substrate consists of Si NWs on an insulating layer (Figure 2.2C and 2.2D).

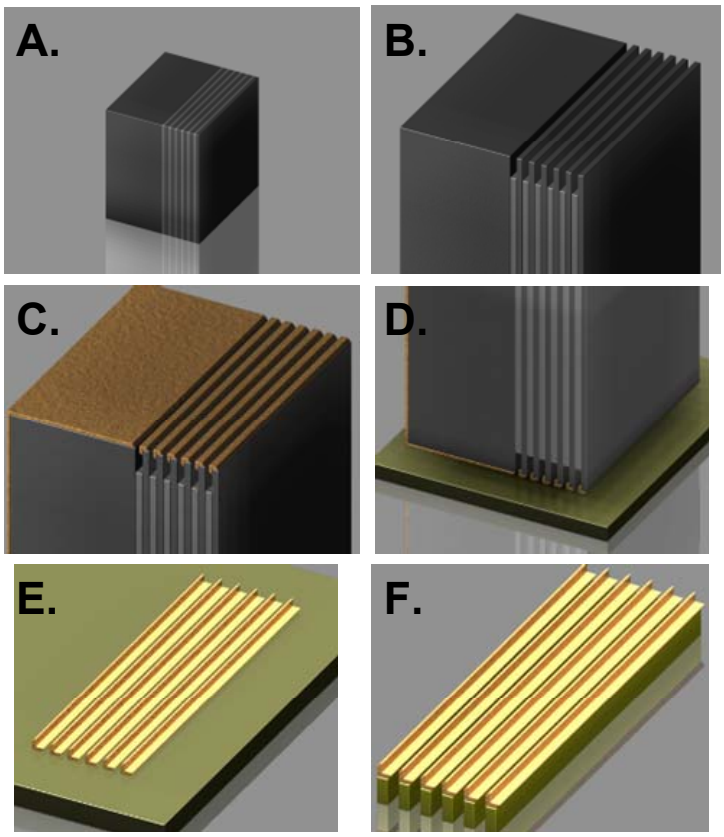

Figure 2.1. The SNAP process. **A.** First, the MBE-grown superlattice (SL) is cleaved, exposing the alternating GaAs/$Al_xGa_{(1-x)}As$ layers. **B.** Next, $Al_xGa_{(1-x)}As$ layers are selectively etched, leaving behind GaAs ridges. **C.** Metal is then anisotropically deposited onto the surface of the SL, forming metal NWs on the GaAs ridges. **D.** The metallized surface of the SL is then put in contact with an SOI substrate. **E.** The metal NWs are transferred using a wet-etch process. **F.** The NW pattern is transferred into the underlying Si epilayer using a reactive-ion etch and the metal NWs are removed

Metal and semiconducting NWs have been generated using this technique with NW widths and full-width pitches down to 8 nm and 16 nm, respectively.[9] Each NW can be as long as several millimeters. Arrays of up to 1400 NWs have been fabricated, however, SLs that generated 400 NW arrays with a 33 nm pitch were used for all of the devices in this thesis. The key strength of this technique is that the formation and the alignment of the NWs occur in a single step. Other methods of non-lithographic NW

formation (such as VLS) require a separate alignment step that all but precludes the fabrication of ordered, highly dense arrays. Another key advantage to this technique is that NW doping can be performed by doping the SOI substrate prior to NW formation. Additional details are discussed in the following section.

Si NWs produced by the SNAP technique have been used in several applications beyond logic circuits, including crossbar molecular memory circuits,[17] a binary-tree demultiplexing scheme,[10] biomolecular[18] and chemical[19] sensors, thermoelectrics,[20, 21] and superconductivity studies.[22] They are currently being used for novel photovoltaic applications.

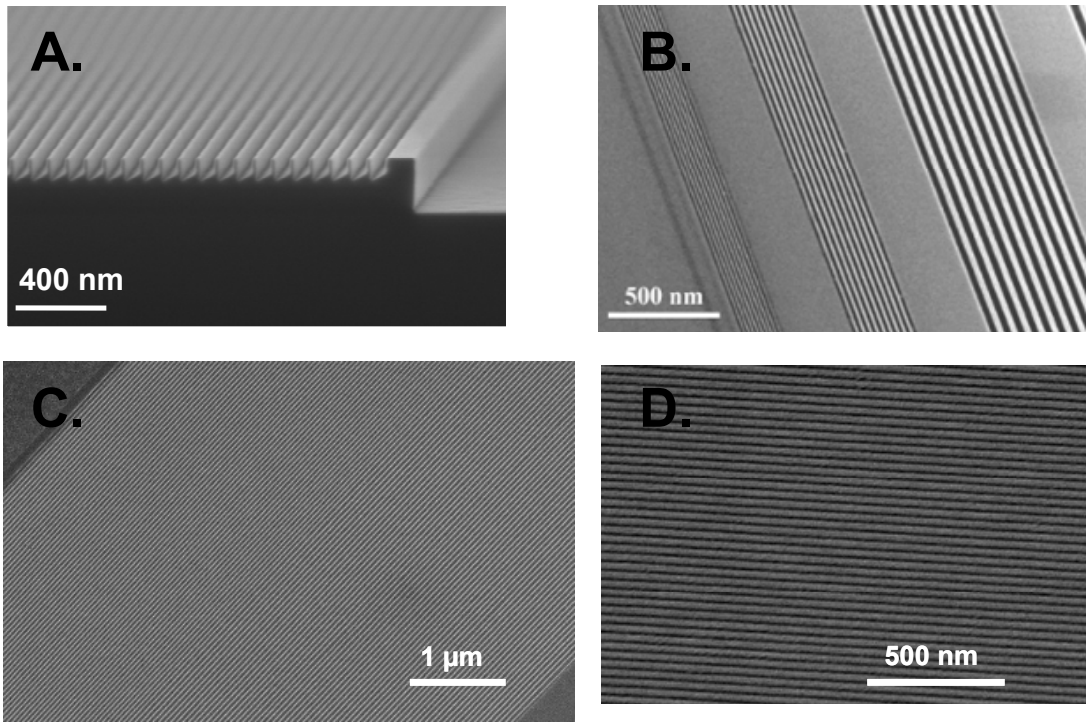

Figure 2.2. Scanning electron micrographs of the SNAP SL and the Si NWs. **A.** Side view of an etched SNAP master. **B.** Top view, highlighting the control over NW width and pitch. **C.** 128 Si NW array produced using the SNAP technique. **D.** Close-up of a 400 Si NW array

2.1.2 Conducting Si nanowire arrays

To fully utilize the SNAP-generated Si NW arrays, it is necessary that they have conductivity comparable to bulk Si. In 2004, Beckman et al. investigated optimizing the choice of substrate, substrate doping, and NW etching steps to maximize NW conductivity.[14] First, the choice of substrate proved to be a critical factor. Si NWs were produced from 4- and 8-inch SIMOX SOI wafers and their conductivities were compared to NWs produced from a high-quality MBE-grown wafer containing a p-type Si epilayer. 10 to 20 nm wide NWs were formed from each substrate using the same fabrication process. Figure 2.3 shows the NW resistance normalized to the bulk-scaled resistance for each substrate.

The 8 inch SOI wafer, which is more commonly used in the semiconductor industry, was shown to match the performance of the NWs generated from the MBE-grown substrate, which had bulk-like conductivity.

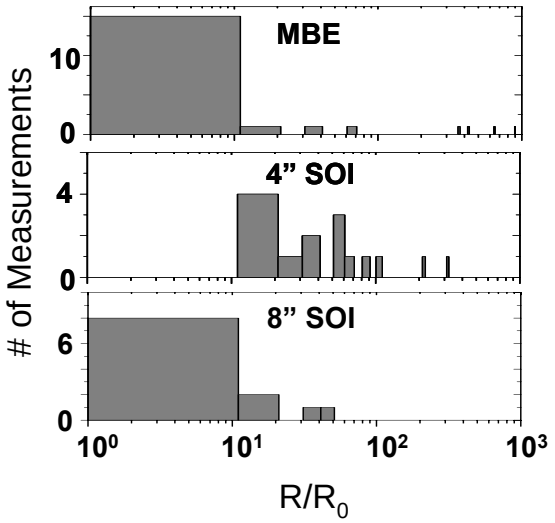

Figure 2.3. NW resistance normalized to the bulk-scaled resistance for NWs formed on 4- and 8-inch SIMOX SOI wafers and on an MBE-grown wafer

An additional factor that contributed to achieving bulk-like conductivity in SNAP-generated NWs was the method used to dope the substrate. Commercially available ion-implanted wafers produced NWs with degraded conductivity when their widths were below 50 nm. This conductivity improved substantially by utilizing diffusion doping. It is hypothesized that ion implantation causes irreversible damage to the Si epilayer lattice, which directly influences carrier transport in nanoscale devices.

Lastly, it was determined that the method to etch the Si NWs was important for maintaining high conductivity. As described in the previous section, reactive-ion etching is employed to transfer the metal NW pattern into the Si epilayer. A RIE system utilizing a high-frequency power supply enables stable plasma formation at low DC bias. This was shown to produce smooth NW sidewalls with no noticeable undercut. The optimizations done for this paper were a key foundation for producing high-performance nanowire transistors and, later, logic circuits.

2.1.3 Organization of the chapter

The next section describes the full fabrication process for the NW FETs. Details are provided on the diffusion doping, SNAP, and device fabrication processes. This information is also used as the foundation for the circuits discussed in Chapters 3 and 4. Next, the results of the p-FET characterization are discussed. Transistor metrics such as mobility and subthreshold swing are defined and calculated for several devices, and the role of surface states on device performance is explored. Lastly, the performance characteristics of NW n-FETS are discussed. The n-FETs did not perform as well as their p-FET counterparts but exhibited consistent performance. A side-by-side comparison of nanowires and microwires was done to determine the cause of this behavior discrepancy.

2.2 Nanowire field-effect transistor fabrication

The fabrication of high-performance Si NW field-effect transistors (FETs) is described in this section. Although FETs using SNAP NWs as the channel material had been previously demonstrated,[10, 14] these devices were not optimized for performance or for use in logic circuits. Several parameters were explored to optimize performance: the substrate doping process, the device fabrication process, and methods to reduce surface states. The first two parameters are discussed in the next two sections. The last parameter is discussed in Section 2.3.

2.2.1 Substrate doping process

As discussed in Section 2.1.2, diffusion doping gave superior NW conductivity results over ion implantation.[14] The diffusion doping process involves exposing the surface of the Si substrate to a high concentration of dopant atoms at an elevated temperature (usually close to 1000°C). The high temperature creates vacancies in the crystal lattice and the impurity atoms diffuse into the Si lattice by hopping into these vacancies.[23] In comparison, ion implantation involves accelerating a beam of dopant ions to high kinetic energies towards the Si surface. The dopant ions come to rest within the Si lattice. The advantage of this technique is that the dopant profile within the Si substrate can be well controlled. However, ion implantation causes lattice damage and a subsequent thermal anneal is needed to restore the lattice. For decreasing device size, the effect of these lattice defects becomes magnified and for nanoscale structures, ion implantation becomes an unsuitable technique.

For the diffusion doping, spin-on dopants (SODs) were used as the dopant source, which consists of a high concentration of dopant ions within a silica matrix. The SODs are diluted in a solvent and are spin-coated onto the surface. The solvent is removed by heating the Si substrates to 100–200°C, which causes the silica matrix to densify. The coated substrates are then annealed via a tube furnace or a rapid thermal processor (RTP). Lastly, the SODs are removed post-anneal using HF or buffered oxide etch (BOE) (6:1 NH_4F:HF).

Eight inch SIMOX SOI wafers were purchased (Simgui, Shanghai, China) consisting of a 32 nm epilayer of intrinsic Si in the <100> orientation and a 150 nm buried oxide layer on a ~ 0.5 mm thick Si substrate. The best method for cleaning the substrate prior to diffusion doping is the RCA cleaning method, which consists of immersing the substrates in three solutions: 5:1:1 H_2O: H_2O_2: NH_4OH at 80°C for 10 minutes; 1:10 BOE: H_2O at room temperature for 30 seconds; and 5:1:1 H_2O: H_2O_2: HCl at 80°C for 10 minutes. Cleaning the substrates with heated ALEG-355 (Mallinckrodt Baker, Phillipsburg, NJ) or heated acid "piranha" (3:1 H_2SO_4: H_2O_2) also yields good results. It is important that the cleaned substrates be hydrophilic prior to applying the SOD.

Several commercially available SODs were tried and recipes that correlated anneal times and temperatures to measured substrate resistivities were tabulated. To guide the development of RTP recipes, the 1-D diffusion model was used to calculate the dopant profile in Si, *C(d,t,T)*:[24]

$$C(d,t,T) = C_S erfc\left(\frac{d}{2\sqrt{D(T)t}}\right). \tag{2.1}$$

Here, *erfc* is the complementary error function, C_S is the concentration of dopant atoms on the silicon surface, *D(T)* is the diffusivity coefficient, and *t* is the anneal time. *D(T)* is empirically determined for each type of dopant atom. The calculated dopant profiles for boron diffusion at 1000°C ($D = 2 \times 10^{-14}$ cm^2/s)[25] for various anneal times are shown in Figure 2.4. Since *D(T)* has an exponential dependence on *T*, *C(d,t,T)* varies more as a function of *T* than anneal time, and thus the RTA recipes were developed more as a function of anneal temperature than anneal time.

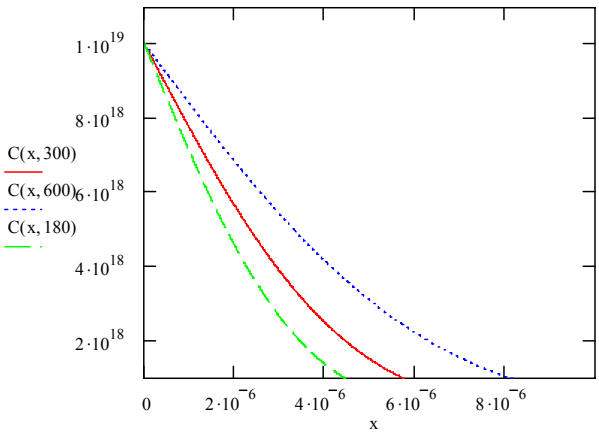

Figure 2.4. Boron concentration as a function of Si depth, for an anneal temperature of 1000°C and for 180, 300, and 600 second anneal times

The two commercially available SODs that yielded the best results were Emulsitone (Whippany, NJ) phosphorosilicafilm 5×10^{20} (the number denotes the phosphorous ion concentration in cm^{-3}), diluted 10-fold in cleanroom-grade methanol, and Filmtronics, Inc. (Butler, PA) Boron A, used without any modification. The SODs can be filtered prior to application but this step is not necessary. The SODs were spin-coated onto the substrates at 4000 RPM for 30 seconds and the substrates were then placed on a pre-heated hotplate set to 100°C. The hotplate temperature was increased to 200°C and the samples were heated for 10 minutes. This temperature ramp is an neccessary step to ensure gas bubbles do not get trapped in the densified SOD.

The substrates were annealed using a tube furnace or a rapid thermal processor (RTP) (RTP 600s System, Modular Process Technology Corp.). The RTP was vastly

superior to use in terms of its temperature control, programmability, sample loading, user interface, consistent performance, and in its ability to anneal under various gas compositions. To anneal using the RTP, substrates were placed on a clean Si wafer and loaded into the RTP chamber. The temperature was monitored by a pyrometer that monitored the temperature of the backside of the Si wafer. Samples were annealed under a flow of N_2. Once the chamber temperature cooled to below 100°C, the samples could be safely unloaded.

The final and most difficult step in the diffusion doping process is removing the SOD post-anneal. During the high-temperature anneal, the SOD matrix densifies further, and for SODs containing organic species such as Boron A, difficult to remove organic films can develop on the Si surface. The best method for removing the SOD and any organic contaiminants without damaging the Si epilayer was the following sequence: 30 seconds BOE immersion, brief DI H_2O immersion, vigorous H_2O rinse using a high-pressure spray gun, immersion in acetone accompanied by surface swabbing, acetone rinse, and another vigorous H_2O rinse. By repeating this sequence, most SODs will be removed without damaging the surface with at most ~ 2 minutes of total BOE exposure.

The impurity concentration of doped substrates was calculated from a four-point resistivity measurement. In this measurement, four aligned metal probe tips with a few mm spacing are brought into contact with the doped substrate. A constant current is passed between the two outer probes and the voltage is measured between the two inner probes. This setup effectively counteracts any probe contact resistance and for thin wafers (where the length and width of the substrate is much larger than the thickness), the sheet resistance, R_S, can be calculated as:[26]

$$R_S = \frac{V}{I} CF \,. \tag{2.2}$$

CF is the correction factor and can be approximated as 4.54 for wafers much larger than the spacing between the probe tips.

To obtain the resistivity, ρ, of the wafer, the sheet resistance is multiplied by the thickness of the Si epilayer:

$$\rho = R_S W \,. \tag{2.3}$$

The resistivity can be used to determine the impurity concentration in the substrate by applying an empirical formula that relates to the two parameters or by a look-up table.[26] Note that this technique does not give any information on the dopant profile through the Si epilayer and that this technique is measuring impurity concentration, not carrier concentration (which are only equal in the case that 100% of the impurities are ionized). However, this method does provide a quick and easy measurement for approximating doping levels.

The four-point measurements were performed using a probe card or a home-built system and a Keithly 2400 SourceMeter (Keithley Instruments, Inc.) operating in four-point mode. The typical current sourced was 100 μA and a minimum of three areas on each substrate were measured, to verify homogeneous doping.

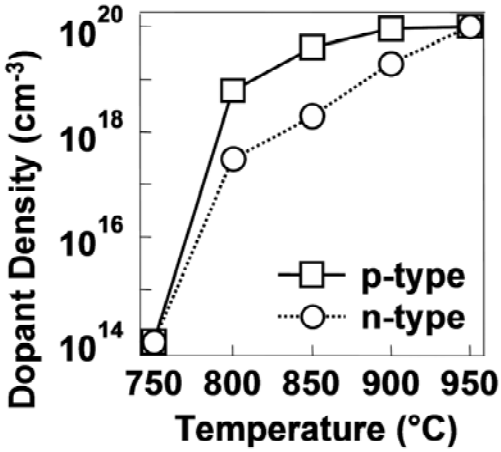

Figure 2.5. Doping levels of boron (p-type) and phosphorous (n-type) under various diffusion temperatures. For all processes, the diffusion time is fixed at 3 minutes.

Samples were annealed for 3 minutes

at temperatures between 750–950°C. The resistivity results were compiled into a graph (Figure 2.5). For various applications, the appropriate doping conditions can be looked up in this plot and selected accordingly.

2.2.2 SNAP technique experimental details

The SNAP technique, qualitatively described in Section 2.1.1, was performed on the doped SOI substrates. A custom-made superlattice (SL) consisting of 800 layers of alternating GaAs and $Al_{0.8}Ga_{0.2}As$ layers grown on top of a (100) GaAs substrate (IQE, Ltd. Cardiff, UK). The superlattice was cleaved in the {110} or {001} plane, forming an atomically flat edge, and diced into ~ 2 mm wide and ~ 5 mm long pieces, referred to as the SNAP masters. The cleaving and dicing processes generate GaAs particles that contaminate the SL. The SNAP masters were sonicated in cleanroom-grade methanol and the cleaved plane was swabbed to remove any contamination visible under 160× magnification.

Once the majority of the particles are removed from the cleaved edge, the SNAP masters were immersed in $NH_4OH/H_2O_2/H_2O$ (1:20:750 v/v) for ~ 10 seconds to selectively etch the $Al_{0.8}Ga_{0.2}As$ regions, followed by an immersion in 30% H_2O_2 for ~ 5 seconds. This second immersion removes residual Ga particles that form on the SL after the etching process.[27] After the etching process, the resulting SL etch consists of GaAs ridges separated by $Al_{0.8}Ga_{0.2}As$ recessions. Pt metal was deposited using e-beam evaporation onto the edge of the GaAs ridges, with the edge of the superlattice held at a 45° angle to the incident flux of Pt atoms. The angle of 45° prevents the Pt from filling in the $Al_{0.8}Ga_{0.2}As$ recessions and determines the Pt NW width.

The doped substrates were prepared by first removing any particles by swabbing the surface in methanol and drying with N_2. The cleaned substrates were coated with a heat-curable epoxy film via spin-coating at 6000–8000 RPM for 30 seconds. The epoxy formulation used is modified from a commercially available epoxy formulation, Epoxy Bond 110 (Allied High Tech, Rancho Dominguez, California). The formulation that yielded the best results was: 5 drops of Epoxy Bond part A, 1 drop of Epoxy Bond part B, and 2 drops of dibutyl phthalate (used as a plasticizer) in 10 mL of anhydrous tetrahydrofuran (THF). The spin-coating speed varies depending on the size of the substrate (large substrates required slower speeds) and is a critical parameter for ensuring successful SNAP results.

Immediately following the spin-coating process, the cleaved edge of the SNAP master was brought into contact with the substrate. The SL/epoxy/SOI assembly was dried on a hot plate (85°C, 30 minutes) and the SL was then released by a selective etch in a concentrated H_3PO_4: 30% H_2O_2: DI H_2O (5:1:50 v/v) solution or a commercially available Au etch solution (containing KI and I_2 in H_2O), leaving a highly aligned array of 400 Pt NWs on the surface of the SOI substrate.

The Pt nanowires served as masks for a reactive ion etch (RIE) process to produce aligned, single-crystal Si NWs. To remove the residual epoxy, the samples were exposed to an O_2/Ar plasma (60 W, 5 mTorr), produced by a 40 MHz Unaxis SLR parallel-plate RIE system. The Si epilayer was then etched using a CF_4/He plasma at 40 W and 5 mTorr for approximately 4 minutes (interferometry can be used to determine the etch time). This plasma recipe generates smooth NW sidewalls with no observable undercutting and no degradation in conductivity. Finally the Pt nanowires were then

removed using aqua regia (4:1 conc. HCl: conc. HNO_3) at 120°C for 10 minutes to produce a ultra-dense array 400 Si NWs at a pitch of 34 nm and width of 17 nm. Residual epoxy can be removed by soaking the substrates in hot ALEG for 30 minutes.

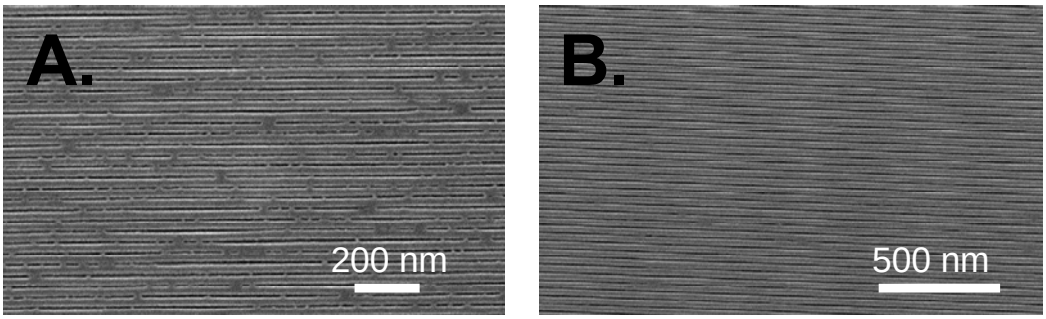

Figure 2.6. Scanning electron micrographs of Si NW arrays before and after surface treatment. **A.** Micrograph of NW array that is shorted together due to problems in the epoxy consistency. **B.** Treatment with an O_2 plasma oxidation and diluted BOE dip removes shorts.

Typically several SNAP masters will be used during the SNAP process to produce several NW arrays on multiple substrates. The typical yield of usable arrays from all the SNAP masters used is 50–80%. The loss of usable arrays was due to a variety of reasons. One common failure is that the SNAP master falls off the substrate during the Pt NW transfer, and no NWs are transferred to the substrate. This is due to particulates between the SNAP master and substrate, which prevents the master from making good contact with the thin epoxy layer. Another failure mode is when the NWs are transferred into the Si epilayer but are shorted together. This is due to a problem in the epoxy consistency. However, this failure can be corrected in some cases. Figure 2.6A shows an example of a NW array containing several shorts. These shorts are significantly narrower than the NWs themselves. After a brief oxidation using an O_2 plasma, followed by a brief dip in 1:100 BOE:H_2O, these shorts are removed (Figure 2.6B) and these NWs are recovered.

2.2.3 Fabrication and measurement of the FET structure

The SNAP process yields a continuous array of NWs that extends over a few millimeters. The first step in fabricating useful devices was to separate the NW arrays into discrete sections. Separated arrays of NWs that are 10–20 μm long were formed by patterning Al sections over portions of the NWs using electron beam lithography (EBL) and electron beam metal deposition. The Al protected the wires underneath from an SF_6 plasma (20 mTorr, 10 W) that removed any exposed Si NWs. The Al was subsequently removed using PAE (80% H_3PO_4 5% CH_3COOH 5% HNO_3 10% H_2O). Alignment markers were carefully patterned around each NW array section, which were then used to pattern source (S) and drain (D) electrodes over the NW sections.

Several different metals were investigated to obtain an ohmic contact to the NWs, such as Ti, Al, Cr, Ni, and Pt. The contacts material that yielded the best results was 10–20 nm Ti (used as an adhesion layer) and 50 nm Pt. Figure 2.7 shows ~ 0.5 μm wide Ti/Pt contacts on Si NWs. The NWs appear brighter between the metal contacts due to their conductivity. Ti/Al/Pt, Cr/Al/Pt, and Ni yielded very poor contacts that could not improved by annealing. Prior to metal deposition, the EBL exposed areas were briefly dipped in 100-fold diluted BOE, which flushes out organic contaminants and removes the native SiO_2. This step was crucial for obtaining ohmic contacts. Several device widths and channel lengths were also explored.

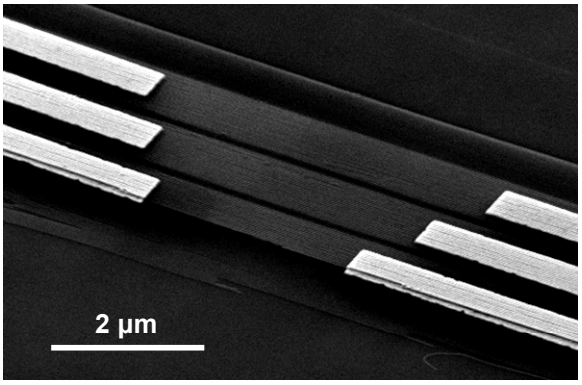

Figure 2.7. Scanning electron micrograph of EBL-patterned electrodes on NWs. NW conductivity is indicated by the brighter areas between the contacts.

On a typical ~ 13 μm wide section of NWs, three S/D electrodes can be patterned to form three FETs with a shared top-gate electrode. Because of the patterning limitations of EBL, the best devices were fabricated from contacts that were over 100 nm wide and with channel lengths of at least 500 nm.

After the S/D contacts were formed, the devices were annealed in the RTP at 475°C for 5 minutes in forming gas (95% N_2 5% H_2). This anneal helped improve the ohmic contacts and reduced the number of surfaces states on the NW channel. The effect of this anneal, which proved to be invaluable for obtaining good device metrics, is discussed further in Section 2.3.

To fabricate the top gate dielectric, 10 nm of Al_2O_3 was deposited at a rate of 0.1Å/s by electron beam evaporation using an Al target in the presence of O_2. The measured dielectric constant of the oxide is ~ 3.7 (see Section 4.2.2 for more details), which is well below the expected value for Al_2O_3. Attempts to improve the dielectric by investigating film thickness, O_2 flow rate, and chamber pressure did not yield any significant improvements. A low chamber pressure (5×10^{-7} Torr) with a moderate-to-high flow rate (+5 to +9 sccm) gave the best results. Increasing the chamber pressure decreased the quality of the Al_2O_3 (as monitored by device on/off ratio) and increasing both chamber pressure and O_2 flow

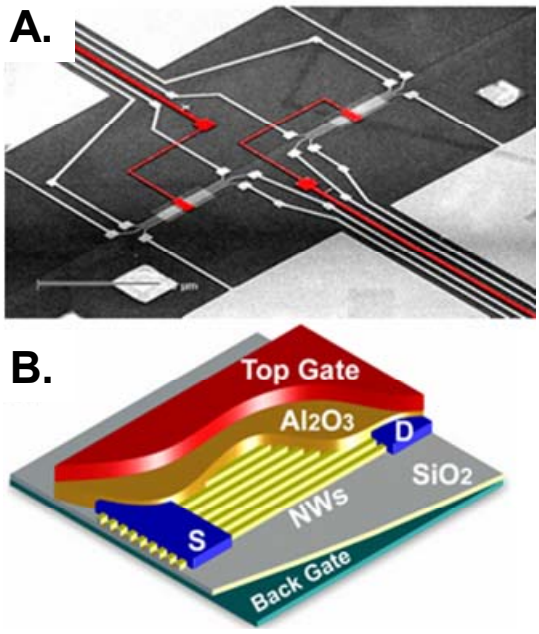

Figure 2.8. NW FET structure. **A.** SEM image of a few devices with top gate color-coded red. Scale bar: 50 μm. **B.** Schematic drawing of the active area of a Si NW FET, with the electrodes labeled.

rate resulted in significant current leakage through the oxide. HfO_2 films were also attempted using electron beam evaporation. All deposited HfO_2 films exhibited significant current leakage.

The last step in the NW FET fabrication process was the formation of the top gate electrode. For the majority of NW FETs, the top gate electrode was patterned using EBL and deposited with 10 nm Ti and 50 nm Pt. The final fabricated FET structure is shown in Figure 2.8A and the idealized device structure is depicted in Figure 2.8B.

To make external electrical contact to the fabricated devices, each electrode fanned out to a 50 × 50 μm contact pad. Devices were contacted using probe tips in a grounded probe station. The S/D contact pads could be contacted through the deposited Al_2O_3 by gently scratching away the oxide using the probe tip. Source to drain current was measured as a function of gate to source and drain to source voltage using using Keithley 2400 SourceMeters and LabVIEW programs (National Instruments).

2.3 Development of high-performance nanowire p-FETs

Once the doping, SNAP, and device fabrication processes were optimized, high-performance NW p-FETs were developed.[28] NW p-FETs consisting of ~ 8 NWs were fabricated with a channel length of 4 μm and a doping level of ~ 10^{18} cm^{-3}. At this doping level, the mobility for bulk Si is ~ 100 cm^2/V-s.[29] Higher doping levels lead to lower mobilities and less gate modulation, and lower doping levels lead to reduced on-current values.

These devices were characterized by utilizing the underlying Si wafer as a bottom gate electrode (Figure 2.9A and 2.9B). Large variations in on-current and on/off switching amplitudes characterized these devices, suggesting the possible presence of defects within the Si lattice or on the surface. Defects can damage performance in a number of ways: they can act as scattering centers that reduce carrier mobilities (leading to lower transconductance and lower on-current values) and they can also serve as charge traps that degrade gating efficiency (poorer on/off ratios and large subthreshold swings).[26]

The performance of the NW p-FETs could be improved significantly with a forming gas (FG) anneal (Figure 2.9A and 2.9C).[29] Prior to gate formation, the NW devices were annealed in FG at 475°C for 5 minutes in the RTP. Prior to annealing, surface adsorbed H_2O could be removed by spin-coating 3% PMMA onto the devices and baking at 130°C for 30 minutes.[28] This was done to eliminate oxidation and charge traps caused by the H_2O.[30] Another method to ensure dry surfaces to simply bake them on a hotplate set to a temperature higher than 100°C for at least 10 minutes. This method can

be used prior to FG anneals and also prior to applying the SOD (but ensure that the wafer has cooled back to RT first).

Once the FG anneal is performed, back-gate FET performance of as-fabricated and annealed devices was compared. Significant improvement in the on/off ratio and the on-current was observed in the annealed devices (Figure 2.9A and 2.9C). This behavior was consistent for over 20 devices made. It was observed that the off-current remained low (~ 100 pA) for all of the measured devices. Longer annealing times did not improve the performance further and high anneal temperatures (650°C) resulted in device degradation. Annealing in pure N_2 yielded at best a marginal improvement in device performance.

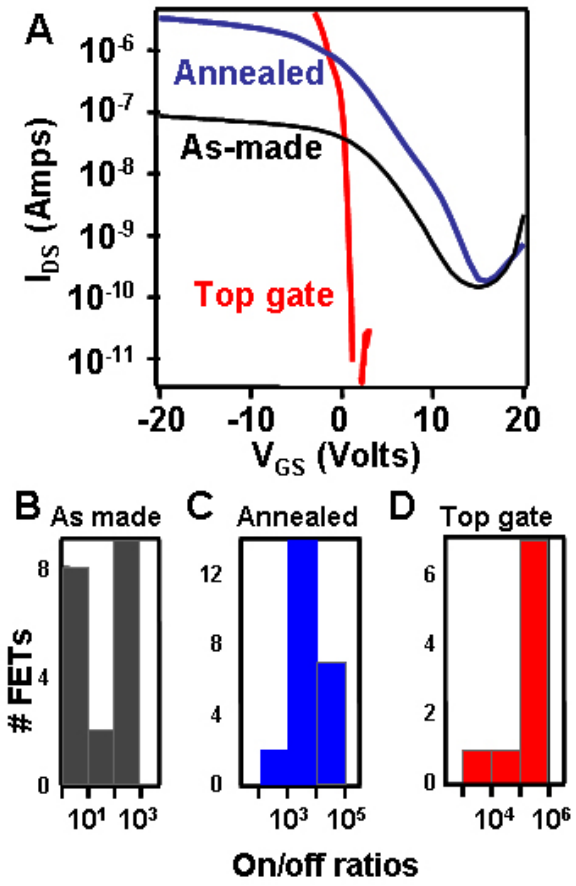

Figure 2.9. Performance characteristics of Si NW FETs for different processing conditions and device configurations. **A.** Source-to-drain (I_{DS}) current values versus applied gate voltages for an as-prepared, back-gated FET (black trace), a back-gated FET post-forming gas anneal (red trace), and a top-gated FET post-forming gas anneal. **B.–D.** Histograms for each of the device parameters shown in A, but representing statistical numbers of device measurements. Relatively fewer top-gate devices were measured due to the fabrication yield of the top-gate processing steps.

The observed improvement of the Si NW FETs following the annealing step can originate from either the removal of Si/SiO_2 interfacial states, or through the promotion of an ohmic contact at the S/D electrodes. It is well known that an FG anneal can reduce defects in Si MOSFETs.[26, 29]

During annealing, Si/SiO_2 interface dangling bonds are terminated by hydrogen from the forming gas and charge traps diffuse out, directly leading to increased on-current and improved on/off ratios.

The effect of promoting an ohmic contact at the NW/contact interface would be a decreased Schottky barrier height. This would typically be manifested as an improved on-current. It is unlikely, however, to significantly reduce off-current. It was observed that similar device performance enhancements (i.e., higher on-current and higher on/off ratios) could be obtained by carrying out the forming gas anneal of the SNAP Si NWs prior to metal contact deposition. Therefore, it is speculated that the charge trap removal plays the most important role. However, since surface states also reside at the NW/contact interface, it is predicted that there is an improvement in electrical contact as well. Cui et al. have also reported on the effectiveness of a much higher temperature forming gas anneal on VLS grown Si NW FETs.[8]

Annealed devices were next characterized after the fabrication of the top gate (see Section 2.2.3 for experimental details). In comparison to the bottom gate devices, the off-current of top-gated devices is greatly decreased, hence increasing the on/off ratios by more than one order of magnitude (Figures 2.9A and 2.9D). This originates not only from an improved gating efficiency through the thin Al_2O_3 dielectric, but also from the diffusion-based SOD doping process. As described in Section 2.2.1, the distribution of dopants through the thickness of the NWs follows the 1D diffusion model.[10, 26, 29] Therefore, most of the carriers reside near the top surface of the NWs, making a gate modulation from the top more effective. This is in accordance with the observations of

improved top-gated devices (Figure 2.9A) and indicates that the SOD doped Si NWs are ideal for a top-gated high-performance FET device.

Another way to illustrate this point is to compare the NW FET I_{DS}-V_{GS} curves using both top-gate and back-gate modulations. V_{GS} sweeps were performed for various back-gate biases and it was observed that the back gate had a negligible effect on the transistor curves (Figure 2.10). Since the buried oxide layer is significantly thicker than the Al_2O_3 layer (150 nm as opposed to 10 nm) and the dopants have the highest concentration on the surface of the NWs, the relative weakness of the back gate was expected.

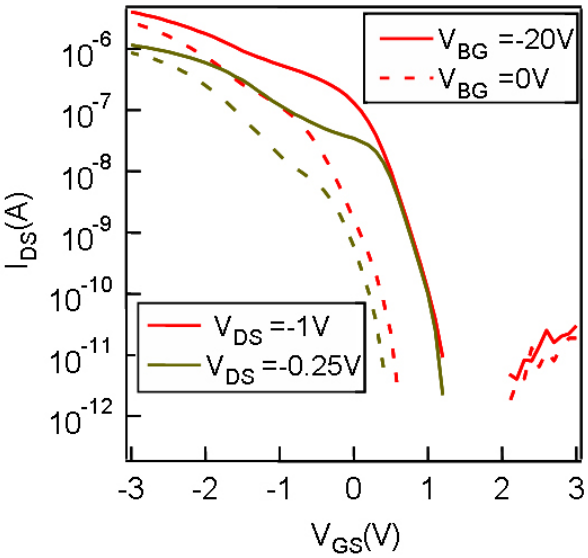

Figure 2.10. I_{DS}-V_{GS} curves with both top-gate (V_{GS}) and back-gate (V_{BG}) modulation

Typical drain current versus gate voltage (I_{DS}-V_{GS}) and I_{DS} versus drain voltage (V_{DS}) data are plotted in Figure 2.11. Several transistor metrics can be extracted from these plots. First, the on-current of the devices is high. As shown in Figures 2.9A and 2.9B, 5 μA on-current through an individual device consisting of ~ 8 NWs was measured. Considering each NW is ~ 17 nm wide × 30 nm high in cross section, the current density equals ~ 1.3 mA/μm^2. Note that this does not represent a fully saturated current value since the V_{DS} values were kept below a certain voltage to prevent any breakdown events in the channel. Furthermore, the 30 nm height does not account for the doping gradient through the thickness of the NWs. This implies that the current density should represent

a lower limit that could easily be increased through, for example, the incorporation of high-κ gate dielectrics through atomic layer deposition.[31] A second positive characteristic was the large on/off current ratios measured—typically 10^5–10^6 (Figure 2.9D). In addition, the measured on-current levels exhibited less than 2-fold variations from device to device. These results confirm the statistical significance of the high-performance characteristics of SNAP Si NW FETs. Mobilities of all devices were extracted in the linear triode regions with V_{DS} = -0.25 V. In this region,[26]

$$\mu = \frac{dI_{DS}}{dV_{GS}} \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{DS}} \tag{2.4}$$

where $\frac{dI_{DS}}{dV_{GS}}$ is the transconductance and a typical value for our devices is ~ 1 μA/V; L is the device length and is 4 μm; C_{ox} is the gate capacitance and is ~ 5×10^{-15} F; and V_{DS} = 0.25 V. The calculated mobility values are summarized in Figure 2.11C. The mean value ~ 100 cm^2/V-s is close to bulk Si value with a doping level of ~ 10^{18} cm^{-3}.

An additional figure of merit is the subthreshold swing (**S**), which is defined as:[26]

$$S = \frac{kT}{q} \ln 10 \cdot \left[1 + \frac{C_G}{C} \right] \tag{2.5}$$

where C is the entire gate capacitance and C_G includes the component of the capacitance that arises from interface states and parasitic capacitance: when C_G = 0, ideal behavior is obtained. A low **S** is desired for low power operation and can only be obtained with low-defect-density devices.

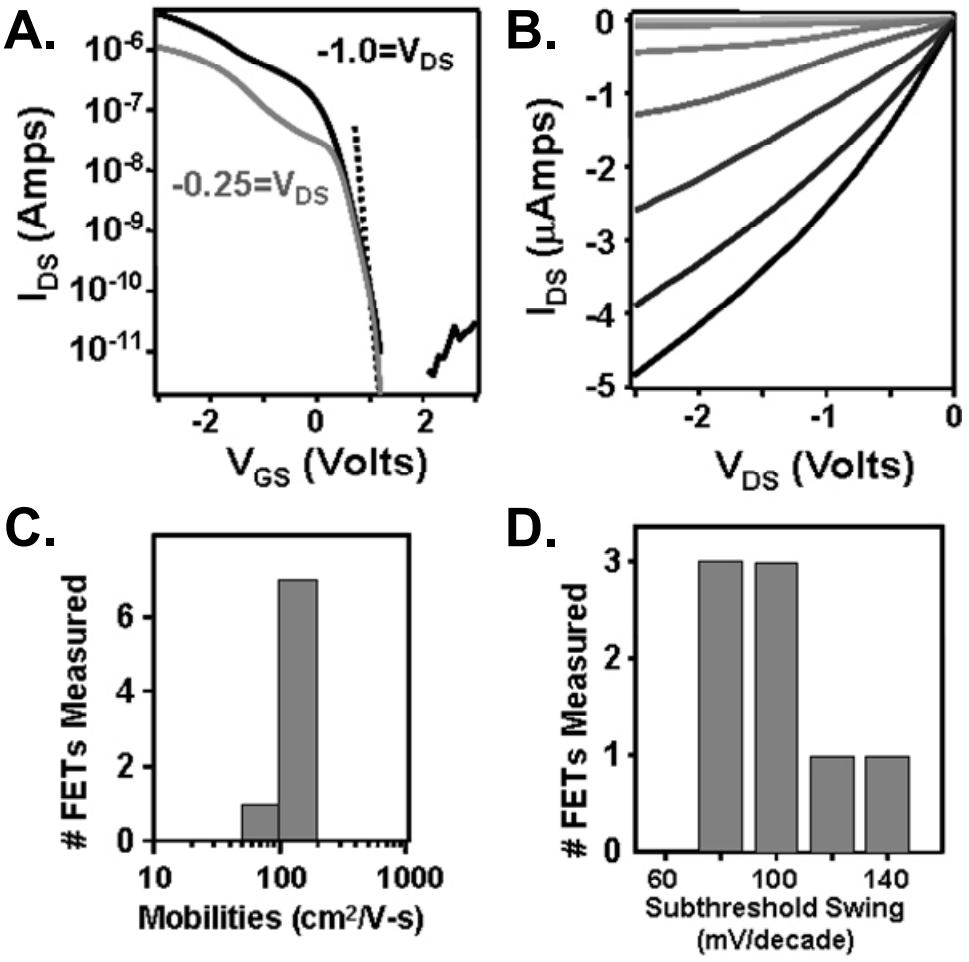

Figure 2.11. High-performance, top-gated p-type Si NW FETs. **A.** I_{DS}-V_{GS} characteristics at different bias source-drain biases. The dashed line represents the fitted sub-threshold slope value of 83 mV/decade. **B.** I_{DS} versus V_{DS} at different gate voltages, from -3 V (darkest colored trace) to 1 V (lightest colored trace), at 0.5 V/step. At least 5 μA current can be driven through a single device (consisting of ~ 8 NWs) without noticeable degradation while the experiments are carried out under ambient conditions without precautions to prevent oxidation. **C. and D.** Statistics from top-gated Si NW FETs for both carrier mobilities and for subthreshold swing values

S was extracted from I_{DS}-V_{GS} curves at current levels below 10^{-10} A using the relationship: [32, 33]

$$S = \frac{dV_{GS}}{d\log\left(I_{DS}\right)}. \tag{2.6}$$

Those values are summarized in Figure 2.11D. The highest performing device yielded an **S** of ~ 80 mV/decade and the poorest performing device yielded **S** = 130 mV/decade.

The 80 mV/decade value represents the lowest subthreshold swing of any p-type NW FET to date, although ~ 70 mV/decade has been reported for n-type (CdS) NW FETs.[34] The record for an n-type Si NW FET is ~ 80 mV/decade.[33] The lowest **S** value previously reported for a Si NW p-type FET was 135 mV/decade.[13] Given the low **S** values and property uniformity of the devices discussed here (Figure 2.9D), these results indicate that the SNAP process can yield very high-quality transistors at device dimensions and circuit densities that far exceed what can be produced using more traditional patterning methods.

2.4 Comparison of nanowire and microwire performance

Initial attempts to produce NW n-FETs with performance metrics comparable to the NW p-FETs were not successful. The n-FETs were fabricated exactly like the p-FETs but using substrates that were doped n-type at a concentration of ~ 10^{18} cm^{-3}. Typical performance metrics included on/off ratios of ~ 5000 and much larger **S** values than their p-type counterparts.

Low dimensional semiconductor materials are characterized by high surface-area-to-volume ratios.[35, 36] Recent studies have shown that the electronic properties of extremely thin (~ 10 nm) SOI films can be dominated by surface states.[37] Similar results have also been demonstrated on Ge NWs as well.[38] In the semiconductor industry, n-type Si devices have been more challenging to develop due to their enhanced sensitivity to surface states over p-type devices.[39] In the NW community, few literature reports exist of

NW n-FETs with high performance metrics.[40] To understand how the high characteristic surface area impacts the performance of Si NW FETs, Si NW FETs and Si microwire (μW) FETs were prepared side-by-side on the same SOI substrate using the SNAP method for the NW FETs and more traditional lithographic patterning for the μW FETs. The device structures are schematically depicted in Figure 2.12C.

A SOI substrate was first doped using either p- or n-type spin-on-dopants (SODs). The SNAP process was then carried out to place a Pt NW array onto the SOI surface. Afterwards, a stripe of ~ 10 μm wide and 10 nm thick Pt thin film was patterned adjacent to the SNAP Pt NWs by e-beam lithography (EBL) and metal deposition. The Pt NWs or microstructures served as masks for a reactive ion etching (RIE) process to transfer the Pt NWs and stripes patterns to form analogous Si NWs and stripes.[9] The resulting structure consisted of an array of Si NWs adjacent to a thin film of Si, both on a SiO_2 dielectric (Figure 2.12C). Ti/Pt (20 nm/50 nm) S/D contacts were patterned by EBL to be 150 nm wide and separated 2 μm apart. Al_2O_3 (10 nm) was then deposited as a gate dielectric, and a Ti top gate electrode was deposited to conclude the fabrication process, as shown in Figure 2.12C.

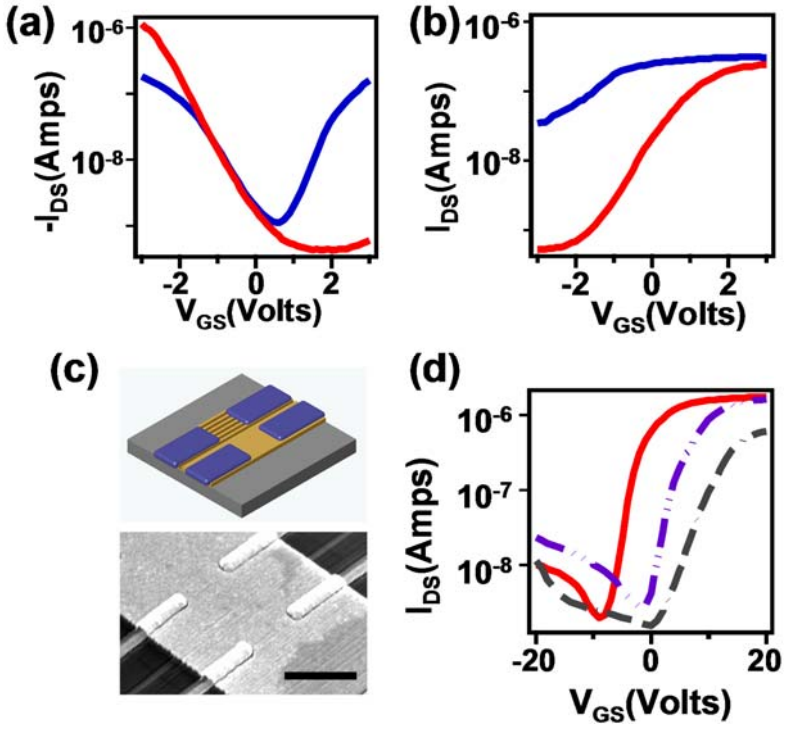

Figure 2.12. Comparison of NW and µW FET performance. I_{DS}-V_{GS} curves of **A.** P-type and **B.** n-type NW FETs (red) and µW FETs (blue). **C.** Device structure with µW NW FETs side by side. Scale bar: 2 µm. **D.** I_{DS}-V_{GS} curves of NW n-FETs after different treatments. Solid red trace: as-fabricated; purple broken line: after O_2 plasma; gray broken line: after H_2 plasma. For all devices, V_{DS}=1.5 V for n-type and -1.5 V for p-type.

In this experiment, four types of devices were characterized and compared, namely NW p- and n-FETs, and µW p- and n-FETs. The as-fabricated NW p-FETs exhibited similar characteristics as those described in the previous section,[28] i.e., high on-current at high negative gate potentials and low off-current at high positive gate potentials (Figure 2.12A). The µW p-FETs, however, were typified as ambipolar: a high on-current was observed at both positive and negative gate potentials and a low off-current was only seen at low gate potentials (Figure 2.12A). This suggests that for µW p-FETs, both hole (at negative gate potentials) and electron carriers (at positive gate potentials) are important for the conductance, whereas in NW p-FETs only hole carriers are significant. Given that the NW and µW FETs are fabricated side by side on the same

substrate and have undergone the same processing sequences, the doping levels, crystal orientations and electrical contacts should be identical. The only difference should be the increased surface-area-to-volume ratio for the NWs. It is therefore reasonable to suspect that the difference in device characteristics is mainly a result of the surface effects. Similar differences were also observed on n-FETs: NW n-FETs could be turned off easily while neighboring μW n-FETs that have identical parameters exhibited a noticeably weaker gate response (Figure 2.12B). It appears that the μW n-FETs have a higher electron carrier concentration than the analogous NW devices.

Considering that all of the measurements were conducted in ambient air, it is suspected that the surfaces of NWs tend to p-dope the channel, hence the hole carriers are enhanced and electrons are suppressed. Similar effects have been widely reported for CNT and organic-material devices.[41–43] To better understand this, systematic surface treatments on all devices were performed and the corresponding changes of transport characteristics were compared. Taking NW n-FETs as an example, the as-fabricated devices were measured with a bottom gate (i.e., using the underlying Si wafer of the SOI substrate as a gate electrode). These devices were then subjected to gentle O_2 and H_2 plasma treatments (Figure 2.12D). Such treatments constitute standard cleaning processes that are often employed during FET fabrication. After the O_2 plasma treatment, the clear trend was that the p-channel was enhanced and n-channel suppressed (purple curve in Figure 2.12D). This may arise because surface-adsorbed O_2 p-dopes the NW channels. By contrast, both the p- and n-channels were suppressed by the H_2 plasma treatment (gray curve in Figure 2.12D). This universal effect likely arises from surface damage that results from the reaction of H_2 or H-atoms with the Si native oxide, and thus

introduces surface states that can trap both holes and electrons. Similar experiments were also carried out on NW p-FETs and μW FETs. And for all devices, O_2 treatments enhanced p-channel and suppressed n-channel while H_2 suppressed both p- and n-channels. Importantly, the effects were always more pronounced for the NW FETs. NW FET performance metrics were clearly more dependent upon the surface treatments that were employed.

2.5 Development of high-performance nanowire n-FETs

The fabrication of the n-FETs was similar to the p-FETs but special care was taken to ensure the surface was clean after every step. The RCA cleaning process was done prior to applying the SOD and after the NWs were formed. Also, the substrate was annealed in N_2 at 450°C for 1 minute to fix surface states. As shown in Figures 2.13A and 2.13B, as-fabricated devices exhibited good n-type characteristics, with on/off ratios $> 10^3$, high on-current (> 1 μA), and acceptable transconductance (~ 1 μS). Equally important was that the n-FET performance was uniform over more than 15 measured devices (Figure 2.13C).

The RCA cleaning and 450°C annealing are important to this result. Devices without these treatments typically showed large variations in performance parameters. Different annealing conditions were explored and it was found that higher temperatures (e.g., 800°C) resulted in lower on-currents, and no working devices were obtained for 900°C annealing. On the other hand, lower annealing temperatures (e.g., 300°C) resulted in less-consistent device performance metrics.

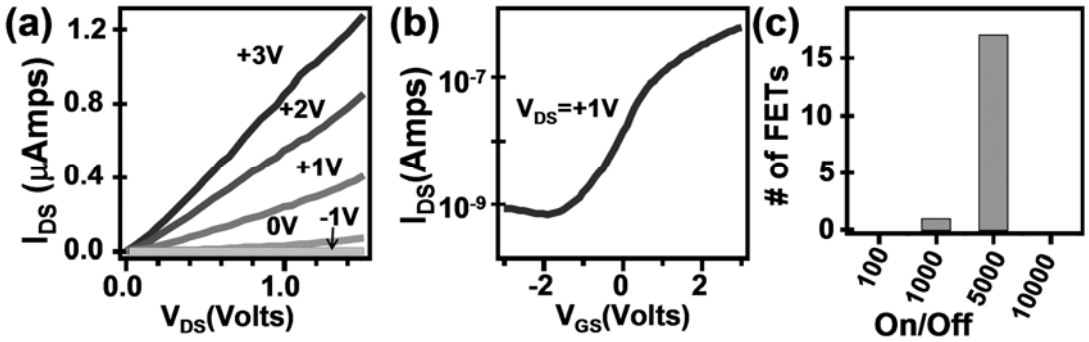

Figure 2.13. N-FET performance metrics. **A.** and **B.** I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics of NW n-FETs. Device dimensions: 150 nm wide with 2 μm channel length. The underlying Si bottom gate is grounded for all measurements. **C.** Histogram of on/off ratios of 17 measured devices

It is worth pointing out that the n-FETs in this study are non-optimized. The gate dielectric was e-beam evaporated Al_2O_3, the poor quality of which may be responsible for the large subthreshold swings (Figure 2.13B). Chapter 4 discusses the significant improvement of the n-FET devices by using in silico design feedback. Nevertheless, these results are significant in that this fabrication process reliably and consistently produced good n-FETs (Figure 2.13C). Moreover, when taken together with the much higher quality p-FETs that were obtained using similar protocols, an opportunity to integrate both p- and n-FETs within the same NW array to produce complementary-symmetry NW logic devices is presented.

2.6 Conclusions

The SNAP method, coupled with spin-on doping techniques and forming gas annealing, was utilized to produce high density arrays of 17 nm wide, 34 nm pitch Si NWs doped at 10^{18} cm^{-3}. FETs fabricated from small groups of these NWs exhibited extremely good performance characteristics, including high on-current, high on/off ratios and low subthreshold swings. In particular, the unprecedented S ~ 80 mV/decade for p-type Si NWs FETs reveals that the SNAP process can produce high-quality Si NWs with negligible numbers of defects. These results were valid for statistical numbers of devices, and provide a compelling argument for the reproducibility of this process.

In addition, it was demonstrated that Si NW FETs are sensitive to the surface properties, and that information was used as feedback to improve the nanofabrication techniques to achieve consistent performance from n-type Si NW FETs. These results opened up the opportunity to produce complementary logic circuits within ultra-high-density NW arrays.

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Chapter 3

Fabrication and characterization of nanowire logic circuits

3.1 Introduction

Complementary symmetry logic gates involve both p- and n-type transistors. Such logic gates outperform structures based upon pure p- or n-type technology with a key characteristic of low static power consumption, implying significant advantages for ever-denser circuit integration.[1] In fact, beginning in the early 1980s, there was a forced move from NMOS to complementary technology despite the increased fabrication complications. Today, a similar trend is occurring in the field of semiconducting nanowires (NWs). These promising building blocks for electronics are not dependent upon existing lithographic limitations.[2, 3] Si NWs, in particular, are appealing because they are relatively straightforward to prepare,[4, 5] the Si/SiO_2 interface is attractive, and Si NWs exhibit some compatibility with more traditional Si-based technologies.[6, 7] Si NW logic gates have been largely based upon p-FETs because they have been historically

more reliable to fabricate.[6, 8, 9] A few complementary NW devices have been reported, including p-type Si/n-type Si or GaN heterojunctions for diode logic,[10, 11] or carbon nanotube (CNT) based inverters.[12, 13] These systems are limited by both the stochastic chemical nature of the NW formation and doping and by the very challenging issues involving the assembly of devices into even the most basic circuits.[6, 10, 12, 14]

For NW electronics to have practical applications, both p- and n-type devices must be integrated onto the same substrate using a technique that is controllable, scalable, and that permits increasingly complex functionalities to be implemented. This chapter presents techniques for combining both p- and n-type Si NWs within a single, ultrahigh-density, highly aligned NW array. By combining traditional diffusion doping and lithographic techniques with the superlattice nanowire pattern transfer (SNAP) process,[15, 16] spatial control over the doping profiles can be achieved within a single NW or in adjacent NWs. Both n-type and p-type Si NW FETs can be co-prepared, and those FETs exhibit consistent and good performance metrics. These concepts are combined to demonstrate statistical numbers of a simple complementary logic circuit: a power-efficient Si NW inverter that exhibits voltage gain.

3.1.1. Overview of logic functions

The foundation of logic circuit operation is Boolean algebra. The Boolean algebraic equations are represented by logic gates. The NOT gate, which inverts the input signal, and either the AND or OR logic gate can be used to synthesize any Boolean alegebraic function (De Morgan's Laws).[17] The common logic functions also include the NAND, NOR, and XOR functions.

The most fundamental logic gate is the NOT function, or inverter. Its function is to invert the state of an input. The logic symbol and truth table appear in Figure 3.1. The CMOS inverter circuit is the most basic logic gate (consisting of 1 p-FET and 1 n-FET) and will be discussed further in this and the next chapter.

The AND and NAND gates are also fundamental logic gates. The AND gate will only output a **1** if both inputs are **1**. The NAND gate is the inverse of the AND gate. Similarly, the OR gate only outputs a **0** if the inputs are both **0** and the NOR is the inverse of the OR gate (see Figure 3.1 for the truth tables and the associated logic symbols). The CMOS AND/OR logic gates require 2 p-FETs and 2 n-FETs to operate and the NAND/NOR gates can be generated by coupling the AND/OR gate to the inverter. Lastly, the XOR, or exclusive OR gate, only outputs a **1** if the inputs are different. The XOR can be synthesized using the other fundamental logic gates and requires a minimum of 6 p-FETs and 6 n-FETs to implement for CMOS.

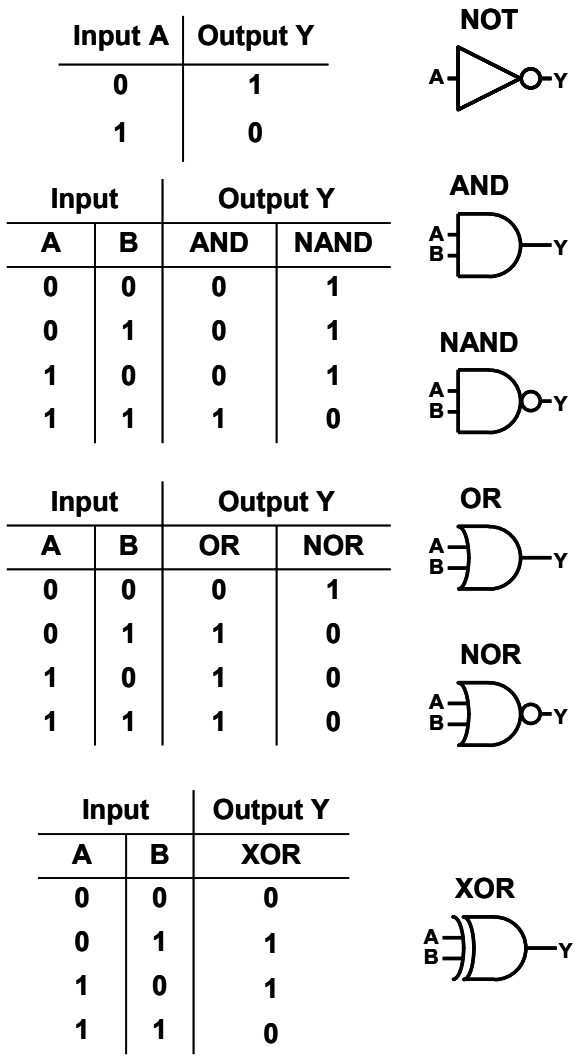

Figure 3.1. Truth tables and logic symbols for the fundamental Boolean functions

Complex logical operations, such as addition and multiplication, can be implemented by connecting these gates together to satisfy the correct Boolean algebraic equations. The level of complexity that can be achieved using these simple logic gates is staggering. For instance, current Intel microprocessors have 500–800 million transistors.[18] However, the implementation of these logic circuits from individual devices is not straightforward and requires the optimization of several performance metrics.

3.1.2 Overview of the chapter

The next section describes the development of a pattern doping technique that allowed for the side-by-side production of NW n- and p-FETs. These surfaces were characterized using electrostatic force microscopy and by measured I-V curves from fabricated diodes. Next, a SNAP master alignment system, which allowed for precise alignment of the SNAP-generated Pt NWs and the pattern-doped substrate, is described. Lastly, the fabrication of characterization of complementary inverters and other logic circuits are presented

3.2 Pattern doping technique

The realization of complementary symmetry (CS) logic circuits requires a method to fabricate adjacent n- and p-type NW FETs. The original method for fabricating SNAP-generated NW FETs involved a single doping step to dope the entire substrate (see Section 2.2.1). To pattern both n- and p-type regions on the same substrate, a pattern doping technique was developed to achieve spatial control over dopant profiles across a substrate. Once the substrate contains both n- and p-type regions, a SNAP master alignment system was implemented to pattern NWs over the desired regions with 1 μm precision. In this section, the development of the patterned doping technique is discussed. In the following sections, the characterization of the doped regions using electrostatic force microscopy (EFM) and by the I-V characteristics from fabricated diodes is discussed.

In order to achieve both n- and p-type regions on the same SOI region, a sequential diffusion doping process was implemented (Figure 3.1).[19] Intrinsic silicon-on-insulator (SOI) substrates (34 nm <100> Si on 250 nm oxide) (Simgui, Shanghai, China) were cleaned using the standard RCA process (see Section 2.2.1 for details). Alignment markers were first formed using photolithography and 20 nm Si evaporation, followed by thorough RCA cleaning. The substrates were then coated with a ~ 180 nm thick undoped spin-on-glass (SOG) film (Accuglass 214, Honey Electronic Materials, Sunnyvale, CA) followed by a photoresist bilayer consisting of a layer 3% PMMA (in chlorobenzene), spun at 4000 RPM for 30 seconds and baked at 130°C for 1 minute, and followed by 3612 (Shipley Corporation) spun on at 3000 RPM for 30 seconds (Figure 3.2i).

To define the p-type regions, windows were opened in the photoresist using optical lithography and the exposed SOG was removed by exposure to buffered oxide etch (BOE) (6:1 NH_4F:HF) (Figure 3.2ii). The etched regions were examined under an optical microscope after every 10 s exposure to monitor the etching process. The process was stopped when a slight undercut was observed which was typically after ~ 25s of etch time. If the etch process occurred too quickly to control, the BOE solution was diluted with DI H_2O.

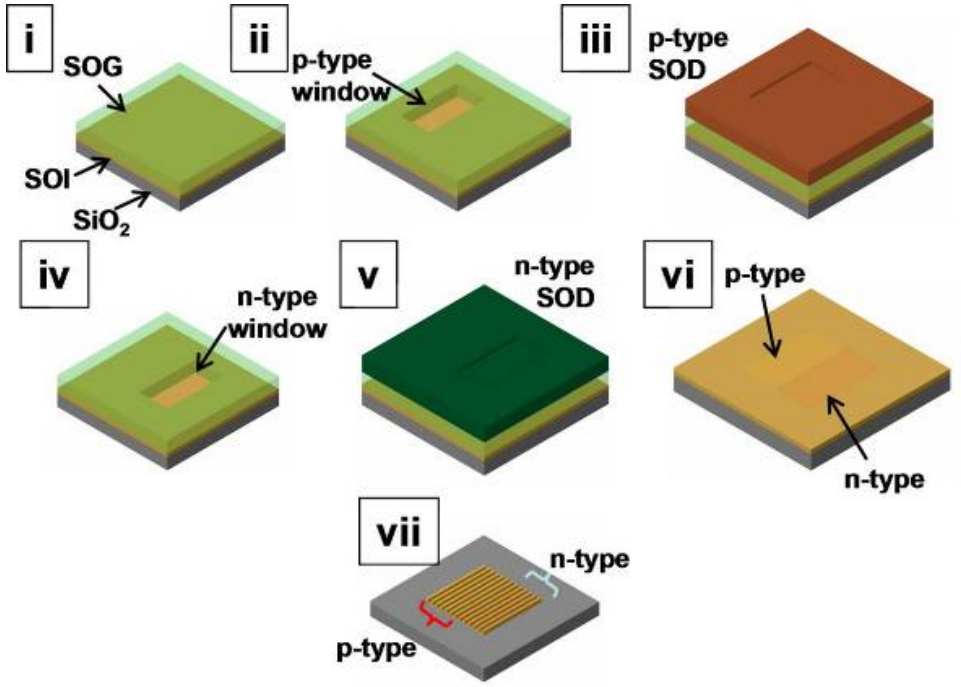

Figure 3.2. Schematic of pattern doping technique. **(i)** Undoped spin-on glass (SOG) is applied to SOI wafer. **(ii)** Electron beam or optical lithography is used to open windows in the SOG film. **(iii)** P-type SOD is applied on the SOG and the substrate is annealed. The only regions of the SOI substrate that are doped p-type are where the windows were patterned. **(iv–v)** The same process is repeated to pattern the n-type regions, resulting in a substrate containing both n- and p-type regions **(vi)**. **(vii)** Lastly, NWs are formed over the patterned doped areas.

The photoresist was then removed using an acetone soak and the p-type SOD (Boron A, Filmtronics, Inc., Butler, PA) was applied to the substrate (Figure 3.2iii). The film was annealed using rapid thermal processing (RTP). The dopants diffuse into the

SOI only where the SODs are directly in contact with the substrate. The SOG/SOD films were then removed using BOE, acetone, and DI H_2O in a process described in Section 2.2.1.

The substrate was cleaned using an additional RCA clean and the process was repeated to form the n-type doped regions, using n-type SODs (1:10 phosphorosilicafilm:CH_3OH, Emulsitone Company, Whippany, NJ) (Figure 3.2iv–v). The resulting substrate contained both n- and p-type regions (Figure 3.2vi). SNAP-generated NWs were patterned over the desired regions (Figure 3.2vii) to form n- and p-type NW FET channels.

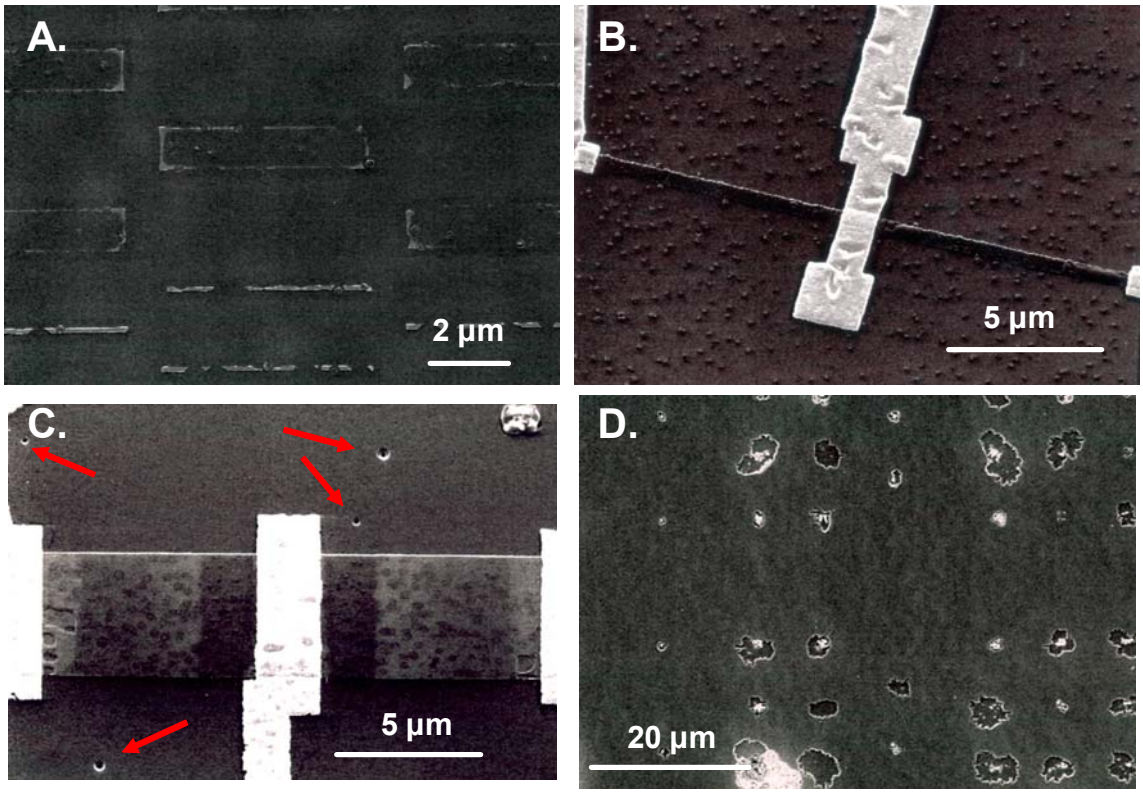

Figure 3.3. Scanning electron micrographs of surface damage from pattern doping. **A.** Reaction between the n- and p-type SODs lead to surface contamination. **B.** Bubbles suspended in the SOD can manifest as contamination on the surface, especially if there was no RCA cleaning. **C.** Etch pits in the underlying SiO_2 layer (denoted by red arrows) and a pitted texture on the Si epilayer can occur from BOE overetching. **D.** The reaction of the BOE with metal alignment markers causes severe etch pits on the surface.

The development of this process required several advancements. First, the use of an undoped SOG as a sacrificial layer was crucial. Studies were performed where n-type regions were patterned in a p-type SOD layer or vice versa. This scheme was attractive because it would only require a single annealing step. However, the n- and p-type SODs would react with each other during the anneal step, creating a contaminated surface that could not be cleaned (Figure 3.3A).

Next, the RCA cleaning process was important for reducing the contamination and Si etch pits on the devices. If contamination was present on the surface after the annealing step, inconsistent BOE etching occurred, leaving small contaminants (Figure 3.3B) or etch pits (Figure 3.2C) on the surface. If it took a significantly longer time than usual to render the surface hydrophobic with BOE, it was very likely that the surface was contaminated and that these microscopic defects would be present.

Lastly, the use of photolithography combined with Si alignment markers was important. Initially, metal alignment markers were used, which were easy to identify for EBL. However, during the BOE etching process, the BOE would react with the exposed metal markers, creating etch pits in the Si (Figure 3.3D). Etched trenches were also tested but were not compatible with the etching process and were not observable using scanning electron microscopy.

3.3 Electrostatic force microscopy characterization

Before NW devices were fabricated, the diffusion doping technique was characterized by electrostatic force microscopy (EFM) using a standard doping pattern consisting of dopant windows in a checkerboard pattern (Figure 3.4A).

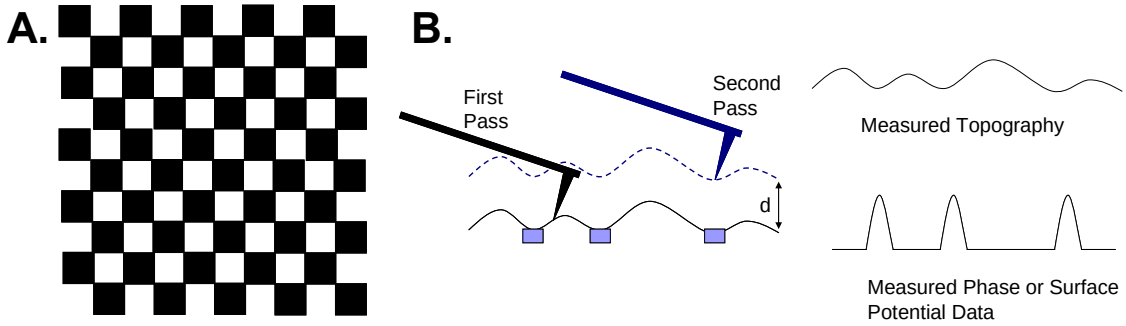

Figure 3.4. Depiction of doping windows checkerboard pattern and the EFM technique. **A.** Schematic of doping windows checkerboard pattern. The alternating black and white squares represents alternating areas of n- and p-type doping. **B.** Schematic of EFM technique. The cantilever scans over the surface twice. The first scan generates the topographical image (upper-right image) and the second scan, which is performed at a set distance, d, above the surface, produces the electric field gradient in response to electric fields (depicted as light blue boxes) on the surface.

EFM is a scanning probe technique, similar to tapping-mode atomic force microscopy (AFM), which allows the mapping of electric field gradients above a sample. The technique uses two scan passes per line (a trace and retrace) to record both topology and the force gradients. First, the scanning probe cantilever scans across the surface while oscillating at the probe tip's resonant frequency. Once the probe reaches the end of the scan, it lifts up by a set distance, d, and retraces the scan line, following the recorded topology (Figure 3.4B). On this retrace step, a voltage is applied across the tip to make it more sensitive to surface electric fields. If the tip is attracted to the surface due to electrostatic interactions, the cantilever resonance frequency will reduce. Conversely, a repulsive interaction will increase the cantilever resonance frequency. The phase shifts

can then be mapped into a two-dimensional image to illustrate the electric field gradients on a surface. EFM is a powerful technique for simultaneously probing the morphology and the electrical characteristics of surfaces, and has been used to explore interesting phenomena in organic heterojunction solar cells,[20] molecular films,[21, 22] nanoscale devices,[23] and semiconductor device failure.[24]

To study the fidelity of the pattern doping technique, a checkerboard pattern of alternating n- and p-type regions was formed on SOI substrates (Figure 3.4A). These checkerboard patterns were originally generated using EBL and PMMA resist. Various sized squares were patterned with areas ranging from 36 μm^2 to 1 μm^2. Once these samples were generated, they were characterized using a Multimode Nanoscope IIIA (Veeco Instruments, Santa Barbara) atomic force microscope and a Nanoscope Extender^{TM} electronics module. The module allowed for phase detection, which improves the instrument's sensitivity to the surface's electric fields. Pt/Ir-coated tapping-mode etched Si probes were used (SCM-PIT from Veeco Instruments). The Pt/Ir coating provides an electrical path from the cantilever to the apex of the tip, which is necessary to provide a DC bias on the probe tip. The AFM hardware and software was configured for phase detection EFM measurements as described in the user's manual.[25]

The topology and associated EFM image of a checkerboard pattern consisting of 3 μm squares is shown in Figure 3.5A and 3.5B. The n-type regions were doped 3×10^{17} cm^{-3} and the p-type regions were doped 9×10^{17} cm^{-3}. The topography image reveals a surface with ~ 5 nm average height variation but no obvious checkerboard pattern. The associated EFM image was taken by a 5 V biased tip lifted 20 nm off of the surface. The scan rate was 0.5 Hz and 512 scans lines were taken per image. Here, the n-type regions

appear darker than the p-type regions due to the differing phase shifts of each region. The n- and p-type squares are not uniform due to overetching of the p-type windows during the lithography steps. The phase shift between the n- and p-type regions was approximately 4°.

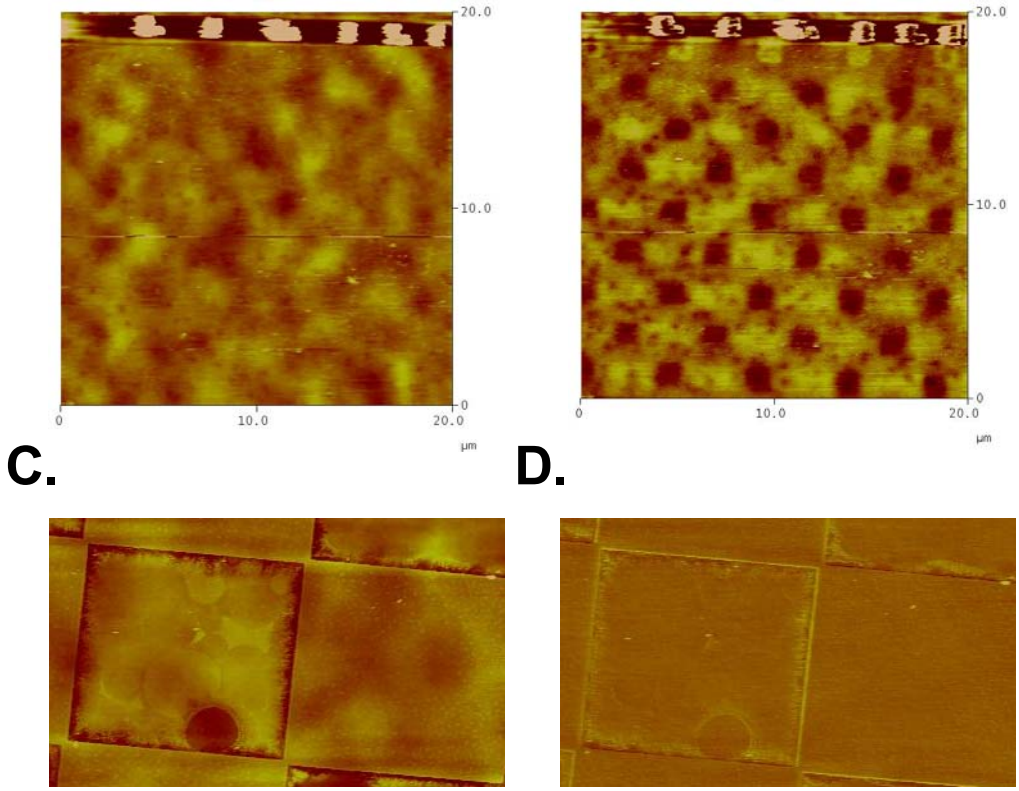

Figure 3.5. EFM images of pattern doped substrate. **A.** Topography image of SOI substrate doped with a checkerboard pattern of 3 μm^2 squares. **B.** EFM image of same area, showing the alternating squares. The darker regions represent the n-type regions and the lighter regions are doped p-type. **C.** Close-up of a topography image of a "control" checkerboard, where the squares are undoped but etched to form topographical variations. **D.** EFM image of the same area, showing negligible phase shifts within each square

A control sample was also characterized with EFM to ensure that the EFM signal was not due to slight changes in the topography (vertical overetching of the n- or p-type regions). A checkerboard pattern was made where alternating squares were etched into undoped Si (Figure 3.5C). The average height variation was ~ 10 nm. The associated EFM image (Figure 3.5D) shows no variation in the phase shift between adjacent

squares. The phase does change at the interface at each square, which is typical in EFM. This is due to the fact that sharp features on a surface concentrate the local force gradient.

The EFM technique allows for the characterization of the Si surface prior to device formation. Since NW devices require the Si epilayer of an SOI wafer to be removed, this technique is the best method for seeing the entire doping pattern and also to easily characterize issues such as SOG overetching.

3.4 Diode fabrication and characterization

To characterize the interface between n- and p-doped regions, thin film diodes were fabricated. The devices consisted of a 0.5 μm x 2.5 μm wire patterned using EBL. At the center of the wire was a pn junction. Fifty-four devices were fabricated and approximately half showed rectification. The device structure and representative pn junction curves are presented in Figure 3.6. The first I-V curve is from a diode biased from the electrode contacting the n-type side (Figure 3.6C) and the second curve is another device biased from the electrode contacting the p-type side (Figure 3.6D). Both curves show the correct rectifying behavior.

A semilog plot of the absolute value of the current versus voltage for the first curve shown in Figure 3.7A indicates correct diode characteristics.[26] Four regions of the semilog plot are labeled A–D and can be related to typical diode behavior: (A) generation-recombination current; (B) diffusion current; (C) high-injection coupled to

series resistance effects; and (D) reverse bias (breakdown not observed). The minima are shifted from zero volts due to miscalibration of the IV software. The curve shape and measurement repeatability provides evidence that the sharp change in current is due to the device turning on and not breakdown.

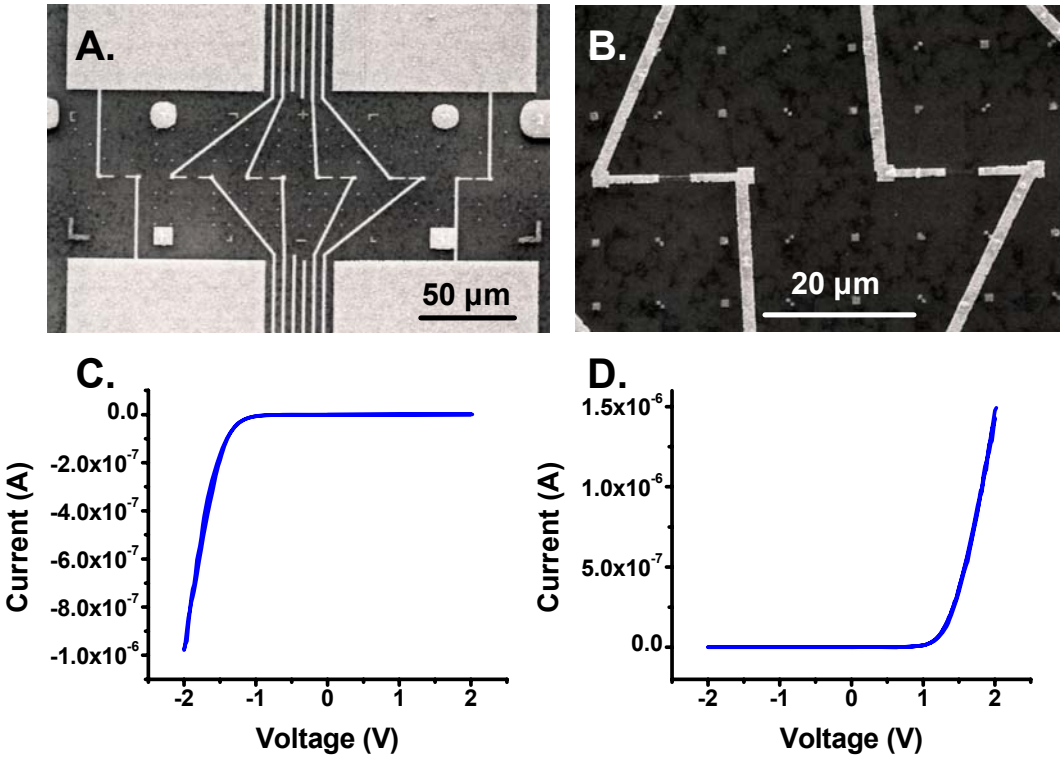

Figure 3.6. Diode curves from devices fabricated from patterned doped substrates. **A.** Diode biased from n-type side. **B.** Diode biased from p-type side.

The semilog plot can be used to perform simple device modeling. Diode behavior can be modeled using the ideal diode equation:[26]

$$I = I_S\left(e^{\frac{qV}{nkT}} - 1\right) \tag{3.1}$$

where I_S is the generation current and n is the ideality factor. The ideal diode equation assumes several conditions: (1) an abrupt depletion layer, (2) that the Boltzmann approximation is valid within the depletion layer, (3) low minority carrier injection, and

(4) no generation current within the depletion layer. Therefore, the ideal diode equation would match the slope of region B in the semilog plot.

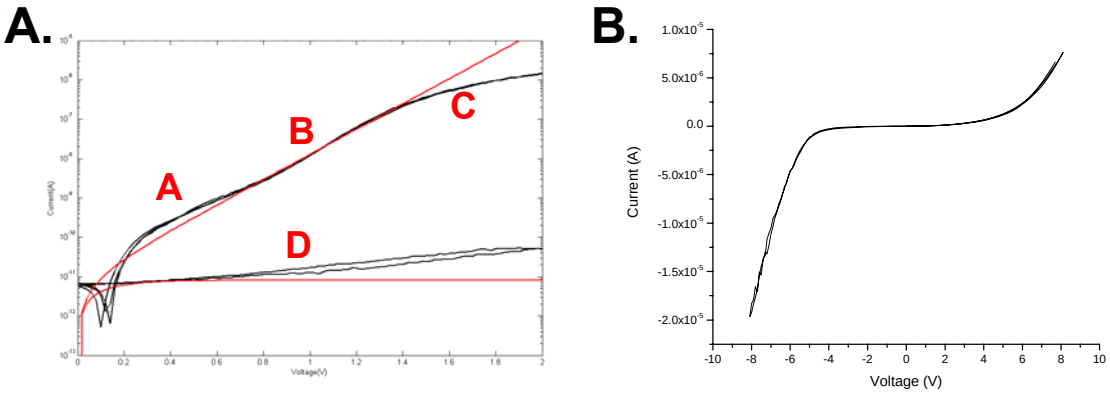

Figure 3.7. IV characteristics of fabricated Si diode. **A.** Semilog plot of IV characteristics of diode with ideal diode equation fitted to the slope in region B. **B.** IV characteristics of diode showing rectifying behavior in the +V direction and diode breakdown in the –V direction.

The fitted plot is shown in red over the semilog plot in Figure 3.7A. The ideality factor n equals 2 in ideal diodes where the diffusion current dominates. For the measured device, n = 5.2. Deviations from the ideality factor are due to surface leakage current, generation/recombination of carriers within the depletion layer, carriers tunneling through the bandgap, high-injection of minority carriers at low forward bias, and/or series resistance. Therefore, the ideal diode equation only gives qualitative agreement for actual silicon diodes. However, because the semilog curve shape matches the shape for typical silicon diodes and the ideality factor is within the same order of magnitude for ideal diodes, the devices are exhibiting normal diode behavior. Figure 3.7B shows a device with a positive turn-on voltage and a breakdown event (indicated by a sharper slope) at high negative voltage, also indicating correct device behavior.

3.5 SNAP nanowire alignment system

In order to produce logic circuits from pattern doped surfaces, it was essential to develop a method to align the SNAP Pt NWs over the appropriate region. Originally, the SNAP masters were placed on the wafer manually, using tweezers. This method was sufficient for homogeneous doped samples. For samples containing pattern doping or existing features (alignment markers, other devices, etc), a high control over the placement of the NWs to within a few μm becomes necessary. Therefore, an SNAP NW alignment system was built and is described here.

The basic concept of the SNAP alignment system is that both the substrate and the SNAP master are aligned to a stationary reference point (in this case, a specific point on a reticle that is projected on a monitor). Photos of the alignment system with individual components labeled are shown in Figure 3.8. The substrate is aligned by positioning it so that the vertical reticle line (Figure 3.8B) is aligned to the appropriate alignment markers on the surface. The SNAP master is affixed to a custom designed holder (Figure 3.8G) using simple suction and brought 0.5–1 mm over the substrate. On the top of the SNAP master holder is a lithographically patterned grid. The holder is moved until the vertical and horizontal reticle lines are aligned to a specific grid point, as determined by calibrations. Both the SNAP master holder and the substrate platform can be moved independently in the x, y, z, and θ directions using high-quality optical stages. The suction is released and the SNAP master drops onto the substrate, which is coated in epoxy. The heat stage (Figure 3.8E) is turned on and the epoxy is heat-cured. At this point, the substrate can be removed from the alignment system.

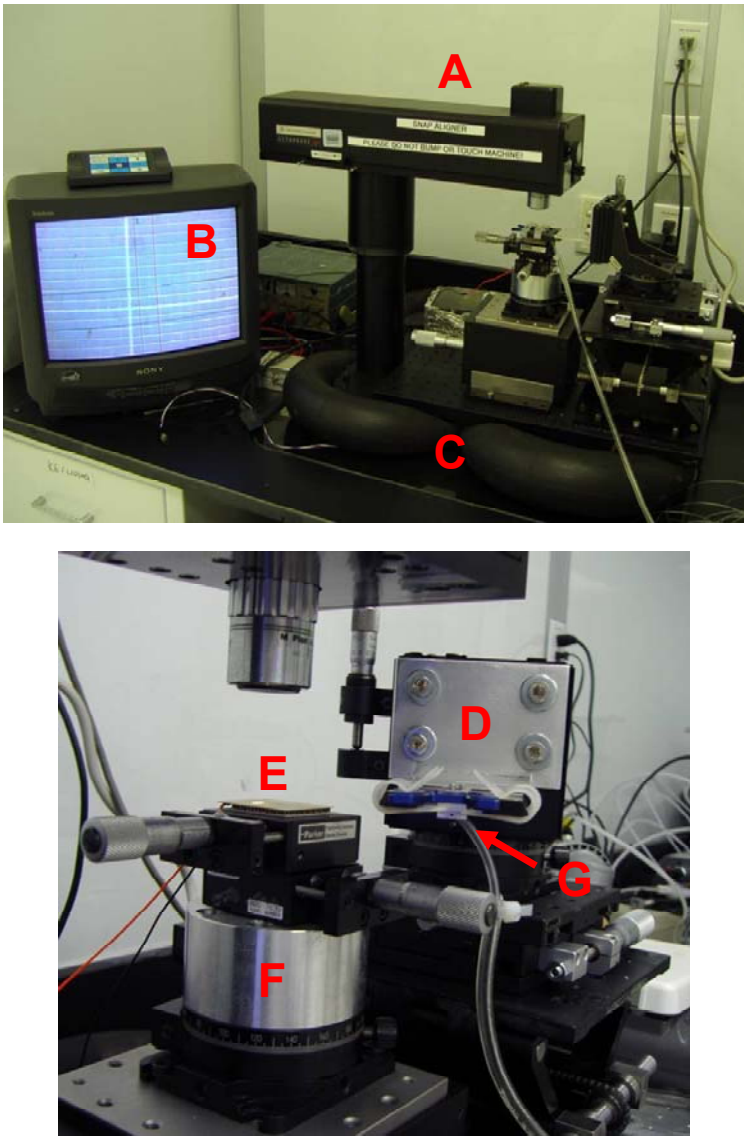

Figure 3.8. Pictures of SNAP alignment system. Individual components are labeled A–G. **A.** Microscope system with 200× objective with a working distance of ~ 0.5 inches. **B.** Monitor that displays the microscope view with a reticle overlay. **C.** Alignment system is attached to an optics board that is placed on 4 inflated inner tubes. The inner tubes suppress room vibrations. **D.** Arm that holds SNAP master holder. It can be moved in the x,y,z, and θ directions using optics stages. **E.** Substrate platform. The platform is a heat stage so that epoxy on the substrate can be heat-cured after the SNAP masters are placed on the surface. **F.** The substrate holder sits on three optics stages, which can move it in the x,y,z, and θ directions. **G.** The SNAP master holder. It holds the SNAP master by suction until it is properly aligned over the substrate. A fine grid is lithographically patterned on the top of the holder. To align the SNAP master and the substrate to each other, the reticle is first aligned to the appropriate alignment markers on the substrate. The SNAP master holder is brought over the substrate and is also aligned to the reticle.

Once the alignment system was built, it was tested for accuracy. 15 μm metal target squares were patterned onto Si substrates, flanked by two 5 × 5 μm alignment markers. The center of each alignment marker was positioned on the correct reticle line. Figure 3.9A and 3.9B show the results of one SNAP NW transfer. The alignment of the NWs was accurate to within 1 μm on several samples.

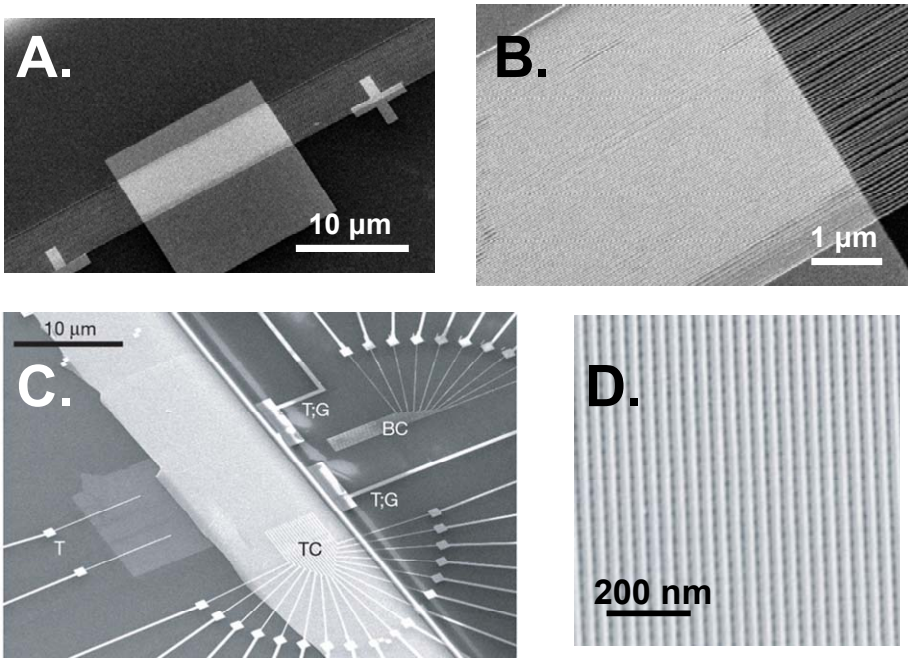

Figure 3.9. Scanning electron micrographs of SNAP NWs dropped from the SNAP alignment system. **A.** SNAP NWs on the target square. The cross-shaped alignment markers were used to line up the reticle. **B.** Close-up of the NWs on target. **C.** A 160 kbit crossbar array memory circuit patterned at 10^{11} bits/cm^2 using two sets of NW arrays. The top plane of NWs were dropped using the alignment system. **D.** Close-up of the SNAP NW crossbar array.

In addition to being used for the logic circuit fabrication, this alignment system was also an enabling technology for the development of a 160 kbit molecular memory circuit patterned at 10^{11} bits/cm^2 (Figure 3.9C).[27] This architecture density was achieved by overlapping two sets of perpendicular SNAP NW arrays, forming a crossbar array (Figure 3.9D). Without the development of the alignment system, the formation of NW circuits would have been significantly more difficult.

3.6 Nanowire logic circuit fabrication

Once the pattern doping process was optimized and the SNAP alignment system was completed, the NW logic circuit fabrication process could be developed. First, new Ti/Pt alignment markers were patterned around the NW array. The Si alignment markers from the pattern doping were used to map out the patterned doped regions on the NW array. As for single devices (see Section 2.2.3), the continuous NW array was divided into discrete sections. Next, Ti/Pt input and output wires were patterned using EBL, using the map of the doped areas to guide the placement of the n- and p-FETs. The Al_2O_3/Ti/Pt top gates were fabricated and the circuits were ready to characterize. The circuits were tested in a probe stations using three Keithley 2400 SourceMeters and custom LabVIEW software.

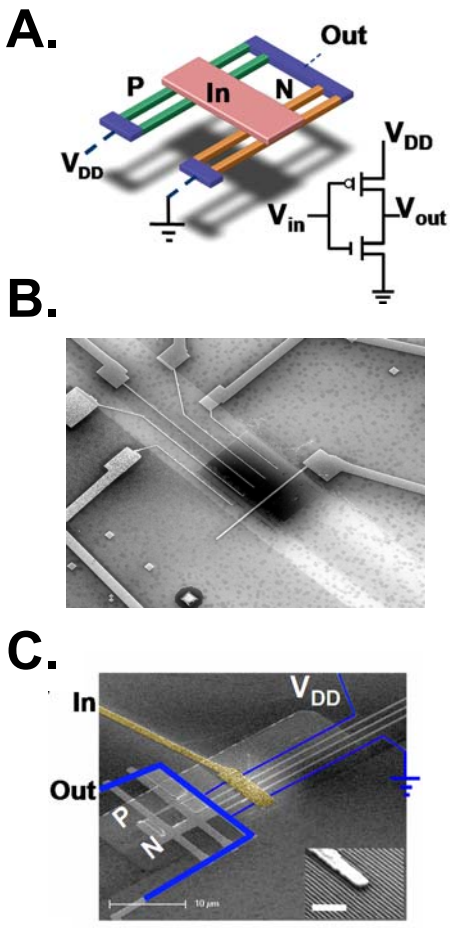

Figure 3.10. The NW inverter circuit. **A**. Schematic of the NW inverter circuit. **B.** Scanning electron micrograph of NWs with EBL-patterned power supply and output wires. **C.** Micrograph of completed inverter circuit with top gate supplying input signal

Figure 3.10 shows the schematic and the scanning electron micrographs of a complementary inverter circuit patterned from a SNAP NW array. A complementary inverter involves a p-FET and n-FET in series (see the circuit diagram in Figure 3.10A), with a shared gate as the input and a shared contact

as the output. The advantage of the complementary symmetry architecture is that there is minimal current flowing from the power supply (V_{DD}) to the ground, whether the input is high (the p-FET is "off") or low (the n-FET is "off"). Therefore, the power consumption is minimized, which is why complementary logic gates comprise an important component in modern digital technology.

During the circuit fabrication, it was interesting to observe that the n- and p-type NWs were distinguishable using scanning electron microscopy. Figure 3.11 shows a micrograph of the NWs at the interface of n- and p-type regions. The p-type NWs appear brighter than the n-type NWs. This is due to the difference in the Fermi energies of the p- and n-type materials. Although the contrast was noticeable, it was still necessary to explore the pattern doping quality using EFM and to carefully map the pattern doped areas using the doping alignment markers.

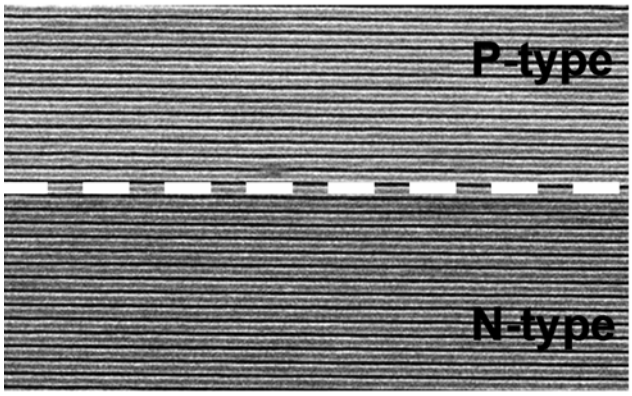

Figure 3.11. Scanning electron micrograph of SNAP NWs at the interface of n- and p-type Si

Prototypes of more complex logic functions were also fabricated, although not electrically characterized, in order to understand the fabrication challenges associated with integrating several n- and p-type FETs. These circuits utilized a design feature called monolithic contacts.[28] Monolithic contacts are formed by patterning Pt microwire contacts by EBL prior to the NW transfer into Si. The NWs, along with the patterned microwires, are transferred in the Si epilayer simultaneously to form both NWs and Si

bars. These bars are then used to route signals to the NWs, analogous to standard metal microwire contacts. The strength of this technique is that the monolithic contacts eliminate any issue of contact resistance to the NWs. The metal contact pads are ohmically contacted to the monolithic contacts, which are large and typically highly doped.

Figure 3.12A shows a scanning electron micrograph of a NW full adder circuit consisting of 14 n-FETs and 14-FETs. The monolithic contacts appear as the dark microwires in the image and the metal top gate. The interface between the NWs, the monolithic contacts and the metal contacts are shown in Figure 3.12B.

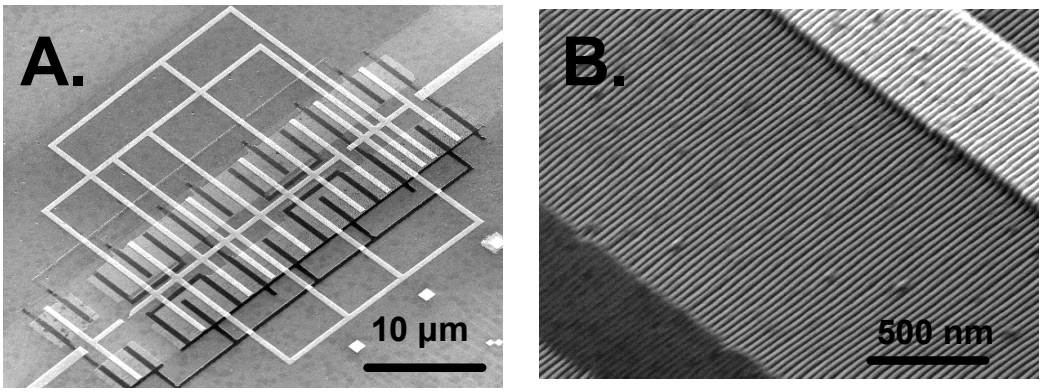

Figure 3.12. Example of the NW 2-bit full adder circuit consisting of 28 NW FETs. **A.** Scanning electron micrograph of adder circuit. The bright microwires are patterned using Ti/Pt and the dark microwires are monolithic contacts. **B.** Close-up of NWs showing comparison of monolithic wire and metal wire

Although these circuits were not tested, their fabrication was a useful exercise for learning more about the fabrication processes involved for complex circuits.[28]

3.7 DC characterization of fabricated FETs and circuits

Several complementary inverter circuits were fabricated and characterized. For the measured inverters, the contact electrode width was 150 nm (which contacted 4–5 Si NWs) and the channel length was 2 μm. P- and n-FETs were first characterized separately (Figure 3.13A). This step helped determine the appropriate power supply voltage (V_{DD}) and the input signal range. For all of the inverters measured in this study, $V_{DD} = 3$ V. Under this condition, both p- and n-FETs are saturated and show symmetrical performance. The input versus output of the inverter is plotted in Figure 3.13B: when the input is low, the output is high, and vice versa. Therefore, a "NOT" logic gate is achieved.

The gain of the inverter, which is defined as the maximum slope during the transition between the output low and output high levels, characterizes the noise margins of the circuit. This yields a metric for how robust the circuit is to signal variation. A gain greater than unity is a minimum requirement and a high gain is desired. The gain can be obtained by taking the first-order derivative of the input/output plot and the result is shown in Figure 3.13C. Out of the 7 devices measured, a gain of ~ 5 was consistently obtained (Figure 3.13D), further suggestive of uniformly performing p- and n-FETs.

In Chapter 4, the optimization of the inverter circuit using device and circuit simulations is discussed and provides more in-depth information about the relevant performance metrics.

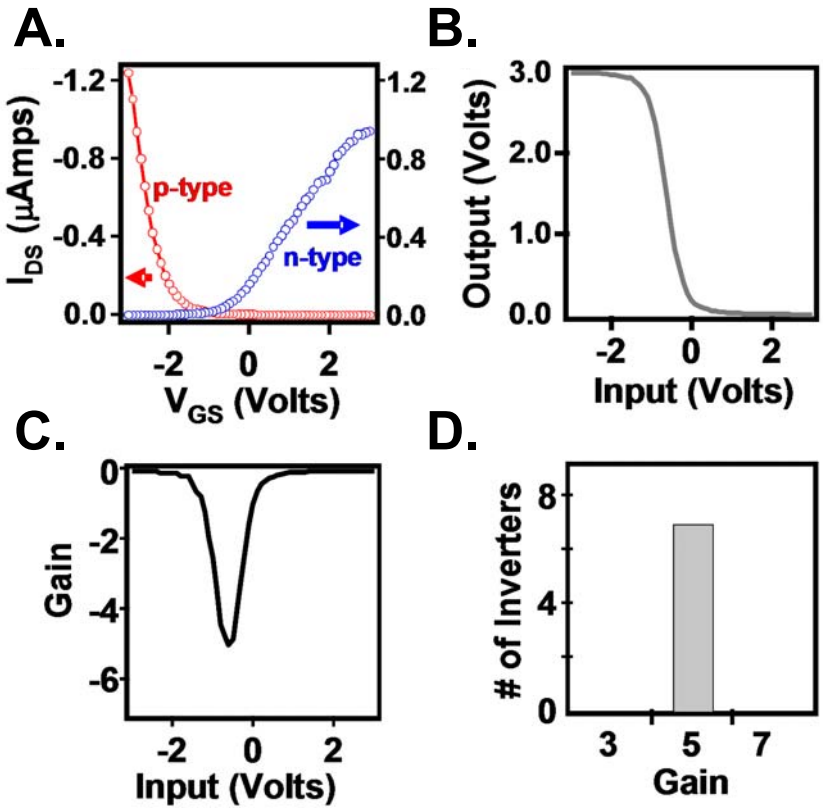

Figure 3.13. Inverter performance metrics. **A.** I-V_{GS} characteristics of p- and n-FETs in the same array. V_{DS}=- 1.5 V for p- and + 1.5 V for n-FETs. **B.** Output versus input signal of the complementary NW inverter. **C.** The gain of the inverter versus input. **F.** Histogram of the gain of 7 measured inverters

3.7.1 Demonstrations of other logic gates

Since the development of the inverter circuit, the rest of the basic logic gates have been fabricated and tested by a colleague.[29] This was a significant achievement since it required several NW FETs to have consistent performance. These circuits were enabled by the SNAP, the in-plane routing, and the pattern doping techniques developed in this chapter.

Figure 3.14 shows a demonstration of a NW XOR circuit, which required 6 n-FETs and 6 p-FETs. Two NW CS inverters are first utilized to create complementary

inputs $\overline{A}$ and $\overline{B}$ from inputs A and B. All four of these logic values are then utilized to drive a circuit of 8 NW FETs, with each input utilized to drive a p-FET and an n-FET.

When all 12 FETs operated consistently, a functional XOR gate was achieved.[29] This circuit utilized the in-plane routing technique, which allowed for the construction of highly doped, NW-to-NW signal routing pathways within the same single-crystal Si epilayer from which the NWs are formed. Without this nanofabrication advancement, it is unlikely that the NW CS XOR gate would have achieved full signal restoration.

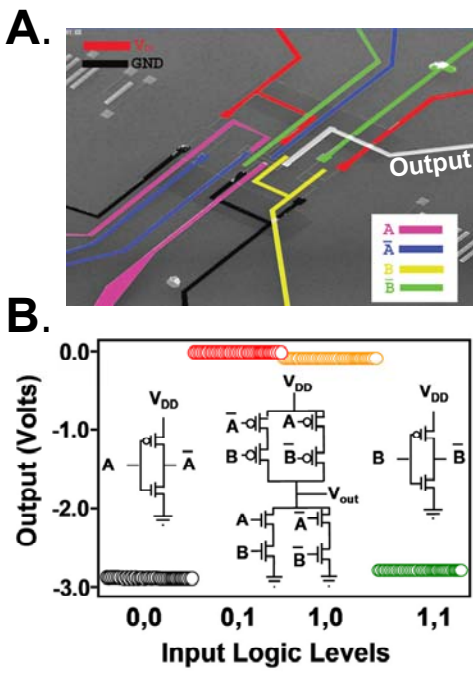

Figure 3.14. Demonstration of a NW XOR logic gate. **A.** SEM of XOR gate. **B.** Output versus input of XOR gate, reproducing the correct truth table.

The yield of working n- and p-FETs was likely near 100%. However, the requirement that the NW n- and p-FETs be well matched with each other so that a CS logic gate exhibits full signal restoration is a very stringent one. 15 XOR gates were tested and it was found that only 5 exhibited full signal restoration. If a single NW FET performed out-of-range within an XOR gate, the XOR gate would fail. This is likely the dominant failure mode. There were 180 FETs tested in the 15 XOR gates, and the 33% yield in XOR gates implies an approximately 93% yield in working and matched FETs.

3.8 Conclusions

Spatially selective doping and a SNAP alignment system were developed, and this allowed for the fabrication of both p- and n-type devices within a single, ultra-high-density Si NW array. The pattern doping method was characterized using electrostatic force microscopy and by characterizing fabricated pn diodes. Complementary Si NW inverters were constructed and demonstrated to exhibit uniform performance. This laid the foundation to generate the other Boolean logic functions.

3.9 References

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Chapter 4

In silico design optimization of nanowire circuits

4.1 Introduction

The continued miniaturization of semiconductor transistors has several associated scientific and engineering challenges. High-κ dielectric/metal gate MOSFETs, strained-Si channel devices, and non-planar (tri-gate or Fin FET) structures are most likely to be the next-generation technologies.[1] Further into the future, more novel transistor-channel options are being explored, including III-V compound semiconductors,[2–4] semiconductor nanowires (NWs),[5–8] and carbon nanotubes (CNTs).[9–15]

NWs and CNTs are not prepared using conventional lithography, implying that NW or CNT-based devices can be scaled to very high device densities. Small circuits, such as inverters,[6, 9–14] basic logic gates,[5, 13, 14, 16] and ring oscillators,[13, 14, 17] have already been demonstrated using NW and CNT field-effect transistors (FETs). However, few demonstrations have provided realistic competition to current CMOS technology. This is

largely because constructing even simple prototype circuits from these materials is a daunting challenge.

Computer-aided design (CAD) tools can increase the efficiency of electronic circuit design and optimization by yielding insights into circuit performance, which in turn provide design feedback, resulting in optimized fabricated circuits. While NW and CNT devices have been modeled in a circuit simulation environment,[18–20] these efforts have been largely independent of the fabrication and materials aspects of these nanocircuits. Adding CAD into the design process will result the more efficient design of high performance nano-ICs.

Therefore, a methodology was developed that couples circuit simulations and fabricated prototype devices into the design process of the nanowire logic circuits.[21] A CS inverter, or NOT gate, was chosen for optimization because it is conceptually easy to understand while also yielding several performance metrics for CMOS logic. CS inverters require both a p- and n-type FET, arranged so that an input logic voltage signal will turn one FET "on" and other "off". This architecture prevents the voltage that powers the circuit from having a direct pathway to ground, which makes the circuit energy efficient.[8] However, such circuits are difficult to fabricate from most NWs or CNTs, because assembling different types of NWs or NTs from well-defined electronic circuits remains a significant challenge. The superlattice nanowire pattern transfer (SNAP) technique[22] eliminates this problem and has been used to successfully fabricate high-performance devices[7] and circuits[8] (see Chapters 2 and 3). Si NWs have the additional benefit of being a highly studied material and are compatible with existing Si processing technologies, making them a realistic choice for nanoelectronics circuits.

From candidate Si NW p- and n-FET devices, current-voltage (I-V), conductance-voltage (G-V), and capacitance-voltage (C-V) measurements were tabulated and introduced into a circuit simulator. DC and transient analyses were carried out to investigate and optimize, in silico, a variety of circuit metrics, with a focus on optimizing the gain. Other metrics that could be readily simulated include the input and supply voltage levels, propagation delays, leakage currents, parasitic resistances and capacitances, and power consumption. Next, the results of these simulations were fed back into the nanofabrication procedures to produce a CS inverter with an optimized gain of 45. This represents a more than 5-fold improvement over the initially fabricated prototype circuit from which the basis set of measurements were extracted.

4.1.1 Organization of the chapter

In this chapter, the fabrication and characterization of the candidate NW FETs are described, followed by a description of the simulation methods and the results of the DC and transient computational analyses. Finally, the simulated results were verified experimentally and high-performance inverters that are competitive, in terms of their gain, with CMOS are demonstrated.

4.2 Large-area nanowire transistors

Special NW FETs were specifically designed for this project that had a large area channel region. This design ensured that high-quality capacitance data could be obtained from these prototype devices. A transistor's gate capacitance can be approximated by a parallel-plate capacitor, which has a capacitance of:

$$C = K\varepsilon_o \frac{A}{d}. \tag{4.1}$$

Here, A is the area of the plate, d is the distance between the plates, K is the dielectric constant of the oxide material, and ε_o is the permittivity of free space. A typical NW FET channel dimensions are 100 × 500 nm and the gate oxide thickness is ~ 10 nm. Assuming a dielectric constant of ~ 3.7, the gate capacitance of the device would be ~ 0.1 fF. This capacitance is too small to accurately measure using conventional equipment,[23] so large area devices were designed with channel widths of 12 μm and channel lengths of 9–11 μm. This increased the expected gate capacitance to 0.3 pF, which could be easily measured.

4.2.1 Fabrication of large-area nanowire transistors

Fabrication of the large-area transistors (Figure 4.1A) was similar to the fabrication of standard-size transistors (see Section 2.2). Si NW devices were fabricated on SIMOX-SOI wafers (34 nm <100> Si on 250 nm Si oxide) (Simgui, Shanghai, China). Substrates were cleaned using the standard RCA process and then doped either n- or p-type by applying a spin-on dopant (SOD) and annealing using rapid thermal processing

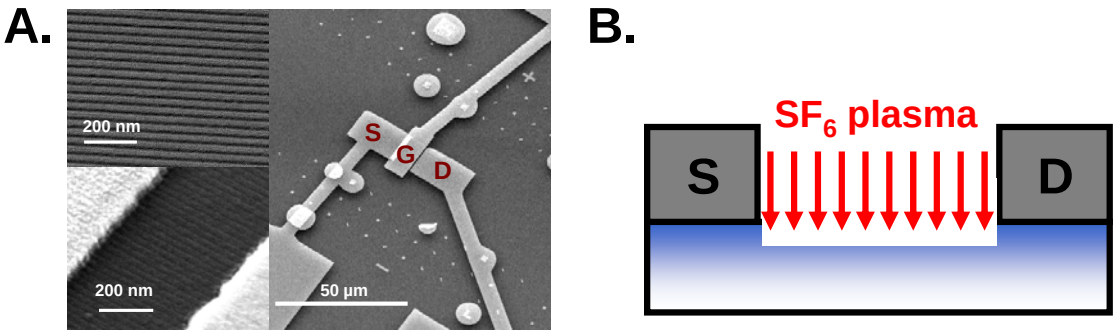

Figure 4.1. Fabrication of NW large-area device. **A.** Scanning electron micrograph of large-area device. Source (S), drain (D), and gate (G) electrodes are labeled in red. **Top Inset:** Close-up of Si NWs. **Bottom Inset:** NWs between the gate and contact, under 10 nm Al2O3. **B.** Schematic of SF_6 plasma etching the NW channel with a Gaussian-like dopant profile (denoted by blue gradient)

(RTP). Immersion in a 6:1 NH_4:HF buffered oxide etch (BOE) removed the SOD post-anneal. 4-point resistivity measurements confirmed the dopant concentration. The SNAP method[22] was used to form the Si NW arrays on the prepared substrates. Portions of the Si NWs were selectively removed using SF_6 plasma, leaving behind 20 µm long NW sections. Source/drain (S/D) contacts were patterned using electron beam lithography (EBL) and Ti/Pt (40/20 nm) was deposited using an electron-beam metal deposition system. For the large-area devices, the S/D contacts were patterned to be 12 µm wide to contact all 400 NWs with a 9–11 µm channel length. After the S/D contract electrode formation, all devices were annealed at 475 ^oC for 5 minutes in forming gas (FG), which is composed of 95% N_2 and 5% H_2. Back-gated I_{DS}-V_{GS} measurements were obtained using the Si substrate as the back-gate electrode. For the n-type devices, the channel was selectively thinned using a directional CF_4 plasma etch to lower the dopant concentration until the back-gate on/off ratio improved to > 10 (Figure 4.4B).[21] For all devices, 10 nm thick Al_2O_3 was deposited onto the device substrate. The top gate was formed over the entire channel length using Ti/Pt (20/40 nm).

4.2.2 DC and AC electrical characterization of large-area devices

For the table look-up model, I-V and G-V data was collected using an Agilent B1500A Semiconductor Parameter Analyzer (Agilent Technologies) and C-V data was collected with a HP 4284 LCR meter (Hewlett Packard Company). The inverter circuits were controlled and measured with three Keithley 2400 SourceMeters (Keithley Instruments, Inc.). All devices were measured in probe stations using probe tips to contact the devices.

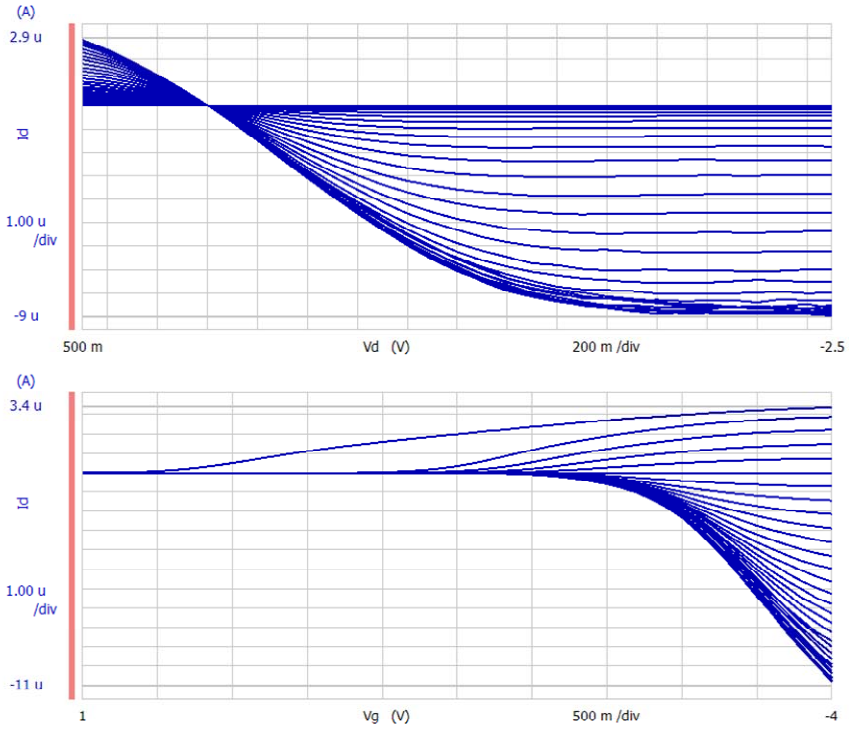

Figure 4.2. Representative DC data from a large-area p-type NW FET. **A.** $I_{DS} - V_{DS}$ curves for V_{GS} values from -4 V to +1 V, in 100 mV increments. **B.** $I_{DS} - V_{GS}$ curves for V_{DS} values from -2.5 V to 0.5 V, also in 100 mV increments

The n-FET devices were biased with V_{DS} values ranging from -0.5 V to +2.5 V in 100 mV increments and with V_{GS} values ranging from +1 V to -4 V, also in 100 mV increments. Similarly, for p-FET devices, V_{DS} varied from +0.5 V to -2.5 V and V_{GS}

varied from +1V to -4V (see Figure 4.2). Both I_{DS} and I_{GS} were measured for both sets of devices. Transconductance, g_m, and channel conductance, g_d, for every V_{GS} and V_{DS} value were calculated automatically by the Semiconductor Parameter Analyzer. The transconductance is defined as:[24]

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G=const.} \tag{4.2}$$

and the channel conductance is defined as:[24]

$$g_d \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=const.} . \tag{4.3}$$

To obtain good g_m and g_d values, the voltage increments were kept very small.

The experimental capacitances obtained were C_{GS} (capacitance from the gate to the source electrode), C_{DS} (capacitance from the drain to the source electrode) and C_{GG} (capacitance through the gate oxide with the source and drain electrodes shorted together in a MOS capacitor geometry). For all of the measurements, the AC voltage was 25 mV. C_{GG} values were obtained using DC biases of -4 V to +1 V, in 100 mV increments (Figure 4.3A). C_{GS} values were also obtained with V_{GS} values of -4 V to +1 V and also with V_{DS} values from -2.5 V to +0.5 V (p-FETs) or +2.5 V to -0.5 V (n-FETs), both with 0.5 V increments (Figure 4.3B). Similarly, C_{DS} values were obtained with V_{GS} values of -4 V to +1 V in 0.5 V increments and with V_{DS} values of -2.5 V to +0.5 V (p-FETs) or +2.5 V to -0.5 V (n-FETs), both in 100 mV increments. Data was interpolated for values between the 0.5 V increments in the C_{GS} and C_{DS} measurements. Both high-frequency (1 MHz) and low-frequency (100 kHz) measurements were made and the high-frequency

measurements were used in the look-up-table model. Data taken below 100 kHz was very noisy and unusable.

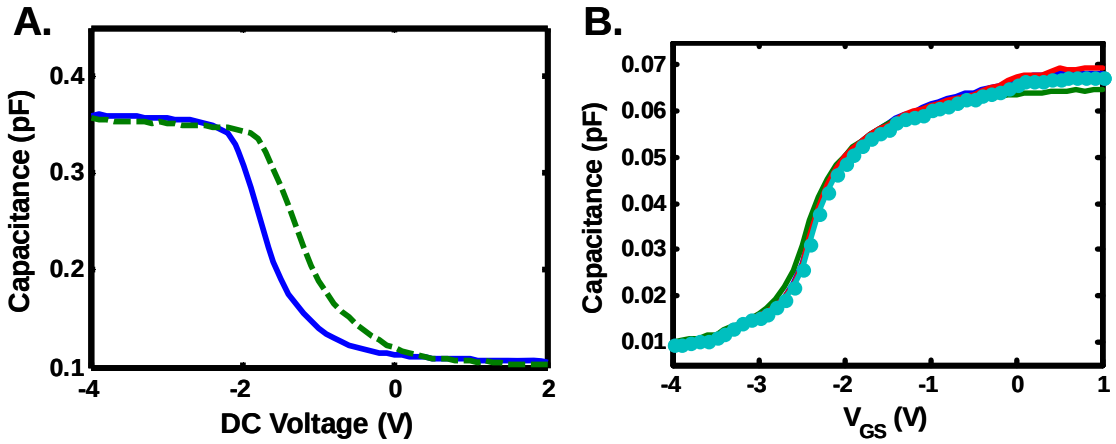

Figure 4.3. Representative capacitance data of NW FET devices. **A.** C_{GG} versus V_{GG} at 1 MHz (solid blue curve) and 100 kHz (dotted green curve). **B.** C_{GS} versus V_{GS} for various V_{DS} values

In addition to measuring the capacitance of the large-area FETs, metal capacitors containing 10 nm of deposited Al_2O_3 were fabricated with several different device areas to directly measure the dielectric constant of the dielectric layer. Assuming a dielectric thickness of 10 nm (as determined by the electron deposition chamber quartz crystal oscillator) and using equation 4.1, the average dielectric constant measured was 3.68. This value is significantly lower than the dielectric constant of high-quality Al_2O_3, ~ 10, and signifies the presence of defects in the film due to poor deposition control.

4.2.3 Calculation of performance metrics

For the fabricated test structures, the threshold voltage was calculated from the I_{DS}-V_{GS} plots. Since these devices do not have the conventional MOSFET structure in which the channel conduction arises from an inversion layer (Figure 4.4A), the definition of threshold voltage (V_T) will be clarified. The NW devices have a similar structure to

buried-channel or depletion-mode MOSFETs (BC-MOSFETs) (Figure 4.4B), where the conduction is modulated by controlling the depth of a depletion region, rather than an inversion layer.[25] The term "buried channel" arises from the fact that the conduction path is below the gate-induced depletion region, not along the surface as is the case for inversion-mode devices. This type of device benefits from a higher mobility, since surface scattering is alleviated. There are two V_T values to consider in this device: the voltage where the channel is completely depleted and the voltage at the onset of surface conduction, where the gate no longer controls the buried channel.[25, 26] This latter V_T is what will be measured in this paper, since it is more analogous to the V_T of conventional, enhancement-mode MOSFETs. At $V_{GS} < V_T$, known as the subthreshold region, I_{DS} varies exponentially with V_{GS}.[27] For this structure, conduction in this region is due to partially depleted carriers in the channel, not the formation of a weak inversion layer. However, in both types of devices, the current is an exponential function of the gate voltage, and so the subthreshold swing can be calculated for BC-MOSFETs using the same techniques used for conventional MOSFETs.[28]

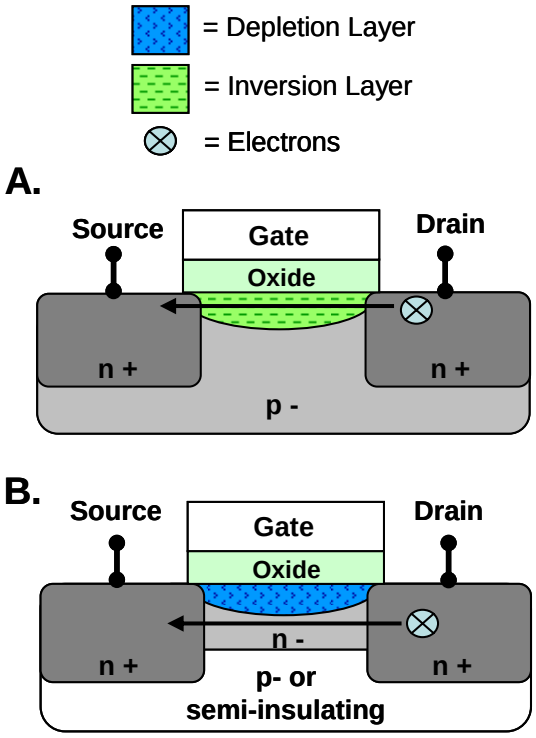

Figure 4.4. Comparison of conventional MOSFET to buried-channel (BC) MOSFET structures. **A.** Conventional MOSFET structure, operating in inversion mode. Carrier conduction occurs at the surface of the channel. **B.** BC-MOSFET structure. The gate creates a depletion region in the channel and conduction occurs away from the surface.

Threshold voltages (V_T) were calculated by fitting the linear region of the I_{DS}-V_{GS} transistor curves and extrapolating to I_{DS} = 0 at low (100 mV) drain bias. This follows the simple model,

$$I_{DS} = \mu_{eff} V_{DS} (W / L) C_{OX} (V_{GS} - V_{TLIN} - V_{DS} / 2). \quad (4.4)$$

Here μ_{eff} is the effective channel mobility, C_{OX} is the gate oxide capacitance, and V_{TLIN} is the linear threshold voltage. This model is effective when $V_{GS} - V_{TLIN} > V_{DS}$.[26] The linear region was determined by fitting to the slope around the voltage at maximum transconductance, g_m (Figure 4.5A).

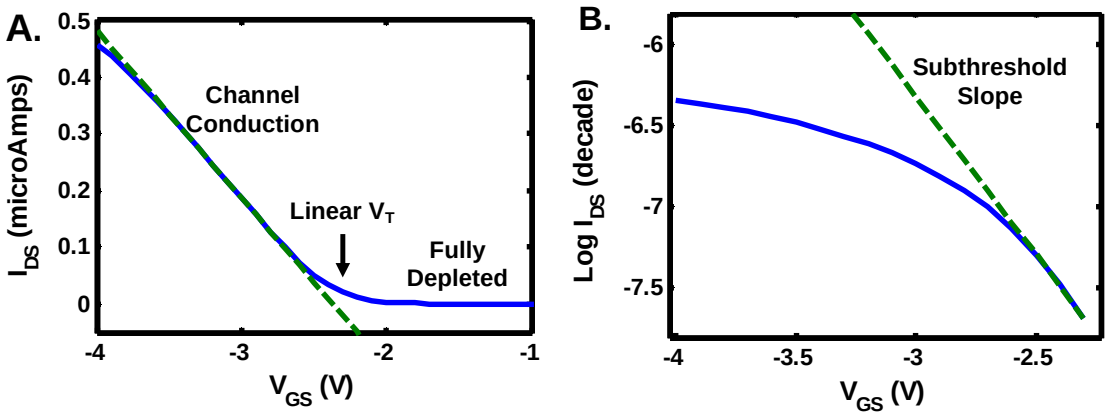

Figure 4.5. Threshold and subthreshold characteristics of NW p-FET. **A.** Plot of I_{DS}-V_{GS} characteristics (solid blue curve). A line was fitted to the linear region (dashed green line), where the x-intercept is the linear threshold voltage. **B.** Log(I_{DS})-V_{GS} plot in the subthreshold region. The dotted green curve was fitted to the linear portion of the blue curve and its inverse slope is the subthreshold swing.

Once V_T was found, the subthreshold swing, **S**, (or inverse subthreshold slope) could also be determined. For each transistor curve, a line was fitted to the linear portion of the log(I_{DS})-V_{GS} plot at $V_{GS} < V_T$ (Figure 4.5B). The slope of this line is the subthreshold slope. Note, this method for determining **S** is different than has been previously been used by various groups for NW or CNT FETs (and from what had been

described in Chapter 2),[7, 15, 29] but yields results that are more comparable to standard MOSFET parameters.

For the n-type NW FET, the threshold voltage was calculated to be -0.9 V. The subthreshold swing was calculated to be ~ 550 mV/dec. For the p-type NW FET, the threshold voltage was determined to be -2.3 V and **S** was ~ 450 mV/dec. For BC-MOSFETs, the ideal value for **S** is > 80 mV/dec (for inversion-type MOSFETS, the ideal is 60 mV/dec) and as the channel thickness increases relative to the substrate, **S** becomes > 100 mV/dec. In these NW devices, there is no substrate junction to help modulate a depletion region so the gate alone must be as effective as possible. Since the gate only modulates the top of the NWs, this leads to a increase in **S**.[30] Other issues, such as the effect of surface states on a large surface-area-to-volume ratio device and the thick (and low-quality) dielectric material also lead to a degradation of **S**. However, these devices still show excellent electrical properties, such as a high on/off ratio (approximately 10^4 for both p- and n-FETs) and high on-currents (p-type: ~ 1 μA; n-type ~ 5 μA).

4.3 Setup of device look-up table model and simulations

Device look-up table-models are not new—they have been implemented using several simulators, including SPICE.[31–34] However, tabular models are typically employed to decrease the circuit simulation evaluation time and are usually constructed using analytical device models, supplemented with experimental data only partially, if at

all. Analytical models are computationally time-consuming to implement during a circuit simulation if the device model becomes very complex. As devices continue to shrink and exhibit non-bulk effects, such as performance degradation due to surface-states, their associated analytical models become increasingly complex and more difficult to develop.[32] Therefore, tabular models become an attractive alternative.

There are two caveats to using an experimentally derived table model. The first is that all device parameters (channel length, dopant profile, source/drain/gate materials, temperature, etc.) are fixed for a given model and cannot be altered in the circuit simulation environment. Second, not every conductance and capacitance value can be directly measured for input into the look-up table. The approximations that were used for the look-up table are described below.

4.3.1 The look-up-table format

The device look-up table, labeled the Device Exploration Workbench (DEW) in the Intel simulation environment, is used to define an n-terminal black box device that can be used as a circuit component in the circuit simulator. The file format is shown in Figure 4.6. An example DEW file appears in Appendix A. Essentially, experimental data is compiled into a large matrix with dimensions of n - 1, where n is the number of device terminals. For instance, for a three-terminal device, a two-dimensional matrix of data is generated since data is taken with respect to the third terminal.

```
model = "ccc1"    length = 0.13  width = 1.2  temp = 110.0
4                                              /*  # terminals (4 for this model) */
1 1  1 1 1 0  1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 0 0 0 1  /* data sparsity pattern (integer) */
s1 s2 s3                                       /* # sample points per direction  (integer) */
v1 v2 v3  I1 I2  G11 G12 G13 G21 G22 G23 G31 G32 G33  C11 C22 C33
…                                              /* actual data, one row per grid point */
…
…
endmod                                         /* end of model */

model = "ccc2"   length = 0.25 width = 3.4  temp = 25.0     /* another model */
3                                              /* # terminals (3 for this model) */
1 1 1 1 1 1 1 1 1 1 1 1
s1 s2
v1 v2  I1 I2 G11 G12 G21 G22 C11 C12 C21 C22
…
…
endmod
….
end                                            /* end of the file */
```

Figure 4.6. The format of the Device Exploration Workbench file

Before the experimental data can be listed in the file, several device and table parameters must be defined. In the DEW file, the first line provides the model name, the device's dimensions (in μm) and the device temperature. The simulator assumes that the current and conductance values listed in the table are given as function of device width (i.e., current is listed as A/μm). Therefore, in the circuit simulation environment, it is possible to change the device width and the simulator will multiply each current and conductance value with the appropriate factor.

The second and third lines in the DEW file provide the number of terminals in the black box device and the data sparsity pattern. A typical MOSFET, for instance, has 4 terminals: source, drain, gate, and substrate. Experimental data is broken up into columns of voltages, currents, conductances, and capacitances. For every column of data present, there is a 1 listed for it in the data sparsity pattern. For any columns missing (for instance, if no data was taken for that column), the data sparsity pattern would list that

column a zero. This lets the simulator realize that the correct column is missing and not misread the subsequent columns.

The fourth line lists the size of each direction in the matrix, which is given by the number of voltage values measured at each terminal. For instance, for each NW transistor, the current and conductance values from 26 drain voltages and 41 gate voltages were measured, generating a 26 × 41 matrix.

The experimental data is then listed with the applied voltages first, followed by the measured current, conductance, and capacitance values. Multiple models can be appended to one file and the simulator can interpolate between models that differ in parameters such as channel width and temperature.

The current values for the given voltages are straightforward to add to the DEW file. However, both the conductance and capacitance values appear in a matrix format. The conductance values required for the DEW file had the matrix format:

$$G = \begin{pmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{pmatrix} = \begin{pmatrix} g_{dg} & g_{dd} \\ g_{gd} & g_{gg} \end{pmatrix}. \tag{4.5}$$

It was assumed that $g_{dd} = g_m$ and that $g_{dg} = g_d$. Since the gate current was very low, g_{gg} and g_{gd} were approximated as zero for all voltages.

The capacitance measurements required some approximations to be made. The

$$C = \begin{pmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{pmatrix} = \begin{pmatrix} C_{DD} & -C_{DG} \\ -C_{GD} & C_{GG} \end{pmatrix}. \tag{4.6}$$

capacitance matrix required the DEW file to have the form:

Here $C_{DD} = C_{DG} + C_{DS}$, where C_{DG} is the capacitance between the drain and the gate electrodes and C_{DS} is the capacitance between the drain and the source electrodes. Similarly, $C_{GG} = C_{GD} + C_{GS}$. The off-diagonal elements are negative.

The capacitance data obtained experimentally were C_{GS}, C_{DS}, and C_{GG}. The C_{DS} values, however, did not seem trustworthy because they had associated large dissipation factor, D, values. D is a measure of capacitor quality[35] and for values of $D >> 1$, there is significant current leakage through the device and the measured capacitance values are not accurate. Therefore C_{DS} was set to zero for all V_{DS} and V_{GS} values. It was also assumed that C_{DG} was equal to C_{GD}. Thus to simplify this matrix into experimental obtained values, C_{DD} was approximated as C_{DG} and C_{DG} was assumed to be equal to $C_{GG} - C_{GS}$. The capacitance matrix then becomes:

$$C = \begin{pmatrix} C_{GG} - C_{GS} & -(C_{GG} - C_{GS}) \\ -(C_{GG} - C_{GS}) & C_{GG} \end{pmatrix}. \tag{4.7}$$

The measurement and calculation of propagation delay was used to verify the accuracy of these assumptions and further details are presented in Section 4.5.

4.3.2 Circuit simulation setup

Python programming language scripts were written and used to compile the experimental data into the DEW file (this is highly recommended as some of the DEW files contained over 16,000 lines of text). The circuit schematics were drawn and converted to the netlist format (a text-based format which describes the circuit using nodes) using Virtuoso® Schematic Editor (Cadence, Inc.). The netlisted circuits were then imported into Presto, the graphical user interface for the Intel Lynx simulator.

The Lynx simulator performs numerical analyses via Newton iterations and sparse matrix solves of the non-linear alegebraic-differential equations that model the behavior of a circuit. Its performance and accuracy is similar to SPICE. Some of the standard analyses that Lynx can perform are DC analyses as a function of a variety of circuit parameters, the time-domain response of the circuit driven by time-varying sources (transient analysis), frequency domain small-signal analyses sweeps, and pole-zero analyses. For this study, only DC and transient analyses were performed.

The circuit simulations were set up to measure the desired DC and AC metrics and run using the standard analytical device models. The purpose of this step was that Presto would generate a simulation file, called the "runinput" file, that contains all of the parameters for the simulation. The runinput file was modified using a Perl programming language script so that the files referenced the appropriate DEW file instead of the standard analytical models. The circuit simulation was re-run using the modified runinput file and output files were viewed using the EZWave waveform viewer (Mentor Graphics Corp.) and analyzed using MATLAB and Microsoft Excel.

This method for simulated circuits using a look-up device model is specific to the Intel simulation environment. However, it would be straightforward to devise an approach for a standard, commercially available simulator.

4.4 Initial DC circuit simulation results

To verify that the simulator was accessing the DEW file correctly, a circuit was designed to contain a single transistor and the transistor curves were simulated. Figure 4.7 shows a comparison of the simulated transistor curves (lines) with the original experimental data (solid circles). The simulation error was ~ 0.1%. The error in the simulated versus experimental curves is due to the fact that the simulator is not only using the current values to calculate the curves but also utilizing the measured conductance values as well.

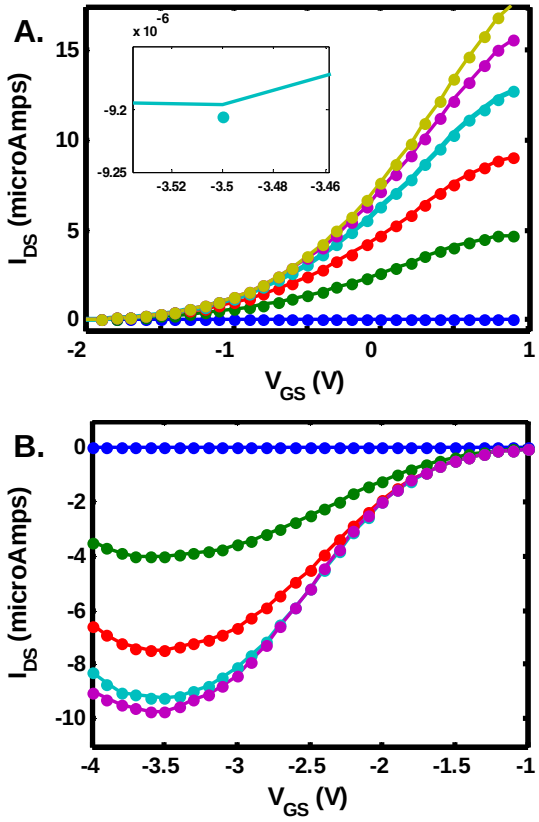

Figure 4.7. Comparison of simulated (solid lines) and experimental (solid circles) device parameters. **A.** N-FET data for drain-to-source current (I_{DS}) versus gate-to-source voltage (V_{GS}) for drain-to-source voltages (V_{DS}) of 0 V (blue) to + 2.5 V (gold). The error between simulated and experimental values is approximately 0.1% (see inset). **B.** Analogous curves for p-FETs for V_{DS} of 0 V (blue) to -2 V (purple)

Once it was confirmed that the simulator was accessing the DEW file correctly, DC simulations were implemented. Note that the DC simulations did not require the capacitance data to be present in the DEW file.

The simplest logic function to implement is the inverter, or NOT function. The inverter requires one p-FET and one n-FET. Through their source electrodes, the p-FET is connected to a power supply, V_{DD}, and the n-FET is connected to ground. The input

controls the gate to both FETs simultaneously. An input high (H) voltage turns "off" the p-FET and turns "on" the n-FET, so that the output is connected to ground. An input low (L) voltage turns "off" the n-FET and turns "on" the p-FET and the output is connected to the power supply. Thus, this circuit inverts the input signal. Because this design uses two transistors, rather than a transistor and resistor (RTL), there is no direct pathway from V_{DD} to ground and this circuit is power efficient. The circuit schematic for this function is shown in Figure 4.8A. A more extensive discussion of logic gate operation appears in Section 3.1.1.

The simulated inverter curve (solid blue line) is shown in Figure 4.8A. The power supply for this circuit, V_{DD}, is at +4 V. The maximum slope of the transition between the H and L voltage states represents the gain of the inverter (Figure 4.8A Inset). A gain > 1 is required for the output voltage levels to restore to the magnitude of the input levels. A larger gain implies better noise margins (NMs), which represent a tolerance to voltage variation in the input signals. NM_{LOW} (NM_{HIGH}) is defined as the difference between the input and output voltages in their L (H) state at unity gain. A gain < 1 implies no NMs. Ideally, NM_{HIGH} and NM_{LOW} should be both large and matched to one another.[36]

The gain of the simulated inverter (~ 4) is comparable to previous circuits (see Chapter 3).[8] Because the gain of the inverter did not drop below 1 at the input L state, the NMs could not be calculated. The inverter does not fully regenerate signal to +4 V at the input L state (indicated by a red arrow on Figure 4.8A). Since the output is lower than V_{DD}, the n-FET is not fully "off", resulting in a high leakage current of 3 μA at the input L state. This suggests that the threshold voltage, V_T, is not optimized for this

device and the device is always "on", regardless of applied gate bias. Also, the center of the inverter curve is shifted towards the input L state, indicating the n-FET has a larger

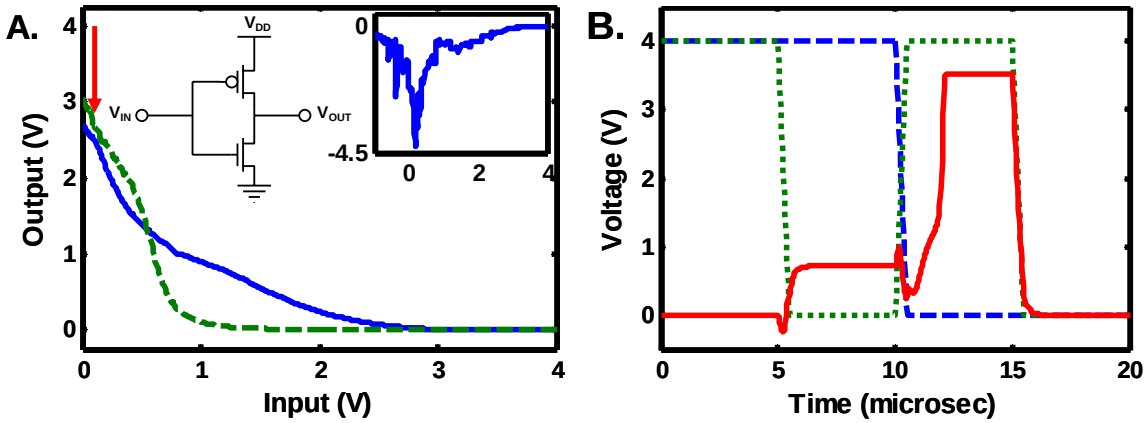

Figure 4.8. DC simulation results of the inverter and XOR logic gates. **A.** Input versus output voltages of initial simulated (solid blue line) and fabricated (dashed green line) inverter. The red arrow indicates where the output voltage is not restoring to the power supply, V_{DD}. **Left Inset:** Circuit schematic of CS inverter. **Right Inset:** Simulated inverter gain as a function of input voltage. **B.** Transient analysis of XOR gate with two inputs (dashed blue line and dotted green line). The output (solid red line) does not match the truth table for this function suggesting a mismatch in NW FET performance.

saturation current than the p-FET.[36]

The fabricated large-area FETs were also connected in the inverter configuration (using off-chip connections) and measured. The experimental DC transfer characteristics are shown in Figure 4.8A (dashed green line). This curve had many similar characteristics to the predicted inverter curve. The measured inverter has a comparable gain (~ 7.5) and NMs also could not be calculated. It also lacks signal restoration at the input L state, and is not symmetric over $V_{DD}/2$.

This mismatch in FET performance becomes more apparent as the circuits become more complex. Figure 4.8B presents the simulated XOR circuit, which comprises 6 p-FETs and 6 n-FETs. This circuit contains two inputs, which are represented on the graph as the dashed blue line and the dotted green line. For the XOR

logic gate, when the two inputs are different (i.e., one is in the H state, the other in the L state), the output should be in the H state. However, for the simulated NW circuit, this does not occur and the function fails to go to its H state (V_{DD} = +4 V). Integrated circuits are comprised of several connected logic gates (for instance, a 2-bit half adder can be generated by coupling a XOR gate with an AND gate) and thus with these devices as-fabricated, more complex computations would fail.

4.5 Transient analysis circuit simulation results

To verify that the capacitance elements in the DEW file were correct and being accessed by the simulator correctly, the propagation delay, t_{pd}, of the inverter circuit was calculated and compared to the simulated results. This metric constitutes the time difference between the mid point of the input swing and the mid point of the output swing, and can be used to estimate the speed of complex circuits.[37] Propagation delay can be calculated from:

$$t_{pd} = \frac{C_L \cdot V_{DD}}{2 \cdot I_{D(SAT)}} \tag{4.8}$$

where C_L is the load capacitance and $I_{D(SAT)}$ is the saturation current for the FET. To measure the propagation delay, the inverter circuit was designed using a second inverter as the load capacitance (Figure 4.9). Since the measured gate capacitance is ~ 0.35 pF for one device, the total load capacitance is ~ 0.7 pF, ignoring any wiring capacitance. V_{DD} = +4 V for this circuit and the saturation currents for the n-FET and the p-FET are 9 μA

and 100 μA, respectively. This leads to a calculated t_{dr} = 160 ns and a t_{df} = 14 ns. The total propagation delay, which is the average of the rise and fall delays, is 87 ns. The same inverter circuit with C_L was also examined in the simulation environment. In Figure 4.9, the transition midpoints for the input (dashed blue line) and the output (solid green line) are denoted by red arrows. The simulated propagation delay values are t_{dr} = 180 ns and a t_{df} = 20 ns, which equals a total propagation delay of 100 ns. The good agreement between the simulated and calculated delay values demonstrates the accuracy of the tabular model-based simulations for transient metrics.

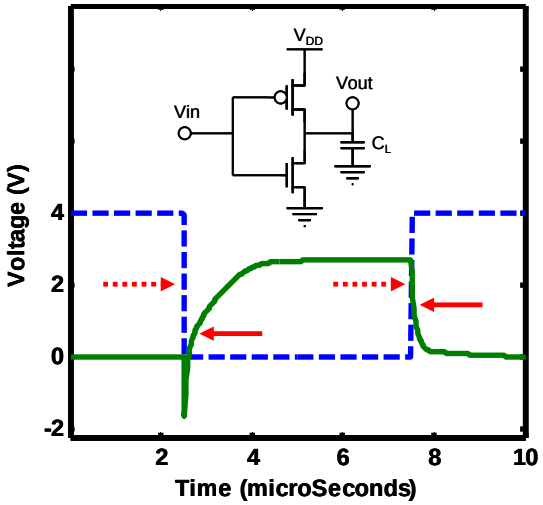

Figure 4.9. Simulated transient plot of inverter. Input voltage is the dashed blue line. Output voltage is the solid green line. Red arrows denote the 50% point of the voltage transitions. **Inset:** Circuit schematic of inverter with load capacitance, C_L

4.6 Optimized DC circuit simulation results

To explore the effects on the inverter circuit by altering the NW FET performance, two aspects of the simulation were modified. First, the number of NWs per device were scaled to 10:1 (p-FET: n-FET), to match the saturation current levels. Second, a battery element that offset the input voltage for the n-FET was incorporated into the simulated circuit (see Figure 4.10A). The addition of the battery mimicked the

effect of a V_T shift for the n-FET. Simulating an n-FET voltage shift of -1.8 V relative to the original V_T yielded significantly improved inverter transfer characteristics (Figure 4.10A).

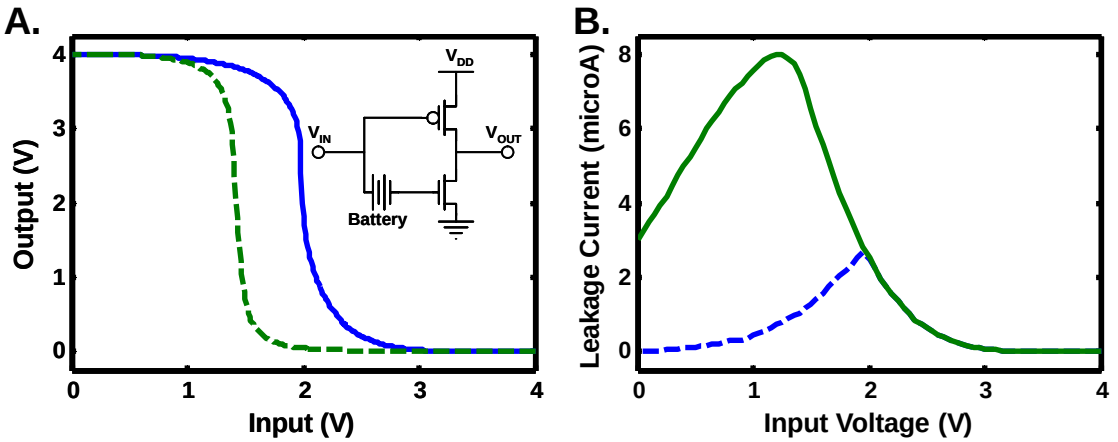

Figure 4.10. DC characteristics of simulated and experimental CS inverters. **A.** Inverter transfer characteristics of simulated (solid blue line) and fabricated (dashed green line) optimized inverter. **Inset:** Circuit schematic of inverter with additional battery element. The fabricated device approximated this circuit through the use of separate power supplies for the p- and n-FETs. **B.** Leakage current of initial (solid green line) and optimized (dashed blue line) simulated inverters. The leakage current at the input L and the short circuit states improved by a factor of ~ 220 and ~ 3, respectively.

The resulting simulated inverter is fully regenerative and has a gain of ~ 45, with large, well-matched NMs of 1.2 V and 1.4 V. The curve is symmetric over $V_{DD}/2$, indicating current-matched devices. The leakage current also improved to 14 nA at the input L state and the short circuit leakage current (the point of maximum leakage current) reduced by a factor of three and became centered over $V_{DD}/2$ (Figure 4.10B). These results show that by shifting the V_T on the n-type NW FET and scaling the device widths to match their saturation currents, the inverter characteristics are significantly improved.

The accuracy of the simulated results was again verified by connecting the fabricated devices in the inverter circuit configuration. An additional power supply was used for separately driving the n- and p-FETs in analogy to the simulated battery element.

With an input voltage shift of -800 mV on the n-FET, the inverter exhibited full signal restoration, NMs of 2.1 V (H) and 1 V (L), and a gain of ~ 30 (Figure 4.10A dashed green curve). The voltage swing shifted to the left due to the mismatched saturation current levels of the n- and p-FETs, which was corrected in the simulations. Otherwise, the curves are in good agreement with each other.

4.7 MEDICI simulations

To facilitate the designing of the NW n-FET device with a shifted V_T, MEDICI simulations were utilized. MEDICI (Synopsys Inc.) is a two-dimensional semiconductor device simulator that models the potentials and carrier concentrations in a device for any given biases.

The graphical representation of the MEDICI modeled NW n-FET is shown in Figure 4.11. The Si NW and Si substrate layers are shown in green and the top gate oxide and buried oxide layers are shown in blue. The grid points determine the points where the potential and carrier concentration distributions are calculated. The modeled NW FET structure consists of, from top to bottom, 10 nm oxide (with $\kappa = 3.5$, determined from measurements), 34 nm thick Si, 250 nm SiO2 oxide substrate, and a substrate Si layer. The device is 1.5 μm long, with 0.5 μm wide source, drain, and gate electrodes with no overlap. The MEDICI code to generate the NW structure and for the following results is presented in Appendix B.

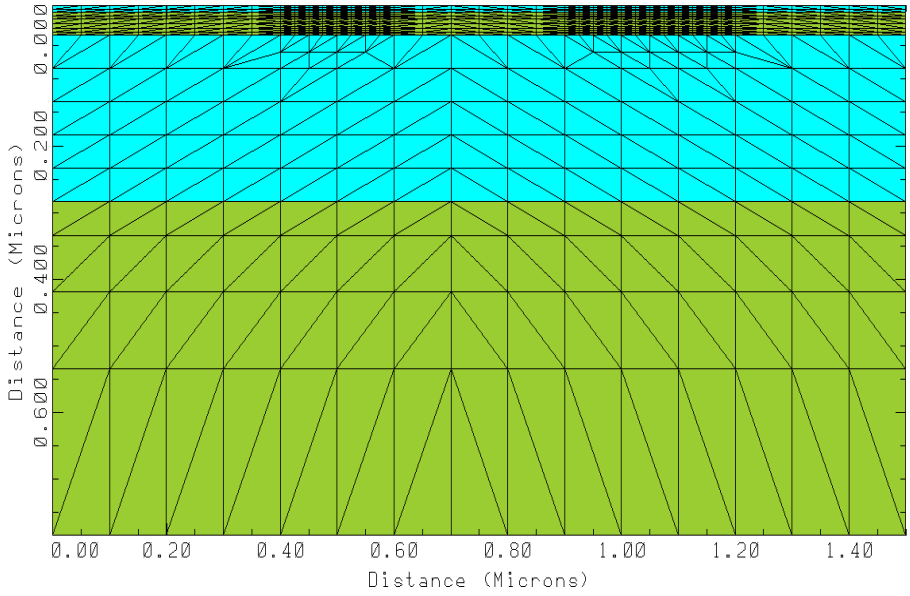

Figure 4.11. Graphical representation of MEDICI modeled NW FET with overlaid grid points. At these points, potential and carrier concentration values are calculated.

Once the modeled NW structure was generated, MEDICI was able to provide some physical insight into the NW device operation. Figure 4.12 shows the side-profile of a NW p-FET doped at different gate biases. The dopant concentration was modeled to be a Gaussian-like profile with its peak concentration, 1×10^{18} cm^{-3}, centered at the surface of the NW. This profile models the experimental profile obtained for diffusion doping (see Section 2.2.1)

At V_{GS} = +2 V, the device is operating in enhancement mode (Figure 4.12A). The hole carriers are attracted towards the gate, as depicted by the dense potential contours, creating an effective peak carrier concentration of 6×10^{18} cm^{-3} under the gate. The device is "on" at this point.

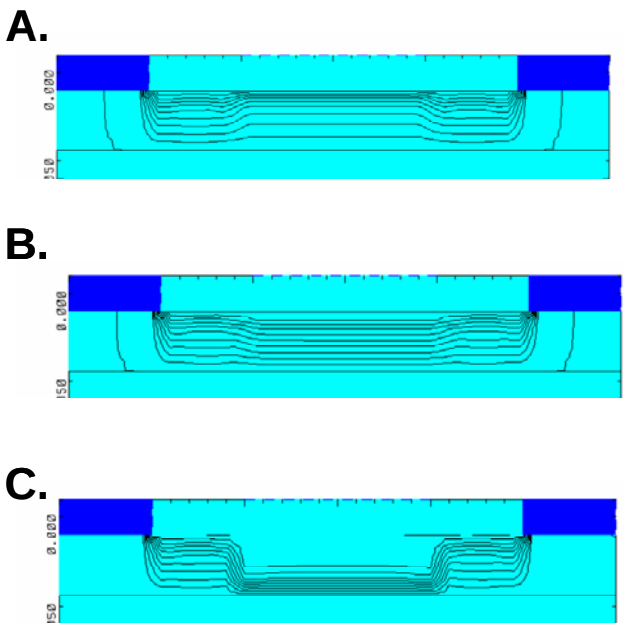

Figure 4.12. NW device potential contours for different gate biases. **A.** Device operating in enhancement mode **B.** Zero gate bias on device. **C.** Device operating in depletion mode

Next, at V_{GS} = 0 V, a depletion region forms under the gate. This is due a mismatch of the gate metal's work function, Φ_M, to the electron affinity of the Si, which leads to band bending at the metal-oxide-Si interface.[24] The effective dopant concentration directly underneath the gate drops to 2×10^{17} cm^{-3}.

Finally, at V_{GS} = -2 V, the negative bias repels the hole carriers from the channel and the depletion region grows significantly larger. Consequently, the device conductivity drops and is "off" at this point. The effective dopant concentration under the gate drops below 1×10^{15} cm^{-3} throughout the entire channel. The behavior of the modeled devices for different gate biases is in agreement with experimental results and with the buried channel MOSFET description used earlier to define V_T and **S**.

Several NW parameters were varied, including the channel dopant profiles and gate metals, using V_T as feedback. The dopant profile of the device with the best V_T consisted of a uniform background n-type dopant concentration of 10^{14} cm-3 with Gaussian-like NW dopant profiles having peak concentrations at the NW surface of 10^{16} cm^{-3} under the gate and 10^{19} cm^{-3} under the S/D contacts. Solutions for the I_{DS}-V_{GS} curves were determined using models that took into account Shockley-Read-Hall

recombination with carrier-dependent lifetimes, a concentration- and temperature-dependent mobility, and an enhanced surface mobility at the semiconductor-insulator interfaces due to scattering from phonons, surface roughness, and charged impurities.[38] The Newton solution method was used for both n- and p-type carriers. For the simulated I_{DS}-V_{GS} curves, V_{DS} was fixed at 100 mV and V_{GS} was measured in 50 mV steps. Both Ti and Pt gate electrode metals were considered, as well as higher channel doping (> 10^{18} cm^{-3}).

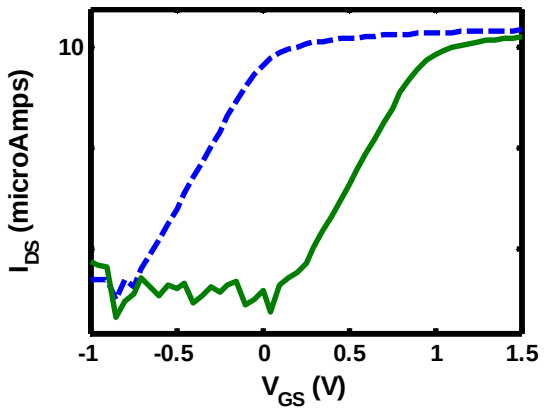

Figure 4.13. Semilog plot of I_{DS} versus V_{GS} for MEDICI modeled n-FET with Ti gate metal (dashed blue line) and Pt gate metal (solid green line)

For devices with a channel doping < 10^{18} cm^{-3}, a large V_T shift was observed in the MEDICI simulations (Figure 4.13) by replacing the Ti gate metal (Φ_M = 4.28 eV) with Pt (5.6 eV). The larger Φ_M promoted a large depletion region in the gate so that at V_{GS} = 0, the device was fully "off". This effect was observed in the modeled structures for low doped channels only; dopant concentrations > 10^{18} cm^{-3} do not facilitate the formation of a large depletion layer. Thus, it was predicted that utilizing these changes to the FET design would yield significantly improved results in the fabricated devices.

4.8 Fabrication of improved n-FETs and inverter circuit performance

The fabrication of the improved n-FETs was the same as the large-area devices except for three modifications. First, the Ti/Pt gate was replaced by a 50 nm thick Pt gate. Second, the S/D contacts ranged from 0.75–1 µm wide with 2 µm channel lengths. Lastly, the device channels, prior to gate formation, were aggressively etched using the same directional CF_4 etch process used in the large-area devices.

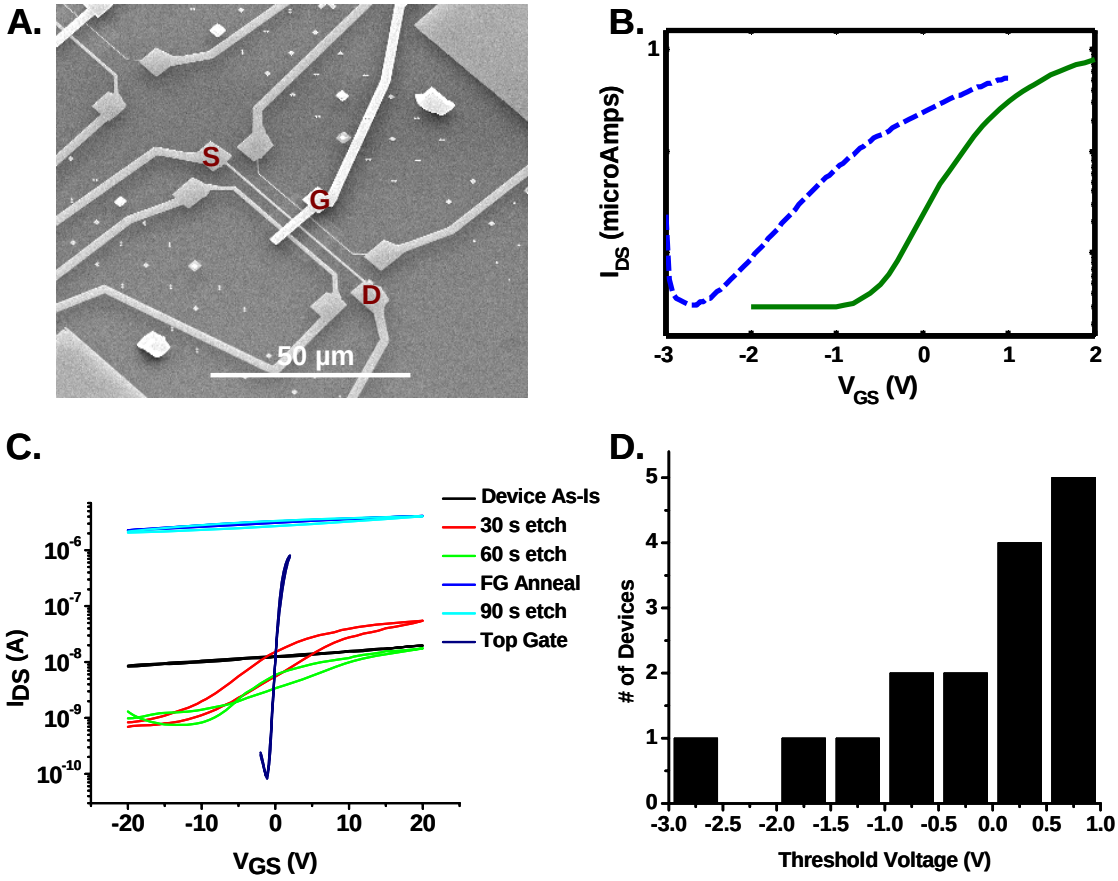

Figure 4.14. Fabrication and characterization of improved n-FETs. **A.** Scanning electron micrograph of improved n-FET. **B.** I_{DS}-V_{GS} plots of devices with Ti/Pt gate electrode (dotted blue curve) and Pt gate electrode (solid green curve). **C.** I_{DS}-V_{GS} plots of representative n-FET after channel etching, FG anneal, and top gate formation. **D.** Bar graph showing the distribution of threshold voltages of improved n-FETs

Figure 4.14A shows the scanning electron micrograph of the fabricated transistors. Three transistors of varying widths were fabricated per top gate electrode. The Pt gate is evident by its brightness in the image, due to the higher work function of the metal. $I_{DS} - V_{GS}$ measurements were taken of the Pt gate n-FETs and compared with devices fabricated with Ti/Pt gates. The comparison is shown in Figure 4.14B. A large V_T shift was observed, in agreement with the MEDICI results (Figure 4.13).

The large observed V_T shift was also due to more careful control over the channel etching procedure. For the original n-FETs, back-gating measurements were first performed after approximately three minutes of channel etching and then after one minute cycles. For the improved n-FET devices, measurements were performed after every 30 s of etching (see Figure 4.14C). Current hysteresis, caused by the interface damage induced by the etching process, was observed after a few etch cycles and could be reduced by a FG anneal. Care was taken so that the optimal etch time was not exceeded.

It was observed during the channel etching that the FET devices did not have identical performance characteristics. Figure 4.14D gives the distribution of threshold voltages for the fabricated improved n-FET devices. The majority of devices have $V_T > 0$ V. High-channel doping (due to variations introduced the doping and etching processes) led to the negative V_T, which can be shown by looking at the device on/off ratios. The devices with $V_T > 0$ V had an average on/off ratio of 2.4×10^4, whereas the devices with $V_T < 0$ V had an average on/off ratio of 5.5×10^2. Both sets of devices have similar "on" currents (in the low μA range) so the lowered on/off ratio is likely indicative of higher channel doping which screens against the gate.

The improved n-FETs were paired with the original large-area p-FETs to form CS inverters (Figure 4.15). The gain of the inverter circuit increased to ~ 45, with well-matched NMs of 1.2 V and 1.5 V. All of the tested circuits had gains > 15 and showed full signal restoration. This substantial improvement over the original devices was consistent with the DC simulated predictions.

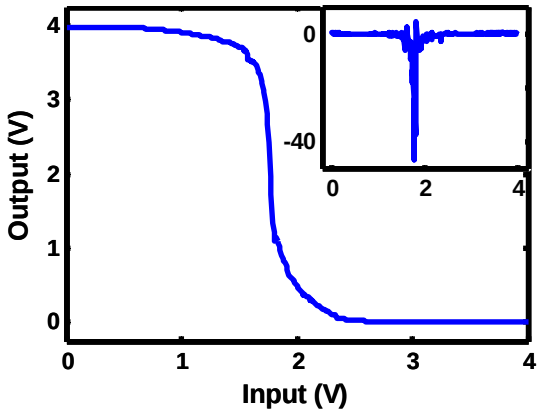

Figure 4.15. Input versus output voltage characteristics of fabricated CS inverter with Pt-gate n-FET. **Inset:** Inverter gain

4.9 Potential directions for simulation methodology

Although optimizing an inverter is a simple demonstration, it does highlight the effectiveness of the simulation methodology and provides a pathway for more complex demonstrations. The optimizations done for the inverter circuit would also lead to optimizations of the other Boolean logic functions, for instance. Also, the number of gates that one gate can drive (fan-in, fan-out) could be addressed. Besides conventional circuit metrics, this approach may be adopted to optimizing circuit architecture to the performance of nanoscale devices. As the channel material shrinks, device variations increase and circuit architecture will need to compensate for device fluctuations.[39] Architectures specific to nanoscale transistors will need to be developed and simulations will play a critical role. Examples of this include reconfigurable logic circuits or

asynchronous logic design, where the high-performance FETs can be used efficiently and the low-performance FETS can be used in non-critical areas or not used at all.

Another important area that will need to be addressed more in-depth is device and circuit operating speed. Preliminary transient analyses were performed that highlighted the accuracy of the table look-up model but no optimizations were done. Transient analyses of circuits could be used as feedback for improving device speed, in an analogous method for optimizing DC metrics. This would allow for the efficient fabrication of circuits that require high frequency or high speed, such as a ring oscillator.

4.10 Conclusions

Si NW n-FETs and p-FETs were optimized using in silico circuit and device simulations in feedback with device fabrication methods to produce complementary symmetry inverters. Inverters with gains of 15–45, well-matched noise margins, and full signal restoration were demonstrated. The presented method provides a highly efficient means for optimizing nanowire logic circuits and is accurate for both DC and transient analysis. By incorporating CAD simulation tools into the design process, nanocircuits can be efficiently optimized and evaluated.

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4.12 Appendix A: Example DEW file

```
model="n" length=1.0 width=1.0 temp=27.0
4
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
21 41 1
0.000000000000000E+00 -2.000000000000000E+00 0.000000000000000E+00 3.494819016187532E-18
0.000000000000000E+00 -8.413427471762958E-23 -2.286826368939761E-16 1.095358791138519E-15
2.882067472186025E-17 -2.194628038929934E-09 4.267492849807550E-09 1.141554607073525E-10 -
9.662736441750363E-12 1.878936109091902E-11 5.026155301586565E-13 7.586759229417460E-15 -
1.442840439478264E-14 -5.205045119839168E-16 -1.970991284762281E-15 3.945077430329101E-15
-9.709500593967943E-18 -1.514938920883643E-16 -7.365236946635662E-17 3.824596329332202E-16
0.000000000000000E+00 -1.899999976158142E+00 0.000000000000000E+00 -8.742570047332274E-18
0.000000000000000E+00 5.283858054845547E-23 5.753081982417774E-16 -9.475566478818960E-17 -
2.695543929085772E-18 1.902112747766376E-10 -3.715140936419881E-10 -9.925124107157983E-12
8.490534845192351E-13 -1.658341941793137E-12 -4.430314005716394E-14 1.256604353786455E-16
8.168715046094403E-17 -1.322994645096927E-16 -1.909745157698016E-15 3.841631683478066E-15
-1.227018346413364E-17 -1.837457239306044E-16 -1.651450826825841E-17 3.835128233023605E-16
0.000000000000000E+00 -1.799999952316284E+00 0.000000000000000E+00 -2.842212425724106E-18
0.000000000000000E+00 -8.887113075780797E-25 7.169239730877883E-16 1.041101040945238E-16
2.701194415527146E-18 -2.140765964608994E-10 4.191172493017711E-10 1.116220479407387E-11 -
9.680030735725471E-13 1.895147776922680E-12 5.047284399423782E-14 5.421640337245608E-16 -
7.335858463398872E-16 -1.539736133211269E-16 -1.799857512063013E-15 3.634563267334810E-15
-1.759786441529534E-17 -1.850858253073832E-16 -1.208756836220104E-17 3.830048256243528E-16
0.000000000000000E+00 -1.700000047683716E+00 0.000000000000000E+00 -2.318141918686450E-18
0.000000000000000E+00 -1.491409872170222E-22 1.887816293244370E-15 -8.233292348890978E-16
-2.180103261088348E-17 1.806820502550434E-09 -3.519897253479962E-09 -9.321131104587970E-11
8.309519201722654E-12 -1.618791339259284E-11 -4.286763224007041E-13 -1.721659912145515E-15
3.681254720899602E-15 -3.690993519431219E-17 -1.602428518185430E-15 3.232302603809384E-15
-2.789871759778593E-17 -1.637681474688418E-16 -5.608605099551391E-17 3.809285847921067E-16
0.000000000000000E+00 -1.600000023841858E+00 0.000000000000000E+00 1.167330893285039E-17
0.000000000000000E+00 2.186120661107577E-22 3.751662992119589E-15 1.121245813175590E-16
3.181073078546008E-18 -2.625568951734413E-10 5.117367619799339E-10 1.344408475988201E-11 -
1.259226195729392E-12 2.454295994235714E-12 6.447803296923181E-14 6.931566664115876E-16 -
1.014320564941197E-15 -1.612113610062498E-16 -1.153251436959112E-15 2.356585947628214E-15
-4.980770002370259E-17 -1.703817069615313E-16 -3.939590555001334E-17 3.798777373907032E-16
0.000000000000000E+00 -1.500000000000000E+00 0.000000000000000E+00 2.260352793302751E-18
0.000000000000000E+00 -1.789882660516643E-23 3.149116370283866E-14 5.252468965438293E-18
5.170473497558339E-19 -1.300582371350667E-11 2.535732826055741E-11 6.543357372073448E-13 -
6.992808230858281E-14 1.363381050169545E-13 3.518141901153155E-15 3.260835772454757E-16 -
2.844640680079088E-16 -1.419967250723943E-16 -2.954442962996048E-16 6.817916174140990E-16
-9.090286532153482E-17 -1.423332536782072E-16 -9.089310608354368E-17 3.755274236313952E-16
0.000000000000000E+00 -1.3999999976158142E+00 0.000000000000000E+00 -4.116770944932168E-19
0.000000000000000E+00 -1.723950248891080E-22 9.962795690967232E-13 -2.764642541973911E-19
```

Figure 4.16. Screen shot of DEW file. First line is highlighted in blue to show the text-wrapping. Each model within the DEW file contains 861 lines of experimental data and there is typically one p-FET and n-FET model per DEW file. To print out the entire DEW file would require 65,525 pages.

4.13 Appendix B: MEDICI code

P-FET structure MEDICI Code:

```
TITLE       P-type Si NW FET on SiO2

COMMENT           Specify a rectangular mesh

MESH        SMOOTH=1

COMMENT           Specify mesh dimensions

X.MESH            WIDTH=1.0   H1=0.1
Y.MESH            N=1         L=-0.005
Y.MESH            N=2         L=0.0
Y.MESH            DEPTH=.034  H1=0.01     H2=0.01
Y.MESH            DEPTH=.25   SPACING=0.05
Y.MESH            DEPTH=.5    SPACING=0.25

COMMENT           Regions

REGION            NAME=Gate_Ox      Y.MAX=0     HFO2
REGION            NAME=NW     Y.MIN=0.0   Y.MAX=0.034 SILICON
REGION            NAME=Box    Y.MIN=0.034 Y.MAX=.284  OXIDE
REGION            NAME=Bulk   Y.MIN=0.284 SILICON

COMMENT           Electrodes
ELECTR            NAME=Gate   X.MIN=.3    X.MAX=.7
+           TOP
ELECTR            NAME=Source X.MAX=0.4   Y.MIN=-0.001
+           Y.MAX=0.0
ELECTR            NAME=Drain  X.MIN=.6    Y.MIN=-0.001
+           Y.MAX=0.0
ELECTR            NAME=Substrate    BOTTOM

COMMENT           Specify impurity profiles and fixed charges

PROFILE           P-TYPE            N.PEAK=1e15       UNIFORM
+           OUT.FILE=pfetdop1
COMMENT           PROFILE           P-TYPE            N.PEAK=1e18
      Y.MIN=0
COMMENT           DEPTH=0.01
COMMENT           +           Y.JUNCTI=0.034

COMMENT           Plot initial Grid

PLOT.2D           GRID  FILL  SCALE TITLE="Simulation Mesh"

COMMENT           Regrid on doping

REGRID            DOPING      LOG   IGNORE=Box  RATIO=2     SMOOTH=1
+           IN.FILE=pfetdop1
PLOT.2D           GRID  TITLE="DOPING"    FILL  SCALE
```

```
COMMENT           Pt's workfunction is 5.6

CONTACT           NAME=(Gate,Source,Drain) WORKFUNC=4.33

COMMENT           MATERIAL    REGION=Gate_Ox PERMITTI=9

MODELS            CONMOB      SRFMOB2     FLDMOB

COMMENT           Zero carriers
SYMB        CARRIERS=0

METHOD            ICCG  DAMPED
SOLVE

REGRID            POTEN RATIO=0.1   SMOOTH=1    IGNORE=Box
+           COS.ANG=0.95
+           IN.FILE=pfetdop1
+           OUT.FILE=pfetpot1
PLOT.2D           GRID  TITLE="POTENTIAL" FILL  SCALE

PLOT.1D           DOPING      X.START=1.5 X.END=1.5   Y.START=0
+           Y.END=1     Y.LOG TOP=1E20    BOT=1E14    POINTS
+           COLOR=2
PLOT.2D           BOUND FILL

MODELS            CONSRH      ARORA SRFMOB2
SYMB        GUMM  CARRIER=0
METHOD            ICCG  DAMPED

SYMB        NEWTON      CARRIER=2
SOLVE       OUT.FILE=pfetsolve
```

N-FET structure MEDICI code:

```
TITLE       N-type Si NW FET on SiO2

COMMENT           Specify a rectangular mesh

MESH        SMOOTH=1

COMMENT           Specify mesh dimensions

X.MESH            WIDTH=1.5   H1=0.1
Y.MESH            N=1         L=-0.01
Y.MESH            N=2         L=0.0
Y.MESH            DEPTH=.034  H1=0.01     H2=0.01
Y.MESH            DEPTH=.25   SPACING=0.05
Y.MESH            DEPTH=.5    SPACING=0.25

COMMENT           Regions

REGION            NAME=Gate_Ox      Y.MIN=-0.01 Y.MAX=0     OXIDE
REGION            NAME=NW     Y.MIN=0.0   Y.MAX=0.034 SILICON
REGION            NAME=Box    Y.MIN=0.034 Y.MAX=.284  OXIDE
REGION            NAME=Bulk   Y.MIN=0.284 SILICON

COMMENT           Electrodes
ELECTR            NAME=Gate   X.MIN=0.5   X.MAX=1
+           TOP
ELECTR            NAME=Source X.MAX=0.5   Y.MIN=-0.005
+           Y.MAX=0.0
ELECTR            NAME=Drain  X.MIN=1     Y.MIN=-0.005
+           Y.MAX=0.0
ELECTR            NAME=Substrate    BOTTOM

COMMENT           Specify impurity profiles and fixed charges

PROFILE           N-TYPE            N.PEAK=1E14       UNIFORM
+           OUT.FILE=nfetdop1
PROFILE           N-TYPE            N.PEAK=1E16 Y.MIN=0     DEPTH=0.005
+           Y.JUNCTI=0.034
PROFILE           N-TYPE            N.PEAK=1E19 Y.JUNC=0.034
+           X.MIN=0           WIDTH=0.5
PROFILE           N-TYPE            N.PEAK=1E19 Y.JUNC=0.034
+           X.MIN=1           WIDTH=0.5

COMMENT           Plot initial Grid

PLOT.2D           GRID  FILL  SCALE TITLE="Simulation Mesh"

COMMENT           Regrid on doping

REGRID            DOPING      LOG   IGNORE=Box  RATIO=2     SMOOTH=1
+           IN.FILE=nfetdop1
PLOT.2D           GRID  TITLE="DOPING"    FILL  SCALE

COMMENT           Ti's workfunction is 4.33; Al = 4.1
```

```
CONTACT           NAME=Gate WORKFUNC=4.33

COMMENT           MATERIAL    REGION=Gate_Ox PERMITTI=3.5

MODELS            SRFMOB2     ARORA CONSRH

COMMENT           Zero carriers
SYMB        CARRIERS=0

METHOD            ICCG  DAMPED
SOLVE

REGRID            POTEN RATIO=0.1   SMOOTH=1    IGNORE=Box
+           COS.ANG=0.95
+           IN.FILE=nfetdop1
+           OUT.FILE=nfetpot1
PLOT.2D           GRID  TITLE="POTENTIAL" SCALE

PLOT.1D           DOPING      X.START=0.75      X.END=0.75  Y.START=0
+           Y.END=1     Y.LOG TOP=1E20    BOT=1E14    POINTS
+           COLOR=2
PLOT.2D           BOUND FILL

PLOT.1D           DOPING X.START=0.25     X.END=0.25  Y.START=0
+           Y.END=1     Y.LOG TOP=1E20    BOT=1E14    POINTS
+           COLOR=2
PLOT.2D           BOUND FILL

PLOT.1D           X.START=0.75      X.END=0.75  Y.START=-0.005
      Y.END=0.03
+           COND  NEG   TITLE="Band Structure"  TOP=4.5     BOTT=-4.5
PLOT.1D           X.ST=0.75   X.END=0.75  Y.ST=-0.005       Y.END=0.03
+           VAL   UNCH  NEG
PLOT.1D           X.START=0.75      X.END=0.75  Y.ST=-0.005
      Y.END=0.03
+           QFN   UNCH  NEG   COL=2

PLOT.2D           BOUND TITLE="Impurity Contours"     FILL  SCALE
CONTOUR           DOPING      LOG   MIN=14      MAX=19      DEL=0.5
      COLOR=1

MODELS            CONSRH      ARORA SRFMOB2
SYMB        GUMM  CARRIER=0
METHOD            ICCG  DAMPED
SOLVE

SYMB        NEWTON      CARRIER=1   ELECTRON
SOLVE

SYMB        NEWTON      CARRIER=2
SOLVE       OUT.FILE=nfetsolve

SAVE        MESH  OUT.FILE=nfetAmesh      W.MODELS
```

MEDICI code for generating potential contours

```
TITLE pFET gate characteristics

COMMENT     Read in simulation mesh
MESH  IN.FILE=nfetpot1
LOAD  IN.FILE=nfetsolve

COMMENT     initial solution
COMMENT     MODELS      CONSRH      ARORA SRFMOB2
COMMENT     SYMB  GUMM  CARR=0
COMMENT     SOLVE

SYMB  NEWTON      CARRIERS=2

COMMENT Setup LOG file for solution

LOG   OUT.FILE=nfet_test1

COMMENT     Solve for Vds=0.1
SOLVE V(Drain)=0.1
SOLVE V(Gate)=0

COMMENT     Look at potential contours
PLOT.2D     BOUND JUNC  DEPL  FILL  SCALE
+     TITLE="Potential Contours"    Y.MAX=0.4
FILL  REGION=NW   COLOR=5
CONTOUR     POTENTIA

COMMENT     look at carrier profile

PLOT.1D     HOLE  X.START=.8  X.END=.8    Y.START=0
+     Y.END=.03   POINTS
+     TITLE="Hole concentration under gate"

PLOT.1D     ELECTRON    X.START=.8  X.END=.8    Y.START=0
+     Y.END=.03   POINTS
+     TITLE="Electron concentration under gate"

PLOT.2D     FILL  BOUND Y.MAX=0.2
+     TITLE="Current flow"
FILL  REGION=NW   COLOR=5     ^NP.COL
CONTOUR     FLOW
```

MEDICI code for generating $I_{DS} - V_{GS}$ curves

```
TITLE nFET gate characteristics

COMMENT     Read in simulation mesh
MESH  IN.FILE=nfetAmesh

LOAD  IN.FILE=nfetsolve

SYMB  NEWTON      CARRIERS=2

COMMENT Setup LOG file for solution

LOG   OUT.FILE=nfet_gate2

COMMENT     Solve for Vds=-0.1 and ramp gate
SOLVE V(Drain)=0.1
SOLVE V(Gate)=-1  ELEC=Gate   VSTEP=0.05  NSTEPS=50

COMMENT     Plot Ids vs. Vgs
PLOT.1D     Y.AXIS=I(Drain)   X.AXIS=V(gate)    POINTS      LOG
      COLOR=2
+     TITLE="Ids vs. Vgs"
LABEL LABEL="Vds is +100 mV"

PLOT.1D           X.START=0.75      X.END=0.75  Y.START=-0.005
      Y.END=0.03
+           COND  NEG   TITLE="Band Structure" TOP=4.5 BOTT=-4.5
PLOT.1D           X.ST=0.75   X.END=0.75  Y.ST=-.005        Y.END=0.03
+           VAL   UNCH  NEG
PLOT.1D           X.START=0.75      X.END=0.75  Y.ST=-.005
      Y.END=0.03
+           QFN   UNCH  NEG   COL=2

EXTRACT     MOS.PARA    IN.FILE=nfet_gate2
```

Chapter 5

Microcontact printing methods for molecular electronics applications

5.1 Introduction

Microcontact printing (μCP) is a highly versatile technique for patterning surfaces using monolayers with submicron resolution.[1] Like other soft lithography techniques, μCP is based on replicating a pattern from a flexible, elastomeric stamp to a surface. In this method, the pattern is transferred by coating the stamp with a molecule capable of forming a covalent bond with the surface and forming an intimate contact between the two materials (Figure

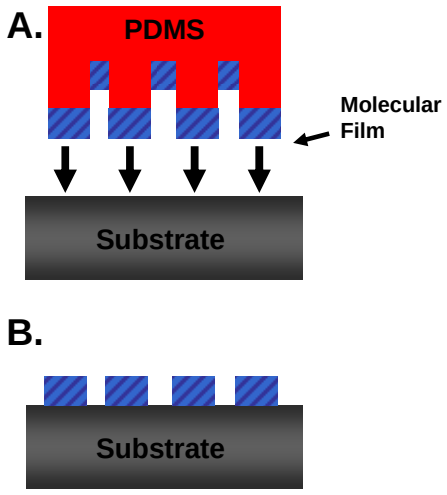

Figure 5.1. Schematic of microcontact printing. **A.** A PDMS stamp coated with an ink solution is brought into contact with a substrate. **B.** The ink covalently attaches to the substrate and the stamp is removed.

5.1A). Due to high local concentration of the molecules, a monolayer rapidly forms on the surface, replicating the pattern on the stamp (Figure 5.1B).

There are several applications for μCP. As an alternative to conventional lithography, μCP has been used to pattern self-assembled monolayers (SAMs) as ultrathin wet etch resists[2, 3] and as templates for the growth or deposition of materials[4]. The flexible nature of the elastomeric stamp also facilitates the patterning on non-planar surfaces, leading to applications in a variety of fields including optics and MEMS.[1]

The key to μCP's success is in its highly simple, high throughput and inexpensive nature. μCP is a bottom-up fabrication technique. Since surface structures are added, not removed, very little waste is generated. Conventional lithography, in contrast, consists of applying a resist and then removing patterns from it. Both the resist and the resist developer are toxic chemicals and generate hazardous waste. Another benefit to μCP is that very large areas can be patterned easily by using a large planar stamp or a rolling stamp (analogous to a paint roller).[1] Standard lithography techniques become progressively more expensive as the exposure area increases. Lastly, the materials involved with μCP: the elastomer stamp (typically polydimethylsiloxane), the ink molecule, and the ink solvent (usually a standard solvent in organic synthesis like acetonitrile) are all inexpensive and quick to assemble. In contrast, the instruments, facilities, and masks used in conventional lithography are very expensive and require specialized training. Thus, μCP is a promising technique for micro- and nanofabrication.

Recently, μCP has been used to facilitate covalent attachments of new molecules to existing SAMs using chemistries such as Cu-catalyzed azide-alkyne cycloaddition, [5, 6] imine bond formation,[7–9] and amide bond formation.[10–12] In this technique, molecules are

stamped on an existing monolayer. The highly confined interface between the stamp and the substrate promotes a reaction between the ink and monolayer, often times with reaction rates much faster than the analogous solution-based reaction and without an added catalyst.[11] This methdology has been used to pattern oligonucleotides for microassays and biosensors,[6, 9] immobilize cells to study cell-cell and cell-surface interactions,[8] generate peptide arrays for proteins studies,[11] and biological ligands for immunoassays and biosensors.[12]

5.1.1 Application for high-density molecular circuits

Covalent surface attachment using μCP has great potential for applications outside of biology as well. In particular, it may be a useful tool in the fabrication of high-density molecular circuits. In 2007, Green et al. described a molecular electronic circuit using a silicon nanowire (Si NW) crossbar array and a monolayer of amphiphilic, bistable [2]rotaxanes as the active memory element.[13] The development of Si NW devices[14] and circuits[15] was described in Chapters 2–4.

The [2]rotaxanes, assembled in molecular switch tunnel junctions (MSTJs), have been shown to switch between a low conductance state and a high conductance state by the mechanical shuttle of

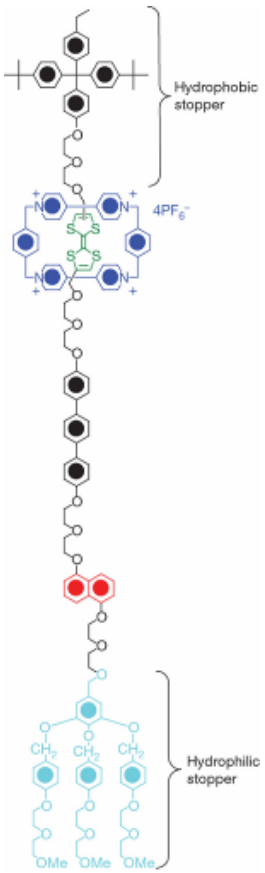

Figure 5.2. Molecular structure of a amphiphilic, bistable [2]rotaxane

the tetracationic cyclophane ring (shown in blue in Figure 5.2) from the tetrathiafulvalene site (shown in green) to the dioxynapthalene site (shown in red).[16, 17] This mechanical shuttle occurs when the tetrathiafulvalene (TTF) group is oxidized by applying a large bias across the solid-state device electrodes. The current levels are then "read" by applying a small, non-perturbing bias.

Although the [2]rotaxane memory devices have been successfully demonstrated, the integration of the monolayer into the device has to be done carefully.[18] The [2]rotaxanes are compressed and aligned via the Langmuir-Blodgett technique and transferred to the bottom electrodes of the memory circuit. The top electrodes are then carefully deposited on top of the monolayer. If the monolayer is compressed at the wrong pressure, the MSTJ fails. Also, the use of the Langmuir-Blodgett technique places design constraints on the molecule and the substrate and the molecules are not covalently attached to the electrodes.

μCP would be a convenient alternative to the Langmuir-Blodgett method for patterning molecular electronic devices directly onto electrode surfaces. This technique has the benefit that the attachment would be covalent, which may lead to better device performance and longer performance times. For instance, this technique may allow the sequential, solvent-free synthesis of [2]rotaxanes directly on devices. Figure 5.3 shows a proposed synthetic sequence. The [2]rotaxane backbone containing the TTF and dioxynapthalene (DNP) sites would be covalently attached to the surface using μCP. The tetracationic cyclophane ring ($CBPQT^{4+}$) would be stamped next, and the electrostatic interactions between the ring and the rotaxane backbone would promote a threading

process. The stopper (which prevents the ring from slipping off the backbone) would then be stamped and covalently attached.

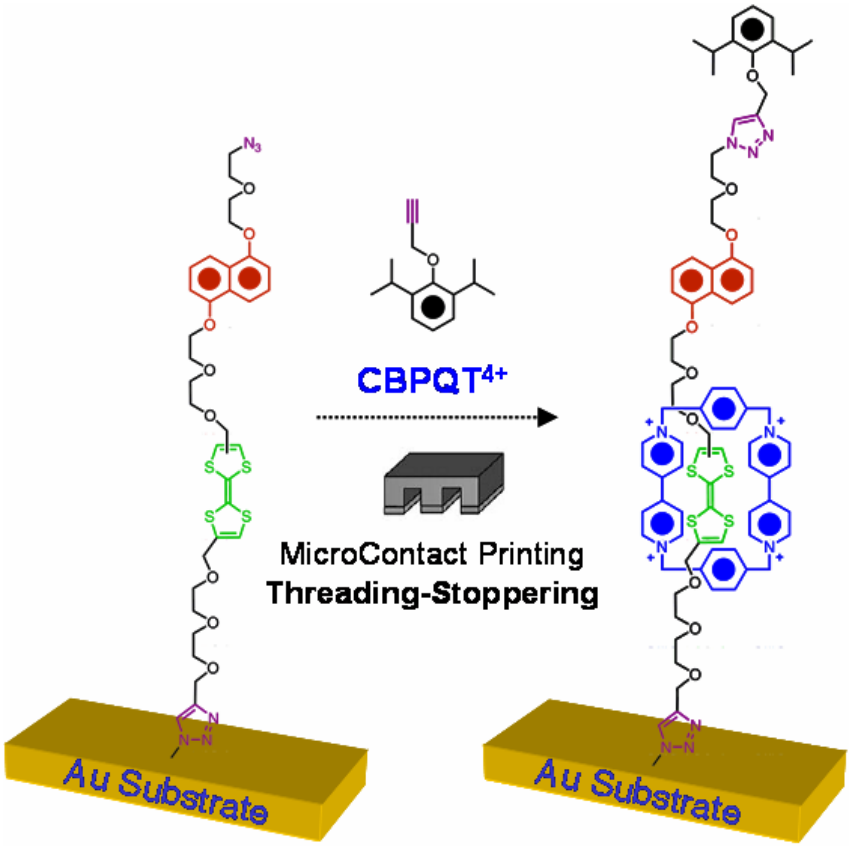

Figure 5.3. Schematic of proposed [2]rotaxane synthesis. The rotaxane backbone would first be covalently attached by μCP. The tetracationic cyclophane ring ($CBPQT^{4+}$) and the stopper would be also sequentially stamped, forming the complete [2]rotaxane on the electrode surface.

This proposed synthesis would allow for the rapid fabrication of both the molecule and device simultaneously. This process would be extremely fast, be high yielding, and generate little waste. Unlike the Langmuir-Blodgett technique, the monolayer would be covalently attached to the surface and also could be patterned into the desired device geometry. Advances in the nanoimprint lithography of nanowires[19] would provide a complement to this technology and be an attractive method for the high-throughput generation of novel nanoscale and molecule-based electronic circuits.

5.1.2 Organization of the chapter

This chapter describes the work done on developing μCP methods for the Cu^{I}-catalyzed azide-alkyne cycloaddition (CuAAC) reaction on Au and Si substrates. Because alkanethiol monolayers on Au are the best characterized SAM system,[20] the majority of the results were obtained using these substrates. μCP was shown to work using both homogeneous and heterogeneous Cu catalysts. The use of the heterogeneous catalyst for μCP was a novel result and its kinetics and mechanism were explored in detail.

In the next two sections, the stamping process and the surface characterization experimental methods are described. Then, the results of the surface characterization are discussed, followed by discussions of the kinetics of the stamping process using the homogeneous and heterogeneous stamps and the mechanism for μCP using the heterogeneous catalyst. Lastly, the generation of azide-terminated silicon surfaces is described, along with preliminary stamping results.

5.2 Generation of azide-terminated monolayers on Au

Mixed monolayers consisting of 50% azide termination and 50% methyl termination were prepared by immersing Au substrates into a 1 mM solution of 50% octanethiol and 50% 1-azido-11-undecanethiol in ethanol. Au surfaces were prepared by depositing 15/150 nm Ti/Au on clean, 4-inch Si(100) wafers. The wafers were cleaved into 1.5 × 1.5 cm^2 pieces and cleaned via a one minute soak in hot acid piranha (3:1 H_2SO_4: 30% H_2O_2), followed by a 15 second immersion in H_2O and a 15 second immersion in concentrated HCl at room temperature. The pieces were then rinsed with DI H_2O and EtOH, and were immediately placed in the thiol solution for 16–36 hours. The reaction was protected from light to prevent photo-oxidation of the thiols.[21] The Au substrates were then removed from the thiol solution, rinsed with EtOH, and dried with N_2. The azide-terminated Au samples can be stored, protected from light, for a few weeks.

5.3 CuAAC reaction conditions in solution and in stamping

The Cu^I-catalyzed azide-alkyne cycloaddition (CuAAC) was used to covalently attach ferrocene and other molecules to the Au surfaces. The CuAAC reaction on the Au surface in solution and using the stamps were compared. Here, the experimental conditions for each reaction are presented.

5.3.1 Solution CuAAC conditions

For the solution-based reaction, the 50% azide-terminated Au substrates were immersed in a 1–10 mM solution of 1:0.1:0.2 molar equivalents of ferrocene alkyne, $CuSO_4 \cdot 5H_2O$, and L-ascorbic acid in DMF. The reaction was protected from light and placed on a rocking platform to gently stir the reagents. Once the reaction was stopped, the Au samples were placed in fresh DMF and sonicated for 10 minutes, then rinsed with methanol and dried with N_2.

5.3.2 Microcontact printing CuAAC conditions using the homogeneous catalyst

For the CuAAC reaction using microcontact printing and an ink-based catalyst, referred to as *HomoCat*, polydimethylsiloxane (PDMS) elastomer stamps were first fabricated. PDMS was molded over either a flat or patterned 4-inch Si wafer. To prepare the Si wafer, it was first cleaned using hot acid piranha for ~ 15 minutes, rinsed in DI H_2O and dried with N_2. The wafer surface was rendered hydrophobic by exposing it to trimethylchlorosilane (TMCS) vapor for ~ 15 minutes. Afterwards, the surface was rinsed with H_2O and dried. The wafer was placed in a foil-covered shallow crystallizing dish and the edges were taped down to prevent PDMS from leaking under the wafer.

A 10:1 wt:wt mixture of PDMS-Sylgard Silicone Elastomer 184 and Sylgard Curing Agent 184 (Dow Corning Corp., Midland, MI) was mixed by hand and added to the crystallizing dish. The dish with the PDMS was degassed under reduced pressure for ~ 1 hour to remove trapped air bubbles in the PDMS and then heated to 60°C for a minimum of 1 hour to cure the PDMS. The cured PDMS was then carefully peeled from the Si wafer and diced into 1.5 × 1.5 cm^2 pieces.

The stamp ink consisted of three solutions mixed immediately prior to stamping: a 5 mM solution of the alkyne molecule in acetonitrile (ACN), and 1 mM solutions of $CuSO_4 \cdot 5H_2O$ and ascorbic acid in ethanol (EtOH). Prior to applying the ink, the PDMS pieces were oxidized using O_2 plasma (50 W, 10 seconds) to increase the ink wettability on the surface. The oxidized stamps were immediately placed in H_2O until needed. The stamps were soaked in ACN for ~ 30 seconds and then placed flat-side-up and dried with N_2. Several drops of the alkyne solution were added to the stamp until the surface was covered. Approximately 2 drops each of the ascorbic acid and the $CuSO_4 \cdot 5H_2O$ solutions were added and the stamp was gently rocked to mix the solutions. The ink solvent was allowed to evaporate (this process takes ~ 15 minutes in a chemical hood with the sash down). Once the solvent was gone, the stamp was gently placed into contact with the azide-terminated Au surface. A ~ 40 g weight was added to the stamp to ensure complete contact with the Au surface. Once the stamping was complete, the stamp was removed and the Au substrate was rinsed with EtOH and dried with N_2.

5.3.3 Microcontact printing CuAAC conditions using the heterogeneous catalyst

In this technique, referred to as *StampCat*, the ascorbic acid solution is eliminated and the $CuSO_4 \cdot 5H_2O$ in the ink solution is replaced by coating the PDMS stamp with a thin layer of Cu. After the PDMS stamp was made but before it was diced into smaller pieces, 10/50 nm of Ti/Cu was deposited onto the flat or patterned surface by electron beam evaporation. The Cu-coated PDMS stamp was then diced into pieces and used without performing the plasma oxidation step. Several drops of the 5 mM solution of the alkyne molecule were added to the Cu-coated surface and allowed to evaporate. The rest

of the stamping process was identical to that described above. In addition to Cu, Pt-coated PDMS stamps were also fabricated and used as a control.

5.4 Surface characterization experimental procedures

All functionalized surfaces were characterized using X-ray photoelectron spectroscopy (XPS), contact angle goniometry, infrared (IR) spectroscopy, frictional force microscopy (FFM), and electrochemical measurements. In this section, the experimental procedure for each characterization method is described.

5.4.1 XPS measurements

XP spectra were collected by a co-worker in a ultrahigh-vacuum chamber using an M-probe spectrometer (VG Instruments) as described previously.[22, 23] Measurements were taken from the center of each sample at room temperature. Monochromatic X-rays of energy 1486.6 eV from the Al Kα line were incident at 35° from the sample surface. Emitted photoelectrons were collected by a hemispherical analyzer located 35° from the sample surface. Data was collected using ESCA-2000 software.

Survey scans were collected in scanned mode from 0 to 1000 eV binding energy. High resolution spectra were collected in unscanned mode in the C 1s (282–289 BeV), F 1s (680–696 BeV), Br 3d (68–74 BeV), N 1s (396–410 BeV), Si 2p (97–106 BeV), Cl 2s (265–275 BeV), Cl 2p (195–205 BeV), and Fe 2p (700–730 BeV) regions.

5.4.2 Contact angle measurements

The sessile contact angle of water was measured using an NRL C.A. Goniometer Model #100-00 (Rame-Hart, Inc.) at room temperature. Each drop had a volume of ~ 1 μL and was applied to the surface using a syringe needle. Before every measurement, the sample platform was adjusted until there was no tilt in any direction. Typically, three drops per sample were measured and both the left and right contact angles were recorded and averaged. After the contact angles were measured, samples were rinsed with methanol and dried with N_2.

5.4.3 Infrared spectroscopy measurements

External reflectance infrared spectra were collected using a Vertex 70 FT-IR spectrometer (Bruker Optics, Inc.) equipped with a liquid-N_2-cooled MCT detector and an AutoSeagull accessory (Harrick Scientific Products, Inc.). Samples were probed at a grazing angle of 85° with p-polarized light. Once the samples were loaded, the sample chamber was purged with dry air for approximately 30 minutes. Spectra were collected from 400 to 5000 cm^{-1} using 128 scans with a resolution of 4 cm^{-1}. A background spectrum was obtained from a freshly cleaned Au substrate and was subtracted from the spectra of functionalized surfaces. Spectra was baseline corrected using the concave rubberband method (25 iterations, excludes CO_2 bands, 256 baseline points).

5.4.4 Frictional force microscopy measurements

FFM measurements were made using a Multimode Nanoscope IIIA (Veeco Instruments, Santa Barbara, CA) atomic force microscope in contact mode. The scan

angle was set to 90° to maximize the friction signal. Topography was measured in trace mode and friction in retrace mode. General purpose, oxide-sharpened silicon nitride probe tips were used (NP-S). The best friction images were obtained using scan rates of approximately 1–2 Hz.

5.4.5 Electrochemical measurements

Cyclic voltammetry (CV) measurements were performed using a VMP Multi-Potentiostat (Princeton Applied Research, Oak Ridge, TN). Before each set of measurements, Ar gas was bubbled in the electrolyte, 1 M perchloric acid, for ~ 30 minutes. The sample was loaded into a custom-made, Teflon cell that held approximately 1 mL of electrolyte. The area of the sample surface exposed in the electrochemical cell was 78.6 mm^2. The counter electrode, a Pt wire, was cleaned by exposing it to a flame for ~ 10 seconds. Both the counter electrode and a Ag/AgCl reference electrode were immersed in the electrolyte. Electrical contact was made to the Au substrate (the working electrode) outside of the electrochemical cell. Cyclic voltammagrams were obtained for scan rates of 50–700 mV/s. Before a new sample was loaded, the Teflon cell was sonicated in H_2O for ~ 30 seconds, rinsed with DI H_2, and dried with N_2. The counter and reference electrodes were also rinsed with DI H_2O between samples. After the CV measurements were made, the samples were rinsed with MeOH and dried with N_2.

It was observed that noisy CV data could almost always be eliminated by re-loading the sample into the electrochemical cell and adding fresh electrolyte. The largest source of noise seemed to be from improperly loaded samples.

5.5 µCP results using homogeneous and heterogeneous catalysts

The µCP method was used to covalently attach **3** to the azide-terminated monolayers (50% **1** and 50% **2**) on Au (Figure 5.2). For the homogenous catalyst (*HomoCat*), the Cu^{I} catalyst was generated in the ink solution by the reaction of $CuSO_4 \cdot 5H_2O$ and ascorbic acid. Heterogeneous catalysis (*StampCat*) was achieved by coating the PDMS stamp with a 50 nm Cu layer. Both methods did facilitate the formation of the 1,2,3-triazole ring. The reaction was confirmed using contact angle goniometry, IR spectroscopy, XPS, FFM, and electrochemistry.

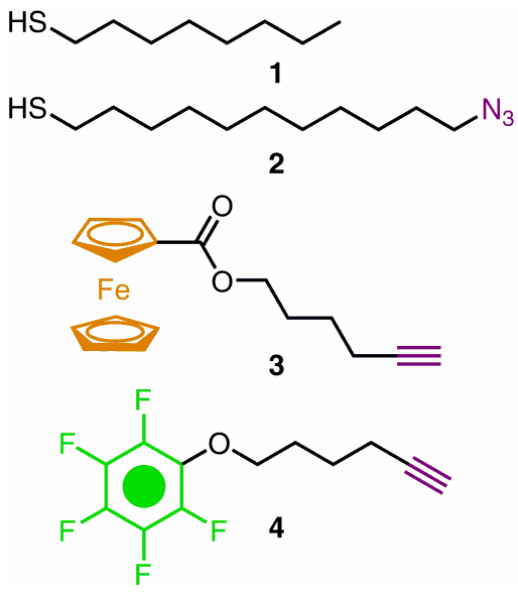

Figure 5.4. Molecular structures from the azido-terminated monolayers (50% **1** and 50% **2**) and the stamp inks: ferrocene alkyne (**3**) and pentafluorophenylether alkyne (**4**)

5.5.1 Contact angles

The contact angle measurements were taken on azide-terminated surfaces for both the *HomoCat* and *StampCat* techniques. The mixed monolayer of **1** and **2** yielded a contact angle of 77°, which is in agreement with previous reports.[24] The covalent attachment of **3**—whether via solution-based, *StampCat*, or *HomoCat* methods—caused an expected reduction in contact angle to approximately 70°. To show generality of the reaction, the *StampCat* technique was also performed using **4** as the ink. The fluorine

groups caused the contact angle to increase as expected. The summary of the contact angles are presented in Table 5.1.

Table 5.1. Contact angle measurements for various modified Au surfaces

Surface	Method	Molecule	H_2O Contact Angle (°)
Au	–	–	56.5 +/- 1.5
50% N_3 on Au	–	–	76.5 +/- 1.7
50% N_3 on Au	*Solution-Based*	**3**	72.6 +/- 3.0
50% N_3 on Au	*HomoCat*	**3**	68.5 +/- 5.3
50% N_3 on Au	*StampCat*	**3**	73.5 +/- 3.4
50% N_3 on Au	*StampCat*	**4**	80.3 +/- 3.6

5.5.2 Grazing angle infrared spectroscopy

IR spectroscopy also confirmed the CuAAC reaction. Figure 5.5A shows the stacked grazing angle IR spectra for the azide-terminated surface and for **3** attached via *HomoCat*, *StampCat*, and solution-based reactions. Note that the CO_2 bands were removed from the spectra.

Figure 5.5B shows the region between 3000–2000 cm^{-1}. The peaks between 2800 and 2900 cm^{-1} are indicative of methylene stretches. Major peaks that appear in each spectra are located at 2867 cm^{-1} and 2932 cm^{-1}, which correspond to the methylene symmetric and asymmetric stretches, respectively.[25] The azide asymmetric stretch appears prominently in the azide-terminated monolayer spectra at 2104 cm^{-1}, reduces significantly in the *HomoCat* and *StampCat* spectra, and disappears completely in the solution-based reaction spectra.

Figure 5.5C shows the IR spectra in the carbonyl region between 1600 and 1800 cm^{-1}. The azide-terminated surface is relatively flat in this region but the ferrocene-terminated surfaces show a large peak at around 1713 cm^{-1}. This peak was absent in the

StampCat reaction with **4**, which suggests this peak may be due to the carbonyl stretch associated with the ester in **3**.

Lastly, figure 5.5D shows the spectra of the *StampCat* reaction with **4** and the azide-terminated surface. The spectrum of 4 has a large peak at 1625 cm^{-1} that was not present in the surfaces containing **3**. This is attributed to the C-F stretches on the phenyl group.[26]

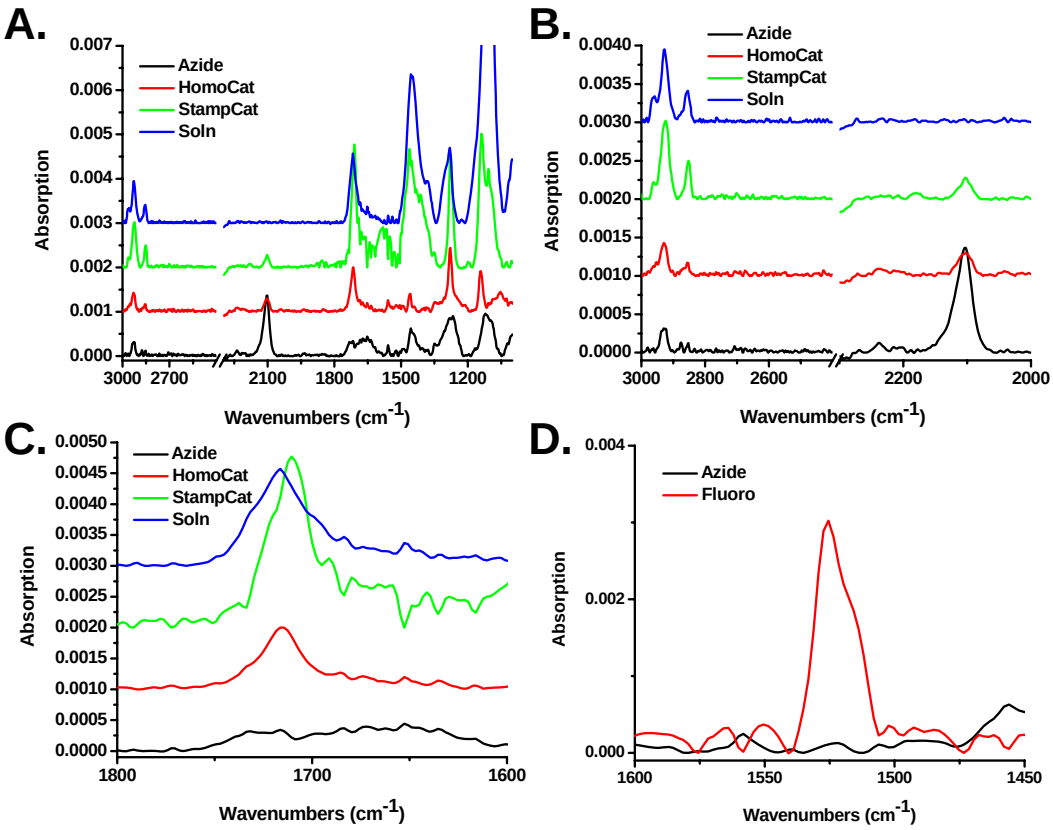

Figure 5.5. Grazing angle IR spectra of azide-terminated and stamped surfaces. **A.** Stacked survey spectra of azide-terminated surface (black) and *HomoCat* (red), *StampCat* (green), and solution-based (blue) reaction with **3**. **B.** Close-up of methylene and azide bands. **C.** Close-up of carbonyl bands. **D.** Close-up spectrum of **4** attached to surface via the *CatStamp* method, showing C-F stretches.

5.5.3 X-ray photoelectron spectroscopy

XPS elucidates the elemental composition on surfaces and is a powerful surface characterization technique. The XPS spectra for surfaces bound with azide, **3,** and **4** are presented in Figure 5.6.

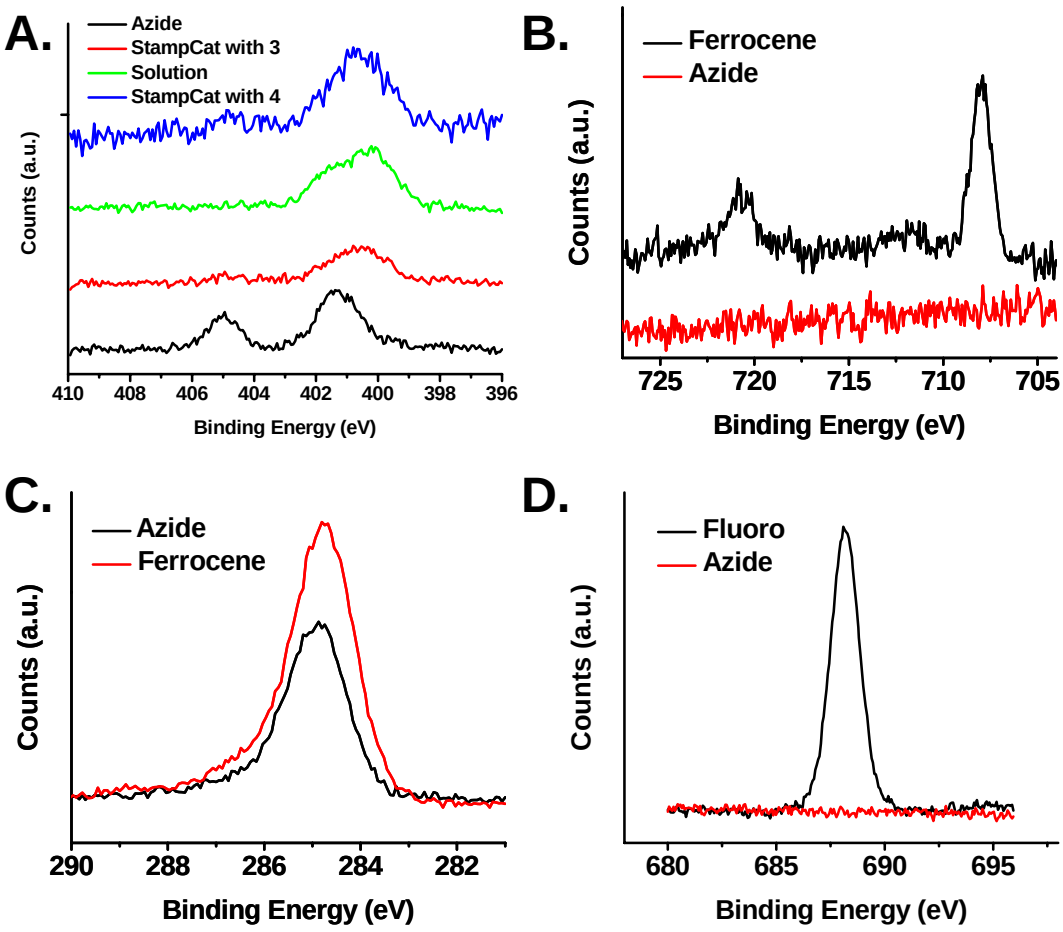

Figure 5.6. XPS data of azide-, **3**-, and **4**-terminated surfaces. **A.** Spectra of azide-, **3**-, and **4**-termated surfaces in N 1s region. **B.** Spectra of same surfaces in Fe 2p region. **C.** Spectra of same surfaces in C 1s region. **D.** Spectra of azide- and **4**-terminated species in F 1s region

Figure 5.6A shows the high-resolution XPS spectra of the azide-, **3**-, and **4**-terminated surfaces in the nitrogen 1s region. The azide spectrum shows the

characteristic two peaks at 400 and 405 eV. The higher peak is indicative of the electron-deficient nitrogen in the azide group. After the solution-based (green curve) and *StampCat* reactions with **3** (red curve) and the *StampCat* reaction with **4** (blue curve), the higher energy peak disappears and the peak at 400 eV broadens. This is suggestive of the chemically distinct nitrogen atoms in the 1,2,3-triazole.

Correlated with the disappearance of the azide group, an iron signal appears in the Fe 2p region (Figure 5.6B). The peak at 720 eV is from the $2p_{1/2}$ electrons and the peak at 708 eV is $2p_{3/2}$ electrons. The corresponding azide-terminated surface shows only the noise level in this region. Additionally, the carbon 1s peak shows an increase in peak area after the attachment of **3** to the surface (Figure 5.6C). Lastly, the attachment of **4** corresponded to the appearance of a large peak in the fluorine 1s region (Figure 5.6D). The peak, centered at 688 eV is indicative of the C-F bond.

5.5.4 Frictional force microscopy

Frictional force microscopy (FFM) is the best tool for characterizing surfaces that are patterned since it yields information about the surface with atomic resolution.[27] Like EFM, which is described in Chapter 3, FFM (also known as lateral force microscopy) is a variant of AFM. In this technique, the AFM is operated in contact mode but the cantilever scans the surface perpendicular to the cantilever's major axis. This makes the cantilever very sensitive to tip-surface interactions. A high-friction or low-friction surface will torque the cantilever to different extents, generating a friction map. Figure 5.7A shows a schematic of an AFM cantilever scanning over a low-friction area (1) and a high-friction area (2).

Silicon wafers patterned with 12 × 9 μm dots or 4.25 μm stripes using EBL was used to mold PDMS stamps to study pattern transfer using *StampCat*. Cu was deposited onto the patterned stamps and the stamping was performed in the same manner as for the flat PDMS stamps.

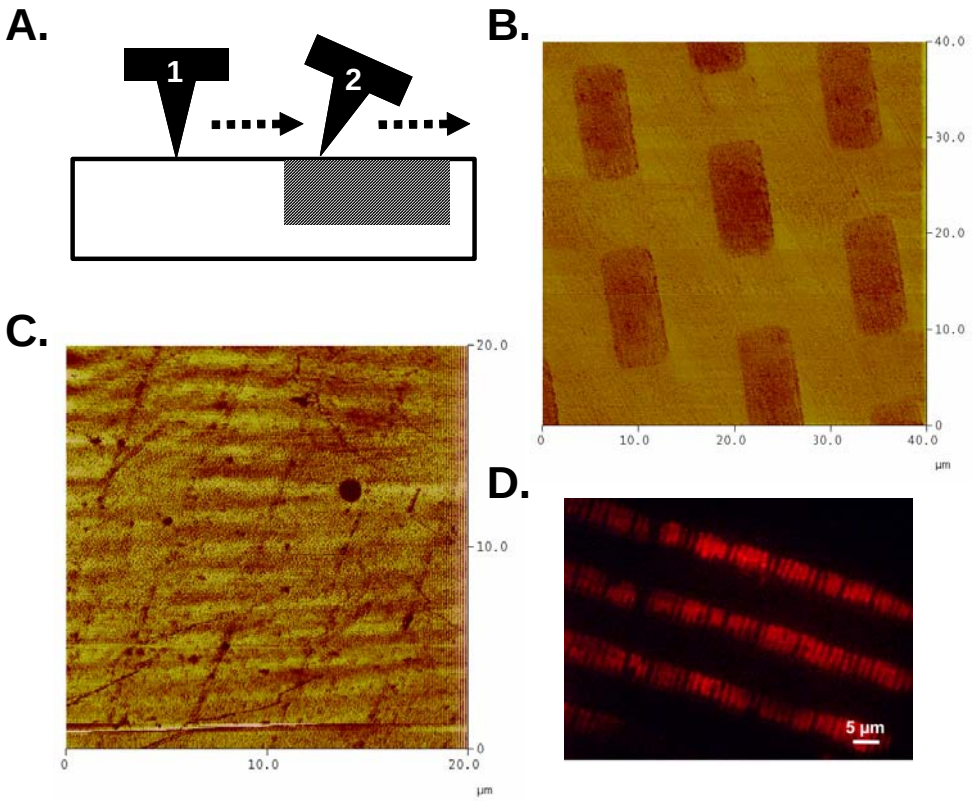

Figure 5.7. FFM and fluorescence characterization of patterned surfaces. **A.** Side-view schematic of AFM tip interaction with a surface containing a low friction area (**1**) and a high friction area (**2**). **B.** and **C.** FFM image of **3** patterned on surface by the *CatStamp* technique. **D.** Fluorescence image of rhodamine patterned on glass, showing that small defects were transferred from the stamp

Figure 5.7B shows the frictional image of the patterned Au monolayer using the stamp patterned with dots. After one hour of stamp time, the dots pattern did not diffuse or distort. This suggests that the nature of the catalyst is truly heterogeneous and that the reaction only occurs where the stamp is in intimate contact with the surface.

Figure 5.7C also provided evidence of this conclusion. The friction image recorded a series of thin lines for the pattern that contained large bars. At first this was attributed to a faulty FFM signal. However, the stamp itself was imaged and the bars were shown to be distorted so that the edges curled up. The pattern transfer in Figure 5.7C was a result of just the edges of the stamp making contact with the surface. Again, no pattern diffusion was evident. This was also observed when patterning rhodamine on glass substrates (experiment was performed by Dorota Rozkiewicz). Small breaks on the patterned bars (Figure 5.7D) were observed both from the fluorescence image of the surface and on the stamp itself.

5.5.5 Electrochemistry

Figure 5.8A and 5.8C shows the cyclic voltammogram of **3** patterned by the *HomoCat* and *StampCat* techniques for various scan rates, υ. The oxidation and reduction of ferrocene is a one-electron process, as evidenced by the single oxidation and reduction peaks centered at ~ 0.5 V. The magnitudes of the oxidation and reduction peak currents are equal, indicating the reaction is Nernstian (reversible). A plot of the peak oxidation current as a function of υ reveals a linear relationship for both *HomoCat* and *StampCat* (Figure 5.8B and 5.8C inset). The correlation coefficients, *R*, for the *HomoCat* and *StampCat* curves were 0.99995 and 0.99998, respectively. This relationship indicates that **3** was fully adsorbed on the surface. For species that can diffuse through the cell, the peak current will have a $\upsilon^{1/2}$ dependence.[28]

Two controls were also measured. The first control was an azide-terminated Au substrate stamped with a bare PDMS stamp and the second control used a Pt-coated

PDMS stamp (prepared in an analogous method to the Cu-coated PDMS stamp). Both controls used an ink solution of **3** with no added Cu catalyst. The electrochemistry indicated that no reaction occurred (Figure 5.8D) for either control stamp, providing evidence that the Cu metal is indeed catalyzing the CuAAC reaction.

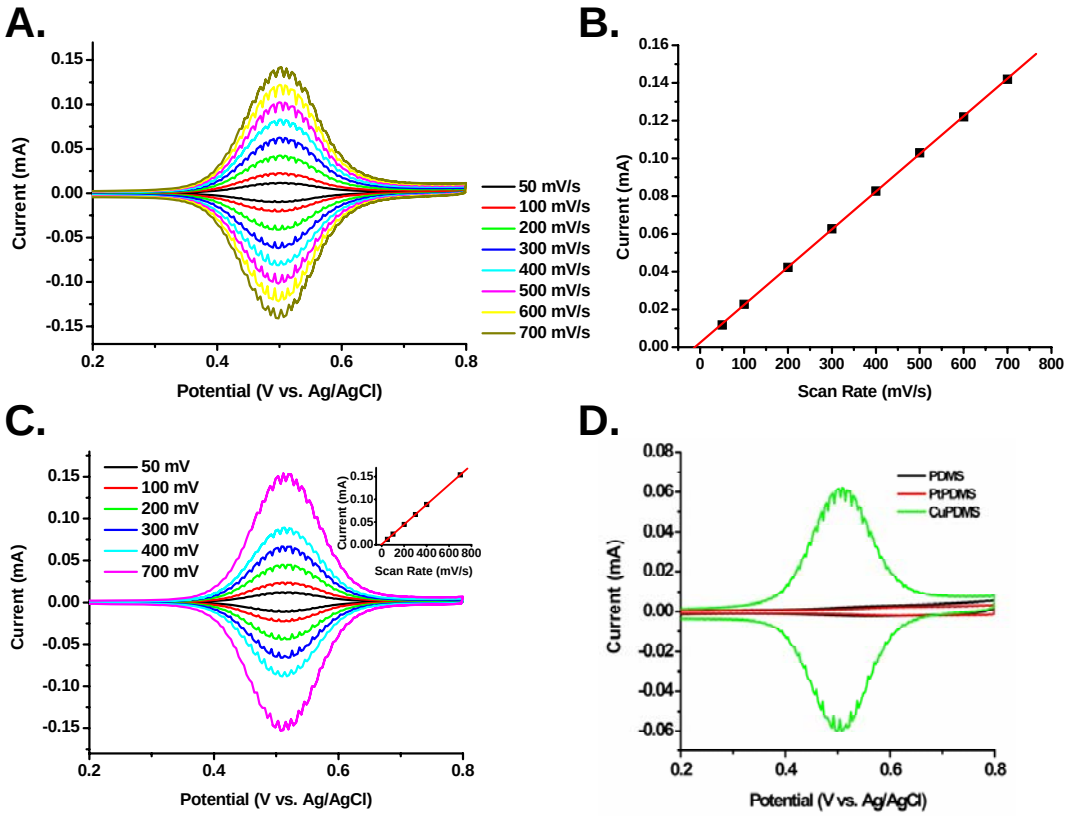

Figure 5.8. Electrochemistry of **3** patterned using the *HomoCat* and *StampCat* methods. **A.** Cyclic voltammogram of **3** stamped via *HomoCat* for various scan rates. **B.** Oxidation peak current as a function of scan rate, showing a linear relationship. C. Cyclic voltammogram of **3** stamped via *StampCat* for various scan rates. **Inset:** Oxidation peak current versus scan rate. **D.** Cyclic voltammetry of surfaces stamped with a Pt-coated PDMS (red trace) and bare PDMS (black trace) stamp with no added catalyst in comparison with a Cu-coated PDMS stamp (green trace).

There has been published evidence of the azide-alkyne cycloaddition occurring without a catalyst using μCP.[5, 6] It is hard to explain the cause of this discrepancy. AFM and fluorescence microscopy were used extensively in these studies to show pattern

transfer from the stamp to the surface. It could be that these characterization tools, neither of which are able to quantify surface coverage, are much more sensitive to a very low surface coverage of molecules. The resolution of florescence microscopy is several hundred nanometers[29] and so a strong fluorescence image may be present even for a few molecules. Similarly for AFM, a height difference may be observable even for a sparse packing density of molecules.

Another explanation is that the azide-alkyne cycloaddition can proceed without the Cu catalyst in elevated temperatures.[30] Although not explicitly mentioned in the published reports, heating the substrates during the stamping process was done occasionally.[31] For this study, it was not necessary to eliminate the catalyst and there was no further attempt to explore these different observations.

5.6 Stamp kinetics comparison

The advantage of doing electrochemical measurements is that they can be used to quantitate the surface coverage of the bound electroactive species. The area under the oxidation peak can be used to determine the amount of charge involved in the oxidation. Since the oxidation of ferrocene is a one-electron process, the amount of charge is equal to the amount of **3** bound to the substrate.

Using scientific plotting software, the oxidation peak over the second scan for each voltammogram was baseline corrected and the area was determined numerically

using the trapezoidal rule. The area in units of V·A is divided by the scan rate (in V/s) to determine the amount of charge, Q. The charge in Coulombs is converted to the amount of electrons by using the conversion factor, 6.24×10^{24} electrons/C. The number of electrons in the oxidation process is also equal to the number of molecules involved (for a one-electron process). By knowing the electrochemistry cell area (in this case, 0.78 cm^2), the number of molecules per unit area can be determined. Based on published results,[24] the amount of azide groups per unit area for a mixed monolayer of 50% **1** and 50% **2** on Au(111) is ~ 2.1×10^{14} cm^{-2} (assuming 45% azide coverage). A ratio of the calculated amount of **3** to this value yields the percent coverage.

Figure 5.9 shows the kinetics of the covalent attachment of **3** using the *HomoCat* and *StampCat* methods. Both reactions go to completion but the *HomoCat* reaction rate is faster than *StampCat* (30 minutes versus 60 minutes to completion). The relationship between percent azide consumed and time shows different rate laws for the two reactions.

The *StampCat* kinetics follow a zero-order reaction rate, as evidenced by the linear relationship between the percent azide consumed and time. The half-life of the reaction is ~ 30 minutes. Reactions involving heterogeneous catalysts can usually be described by using the Langmuir-Henshelwood or Eley-Rideal mechanisms.[32] The Langmuir-Henshelwood mechanism describes a mechanism in which two

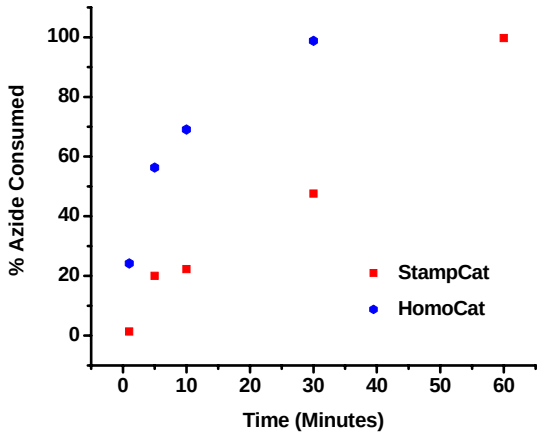

Figure 5.9. Kinetics plot of the StampCat and HomoCat techniques with **3**

reactants, A and B, adsorb onto a surface (typically the heterogeneous catalyst), diffuse and react once in close proximity. This mechanism is not likely since the azide groups are immobilized to the Au substrate. The Eley-Rideal mechanism describes a scenario where only one reactant adsorbs onto the surface. The reactant desorbs when it is in close proximity to the other reactant (which does not adsorb onto the surface). At high concentrations of the adsorbed reactant, the reaction becomes zero order.[33] Since the *StampCat* reaction is solvent-free, it has an extremely high concentration of the alkyne reactant. Although Eley-Rideal mechanisms are rare, the unique nature of having two immobilized reactants (the azide groups and the Cu catalyst) makes this the most likely mechanism.

It appears that the *HomoCat* kinetics follow a first-order exponential growth function. The half-life of the reaction is ~ 5 minutes. It is likely that because the alkyne is present in excess that the mechanism would follow a pseudo-first-order rate law. However, because there were no error bars on the data, it was not possible to estimate a rate constant, k, from the plot. More data points would most likely lead to a confirmation of the pseudo-first-order rate law.

5.7 The *StampCat* mechanism

The azide-alkyne cycloaddition to 1,4-disubstituted 1,2,3-triazoles is catalyzed by Cu in its +1 oxidation state.[34, 35] This reaction occurs via a step-wise mechanism. First, a Cu^{I} acetylide species is generated via a π complex which leads to the insertion of Cu onto the terminal end of the alkyne.[36] A ligation sequence begins where the azide's electron-rich nitrogen binds to the Cu^{I}, followed by a ring closure by the terminal nitrogen and the secondary carbon in the alkyne group.[34] DFT calculations have shown that the addition of the Cu^{I} ions lowers the activation energy of this process by as much as 11 kcal/mol and the reaction rate occurs up to 10^{7} times as fast as the uncatalyzed reaction.[36]

Cu^{I} salts, such as CuI, can be used directly. However, undesired side reactions can limit the use of these salts.[35] Typically, Cu^{II} (such as $CuSO_4 \cdot 5H_2O$) is added and reduced to the Cu^{I} state *in situ* using a reducing agent. There have also been reports of Cu metal, in the form of turnings,[34] Cu/C,[37] and Cu clusters,[38] catalyzing this reaction. The removal of Cu from these reactions typically requires simple filtration, which makes this an attractive alternative to solution-based catalysts. However, the use of Cu^{0} in CuAAC reactions is still rare (possibly due to the slower reaction rates observed for Cu^{0} systems) and there have been few reports on the mechanism of the catalysis.

Studies have shown that for CuAAC reactions using high surface area Cu^{0} catalysts, there was no evidence of Cu atoms or ions leaching into the reaction.[38, 39] In one experiment, the conversion to the triazole product between prop-2-yn-1-ol and benzyl azide was monitored as a function of time. When the catalyst, Cu powder, was filtered out of solution, no evidence of any further conversion was observed. The powder was

added back to the reaction and the reaction proceeded again at the same rate. This observation is consistent with the evidence in this study where after 1 hour of stamp time using a patterned stamp, no evidence of pattern diffusion was observed (see Section 5.5.4).

Since free Cu^{I} is not responsible for catalyzing the cycloaddition, it has been proposed that CuO and Cu_2O present on the surface of the Cu metal are responsible.[37, 40] An experiment was performed that examined the reusability of Cu-coated PDMS stamps. The stamping procedure was performed using **3** as the ink on the azide-terminated Au surfaces as described earlier. After 15 minutes of stamp time, the stamp was carefully removed from the substrate and the ink was reapplied. Three more substrates were stamped using the original stamp and their ferrocene concentration was measured using electrochemistry (Figure 5.10A).

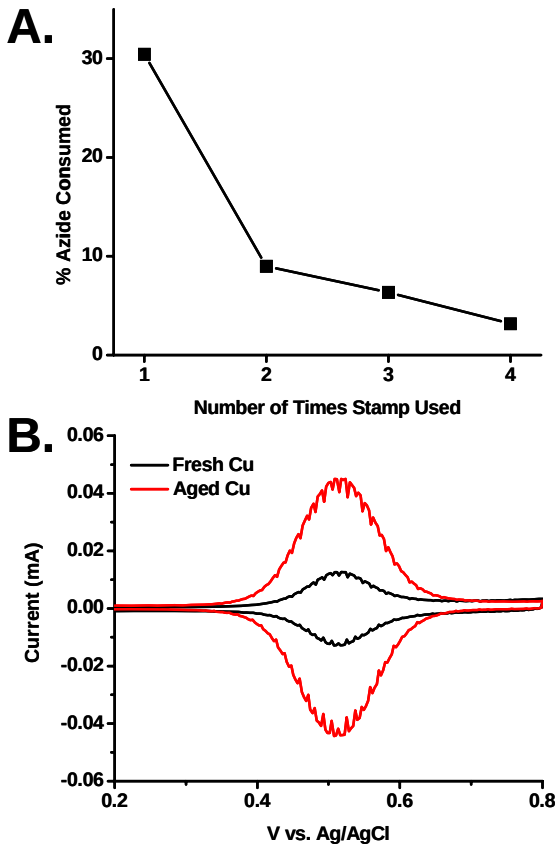

Figure 5.10. Elucidating the mechanism of *StampCat* using electrochemistry. **A.** Percent azide consumed as a function of repeated stamp use. **B.** Cyclic voltammograms of **3** patterned using *StampCat* using a freshly deposited Cu (black trace) and two day old Cu (red trace)

The stamp reusability results suggest an immediate loss of catalytic behavior after one use. The subsequent stampings show significantly smaller decreases. The structure

of the native oxide on Cu consists of an inner layer of Cu_2O and an outer layer of CuO. The growth of CuO is very slow and for freshly deposited Cu films at room temperature, the oxide would predominantly be Cu_2O.[41] After the first stamping, the majority of the Cu_2O on the surface of the stamp is somehow depleted from the stamp. This is consistent with the observation of an increase of the ink wettability on the surface after the first stamping (the ink wets Cu^0 much better than Cu_2O). The other reactions were limited by the regrowth rate of the Cu_2O between stamping. Similar observations were reported reusing Cu nanoclusters to catalyze the cross-coupling of alkynes and aryl halides.[39] After three uses, the nanoclusters could not catalyze the reaction to completion after 24 hours. Further evidence was provided by comparing the reaction rates of stamps used immediately after the Cu deposition versus after a two day delay. Older stamps displayed a higher catalytic ability (Figure 5.10B) for the same stamping time (~ 1 hour).

Due to the limited wettability of the deposited metal on PDMS and the flexible nature of the stamp, the Cu coating on the PDMS stamps was noticeably cracked on the microscale. It is likely that the deposited Cu also has significant surface roughness and contains many vacancies and dislocations. Cu films of this quality grow native oxide significantly quicker than higher quality films.[41] It is believed that this only helps the catalytic nature of the stamp. For other heterogeneous Cu catalysts, a higher surface area and more irregular consistency results in an enhancement of reaction rate.[38] Based on the evidence from this study and others, it is believed that the initial Cu^I acetylide species is generated from the Cu_2O present on the Cu stamp's surface.

5.8 μCP on silicon surfaces

Thiol monolayers on Au substrates, while well characterized, have limited utility. The dominant material for electronics is silicon and transferring the μCP process to silicon substrates would enable many technologies. For instance, the [2]rotaxane synthesis would need to be performed on Si substrates. The following sections describe two methodologies for generating azide-terminated silicon surfaces and preliminary stamping results on each.

5.8.1 Generation of azide-terminated alkane monolayers on Si(111)

One appealing chemistry for producing azide-terminated Si(111) surfaces is the hydrosilylation reaction using a diacyl peroxide as a radical initiator.[42, 43] In this reaction, a linear alkane molecule containing a alkene or alkyne termination is inserted into the silicon-hydride group of a hydrogen-terminated Si surface.[44] This reaction proceeds via a radical mechanism in which the diacyl peroxide undergoes a homolytic cleavage and subsequent decomposition to form an alkyl radical. This radical is transferred to the Si surface where it can react with the unsaturated group in the alkane molecule. This process continues until a complete monolayer is generated.

This chemistry is attractive because it forms densely packed, high-quality monolayers that are very resistant to oxidation. Chidsey et al. reported that hexadecyl monolayers synthesized using this chemistry were resistant to oxidation when exposed to boiling $CHCl_3$ (2 hours), boiling H_2O (7 hours), and air (11 weeks).[43] In comparison, hydrogen-terminated Si(111) and methyl-terminated surfaces prepared using

electrochemical anodization or the Lewis acid-mediated reduction of a terminal alkene form oxide within minutes of air exposure.[23] The high stability of the monolayers formed via hydrosilylation is useful for applications that require the Si surface to be exposed to air or aqueous environments, such as electronics and biological sensing.

The azide-terminated monolayers were generated by first forming chlorine-terminated alkyl monolayers on the surface, followed by the SN_2 substitution of chlorine to azide. To generate Si(111) surfaces, 1 cm^2 Si(111) pieces were first cleaned for 1 hour in hot acid piranha (3:1 H_2SO_4: 30% H_2O_2), followed by 15 minutes in hot basic piranha (30% NH_4OH: 30% H_2O_2) and an additional 30 minutes in acid piranha again. The substrates were rinsed with DI H_2O after each cleaning step. Next, the Si pieces were immersed in 40% NH_4F until the surfaces were covered in small bubbles (indicative of hydrophobicity), ~ 5 minutes. The samples were rinsed in DI H_2O for 30 seconds, dried with a N_2 stream and used immediately.

The hydrosilylation reaction was performed successfully using a 1:1 wt:wt ratio of 1-chloro-11-undecene (Aldrich, 97%) and lauroyl peroxide (Luperox LP, Aldrich, 97%), as well as a 9:1 ratio. Chidsey reported that 90% of the monolayer will be derived from the alkene molecule, regardless of ratio. Both reagents were used without further purification. The alkene/peroxide mixture was placed in a round bottom flask

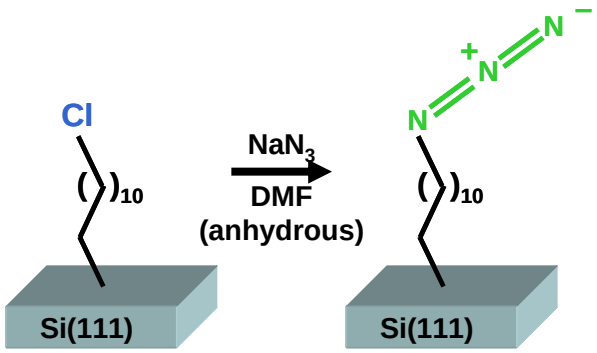

Figure 5.11. Schematic of azide-terminated monolayer on Si via hydrosilylation of 1-chloro-11-undecene and subsequent substitution to the azide

containing at least two necks, connected to a Shlenk line, and heated to 70°C under vacuum until the peroxide dissolved. The flask was backfilled with Ar and the hydrogen-terminated samples were carefully added. The flask was evacuated again, backfilled with Ar and heated to 100°C for 1 hour. Note, the reaction vessel must be vented to a mineral oil bubbler to reduce the risk of explosion! After the reaction was stopped, the samples were rinsed with EtOH and hexanes, sonicated twice for 5 minutes in $CHCl_3$, rinsed with EtOH and dried with N_2.

The azide substitution reaction (Figure 5.11) was performed in the glovebox to prevent surface oxidation. The chlorine-terminated samples were placed in vials containing a saturated solution of NaN_3 in anhydrous DMF. The vials were sealed with aluminum foil and placed on a hotplate set to 100°C for at least 16 hours. The samples were then rinsed with DMF and methanol, and dried.

5.8.2 Generation of direct azide-terminated silicon surfaces

An alternative method for generating azide-terminated Si surfaces is to form direct azide bonds to the surface Si atoms. This is a novel approach, developed by Peigen Cao in the Heath group, and has not been previously reported by other groups. Since the alkane spacer is eliminated, subsequent CuAAC reactions would generate interesting monolayers with better electrical contact to the substrate. This would have a large impact on chemical and biosensors, as well as molecular electronics.

The first step in generating azide-terminated Si surfaces is to form a high quality hydrogen-terminated surface. Si(111) wafers were cleaved into 1 cm^2 pieces and sonicated in methanol for 5 minutes. Teflon reaction beakers and sample tweezers were

cleaned by filling them with diluted basic piranha (1:1:4 NH_4OH: H_2O_2: H_2O) at 80 ^oC for 10 minutes. After rinsing the beakers out with DI H_2O, they were filled with a new solution of basic piranha. The samples were rinsed with water and placed in the basic piranha solution for 10 minutes at 80^oC. Samples were removed from the basic piranha solution, rinsed with DI H_2O, and dried with N_2. It is important that the samples be completely dry. The samples were then immersed in NH_4F at room temperature for at least 15 minutes. The samples were then rinsed with DI H_2O (the samples should be very hydrophobic at this point) and dried with N_2.

Next, the hydrogen atoms on the Si surface were replaced with chlorine atoms. The samples were loaded into a glove box containing an inert atmosphere for the chlorination reaction. A scant amount (~ 1 mg) of benzoyl peroxide, the reaction initiator, was added to large, glass test tubes. One substrate is added per test tube and several mL of a saturated solution PCl_5 in chlorobenzene was added. The test tubes were headed to 95^oC for 45–50 minutes. The reaction can also be done at RT for ~ 5 hours to generate a smooth surface for STM measurements. Once the reaction is complete, the samples were rinsed with THF, followed by methanol (MeOH) and immediately used for the azide substitution reaction.

Several substitution reaction conditions were tried to generate azide surfaces from the chlorine-terminated surfaces with the highest surface coverage (Figure 5.12). Here, the

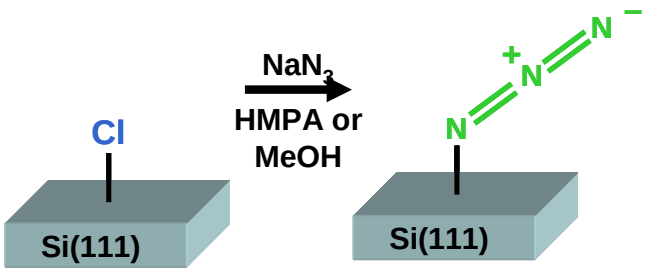

Figure 5.12. Schematic of synthesis of direct azide-termination on Si(111)

procedures that yielded surface coverages of ~ 30% and ~ 65% will be described here. For the lower coverage reaction, the freshly prepared, chlorinated Si samples were added to a saturated solution of sodium azide (NaN_3) in anhydrous methanol and left at room temperature overnight. For the high coverage reaction, an excess of CaH_2 was added to a vial of 99% Hexamethylphosphoramide (HMPA) for 1–2 days to remove water. The mixture was filtered using a 0.25 μm filter prior to the reaction. A large excess of NaN_3 was added to the filtered HMPA. Upon the addition of NaN_3, the solvent changed from yellow color to a dark orange. Chlorine-terminated samples were placed in the NaN_3 solution for 5 minutes at RT. Note that the NaN_3/HMPA mixture is photosensitive. For both reactions, the substrates were then removed, rinsed with copious amounts of tetrahydrofuran (THF) and methanol, and used immediately.

5.8.3 Stamping results on azide monolayers formed via hydrosilylation

XPS analysis confirmed that the SN_2 reaction to form the azide-terminated monolayers was successful. The spectra for both surfaces in Cl 2s region (Figure 5.13A) show the disappearance of the chlorine peak after the azide reaction. The chlorine 2p peak, located at 201 eV, also disappears after the azide reaction. At the same time, nitrogen peaks at 401 and 405 eV, characteristic of the azide group, appear. Additionally, the contact angle dropped from 99° to < 65° after the SN_2 reaction.

The ferrocene alkyne, **3**, was attached to the azide-terminated monolayers by *StampCat* and by the solution-based reaction, as described in Section 5.3. The reaction was successful for both reaction conditions. The XPS data in the nitrogen region show the disappearance of the peak at 405 eV and the broadening of the 401 eV, as expected

for the formation of the triazole ring (Figure 5.13B). The appearance of iron peaks are also observed for both reactions (Figure 5.13C). The contact angle of the surface from the solution-based reaction increased to 68°.

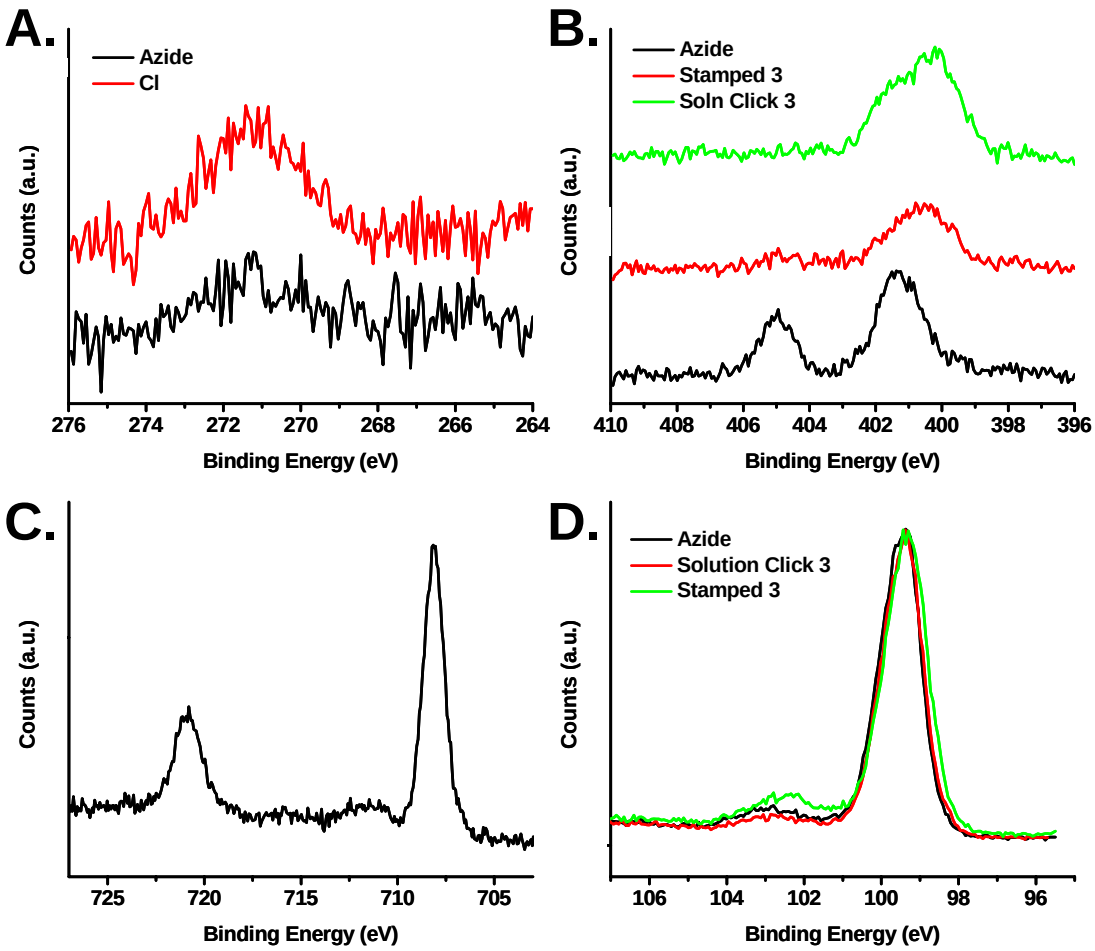

Figure 5.13. XPS data for CuAAC reactions on azide-terminated surfaces made via hydrosilylation. **A.** Stacked spectra of the chlorine- (red) and azide-terminated (black) surfaces in the C 2s region. **B.** Stacked spectra of the azide-terminated surface (black) and surface patterned with **3** via *StampCat* (red) and by solution-based CuAAC. **C.** Spectra of the solution-based reaction in the Fe 2p region. **D.** Spectra of the azide-terminated surface (black) and surfaces patterned with **3** via solution (red) and *StampCat* (green)

Because the monolayer on the surface contains 11 carbons, it was difficult to quantify monolayer surface coverage using the carbon 1s region. Instead, the ratio of the SiO_x peak (centered at 103 eV) to the Si 2p peak (centered at 99.5 eV), divided by the

normalization constant of 0.21, was used to determine the amount of surface atoms that were oxidized.[23, 45]

For the azide-terminated surfaces, the amount of surface Si atoms oxidized was ~ 0.3, which corresponds to ~ 70% monolayer surface coverage (Figure 5.13D). There was no further oxidation observed after the solution-based reaction. This is not surprising since the reaction was carried out in the glove box. The stamped surfaces, however, did show an increase in the SiO_x peak. The resulting surface coverage dropped to ~ 60%. The stamping was done outside of the glove box so the sample was exposed to ambient air for a few hours. Stamping inside of the glove box should eliminate any additional oxidation. Although the surface does not appear to be as robust as reported,[43] reaction conditions have not yet been extensively explored.

5.8.4 Stamping results on direct azide-terminated silicon

Several solution-based and stamping experiments were performed on the direct azide-terminated silicon surfaces. XPS and contact angle results indicated that the CuAAC reaction with **3** proceeded very poorly. Solution-based reactions were performed using several different solvents, including DMF, MeOH, acetonitrile, and HMPA. Reactions were also performed with 0.2 equivalents of tris-(benzyltriazolylmethyl)amine (TBTA), which strongly facilitates the formation of the 1,2,3-triazole and also inhibits oxygen reduction by the Cu catalyst.[24] The addition of TBTA did not have any effect. As a control, the same reaction conditions were used on a 50% azide-terminated monolayer on Au and XPS confirmed that the reaction went to completion. Other alkyne species were tried without success. Molecules that contained a carbonyl group next to

the alkyne group were tried in hopes that the carbonyl group's electron withdrawing nature would facilitate a Cu-free "click" reaction,[46] but no reproducible evidence of this reaction was observed.

Numerous stamping experiments were also performed. Cu-coated stamps were stamped onto freshly prepared, azide-terminated Si(100) and Si(111) substrates for 1 hour using **3** as the ink. Azide-terminated surfaces with both 30% and 70% coverage were used as substrates to see the effect of coverage and reaction efficiency. Again, no evidence was observed using XPS or contact angle measurements that the reaction occurred beyond a few percent conversion. These results are not surprising since the *StampCat* mechanism is not expected to be different from the solution-based reaction, which also failed. To facilitate the reaction, substrates were also heated to 40–50°C during the stamping with no effect. The XPS results suggested that not only does the reaction not proceed quantitatively, the azide-termination provides little protection from oxide growth, which occur within hours for Si(111) surfaces and minutes for Si(100) surfaces.

Since the azide-terminated surface is so fascinating, it is important to understand why the CuAAC reaction does not proceed readily and if conditions exist that would make it favorable. It is interesting that, regardless of azide surface coverage, the reaction fails. This suggests that the Si surface itself may be sterically or electronically inhibiting the reaction.

The XP spectra of the azide region of the azide-terminated surfaces itself has some interesting features. For instance, an experiment performed by a colleague showed that a third peak at ~ 398 eV appears in the nitrogen region when HMPA is used as a

solvent and as a function of reaction time (Figure 5.14). This peak is not present when MeOH is used as the solvent. Also, Si oxidation is observed in the glovebox after long reaction times with HMPA. This third peak, however, is not directly correlated with surface oxidation. The peak at 398 eV does not change after the substrate is explored to ambient conditions for several hours but the SiO_x peak continues to increase. Additionally, a third peak has been observed at ~ 407 eV when MeOH is used as solvent, which suggests the mechanism of azide-termination varies depending on the solvent choice. Further exploration of the mechanism behind the reaction and how it is affected by the solvent choice, and why the CuAAC reaction does not proceed readily on these surfaces is needed and will most likely reveal many interesting insights.

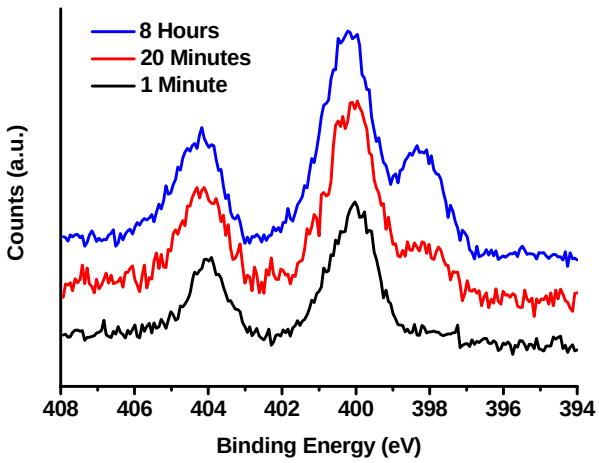

Figure 5.14. XP spectra of azide-terminated Si(111) surfaces after 1 minute (black), 20 minutes (red), and 8 hours (blue) reaction time using HMPA as the solvent

5.9 Conclusion

A new microcontact printing technique was developed that utilized a heterogeneous catalyst coated directly on the stamp. The Cu-catalyzed azide-alkyne cycloaddition was used to covalently attach interesting molecules onto Au or Si substrates. The heterogeneous catalyst reaction was shown to proceed almost as quickly as the homogeneous catalyst reaction. The benefits to using a heterogeneous catalyst is that the surfaces are not contaminated by residual catalyst and the Cu^{I} solubility issues in the ink are eliminated. Not only is 100% conversion achievable after ~ 1 hour of stamp time using a flat stamp, but patterns using patterned stamps are transferred to the substrates with high fidelity. It is expected that this technology will be important in making new molecular electronics devices and circuits easily and quickly.

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