A two-step binary particle swarm optimization approach for routing in VLSI

Abstract

Manipulation of wire sizing, buffer sizing, and buffer insertion are a few techniques that can be used to improve time deley in very large scale integration (VLSI) circuit routing. This paper enhances an existing approach, which is based on Particle Swarm Optimization (PSO) for solving routing problem in VLSI circuits. A two--step Binary Particle Swarm Optimazation (BPSO) approach, wich is based on BPSO, is chosen in this study to improve time delay through finding the best path of wire placement with buffer insertion from source to sink. The best path wire placement is found in the first step by the first BPSO and then the second BPSO finds the best location of buffer insertion along the wire. A case study is taken to measure the performance of the proposed model and the result is obtained compared with the previous PSO approach for VLSI routing.