

ABSTRACT:

This paper, presents a new full-swing low power high performance full adder circuit in CMOS technology. It benefits from a full swing XOR-XNOR module with no feedback transistors, which decreases delay and power consumption. In addition, high driving capability of COUT module and low PDP design of SUM module contribute to more PDP reduction in cascaded mode. In order to have accurate analysis, the new circuit along with several well-known full adders from literature have been modeled and compared with CADENCE. Comparison consists of power consumption, performance, PDP, and area. Results show that there are improvements in both power consumption and performance. This design trades area with low PDP.