Open source microprocessor and on-chip-bus for system-on-chip

Abstract

A System-On-Chip (SoC) is a complex integrated circuit that combines blocks of processor, memory and peripheral devices in one chip. SoCs often form the main or the only component of embedded systems. The advantages of the SoC include improvements in performance, size, reliability, power dissipation, cost, and design turn-around time. The hardware blocks – sometimes referred to as intellectual property cores or just IPs – are connected using a proprietary or open on-chip bus (OCB). The SoCs may be fabricated as application-specific integrated circuits (ASICs) or field-programmable gate arrays (FPGAs). The non-recurring engineering (NRE) costs for ASICs are much higher although the unit cost for the finished product is lower. For simpler designs and/or lower production runs, FPGAs are usually more cost-effective. One of the costs in implementing an SoC is acquiring the source code or designing the required cores. An approach for reducing costs is to use open source hardware. Open source cores have the advantages of zero license and royalty cost, ability to modify the cores at will, no limitation on supply and maintenance, portability and simplified prototyping. We discuss our implementation of a skeleton SoC incorporating a DLX processor, the Wishbone on-chip bus, and a memory system. The processor bus- memory combination forms a foundation to which a designer can add more cores such as memory and peripherals as long as they comply with the Wishbone protocol. The DLX processor and memory are described in VHDL, while the Wishbone module is in Verilog HDL. Quartus II software is used to synthesize, compile and verify the functionality of CPU and Wishbone by simulation and timing analysis. The partial SoC system is implemented in Altera APEX20KE200 FPGA board. Nios, which is the core processor in the FPGA board, is used as an intermediate processor which communicates with DLX and the rest of the system via Avalon Bus Protocol to verify system operation and functionality in real hardware environment.