

MKAS: A Modular Knockout ATM Switch

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Abstract: Simple Knockout Switch [1] exhibits excellent traffic performance (cell loss, cell delay and maximum throughput etc.) under uniform as well as non-uniform traffic patterns [2-6]. But being a single stage, its hardware complexity is directly proportional to the switch size N . This problem may bind its implementation for large-scale requirements because of the technological and physical constraints of packaging (e. g. chip or board size). Here, we are proposing a two-stage Modular Knockout ATM Switch architecture, which is extendable to large-scale switch sizes without sacrificing any significant decrease in switch performance. The concept of Generalised Knockout Principle in conjunction with Simple Knockout Principle has been utilised to filter, route and resolve the output contention problems in distributed fashion. Using distributed address filtration and shared concentration techniques simplifies the switch functions and reduces the switch complexity to large extent in terms of filters, switching elements and input output interconnection wires.

I. INTRODUCTION

Asynchronous transfer mode (ATM) has been a hot topic of research since its recommendation by ITU-T for B-ISDN. The standard operating speed of an ATM switch can be in the ranges of 155 M bits/s or 662 M bits/s to G bits/s.

Because of the high-speed requirements an ATM switch can only be implemented in hardware using Very Large Scale Integration (VLSI) technology. However the physical constraints of the VLSI chips do not support very large size switch fabrication. Here the modularity of the switch is the only solution that leaves to build large-scale ATM switches, which are required to construct the global information infrastructure.

To solve this problem several efforts have been made [7-10] to date. Among them, Knockout Switch [1], proposed by Y. S. Yeh et al shows outstanding cell loss, cell delay and switch throughput performance under uniform as well as non-uniform traffic patterns [2-6]. But being a single stage and

using direct interconnection topology the switch complexity and switch cost increases in direct proportions to switch size N and may create bottleneck for its large-scale implementation [4,8].

This paper proposed A Modular Knockout ATM Switch, which can be extended to any switch size N modularly for its large-scale implementation. The proposed ATM switch is actually a modification of original knockout switch by using Generalized and Knockout Principles [7,10] to route and resolve the contention problems in two stages distributedly. Although Chao [7,8], Eng [10], and Chen [11] used the same technique in their work but our proposed switch is bit different from them in architectural as well as routing point of view. The novel aspect of the proposed switch is that the last stage of the switch can be constructed either by using Filter's approach or Banyan Network approach. However, whatever the technique is used the proposed switch offers from 50% to 65% reduction in switch complexity as compared to Knockout Switch.

The rest of the paper has been organised such that section II describes switch architecture and switch operation in detail. Section III briefly explains the switch modules whereas section IV sketches the switch complexities of MKAS with Knockout Switch under Filter & Banyan approaches. Concluding remarks has been given in section V.

II. THE PROPOSED SWITCH ARCHITECTURE AND ITS OPERATIONS.

Modular Knockout ATM Switch (MKAS) is a $N \times N$ two-stage space-division, self-routing, non-blocking switch architecture with all inputs and outputs operating at the same speed. Figure 3.1 depicts the block diagram of the switch architecture. The proposed switch architecture mainly consists of N broadcast buses and M Group Bus Interface Modules (GBI), $M \ll N$, provided that all switch inputs are directly connected to all Group Bus Interfaces and each GBI consists of a group of n output ports. Interconnecting the switch outputs and inputs through Group Bus Interfaces makes MKAS internally non-blocking. Remember that each GBI provides enough

routing paths to its group members to access switch inputs and maintains the cell loss probability less than 10^{-6} , which is less than the cell loss probabilities that may occur in the packet switching networks due to network failure, buffer overflow or routing errors [1].

As shown in Figure 1, each GBI is a two-stage module and consists of a row of N cell filters, a Group Concentrator, a Destination-sorting Network (DSN) and first-in-first-out shared output buffers. The function of cell filters is to sort out the ATM cells from the broadcast buses by examining their group address bits whereas the group concentrator performs group-concentration from $N:m$ on the filtered ATM cells and forwards the m winners to DSN in the second stage.

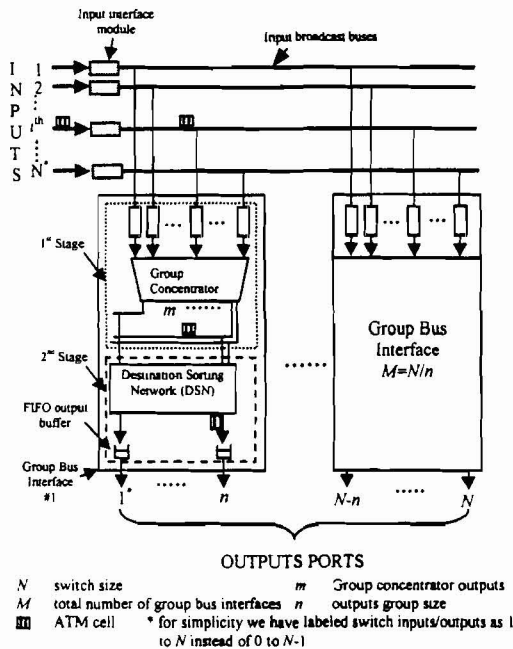


Figure 1. Proposed Switch Architecture

At second stage, DSN filters the cells, which have been filtered by the first stage cell filters under one group address, to their destined output ports based on the provided destination address bits in the header of the cells and store them into h -input one output FIFO buffers accordingly. As mentioned, destination sorting-network of MKAS can be constructed either by using Filters or Banyan approach and will be discussed in detail in the subsequent sections.

To describe the switch operations in detail consider an ATM cell arrives at i^{th} input port of the switch in a time slot which needs to be switched to an output port $\#n$ of GBI $\#1$. First of all, Input Interface Module at i^{th} input port retimes and synchronizes the arriving cell to the local switch reference clock. Then based on the given virtual path and virtual channel identifiers (VPI/VCI) values in the header of the incoming ATM cell, input interface module translates the destination address relevant to the local routing address of the cell by using look up table. It is mentioned, that the local address only has the local significance, as it is just required to route the cell inside the switch to access the particular output port and the output

interface module removes it instantly before transmitting the cell on the output links. However it is desirable to keep the length of local address as small as possible to avoid unnecessary delay in the transmission of ATM cells inside the switch. MKAS requires only $\log_2 N$ bits, where N is a switch size.

As mentioned each GBI consists of two stages therefore to facilitate self-routing functions at both stages of MKAS independently the local address bits ($\log_2 N$) has been partitioned into group address bits and destination port address bits where the number of bits required for group or destination addresses depends upon the selected output group size n and switch size N . The following equations show the break up of local address into its group and destination addresses.

Local address bits = Group address bits + Destination address bits

$$\log_2 N = \log_2 g + \log_2 n \quad (1)$$

where;

$$\log_2 g = \log_2 N - \log_2 n \quad (2)$$

Now the first stage cell filters, mounted on the top of each GBI, actively try to filter out the incoming cell by examining just its $\log_2 g$ group address bits. Because the group address bits of the cell has been mentioned only for GBI $\#1$, therefore the cell filters of GBI $\#1$ will filter it out successfully and allow it to travel to one of the N inputs of group concentrator where it undergoes group-concentration along with other ATM cells arriving on the other inputs of the group concentrator from different switch input ports by following the same procedure. The group concentrator, located at the first stage of each GBI concentrates these ATM cells on its rightmost output from $N:m$, where $m < N$. Remember that the outputs of group concentrator has been optimised against the selected outputs group size n by using Generalized Knockout Principle [20] to keep the cell loss probability less than 10^{-6} or 10^{-10} during this concentration process.

After making through the group concentrator successfully, the ATM cell emerges as a winner on one of the m outputs of the group concentrator and is forwarded to DSN in the second stage. In Destination Sorting Network (DSN) it again follows the same filtration and concentration (from $m:h$) functions and finally reaches at output port $\#n$ where it is buffered into h -input one output shared FIFO buffers to guarantee its sequencing in order and departed on output link in the subsequent time slots. Note that by using Knockout Principle $h \geq 8$ is enough to maintain the cell loss probability less than 10^{-6} .

The novel aspect of the proposed switch is that even externally it has the same number of routing paths as in the Knockout Switch but internally each GBI is sharing m ($m \gg 8$) routing paths among its group members, making it most suitable and stable for bursty traffic which offcourse ATM networks naturally exhibit. For example if the switch size $N=64$ and the selected group size $n=8$ then each GBI module of HMKS will be using externally 8 paths but internally it will be sharing 22 routing paths among

its group members thus making it more reliable for bursty traffic environments. The other advantage of this technique is this it also reduces switch circuitry greatly without sacrificing the switch performance.

III. DESCRIPTION OF SWITCHING MODULES

As mentioned, HMKS comprises of M Group Bus Interfaces and each GBI performs the identical functions to route the cells to their destination ports belonging to its group and consists of the following components:

- Cell Filters
- Group Concentrator
- Destination Sorting Network
- Output Buffers

i) Cell Filters

The cell filters of Group Bus Interface examine the $\log_2 g$ bits of group address of the incoming ATM cells and accept those cells $\log_2 g$ bits of which match with their mentioned group address bits. Figure 2 shows the ATM cell format as it traverses the cell filters.

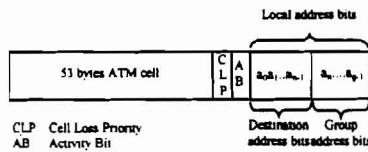


Figure 2 ATM Cell format

ii) Group Concentrator

After undergoing the group filtration process the filtered cells are forwarded to the inputs of group concentrator, which achieves from N : m concentration on them. Note that group concentrator carries out this process on a group of n outputs rather than a single output as does Knockout Switch [1] and the chances of more cells will be selected as winners for first stage are increased for by adding up $m-L$ more outputs to the simple knockout concentrator. However there might be a cell loss in the group concentrator when more than m cells contend for one particular GBI in one time slot. Using Generalised Knockout Principle the likelihood of more than m cells will arrive at a small group of n outputs is extremely small for an arbitrarily large switch size N , with $m \ll N$ is less than 10^{-6} [10]. Thus, the cell loss probability in a group concentrator with N inputs and m outputs will be:

$$P[\text{cell loss}] = \frac{1}{np} \sum_{r=m+1}^N (r-m) \binom{N}{r} \left(\frac{np}{N}\right)^r \left(1 - \frac{np}{N}\right)^{N-r} \quad (3)$$

$$P[\text{cell loss}] = \left(1 - \frac{m}{np}\right) \left(1 - \sum_{r=0}^m \frac{(np)^r e^{-p}}{r!}\right) + \frac{(np)^m e^{-p}}{m!} \quad (4)$$

Where;

n =number of grouped outputs

m =group concentrator outputs

p =load at switch inputs

r =number of cells which arrive at a group bus interface in one time slot.

From designing point of view the group concentrator is similar to that of simple knockout concentrator [1] and there is no difference in the both except that the outputs of group concentrator have been increased from L to m just adding up $m-L$ more outputs to the simple concentrator or in other words by increasing the knockout rounds from L to m .

iii) Destination Sorting Network

Figure 1 shows that the second stage of each GBI comprises of a DSN, directly connected to m outputs of a group concentrator to sort out the cells to their destined output ports based on the destination address bits mentioned in the header of these cells. HMKS proposes two different aforementioned approaches to construct Destination Sorting Network as follows:

- Filters approach
- Banyan Approach.

a) Filters Approach

To build destination sorting-network by using Filters Approach requires n Sub-bus Interfaces (SBI) one for each output port in one GBI in second stage. From Figure 3 each Sub-bus Interface is a mirror image of bus interface module used in Simple Knockout Switch and consists of a row of m filters at top of the concentrator to filter out the cells, forwarded by the group concentrator, by examining the $\log_2 n$ destination address bits (Figure 2). The filtered cells here undergo concentration from m : h once again and get stretched to the rightmost outputs of the concentrator. Recall that by using Knockout Principle $h=8$ enough to keep the cell loss probability less than 10^{-6} . Now these cells are queued into h -input one output *FIFO* shared output buffers at their respective output ports and are departed on the output trunks one in every time slot.

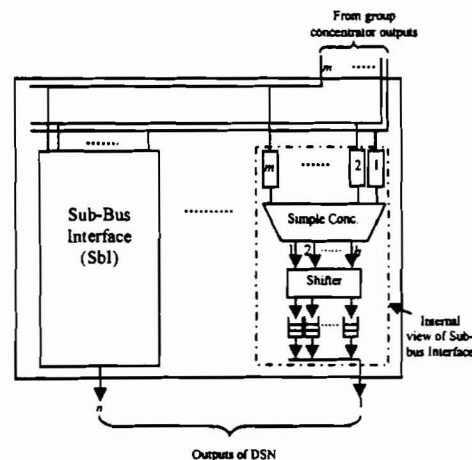


Figure 3 Destination Sorting Network with Filters Approach

b) Banyan Network Approach

Figure 4 shows the designing of Destination Sorting Network (DSN) by employing Banyan network structure.

Using Banyan technique has the advantages of reduction in switch complexity and cost to large extent as compared to even Filters Approach. The other benefit of using this technique is that it provides internally m and externally $m/2$ -dedicated paths to cells to access their port buffers. Figure 5 shows the architecture of 2-inputs 8-outputs Banyan network used to construct the DSN. Note that this 2-inputs and 8-outputs Banyan structure is a non-blocking, self-routing and it does not require any shuffle exchange or sorter networks [11,12] at its inputs to arrange the cells in order to avoid the possible blocking inside the network. Thus the cells coming out of the outputs of the grouped concentrators are directly fed into this network and it routes them to their destined output ports based on the provided destination address bits in the header of each cell. This network is a complete replacement of second stage filters and concentrators in Filters Approach (Fig 3).

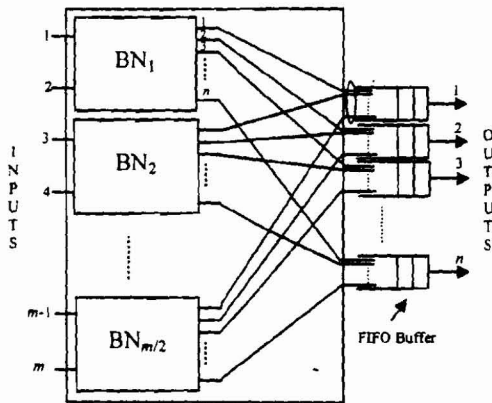


Figure 4 Destination Sorting Network architecture using Banyan approach

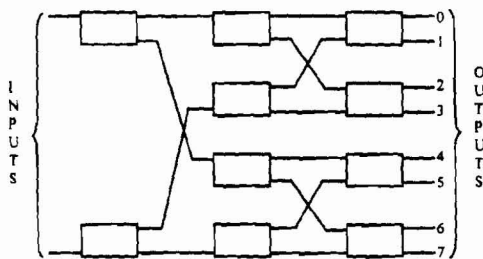


Figure 5 a 2x8 Banyan network architecture for Destination Sorting Network

IV. COMPLEXITY OF MKAS

Figure 6 compares the complexity of Modular Knockout ATM Switch with Simple Knockout Switch in terms of switching elements. For the sake of simplicity the complexities of both switches have been estimated by calculating the number of gates for each switch. As both switches has been constructed by using cell filters and concentrators thus counting

the total number of required gates for filters as well as for switching elements the complexities could be compared.

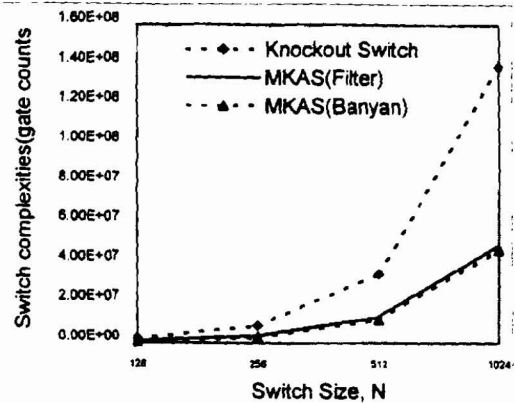


Figure 6 Comparison of MKAS with Knockout Switch under both techniques for different switch sizes N & $n=8$

On the other hand to show the significance of using Filters or Banyan approach to construct DSN in the MKAS, Figure 6 also compares the complexities of both techniques and illustrates that Banyan approach offers more reduction in switch complexity as compared to Filters approach.

V. CONCLUSION

In this paper we have proposed a two-stage Modular Knockout ATM Switch, which can be extended to any switch size modularly. The proposed ATM switch is a redesigning of Simple Knockout Switch by using Generalized and Simple Knockout Principles simultaneously. Employing Generalised Knockout enables MKAS to treat its outputs under one group address and reduces the switch complexity (interconnections wires and switching elements) greatly whereas the Simple Knockout Principle demultiplexes these grouped cells and route them to their final destination output port. Splitting Knockout Switch into two stages has the advantages of simple and distributed filtration and routing functions as well as large reduction in switch circuitry, estimated as 50 to 65% by using Filters or Banyan approach respectively.

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