A Comparative Study on the Performances of the Boost PFC Circuit

M. R. Sahid, N. A. Azli and N. D. Muhammad

Abstract-- **Power Factor Correction (PFC) circuit using Boost converter for low power applications are developed and analyzed in this work. Average current mode control is utilized in this work to control the circuit in the closed loop system. Simulation is done for the Boost PFC circuit to validate the designed parameters. Furthermore, an experimental circuit is developed to verify and compare the results with the simulation. The frequency spectrum of the input current is then compared with the EN/IEC61000-2-3 Standard on Harmonic Distortion. The dynamic response of the input current and output voltage are discusses as well. A 500W output load is first chosen to illustrate the performances of the circuit. Several values of output load and input voltage would conclude the overall performance of the circuit.**

Index Terms-- **Boost converter, PFC circuit, power quality, harmonic, IEC Standard.**

I. Introduction

Power Electronics is one of the areas, which shows a rapid development and improvement in its technology. A wide range utilization of its circuit in the real application system; namely in lighting circuit (electronic ballast), power amplifier, personal computers, backup power supply (UPS) and motor drives; were the main contribution to its popularity. In addition, the advancement of the switching devices has led to the improvement of power electronic technology as well [1].

Nevertheless, these power electronic circuits have several drawbacks. For example, it is a well-known fact that most equipment required an AC to DC conversion from the AC mains supply. This conversion normally required a filter in order to obtain low ripple voltage and for that purpose, a bulk capacitor is used. The combination of AC to DC converter (rectifier), bulk capacitor and passive load (purely resistive or resistive-inductive load) would create a so-called non-linear load. This non-linear load would normally generate a high-pulsating input current from the mains with non-sinusoidal waveform as shown in Fig. 1 and it's contains low order harmonic current. These low-order harmonic current would severely distort the mains voltage at point of common coupling, overheating at some particular device, create noise and reduce the power line reliability and capability in providing energy [2]. The total harmonic distortion of the input current (THD_i) is 202.35%. Most countries disallowed the usage of this low power quality due to its incompliance to the International EN/IEC 61000-3-2 Standard on Harmonic content. The incompliance of the input current harmonic and the IEC standard is depicted in Fig.2.

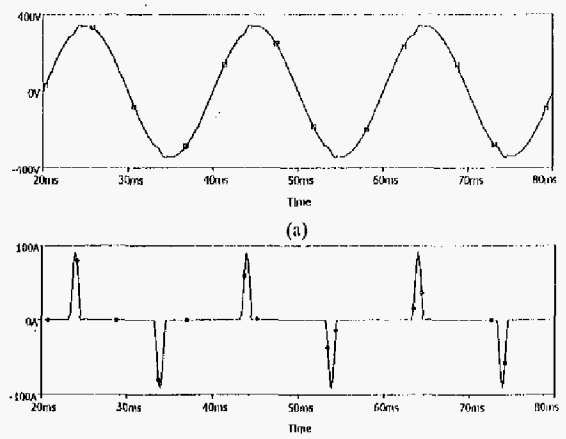

Fig.1 (a) Input voltage and, (b) input current waveforms

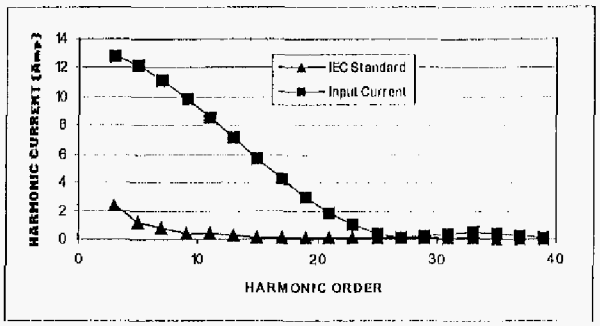

Fig. 2 Comparison of the input current harmonic with EN61000-3-2 Standard

Several approaches have been proposed in order to cater with the above-mentioned problems. Active Power Factor Correction (PFC) circuit is one of the most suitable solutions that can reduce the effect of high-pulsating input current generated by the non-linear load. This PFC circuit works well in low power application that is handling power below 100kW. The previous work [3,4] mentioned that among various types of PFC circuit, it could be concluded that Boost type PFC shows better performance in terms of efficiency, power factor, total harmonic distortion of current (THD_i) and gate drive circuit simplicity.

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In this paper, a study is carried out to emphasize on the performances of the circuit in terms of several aspects mentioned above. The PFC circuit is initially simulated in order to verify the selected design parameters. Validation of the PFC circuit is proves by constructing the experimental circuit. The input current is then compared with the international EN/IEC61000-2-3 Standard on Harmonic Distortion. Analysis is carried out with different loads and input voltage values. The dynamic response of the input current and output voltage is monitored as well.

II. Boost PFC Circuit Design

In power electronics circuit, the whole system design is determined by the selection of the circuit specifications. For Boost PFC circuit, the main specifications are mentioned in terms of output power, input voltage, output voltage and its ripple, operation of the current mode (whether continuous or discontinuous), switching frequency and desired efficiency as represented in Table I. The overall circuit design can be divided into two main groups namely Power Circuit design and Controller Circuit design. Fig 3 shows the circuit diagram for the Boost PFC circuit consists of the power circuit part and the controller circuit part.

TABLE I
Boost PFC Circuit Specifications

Parameters	Value
Output Power, P_O	600W
Input voltage, $V_{in(RMS)}$	160-240 V_{RMS}
Line Frequency	50 Hz
Regulated Output Voltage, V_O	390V_{DC}
Output Voltage ripple	< 4%
Current Mode Operation	CCM
Switching Frequency, f_S	60 kHz
Desired Efficiency, η	99%

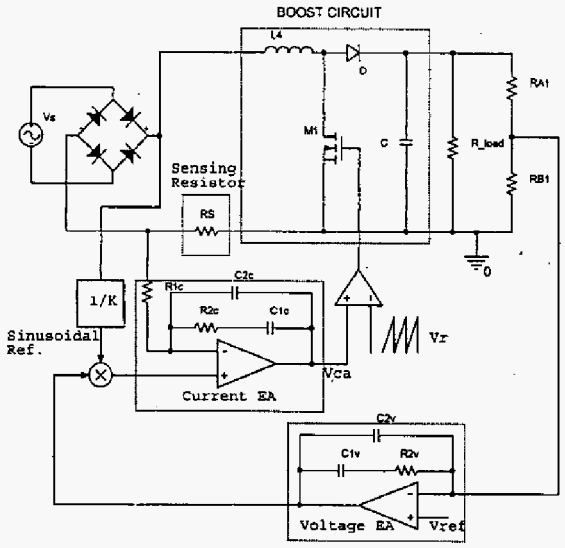

Fig. 3. Boost PFC circuit diagram

A. Power Circuit Design

Power circuit consists of all high power ratings components and devices. In order to design the power circuit, the value of each component will be determined such as inductor value and its design procedures, output capacitor value, input capacitor, inductor current sense resistor and the current flow through switch. Besides that, the design of each power component would be strongly affected by the switching frequency. Higher switching frequency would reduce the size of each components but the drawback is increasing in power losses due to switching losses.

Firstly, the value of the inductor would be calculated based on the design specifications. The inductor/input peak current is obtained from the equation on the efficiency of the circuit, which is

$$\eta = \frac{P_O}{P_{in}} = \frac{P_O}{I_{in\_rms} V_{in\_rms}} = \frac{2P_O}{I_{Lp} V_{Lp}} \quad (1)$$

and solved for I_{Lp}, where V_{Lp} is peak inductor/input voltage . All the variables in (1) are calculated based on worst-case condition for the maximum output power and minimum input peak voltage. The inductor value is determined by calculating the minimum inductor value [5], which is

$$L_{min} = \begin{cases} \dfrac{V_{Lp}\left(V_O - V_{Lp}\right)}{\Delta I_{L\max} V_O f_S} & if\ V_{Lp} \le \dfrac{V_O}{2} \\ \dfrac{V_O}{4 \cdot \Delta I_{L\max} f_S} & if\ V_{Lp} > \dfrac{V_O}{2} \end{cases} \quad (2)$$

where ΔI_{Lmax} is the maximum ripple inductor current.

From (2), it can be seen that the minimum inductor value, L_{min}, is actually a function of input peak voltage, (V_{Lp}). The upper equation is used when the input peak voltage is less than or equal to $V_O/2$ while the lower equation is used when the input peak voltage greater than $V_O/2$. The maximum ripple inductor current, (ΔI_{Lmax}), is obtained based on the requirement of the current operation, which is Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM. If the value of ΔI_{Lmax} is smaller than $2 \cdot I_{Lp}$, then the circuit will operate in CCM and vice versa.

Choosing inductor ripple current to be less than 50% of the peak inductor current would ensure operation in CCM. Using (2), with input peak voltage, V_{Lp}, ranging between 100V to 340V a graph is plotted to get the minimum value of the inductor as depicted in Fig. 4 below. From Fig. 4, it can be seen that the inductor value must be selected greater than 480μH. The inductor is then constructed according to the design procedures in [6] using the appropriately ratings and values of the circuit.

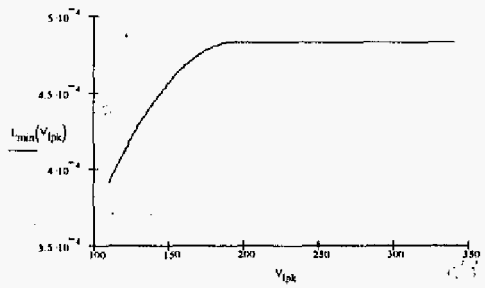

Fig. 4. Minimum inductance as a function of input peak voltage, V_{Lp}.

The next important thing in designing the power circuit part is the value of the input and output capacitors. The input capacitor would specifically used to filter the high frequency current generated by the switch at the converter, from being fed back to the mains. This is vital in order to obtain low ripple input current. For the output part, the output capacitor is used to reduce the output voltage ripple. However, the effect of the output capacitor to reduce the output ripple voltage is not significant due to the existence of the voltage feedback loop. The operation of the voltage feedback loop would be discussed in the Controller Circuit Design part. The selection of power semiconductor switches ratings must be considered as well to avoid damages to the switches itself. Appropriate selection would ensure the power semiconductor switches to withstand the voltage and current flow through it.

B. Controller Circuit Design

Average current mode control is utilized as a feedback control method in this circuit. In designing the control parameters, the most critical part is in determining the poles and zeros placement of the current and voltage loop. In this circuit, the current loop is used to regulate the input current to be near sinusoidal and in phase with the input voltage. Besides that, it must ensure a good dynamic response of the input current for sudden changes in the input voltage or output load. The voltage loop would regulate the output voltage at a constant value and it must ensure the dynamic response of the output voltage is good enough for any disturbances in the system.

Referring to Fig. 3, it can be seen that both the current and voltage loop are actually using the same error amplifier and compensator circuit. However, the placement of the pole and zero (i.e. the value of C1, C2, R1 and R2) are differed to each other. The error amplifier's transfer function with the compensator as depicted in Fig. 5 is as follows,

$$G(s)=\frac{1}{R_1C_2}\cdot\frac{s+\omega_z}{s(s+\omega_p)} \tag{3}$$

where, $\omega_z=\frac{1}{R_2C_1}$; and $\omega_p=\frac{C_1+C_2}{R_2C_1C_2}$.

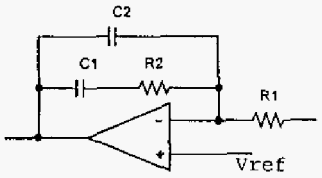

Fig. 5. Error amplifier with compensator

Equation (3) shows that the error amplifier circuits consist of one pole (ω_P), one zero (ω_Z) and an integrator (1/s). Normally, the zero would be placed lower than half of the switching frequency in order to ensure that the input current (current loop) is stable. In addition, the integrator and the pole would eliminate the steady state error and high frequency noise in the circuit respectively.

In designing the feedback controller, the current loop would operate at higher bandwidth compare with voltage loop in order to ensure better and faster dynamic response of the input current [7]. This high bandwidth can be achieved by letting the cutoff frequency located at higher frequency. In addition, the cutoff frequency of the current loop is determined by the current error amplifier gain and the control to input gain derived in [8]. The maximum current error amplifier gain is,

$$G_{CA}=\frac{V_s f_s L}{V_o R_s} \tag{4}$$

and the control to input gain is,

$$G_{CI}=\frac{R_s V_o}{V_s s L} \tag{5}$$

where, V_S is the peak voltage of the triangular wave, f_S is the switching frequency, L is the inductor, V_O is the output voltage and R_S is the sense resistor. It is known that the overall gain is zero at cutoff frequency, and it can be presented as,

$$20\log(G_{CA}G_{CI})=0 \tag{6}$$

Then solving for $G_{CA}G_{CI}$,

$$G_{CA}G_{CI}=1 \tag{7}$$

To obtain the overall gain of the circuit, equation (4) and (5) is substituted to (7). Equating $s = 2\pi f_C$ in (5), the cutoff frequency, f_C for current loop is set to $f_S/2\pi$. The zero must be placed at frequency lower than f_S, which is at half of the switching frequency while the pole is placed at frequency higher than f_S, which is at three times switching frequency.

In voltage loop design, the same error amplifier circuit with compensator is used but the pole and zero placements differ with the current loop. The aim of the voltage loop design is to regulate the output voltage at certain fixed value with large bandwidth. It must not as well filter the second harmonic components (at 100Hz) in order to avoid input current distortion. For a resistive load, the zero is placed at the control to output transfer function pole, which is at $2/(R_LC_{out})$ where R_L is the load resistor value and C_{out} is the output bulk

capacitor. The crossover frequency, f_c, for the current loop is choosed at,

$$\left(\frac{V_{in\_min}}{V_{in\_max}}\right)^2 \cdot \frac{f_{line}}{2} < f_c < \frac{f_{line}}{2} \qquad (3.29)$$

where V_{in_min} is the possible minimum RMS input voltage, V_{in_max} is the possible maximum RMS input voltage and f_{line} is the frequency of input voltage.

III. Simulation And Experimental Results

The Boost PFC circuit is constructed based on the designed parameter value and circuit specification mentioned in Table 1 and Section II. Prior to that, simulation is done in order to study the behaviors of the circuit and thus will increase the understanding of the circuit. The same situation is done in this work, which is mainly used to study the behavior of the input current, output voltage and other important parameters. Two types of circuit model are developed in this work namely the average model and the switch model.

Actually, the switch model (sometimes called cycle-by-cycle model) is performed by real device model having non-linearity characteristics, which may lead to convergence problems. This type of model shows detail results on each switching cycles and thus the overall simulation times is long due to large computational points. In average model, the device models are simplified. Thus, the non-linearity effect is eliminated which results in faster simulation times. Both models are developed in this work using PSpice. Fig 6 shows the results on output voltage, and input current waveform with respect to input line voltage for a 400W output power. Both model shows reasonable results and resemble to each other. Thus, it validates the designed parameter of the Boost PFC circuit.

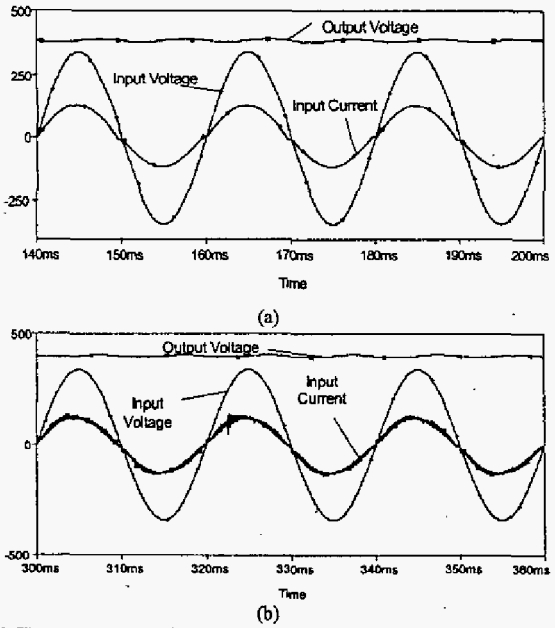

Fig. 6: The waveforms for input voltage, input current and output voltage based on simulation (a) averaged model (b) switch model.

Comparison between the simulation and experimental results for voltage and input current waveform are depicted in Fig 7 (a) and (b), for 240Vrms input and 500W output power. It can be seen that the current waveform of the simulation result and the experimental result are near a sinusoidal waveform with small distortion. The simulation and experimental current waveforms show reasonable relation.

Fig 8 shows the frequency spectrum of the current waveform based on the simulation and the experimental result.

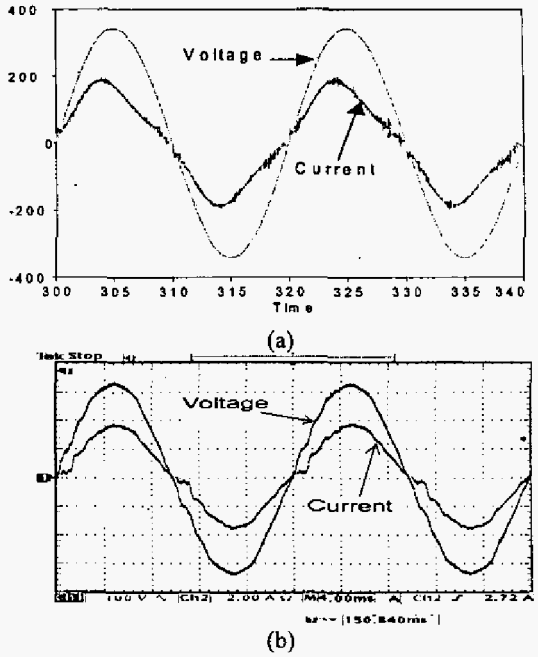

Fig 7: Input Voltage and Current waveform for 240Vrms input voltage and 500W output power; (a) simulation result, (b) experimental result.

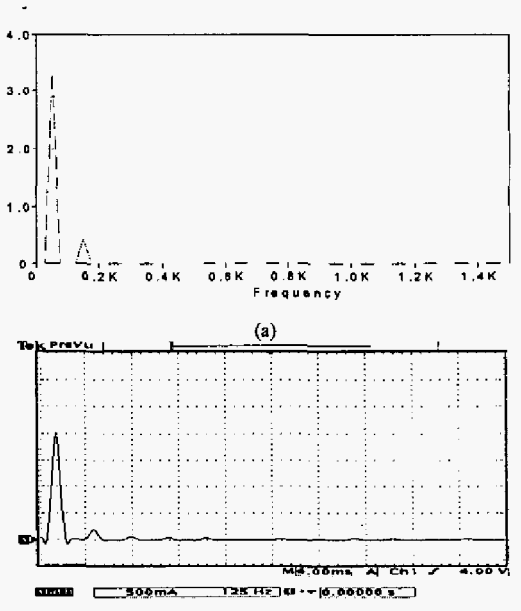

Figure 8: Frequency spectrum for 240Vrms input voltage and 500W output power; (a) simulation result, (b) experimental result.

Notice that the simulation results are shown in terms of peak current while the experimental results (measured from the oscilloscope) are shown in terms of RMS current. It can be seen that the low order harmonic contents (3rd, 5th, 7th and so on) are suppressed and some of them are eliminated.

The harmonic content for the input current are then compared with the Class A, IEC61000-3-2 Standard as shown in Fig. 9. From the figure, the entire harmonic content up to 29th order, complies with the standard.

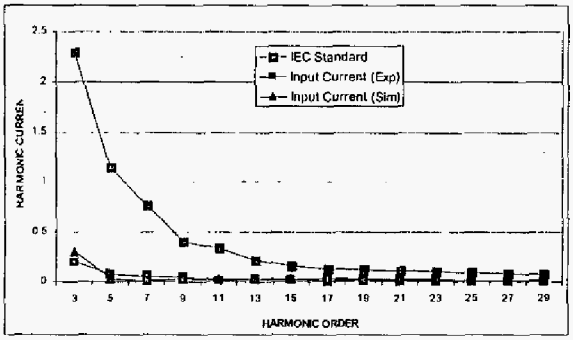

Fig 9. Comparison of the input current (for 240Vrms, 500W) with IEC61000-3-2 Standard

In Fig. 10, the results show the dynamic response of the input current and output voltage waveform when a step load change from 200W to 400W is applied. In the simulation and experimental results, the output voltage is drops but starts to recover after one cycle and then maintains the output voltage at 390Vdc. The input current for both results maintains the sinusoidal wave shape as well.

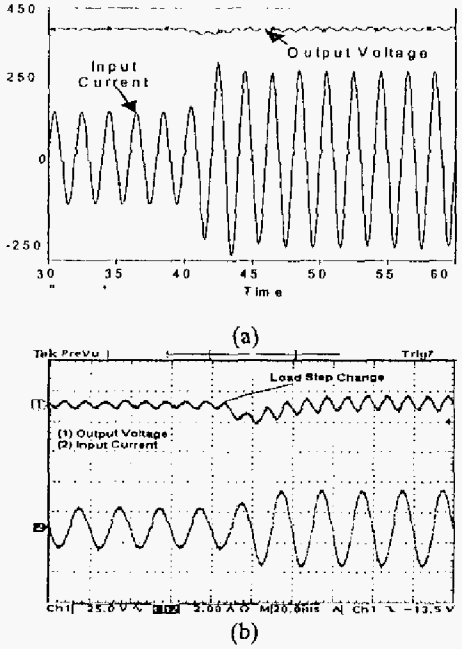

Fig. 10 Input Current and Output Voltage waveform for when the output power change from 200W to 400W; (a) simulation result, (b) experimental result.

The performances of the Boost PFC circuit for all the conditions that have been discussed above are represented in Table II. The performances of the rectifier without PFC circuit (W/o PFC) are represented as well for comparison purposes. It can be seen that for the same input voltage and output power (240Vrms, 300W), the Total Harmonic Distortion (THD) of the current are improves from 107% to 13.94% while the power factor improves from 0.654 to 0.979. Besides that, the THD of the input voltage, the efficiency improves to 89% and the output voltage ripple improves as well. For higher output power, which is at 500W, the current THD is the best at 11.61% while the power factor is 0.991. Lower output power however shows slightly better efficiency and much better output voltage ripple.

TABLE II
Performances of the Boost PFC circuit

	W/o PFC	With PFC		
	240V, 300W	240V, 300W	240V, 500W	190V, 300W
Current THD	107%	13.94%	11.61%	18.47%
Power Factor	0.654	0.979	0.991	0.983
Voltage THD	4.9%	2.3%	2.4%	2.6%
Efficiency	65.55%	89%	88.6%	89%
V_O ripple	22 V	8.6 V	14V	8.6V

IV. Conclusions

The theory of Boost Power Factor Correction (PFC) circuit as the best solution for the above-mentioned problems that arises in power electronic converters has been discussed. The results show that the Boost PFC circuit has the capability to reshape the input current to near a sinusoidal waveform, improve the power factor up to 0.99, improve the efficiency of the circuit, improve the Total Harmonic Distortion (THD) of the input current and voltage, reduce the output voltage ripple and comply with the IEC61000-3-2 Standard on Harmonic Distortion.

V. References

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