CHAPTER I

INTRODUCTION

1. Introduction

High speed data transfer between the CPU and peripherals on the PC motherboard is needed to support data traffic in future generation applications such as multimedia, games and broadband networks. The high speed I/O differential bus is developed to meet these applications. At higher speed with multi Gbits/sec, impedance mismatch between the CPU and peripherals becomes critical and limits the possible maximum throughput. This effect can be modeled as a convolution process where the I/O high speed behaves as a linear time invariant system that is defined by a channel impulse and frequency response. Since there are variations in the characteristic of the motherboards due to the fabrication and assembly process, it is desired to estimate the impulse response and frequency response of the bus. This information can be used to gage the capability of the motherboard and use it as feedback to the relevant fabrication and assembly processes. By using simulation on MATLAB and EDA tools, two candidate methods will be evaluated: PDA and correlation method using simulated channel characteristics. Robustness of both methods will be evaluated in the presence of noise and cross talk. Further evaluation will be performed on data collected from actual production test of the

high speed I/O bus. This is to evaluate the capability of the evaluated methods under actual manufacturing environment.

1.1. Background

1.1.1. High Speed I/O challenge

Computer system organization has three main components, the CPU, the memory subsystem and the I/O subsystem. Bus is a terminology used to describe the interconnecting between the components in the architecture organization. Physically, a bus is a set of wire to send the information from one component to another; the source output the components onto the bus. The destination component then inputs this data from the bus. Due to the increasing complexity of computer architecture, the bus system is much more efficient in less power consumption; less space and fewer pin than direct connect from component to component[1].

Moore's Law drives transistor scaling by 2x for every 21 months. Advanced computer system benefits from the transistor scaling allowing more processing capabilities can be achieved and higher data bandwidth is needed to support the increasing processing power (refer to Figure 1)[2]. The performance degrades if the computer spends most of its time waiting for the data. The needs of data bandwidth is even critical with the introduction of parallel processing, distribution computing system, multi core CPU and more efficient pipeline architecture while keep cache size smaller size or slower growing rate.

[1] John D. Carpinelli, "Computer System Organization and Architecture", Chapter 4, page 141, Addison Wesley, 2001
[2] Maynard Falconer, "Bus Design Boot Camp", Chapter 1, Intel Corp, 2005

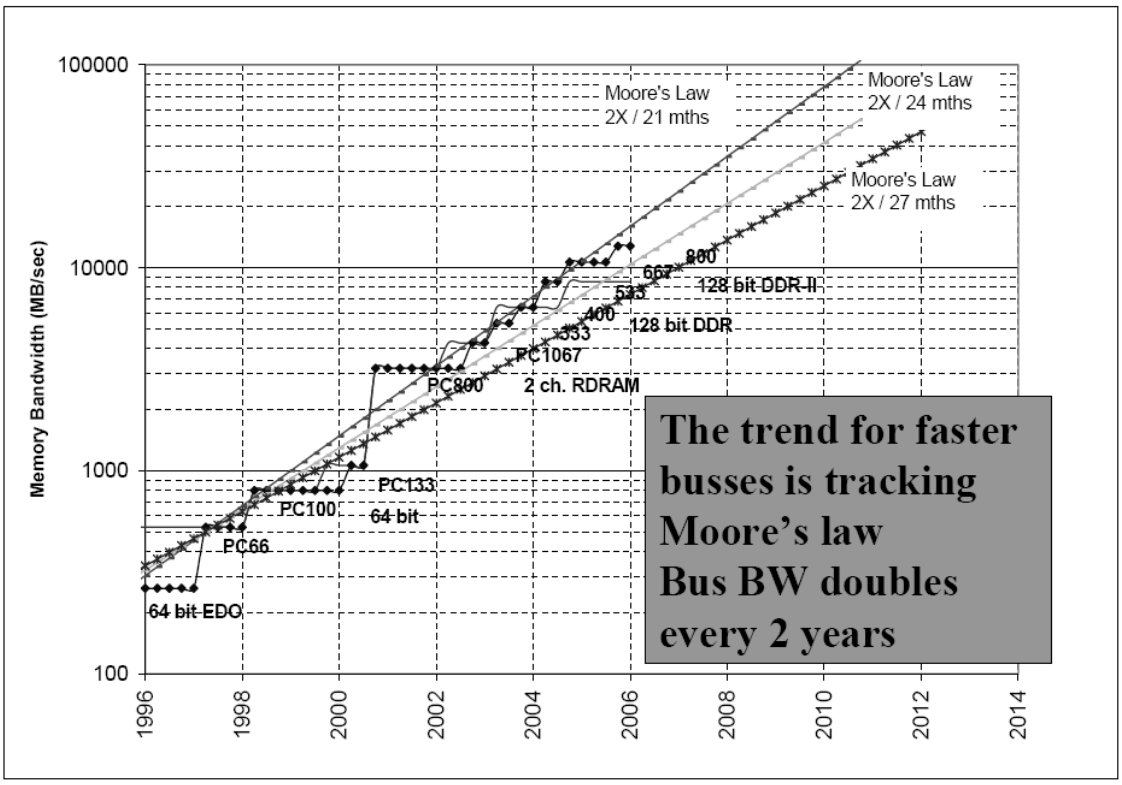
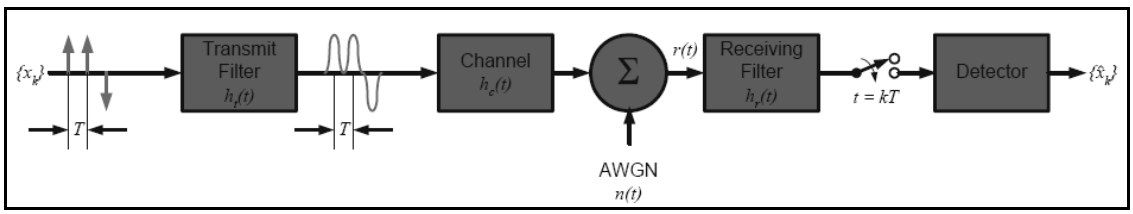


Figure 1: Relationship of Moore's Law and Bus Bandwidth (Courtesy of Intel® Corp)

1.1.2. Communication Block of Transmission Bus Channel

From communication view of point, the transmission bus channel is composed of transmitter block, bus channel block and receiver channel block as illustrated in Figure2. The source output is x(t), channel impulse response is h(t) and the receiver output is r(t) where n(t) is Additive White Gaussian noise. The receiver output is the convolution of h(t) and x(t) plus summation of n(t)[3].

$$r(t) = x(t) \otimes h(t) + n(t)$$



[3] Maynard Falconer, "Bus Design Boot Camp", Chapter 8, Intel Corp, 2005

Figure 2: Transmission line can be modeled into communication blocksets

The transmission bus channel is behaves a low pass filter where the channel loss increase with the frequency. It is due to skin effect loss and dielectric loss. Instead of amplitude loss, the channel also suffers from phase distortion as Figure 3. Phase distortion is due to the channel length, dielectric length change, inductance change over the frequency. As the result, the receiver has closed Eye Diagram[4].

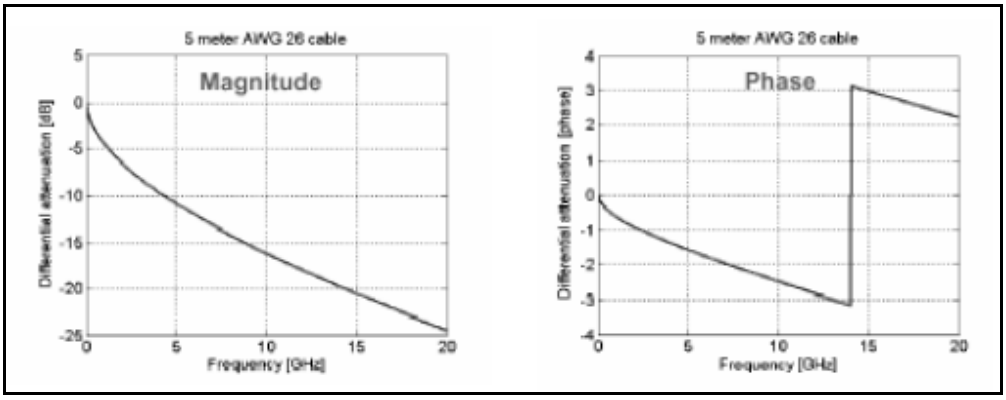


Figure 3: Frequency response of transmission line behaves like a low pass filter

Equalizer is implemented to improve the signal quality by introducing the inverse characteristic of the transmission bus channel so that both equalizer and channel can cancel each other to retrieve the original transmitting data as Figure 4. The equalizer, $C(f) = H^{-1}(f)$, can be placed at the transmitter, receiver or both. The equalizer can be an analog passive high pass filter or discrete FIR filter. Some popular discrete FIR filter used are pre-emphasis (used in transmitter), Discrete Linear Equalizer (DLE) and Decision Feedback Equalizer (used at receiver) or advance adaptive equalizer. No matter which equalizer is used, the $H(f)$ must be characterized.

[4] Eye Diagram is electrical specification for transmitting or receiving signals. Signal is considered fail to the specification when it breaks the boundary of the Eye Diagram, where the Eye Diagram looks close.

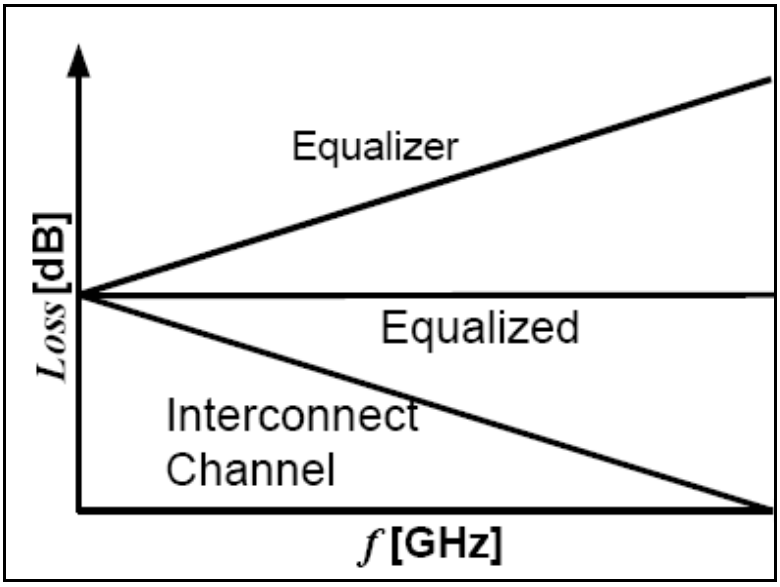


Figure 4: Implementation of equalizer aims to resolve the lossy transmission line

1.2. Objective

The research aims to evaluate the performance and parameters of the proposed correlation method in transmission bus channel characterization. The evaluation includes comparison with pulse response method and Scattering parameter measurement on robustness, algorithm complexity, effectiveness, accuracy and immunity to the environment noise. An equalizer based on the correlation algorithm is build to evaluate the performance in the transmission bus channel system.

1.3. Scope

The analysis is done using SPICE and MATLAB focusing on behavior level simulation excluding any RTL level simulation. The study is based on offline simulation and the measurement can only be done depending on the hardware readiness. The study focuses on electrical parameters and assumes the transmission bus channel is a time invariant system.

1.4. Problem Statement

High speed I/O bus design is always hungered due to its significant impact to the system performance. The challenge consists of large number of process variable, effecting high volume manufacturing, complex computer organization and cost impact. Parallel source synchronous bus which it used to be dominant Bus interconnect, cannot simply increase its bandwidth by scaling the number of bus size and bus speed due to the ISI (Inter Symbol Interfering) effect, increasing pin count, more variables, larger space and more tighten timing requirement. Therefore these buses such as PCI migrate to PCIe, a serial differential bus for the following advantages: noise immunity, fewer pin counts, less routing space and cost effective. Due to the limited bandwidth of transmission media, high data rates on printed circuit boards and communication networks impose significant signal integrity degradation, equalization techniques must be included in the transmitter and receiver circuitry to compensate for the lossy characteristics of the transmission channel[5]. Conventional method such as Scattering Parameters measurement cannot characterize the bus in active operation condition thus an active bus channel characterization is proposed to resolve the problem

[5] M. Cases, D. N. de Araujo, E. Matoglu, "Electrical Design and Specification Challenges for High Speed Serial Links", 2005 Electronics Packaging Technology Conference