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CHAPTER I

INTRODUCTION

1.1 Introduction

This chapter covers the material on project background, project objectives, project scope and the thesis outline. Introduction on this chapter covers about the OFDM implementation method and description on the available hardware for implementation. The problem statement of the project will also be carried out in this chapter.

With the rapid growth of digital communication in recent years, the need for high-speed data transmission has been increased. The mobile telecommunications industry faces the problem of providing the technology that be able to support a variety of services ranging from voice communication with a bit rate of a few kbps to wireless multimedia in which bit rate up to 2 Mbps. Many systems have been proposed and OFDM system has gained much attention for different reasons. Although OFDM was first developed in the 1960s, only in recent years, it has been recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-speed digital signal processing. This method has only recently become available with reasonable prices versus performance of hardware implementation.

Since OFDM is carried out in the digital domain, there are several methods to implement the system. One of the methods to implement the system is using ASIC (Application Specific Integrated Circuit). ASICs are the fastest, smallest, and lowest power way to implement OFDM into hardware. The main problem using this method is inflexibility of design process involved and the longer time to market period for the designed chip.

Another method that can be used to implement OFDM is general purpose Microprocessor or Micro Controller. Power PC 7400 and DSP Processor is an example of microprocessor that is capable to implement fast vector operations. This processor is highly programmable and flexible in term of changing the OFDM design into the system. The disadvantages of using this hardware are, it needs memory and other peripheral chips to support the operation. Beside that, it uses the most power usage and memory space, and would be the slowest in term of time to produce the output compared to other hardware.

Field-Programmable Gate Array (FPGA) is an example of VLSI circuit which consists of a “sea of NAND gates” whereby the function are customer provided in a “wire list”. This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility. An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

1.2 Project Background

This project is the continuation from the previous master student project which entitled “Design of an OFDM Transmitter and Receiver Using FPGA” by Loo Kah Cheng. The works involved from previous student is focused on the design of the core processing block using 8 point Fast Fourier Transform (FFT) for receiver and 8 point Inverse Fast Fourier Transform (IFFT) for transmitter part. The implementation of this design into FPGA hardware is to no avail for several reasons encountered during the integration process from software into FPGA hardware.

The project was done up to simulation level using Max+Plus II software and only consists FFT and IFFT processing module. Some of the problem encountered by this student is that the design of FFT and IFFT is not fit to FPGA hardware. The design used a large number of gates and causes this problem to arise. Logic gates are greatly consumed if the number of multiplier and divider are increase. One method to overcome this problem is by decreasing the number of multiplier and divider in the VHDL design.

Beside that, the design does not include control signal which cause difficulties in controlling the data processing in FFT or IFFT module. The control signal is use to select the process executed for each computation process during VHDL design. As a result, the design is not applicable for hardware implementation in the FPGA development board. New design is required to overcome this problem. Since the design is not possible to use, this project will concentrate on designing the FFT and IFFT module which can be implement in the dedicated FPGA board. To ensure that the program can be implemented, the number of gates used in the design must be small or at least less than the hardware can support. Otherwise the design module is not able to implement into the dedicated bord.

1.3 Project Objective

The aim for this project is to design a baseband OFDM processing including FFT (Fast Fourier Transform) and IFFT (Inverse Fast Fourier Transform), mapping (modulator), serial to parallel and parallel to serial converter using hardware programming language (VHDL). These designs were developed using VHDL programming language in design entry software.

The design is then implemented in the Apex 20k200EFC484-2X FPGA development board. Description on the development board will be carried out at methodology chapter.

In order to implement IFFT computation in the FPGA hardware, the knowledge on Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) programming is required. This is because FPGA chip is programmed using VHDL language where the core block diagram of the OFDM transmitter implements in this hardware. The transmitter and receiver are developed in one FPGA board, thus required both IFFT and FFT algorithm implemented in the system.

Several tool involved in the process of completing the design in real hardware which can be divided into two categories, software tools and hardware tool. The software which include in this project is using CAD tools software, VHDL module generator v.109, Synopsis FPGA Express v3.31.4719 and Altera Max+plus II. While the hardware use is UP1 board of ALTERA Flex 10K FPGA chip.

1.4 Project Scope

The work of the project will be focused on the design of the processing block which is 8 point IFFT and FFT function. The design also includes mapping block, serial to parallel and parallel to serial block set. All design need to be verified to ensure that no error in VHDL programming before being simulated. Design process will be described on the methodology chapter.

The second scope is to implement the design into FPGA hardware development board. This process is implemented if all designs are correctly verified and simulated using particular software. Implementation includes hardware programming on FPGA or downloading hardware design into FPGA and software programming.

Creating test vector program also include in the scope of the project. Test vector is a program developed using c programming and is intended as the input interface for user as well as to control data processing performed by the hardware. Creating this software required in understanding the operation of the FFT and IFFT computation process. Further chapter will discuss the method on developing the program from mathematical algorithm into behavioral synthesis.

The last works is to verify the result of the output for each module which has been developed. Test vector program is used to deliver the computation result if input value is provided by the user. These computation values should be verified and tested to ensure the correctness of the developed module. Appropriate software is used to compare the computation performed by the FPGA hardware with the software. There are several test performed to the design modules and the test process also will be discuss in the methodology chapter.

1.5 Project Outline.

The project is organized into six chapters, namely introduction, literature review, methodology, hardware design, software design, result, analysis and discussion, and conclusion.

Chapter 1 discusses the general idea of the project which covers the introduction, project objective, project background and scope of the project.

Chapter 2 shows the literature review of the OFDM system, basic principles of OFDM system, advantages and disadvantages of OFDM system, and lastly is the application of the OFDM in recent technology.

Chapter 3 describes the methodology of the project. The project is divided into several stages which basically include study relevant topics, design stage, implementation stage and testing stage. Further description will cover in this chapter.

Chapter 4 explains regarding the hardware design which is developed from mathematical equations. The chapter also includes on the theoretical part of FFT and IFFT and describes until the hardware design.

Chapter 5 enlightens the software design process involved in the project. This part basically discussed on the works involved to download the modules into FPGA board. Besides that, development of test vector which is used to test the modules will be carried out in this chapter.

Chapter 6 shows the results obtained from the FPGA hardware. The results obtained are captured and show in the figure as an examples. Further results will be shown in the tables.

Chapter 7 describes on the analysis and discussion of the result. Some results which gives error output will be discussed in this chapter and provide the reason behind the problem occurred.

Chapter 8 consists of the conclusion and proposed works to enhance the project in the future.