A New Hybrid Multilevel Inverter Topology with Harmonics profile improvement

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Abstract - **A new hybrid multilevel inverter topology with harmonics profile improvement is presented in this paper. From the literature, it is agreed that hybrid multilevel inverter with its DC sources configured in trinary fashion presents the largest output levels and the lowest Total Harmonics Distortion (THD) percentage. However the output contains low order harmonics due to the impossibility of modulating all adjacent voltage levels at high frequency. With this proposed topology, all adjacent voltage levels are possible to be modulated at high frequency. As a result, the output voltage waveform presents better harmonics profile. The proposed topology and its modulation scheme are presented and verified with simulation results.**

Keywords: voltage source inverter; cascaded multilevel inverter; harmonics improvement.

I. INTRODUCTION

Multilevel voltage source inverter (VSI) has been recognized as an important alternative to the normal two levels VSI, especially in high power application. Using multilevel technique, the output voltage amplitude is increased, switching devices stress is reduced and the overall harmonics profile is improved. Several multilevel topologies are reported [1, 2, 3], and the most popular topology is Cascaded Multilevel Inverter (CMI). It offers several advantages compared to other topologies such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, this topology becomes highly cumbersome because the number of power devices is increases.

Then, hybrid multilevel inverter is proposed. This topology generates larger number of output levels with the same number of power devices of the Cascaded Multilevel Inverter with equal DC voltage sources. It consisted of a series-connected full-bridge inverter module with its dc voltage sources is configured in geometric progression e.g. trinary and binary. Moreover, different types of switching devices are used and modulated differently to reduce voltage stress on the devices and switching losses.

From the literature, it is agreed that trinary hybrid multilevel inverter offers larger number of output voltage level and smaller THD percentage compared to binary hybrid multilevel inverter [4]. However, the output contains low order harmonics, due to the impossibility of modulating all adjacent voltage levels at high frequency.

Thus, this paper proposed a new hybrid multilevel inverter topology, so that it is possible to modulate at high frequency among all adjacent levels of output waveform. As a result, the output voltage presents a better harmonics profile.

II. THE PROPOSED HYBRID MULTILEVEL INVERTER TOPOLOGY

Fig. 1 shows M modules of the proposed hybrid multilevel topology. The topology is constructed of a series –connected full bridge inverter module and is separated into two sets of inverters, namely Low Frequency (LF) inverter and High Frequency (HF) inverter. As shown in Fig. 1, HF inverter consist a single full bridge inverter with 1aV dc source while Low Frequency (LF) inverter consists of (M-1) full bridge inverters with their dc sources are configured in geometric progression for example: trinary and binary fashion.

The number of voltage level (N) produced is given by (1):

$$N=2\sigma+3 \qquad (1)$$

Where σ :

$$\sigma = \sum_{1}^{M-1} 3^{(n-1)} \quad n = (1,2..) \text{ for trinary configuration}$$

or

$$\sigma = \sum_{1}^{M-1} 2^{(n-1)} \quad n = (1,2..) \text{ for binary configuration}$$

III. THE MODULATION SCHEME

The output waveform is a combination of stepped voltage waveform synthesized in LF inverter and a high frequency

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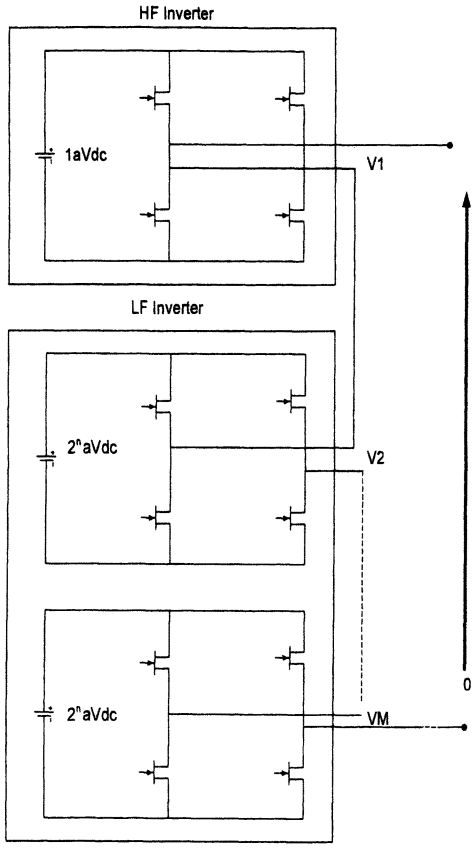

Figure 1. *M modules of the proposed hybrid multilevel inverter*

variable pulse width modulation waveform synthesized in HF inverter. TABLE 1 and TABLE 2 show the switching combinations to synthesize specific voltage levels for the proposed topology with LF inverter's dc source is configured in binary and trinary, respectively. From TABLE 1, it can be seen that several specific levels for binary configuration could be generated using more than a single switching combination.

Fig. 2 shows the block diagram of the control circuit for the modulation scheme utilized to determine the switching signal for all inverter modules. From the figure, it shows that the reference signal (pure sinusoidal with frequency f_s and amplitude A_s) is the command signal for the 1st comparator block. The signal is compared with the HF Inverter's dc voltage factor, which is unity. If the command signal is greater than unity, the output must be equal to unity, otherwise the output is set to zero.

The command signal of the 2nd comparator block is the difference between the command signal of the 1st comparator block and the output of the 1st comparator block. This command signal is then compared again with HF Inverter's dc voltage factor. In the same way that presented for the 1st block, the output is synthesized from the comparison of these two signals. This process is repeated until reach the $(\sigma+1)^{th}$ comparator block. The command signal of the $(\sigma+1)^{th}$ comparator block is compared with a train of triangular waveform with frequency f_c, resulting the high frequency pulse width modulation waveform. Thus, the modulation index can be determined by:

$$m_i = \frac{f_c}{f_s} \tag{2}$$

The modulation ratio for the proposed scheme also can be given as:

$$m_a = \frac{A_s}{\sigma + 1} \tag{3}$$

TABLE 1. SWITCHING COMBINATIONS FOR THE PROPOSED TOPOLOGY WITH LF INVERTER'S DC SOURCE IS IN BINARY CONFIGURATION.

	1V	2V	2V	3V	3V	4V	4V	5V	6V	6V	7V	8V
HF (1aV)	1	1	1	1	1	0	1	1	1	1	1	1
LF1 (1aV)	0	1	-1	0	0	0	1	0	1	-1	0	1
LF2 (2aV)	0	0	1	1	-1	0	1	0	0	1	1	1
LF3 (4aV)	0	0	0	0	1	1	0	1	1	1	1	1

TABLE 2. SWITCHING COMBINATIONS FOR THE PROPOSED TOPOLOGY WITH LF INVERTER'S DC SOURCE IS IN TRINARY CONFIGURATION.

	1V	2V	3V	4V	5V	6V	7V	8V	9V	10V	11V	12V	13V	14V
HF (1aV)	1	1	1	1	1	1	1	1	1	1	1	1	1	1
LF1 (1aV)	0	1	-1	-1	1	-1	0	1	-1	0	1	-1	0	1
LF2 (3aV)	0	0	0	1	1	-1	-1	-1	0	0	0	1	1	1
LF3 (9aV)	0	0	0	0	0	1	1	1	1	1	1	1	1	1

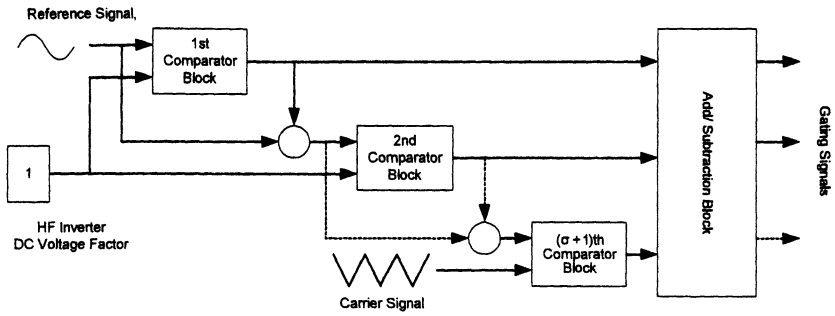

Figure 2. *Block diagram of gating signals generator*

Then, all the outputs of comparison blocks are fed forward to the addition/subtraction block. Here, the signals are manipulate to produce the desired switching signals for each inverter module. Fig. 3 shows the reference signals for each inverter modules for the proposed topology.

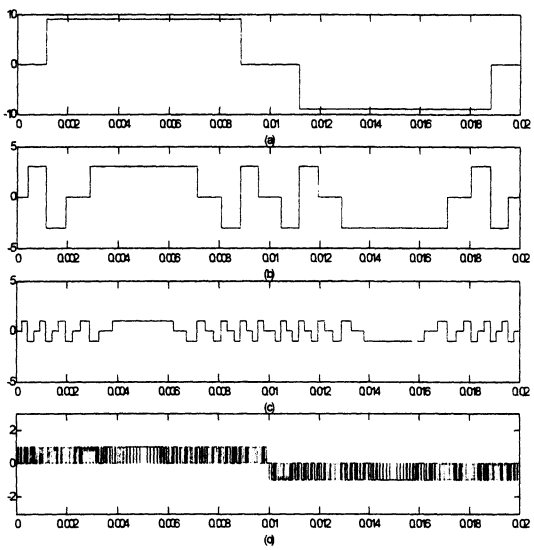

Figure 3. *Reference signals for 4 inverter modules with LF inverter's dc source are in trinary configuration. (a) Reference signal for LF1 (b) Reference signal for LF2 (c) Reference signal for LF3 (d) Reference signal for HF inverter.*

IV. SIMULATION RESULT

Figure 4 and 5 present output voltage waveform for the proposed topology with LF inverter's dc source is configured in binary (17-level output) and trinary (29-level output) with their harmonic spectrums, respectively. For both dc configurations, as can be seen from the figures, all adjacent levels of their output waveforms are modulated in high frequency. As a result, better harmonic profile is obtained without the presence of low-order harmonics in their waveform harmonics spectrums.

Finally, it can be concluded that with the proposed topology, better harmonics profile can be obtained. The Total Harmonic Distortion (THD) of the output voltage using the proposed topology with its LF inverter's dc source is configured in trinary yields 4.02%, while with binary configuration yields 7.02%. It was also found that for different m_i values, different numbers of output levels are obtained. Fig. 6 summarized the output levels obtained according to m_i for M=4.

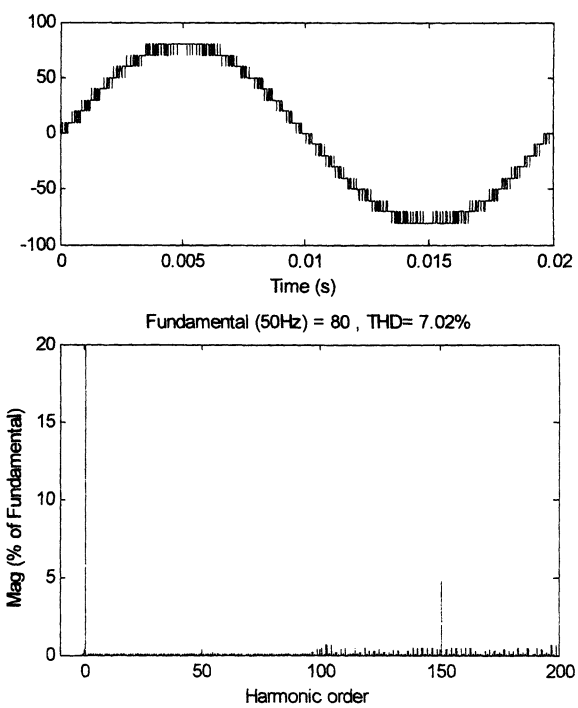

Figure 4. *Output waveform for LF inverter's dc source is configured in binary and its harmonics spectrum.*

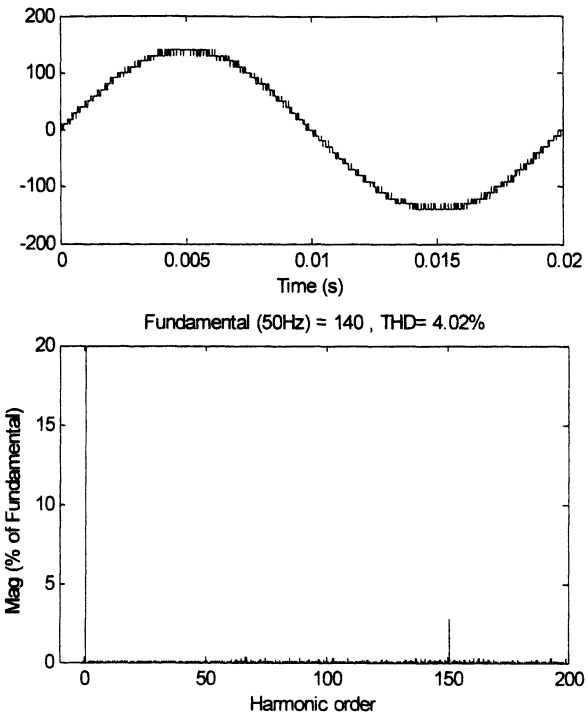

Figure 5. *Output waveform for LF inverter's dc source is configured in trinary and its harmonics spectrum.*

V. CONCLUSION

This paper presents a new hybrid multilevel inverter topology for harmonics profile improvement. It is agreed that hybrid multilevel inverter with its DC sources configured in trinary fashion presents the largest output levels and the smallest Total Harmonics Distortion (THD) percentage. However the output contains low order harmonics, due to the impossibility of modulating all adjacent voltage levels of output waveform at high frequency. With this proposed topology, high frequency modulation among all adjacent voltage levels can be made possible. As a result, the output voltage waveform presents better harmonics profile. It was also found that for different values of m_i, different numbers of output levels are obtained.

VI. REFERENCES

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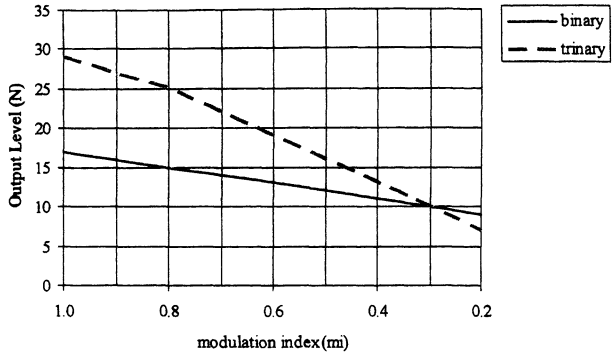

Figure 6. *Output level (N) obtained according to modulation index for M=4*