

# A 4.5-5.8 GHz Differential LC VCO using 0.35 $\mu\text{m}$ SiGe BiCMOS Technology

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**Abstract.** In this paper, design and realization of a 4.5-5.8 GHz,  $-G_m$  LC voltage controlled oscillator (VCO) for IEEE 802.11a standard is presented. The circuit is implemented with 0.35  $\mu\text{m}$  SiGe BiCMOS process that includes high-speed SiGe Heterojunction Bipolar Transistors (HBTs). A linear, 1300 MHz tuning range is measured with accumulation-mode varactors. Fundamental frequency output power changes between -1.6 dBm and 0.9 dBm, depending on the tuning voltage. The circuit draws 17 mA from 3.3 V supply, including buffer circuits leading to a total power dissipation of 56 mW. Post-layout phase noise is simulated -110.7 dBc/Hz at 1MHz offset from 5.8 GHz carrier frequency and -113.4 dBc/Hz from 4.5 GHz carrier frequency. Phase noise measurements will be updated in the final manuscript. The circuit occupies an area of 0.6 mm<sup>2</sup> on Si substrate including RF and DC pads.

**Index Terms**— VCO, SiGe BiCMOS, WLAN, Differential tuning, RFIC.

## I. INTRODUCTION

5-6 GHz Unlicensed National Information Infrastructure (UNII) band has been authorized in many countries for WLAN high-speed applications. As the numbers of products grow and the types of the products evolve, high performance oscillators with low phase noise, low power dissipation, satisfactory output power and tuning range increase their importance in today's wireless applications [1].

Voltage controlled oscillators (VCOs) are utilized in a number of applications as the sources of signal generation as a part of data or clock recovery systems. Among these applications of VCOs, design for wireless communications has more stringent specifications than for other applications. IEEE 802.11a standard uses Orthogonal Frequency Multiplexing (OFDM) based modulation scheme which is more sensitive to phase noise compared to single carrier modulation schemes. In order to meet the requirements for IEEE 802.11a standard, the phase noise of the VCO should be lower than -110 dBc/Hz at 1MHz offset from the carrier frequency [2].

Tuning Range is also an important performance parameter and has been a major problem for VCOs in CMOS or BiCMOS technologies. Due to the limited tuning range of p-n junction varactors and inversion MOS varactors, accumulation mode is generally preferred [3].

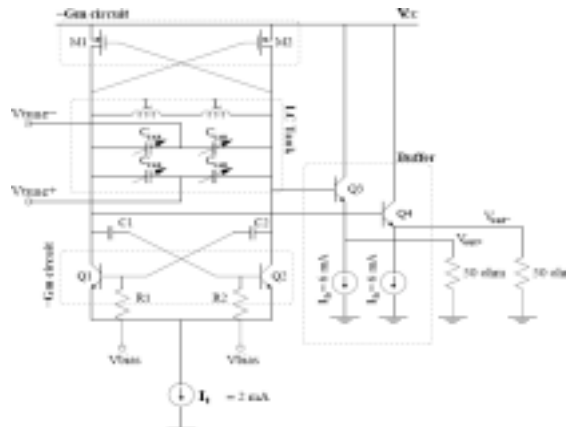
Another issue in VCO design is high varactor sensitivity. A high  $C_{\text{max}}/C_{\text{min}}$  ratio over a low voltage tuning range degrades the phase noise performance. Differential tuning provides a simple but effective solution to avoid the drawbacks of this effect [4]. Output power and power dissipation are other

parameters determining the performance of VCOs. A well-designed VCO should send enough power to its output to drive the mixer and should dissipate the minimum power for a longer battery lifetime.

## II. VCO DESIGN

A VCO meeting the specifications of IEEE 802.11a standard may be implemented utilizing various technologies. Previous works include realizations with GaAs HBT, SiGe BiCMOS, Si CMOS and Silicon-on-insulator (SOI) CMOS. Among these technologies SiGe BiCMOS technology leads others from an application point of view. This is because it combines the cost and integration advantages of Si material system with the performance advantages of SiGe HBTs. Considering topologies, RF VCOs can be realized as resonator (LC) based oscillators, ring oscillators or multivibrator oscillators. Among the three topologies, LC based oscillators are most prominent ones due to their relatively low phase noise [5].

The technology used in this design is a 0.35  $\mu\text{m}$  4-metal double-poly SiGe BiCMOS process with a thick metal option. It includes high-speed SiGe HBTs with 59 GHz and 63 GHz  $f_t$  and  $f_{\text{max}}$  values respectively. HBTs with two base contacts are utilized to reduce the base resistance, which is the critical source of noise in bipolar transistors. The topology for the VCO is a differential  $-G_m$  LC configuration, given in Figure 1. It consists of three parts, namely the  $-G_m$  circuit (Q1, Q2, M1, and M2), the LC tank (L and  $C_{\text{var}}$ ) and the buffer (Q3 and Q4). The PMOSs together with the npn HBTs in the  $-G_m$  part are utilized to obtain additional negative resistance.



**Figure 1** VCO Schematic

This HBT-PMOS cross-coupled pair brings two important

improvements over the HBT-only structure; first, it has bigger tank amplitude for a given current reducing the power dissipation; second, it can be optimized to have more symmetrical output wave leading to a better phase noise.

The main difference of the circuit from the conventional VCOs is the differentially-tuned accumulation-mode MOS varactors in the LC tank. Differential tuning provides a solution to avoid the drawbacks of high varactor sensitivity ( $k_v$ ) effect. A high  $C_{max}/C_{min}$  ratio over a low voltage tuning range, meaning high varactor sensitivity, degrades the phase noise performance as described by the modified Leeson's Formula [4];

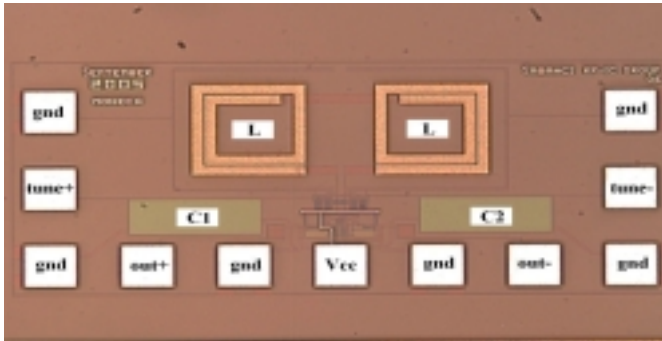
$$L(\Delta f, k_v) = 10 \log \left\{ \left( \frac{f_0}{2Q\Delta f} \right)^2 \left[ \frac{FkT}{2P_s} \left( 1 + \frac{f_c}{\Delta f} \right) \right] + \left( \frac{k_v v_n}{2k_{LC}\Delta f} \right)^2 \right\} \quad (3)$$

Here,  $f_0$  is the frequency of oscillation,  $Q$  is the quality factor,  $\Delta f$  is the frequency offset from the carrier,  $F$  is the noise factor,  $k$  is the Boltzmann's constant,  $T$  is the temperature,  $P_s$  is the RF power produced by the VCO,  $f_c$  is the Flicker noise corner frequency,  $v_n$  is the common mode noise voltage and  $k_{LC}$  is a constant that is a function of  $L$  and  $C$  of the resonator. Utilizing differentially-tuned varactors at the tank circuit enables one to suppress common-mode noise such as flicker noise, resulting in a better phase noise performance in wide tuning range oscillators.

Buffer is the link between the output stage of the VCO core and the output port. It should provide adequate power to the output 50-Ohm termination impedances as well as adequate isolation between the output and the VCO core. The input impedance of the buffer must be high enough to prevent the measurement equipment from degrading the  $Q$ -factor of the LC tank.

### III. EXPERIMENTAL RESULTS

Micrograph of the fabricated VCO is shown in Figure 2. The layout is symmetric to minimize the even order distortion of the output waveform. The most critical nodes are the positive and negative oscillation nodes which have to be carefully designed to prevent capacitive and resistive parasitic effects. The connections of these nodes is done by the top metal layer of the process to reduce the capacitance with substrate.

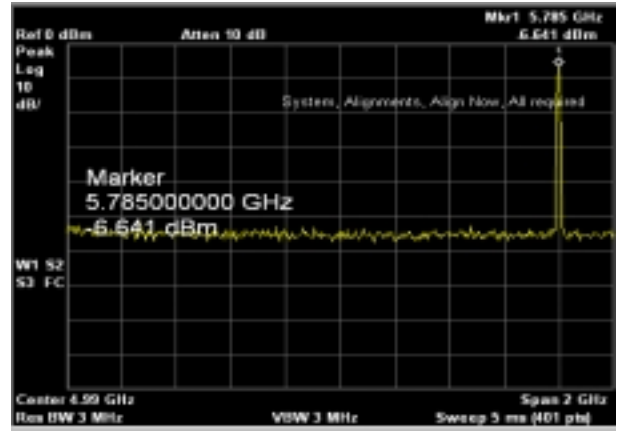


**Figure 2** VCO Micrograph

Again for the oscillation node, Metal-Insulator-Metal

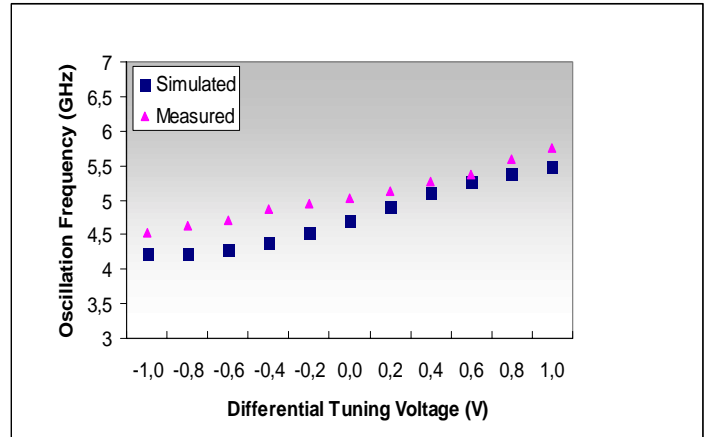
(MIM) capacitances are utilized due to their higher quality factor and linearity. Corners and sharp turns in the RF path are avoided to prevent the degradation of RF signal. The whole circuit has dimensions of 1.16mm\*0.52mm occupying an area of 0.6 mm<sup>2</sup> on Si die including RF and DC pads.

Measurements of the naked prototype VCO are accomplished by Karl-Suss RF probe station and measurement data is obtained from Agilent E4407B Spectrum analyzer. The highest frequency obtained is 5.78 GHz with a +1V differential tuning voltage (**Figure 3**). The output power of -6.6 dBm is measured with the additional losses from the connecting cable and the attenuator at the spectrum analyzer input. Without losses, 1 dBm output power can be obtained from a single output of the differential circuit. Additionally with a differential measurement setup, the output power will reach to 4 dBm.



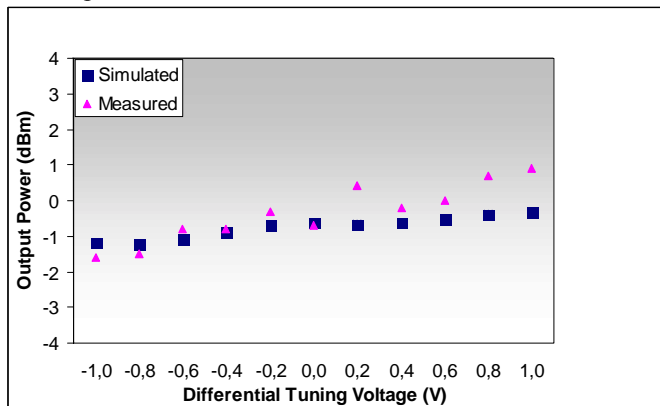
**Figure 3** Spectrum of the free-running VCO

According to measurement results, the circuit can be tuned 1.3 GHz changing the differential tuning voltage  $\pm 1V$  over 1.5 V DC (Figure 4). This means an effective change of the tuning voltage from 0.5 V to 2.5 V. Choosing the zero-tuning voltage at about  $V_{CC}/2$  for a differentially-tuned VCO; one is able to get higher voltage headroom for tuning the circuit. In addition, it decreases the oscillator sensitivity. So the effect of high varactor sensitivity, which degrades phase noise, is reduced.



**Figure 4** Simulated vs. measured tuning range of the VCO Output power of an oscillator should be high enough so that

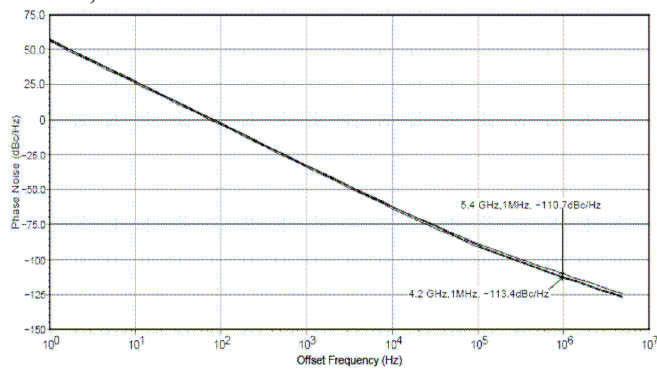
it can deliver enough power to the following stage in the transceiver architecture, the mixer. At the output of the oscillator, fundamental frequency power changes between -1.6 dBm and 0.9 dBm when swept within the corners of the tuning voltage. Measured carrier frequency output power can be observed in Figure 5. The difference in the power levels for different tuning voltages can be explained as the result of wide frequency coverage. The power levels for the whole tuning range can be equalized; however, this approach is avoided since it will increase circuit complexity and power consumption.



**Figure 5** Simulated vs. measured output power of the VCO

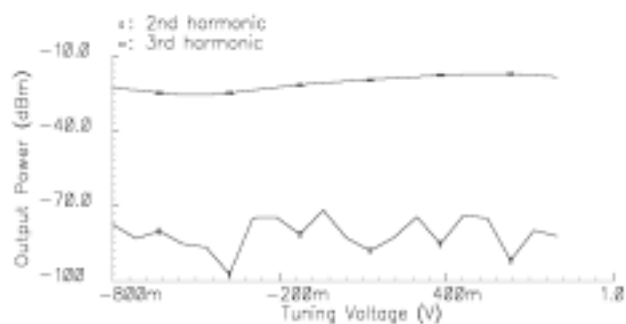
Total current drawn from the 3.3 V supply is 17 mA, which means a DC power consumption of 56 mW.

The measurements of phase noise as well as second and third harmonic levels have not been completed yet. This work is ongoing and will be uploaded to the final manuscript. According to post-layout simulations, phase noise at 1MHz offset from 5.8 GHz carrier is -110.7 dBc/Hz and it is -113.4 dBc/Hz from 4.5 GHz carrier, as shown in Figure 6. Both of these values exceed the phase noise specification of the standard, which is -110 dBc/Hz for the same offset.



**Figure 6** VCO phase noise (post-layout simulations)

Again, according to post-layout simulations, expected second and third harmonics levels are -82 dBm (87.5 dBc) and -21 dBm (26.5 dBc), respectively (Figure 7). The remarkable suppression in the second harmonic is due to differential circuit topology that rejects the common mode noise and provides a linear tuning across the covered frequency band.



**Figure 7** Second and third harmonic levels (post-layout simulations)

#### IV. CONCLUSION

A fully integrated 4.5-5.8 GHz VCO for IEEE 802.11a standard is designed and fabricated with 0.35 $\mu$ m SiGe BiCMOS technology. The VCO can be tuned using a DC voltage of 0.5 to 2.5 V for a bandwidth of 1.3 GHz. Output power between -1.6 dBm and 0.9 dBm can be obtained by changing the tuning voltage  $\pm$ 1 V over a DC voltage of 1.5 V. The circuit draws 17 mA DC current from 3.3 V supply including the buffers leading to a power consumption of 56 mW. The dimensions of the fabricated chip are 0.6 mm<sup>2</sup>.

Based on the post-layout simulations, typical second and third harmonics levels are -82 (87.5 dBc) dBm and -21 (26.5 dBc) dBm, respectively. Phase noise of -110.7 to -113.4 dBc at 1 MHz offset can be obtained through the frequency of interest. The measurement results of these data will be uploaded to the final manuscript.

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