



PROGRAM STUDI

S1 SISTEM KOMPUTER

UNIVERSITAS DIPONEGORO

MEMORY

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Istilah/Jenis Semikonduktor Memori

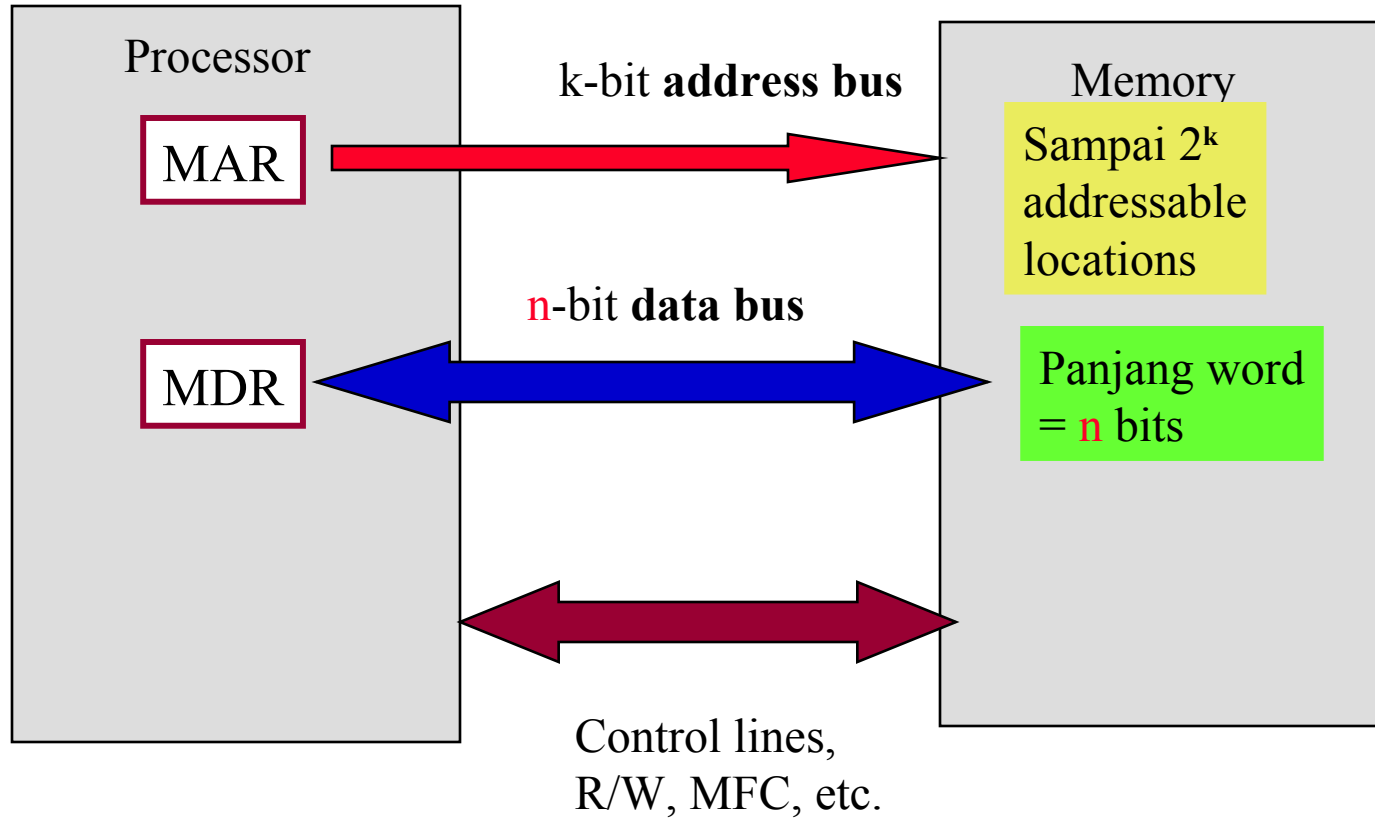
RAM	--Random Access Memory	time taken to access any arbitrary location in memory is constant
SRAM	--Static RAM	A RAM chip design technology (see later)
DRAM	--Dynamic RAM	A RAM chip design technology (see later)
ROM	--Read Only Memory	ROMs are RAMs with data built-in when the chip is created. Usually stores BIOS info. Older uses included storage of bootstrap info
PROM	--Programmable ROM	A ROM which can be programmed
EPROM	--Erasable PROM	A PROM which can be programmed, erased by exposure to UV radiation
EEROM	-- Electrical EPROM	A PROM programmed & erased electrically

Masih tentang Istilah ...

Tambahan istilah:

SIMM	Single In-Line Memory Module A packaging technology (single 32-bit data path)
DIMM	Dual In-Line Memory Module A packaging technology (dual 32-bit data paths)
FPM RAM	Fast Page-Mode RAM An older technology capable of about 60ns cycle time
EDO RAM	Extended-data-out RAM More modern FPM RAM, exploiting address coherency (see cache`later) capable of about 20ns access speed
SDRAM	Synchronous DRAM Synchronous Dynamic RAM; allows access speeds as low as about 10ns PC 100, PC133, PC2100, PC2600 => memory product you can buy

Connection: Memory - Processor



Konsep Dasar

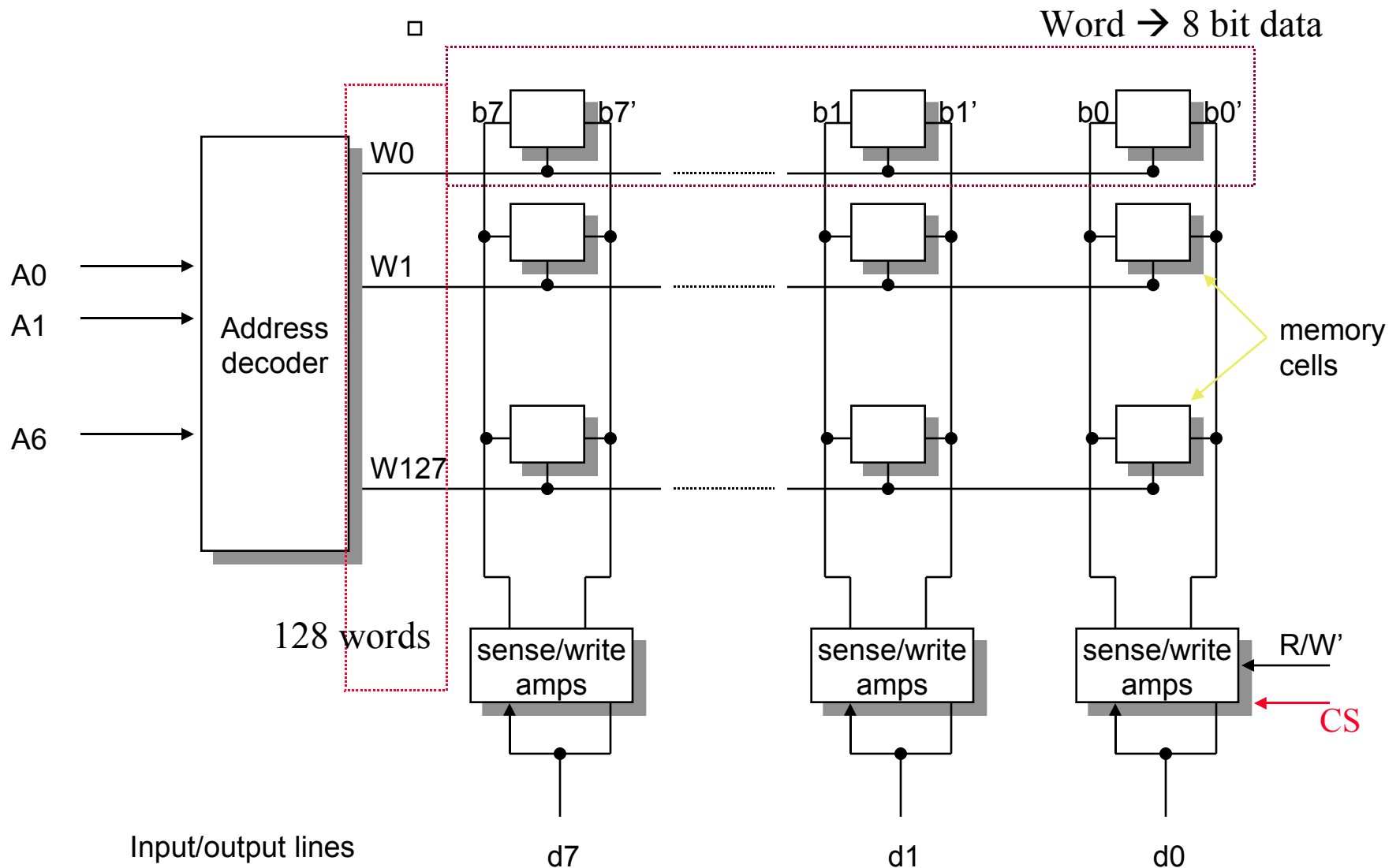
◦ Memory: akses per byte

- Transfer dilakukan per-word (cepat, kelipatan bytes)
- Misalkan: 32-bit komputer => address 32 bit
Kemampuan addressing: $2^{32} = 4 \text{ Gbytes}$
- Jika transfer data per-word: 32 bit (data bus) => 4 bytes
- Bytes mana yang diakses dari kemungkinan word tsb?
 - Perlu 2 bits untuk menentukan bytes yang mana dari word
 - Sisa bit: 30 bits digunakan untuk address word

Organisasi Internal Memori

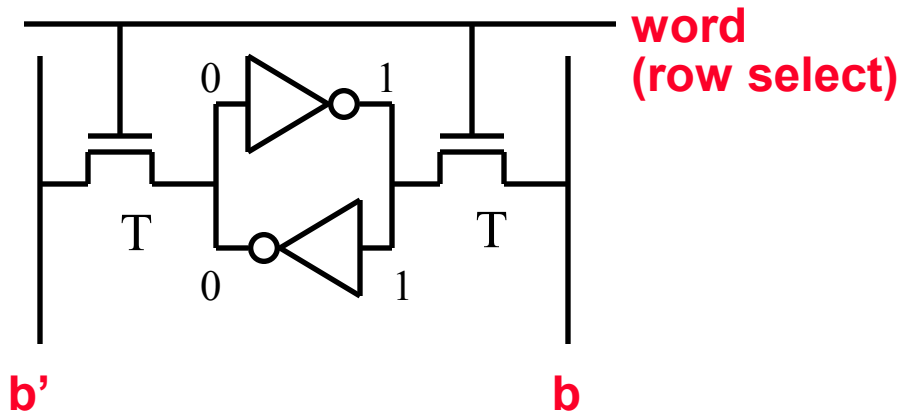
- **Bentuk array: terdiri dari sel memori**
 - Sel berisi 1 bit informasi
 - Baris dari sel membentuk untaian satu **word**
 - Contoh: 16 x 8 memori
 - memori SRAM mengandung 16 words
 - setiap words terdiri dari 8 bit data
 - Kapasitas memori: $16 \times 8 = 128$ bits
 - Decoder digunakan untuk memilih **baris** word mana yang akan diakses
 - Tipikal SRAM, array 1 dimensi => indeks dari baris pada array tersebut.

Organisasi Memori: 1-level-decode SRAM (128 x 8)



Review: Static RAM Cell

6-Transistor SRAM Cell



Latch → menyimpan state 1 bit
Transistor T bertindak sebagai switch
Contoh: state 1

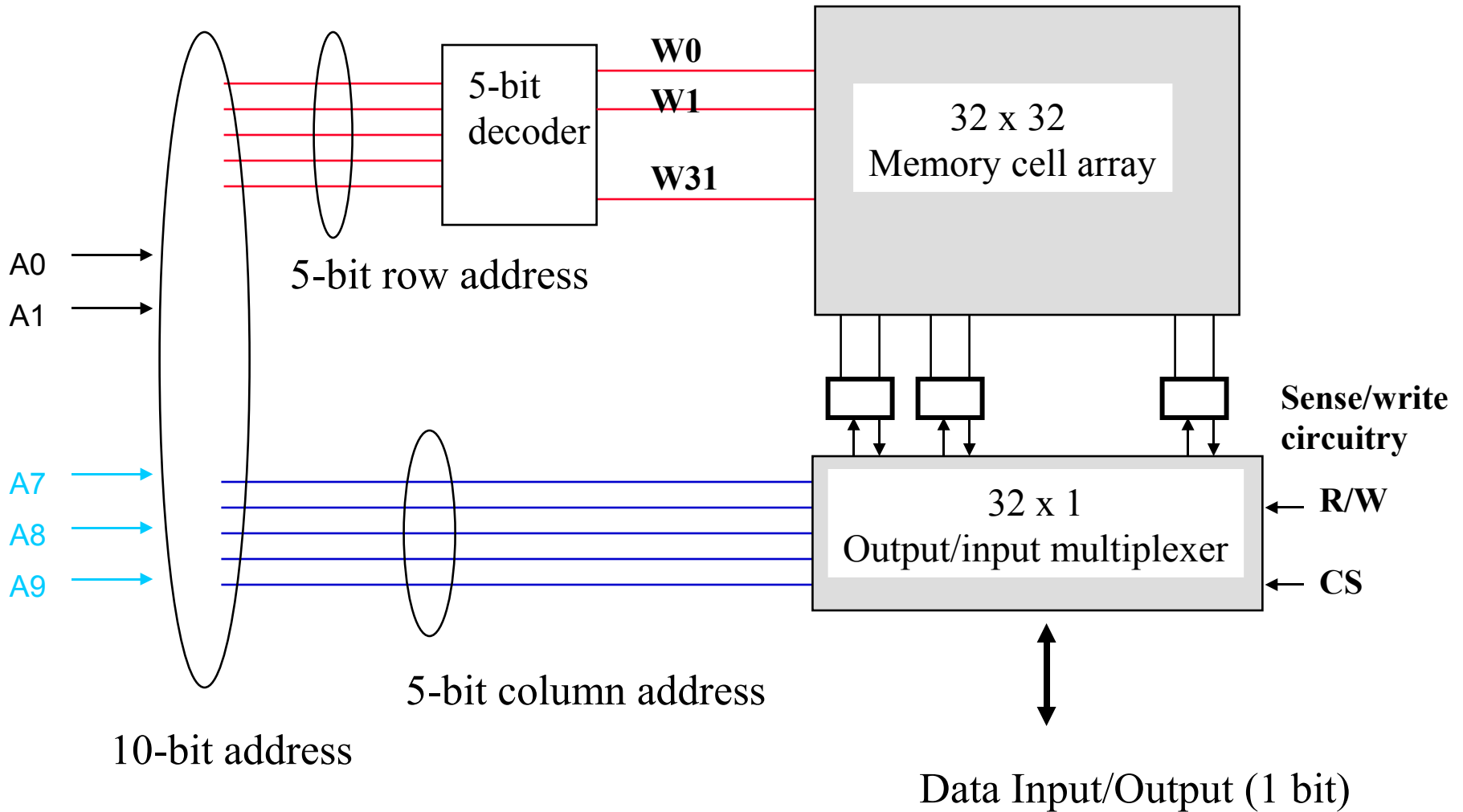
Latch dapat berubah dengan:
- put bit value pada b dan b'

- **Read:**
 1. Jika sel dalam keadaan 1, maka bit b akan memberikan sinyal high, dan b' memberikan sinyal low
 2. Jika sel dalam keadaan nol, maka bit b dan b' merupakan komplement dari keadaan 1
 3. Sirkuit sense/write mengawasi keadaan b dan b', mengawasi output sesuai dengan keadaannya
- **Write:**
 1. Sel di-set dengan meletakkan nilai yang tepat pada jalur bit b dan b'
 2. Sinyal yang diminta dihasilkan oleh sirkuit sense/write

Stat

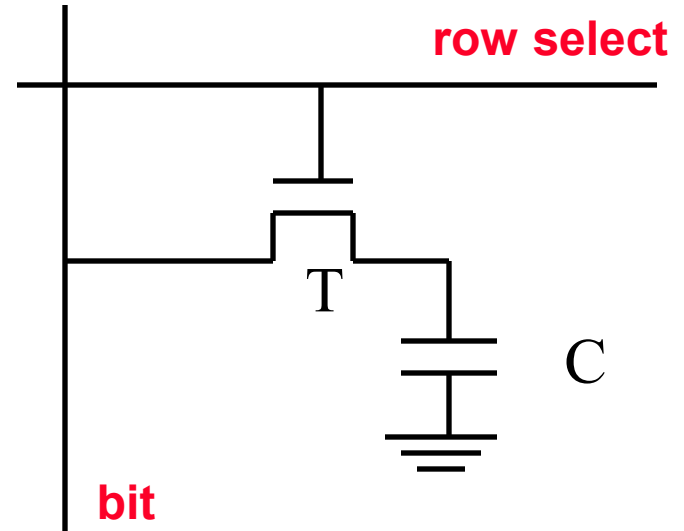
- **SRAM** dapat menyimpan “state” (isi RAM) selama terdapat “tegangan” power supply
- **(SRAM)** Sangat cepat, **10 nano-detik**
- Densitas rendah (bits per chip) → memerlukan 6 transistor per-sel → **mahal**
- Pilihan teknologi untuk memori yang sangat cepat dengan kapasitas kecil → **cache**

Organisasi Memori: 2-level-decode SRAM (1 K x 1)



Review: 1-Transistor Memory Cell (DRAM)

Kapasitor menyimpan
state 1 (charged) atau 0 (discharge)
Hanya bertahan sepuluh milidetik
Perlu refresh secara periodik!



◦ Write:

- 1. Drive bit line
- 2. Select row (T sebagai switch)

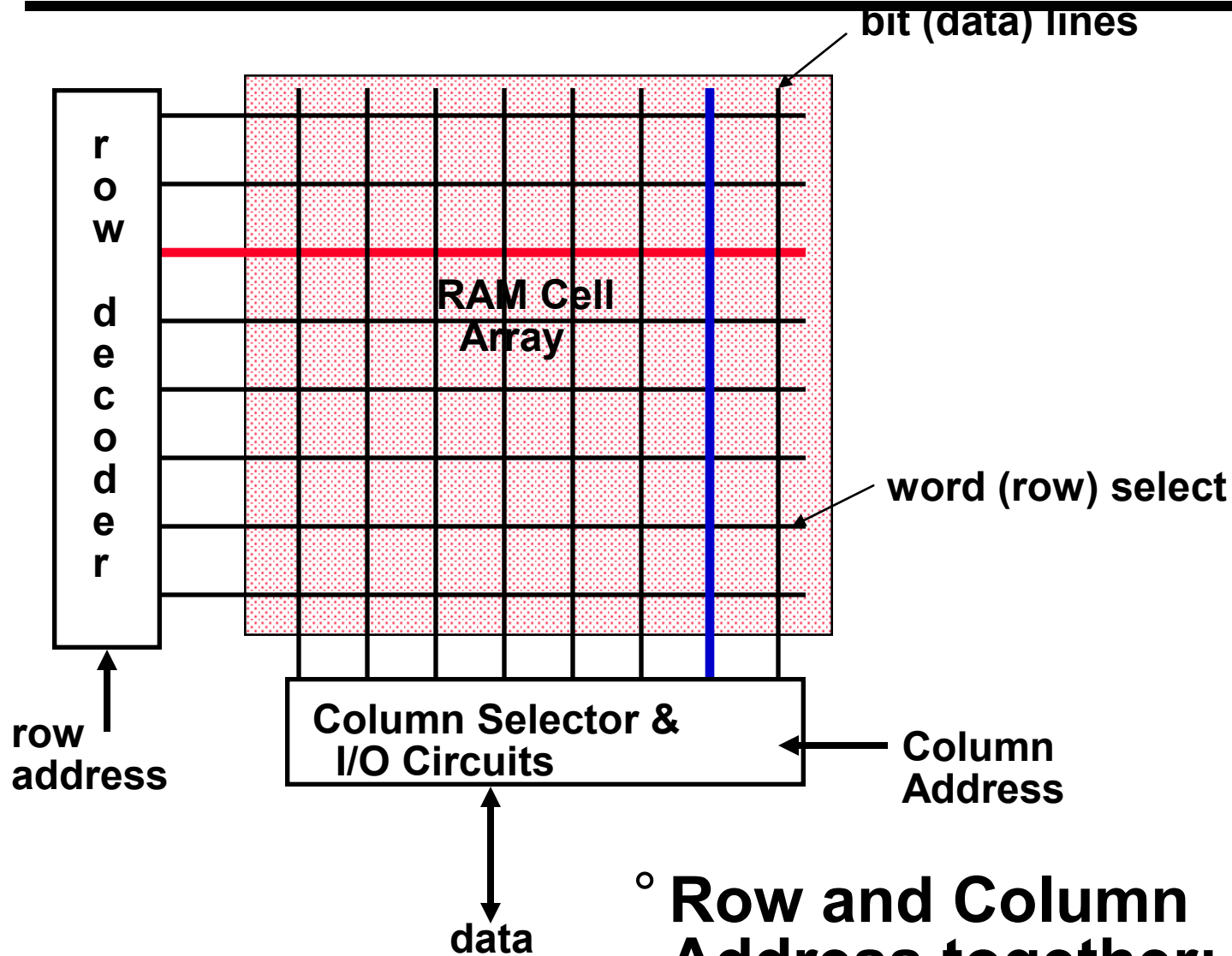
◦ Read:

- 1. Select row
- 2. Sense Amp (terhubung dengan bit line): sense & drives sesuai dengan value (threshold)
- 3. Write: restore the value (high or low)

◦ Refresh

- Just do a dummy read to every cell.

Classical DRAM Organization (square)

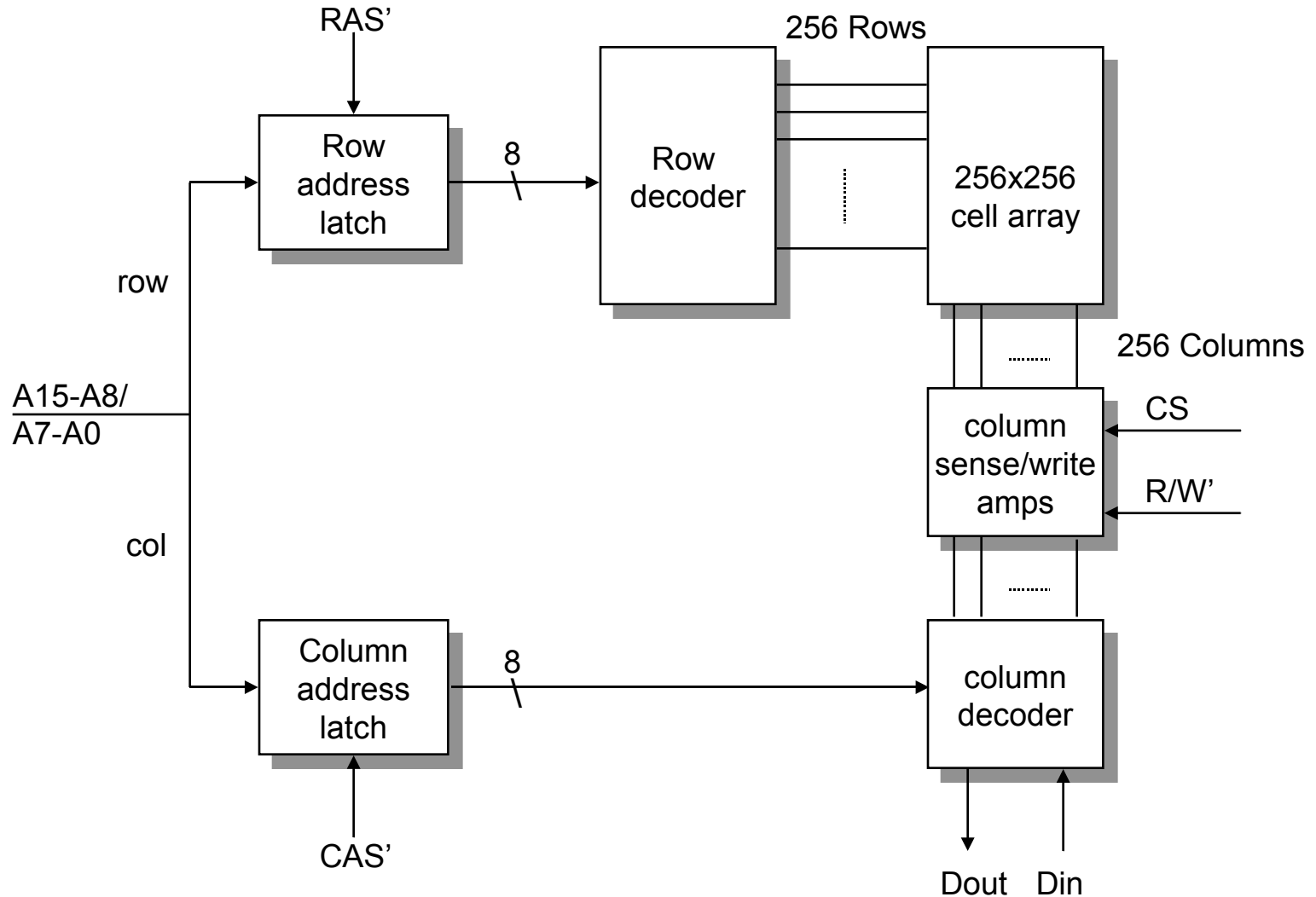


- **Row and Column Address together:**
 - **Select 1 bit a time**

Dynamic RAM (DRAM)

- **Slower than SRAM**
 - access time **~60 ns** (paling cepat: 35 ns)
- **Nonpersistent**
 - every row must be accessed every ~1 ms (**refreshed**)
- **Densitas tinggi: 1 transistor/bit**
 - **Lebih murah dari SRAM**
 - ~\$1/MByte [2002]
- **Pilihan teknologi memori untuk kapasitas besar dan “low cost” → main memory**

Organisasi DRAM 2-level (64Kx1)



Operasi DRAM

◦ Row Address (~50ns)

- Pilih Row address pada address lines & strobe **RAS**
- Alamat di-load ke latch baris sebagai respon sinyal RAS
- Read diinisiasi, sel baris yang dipilih akan dibaca dan **di-refresh**

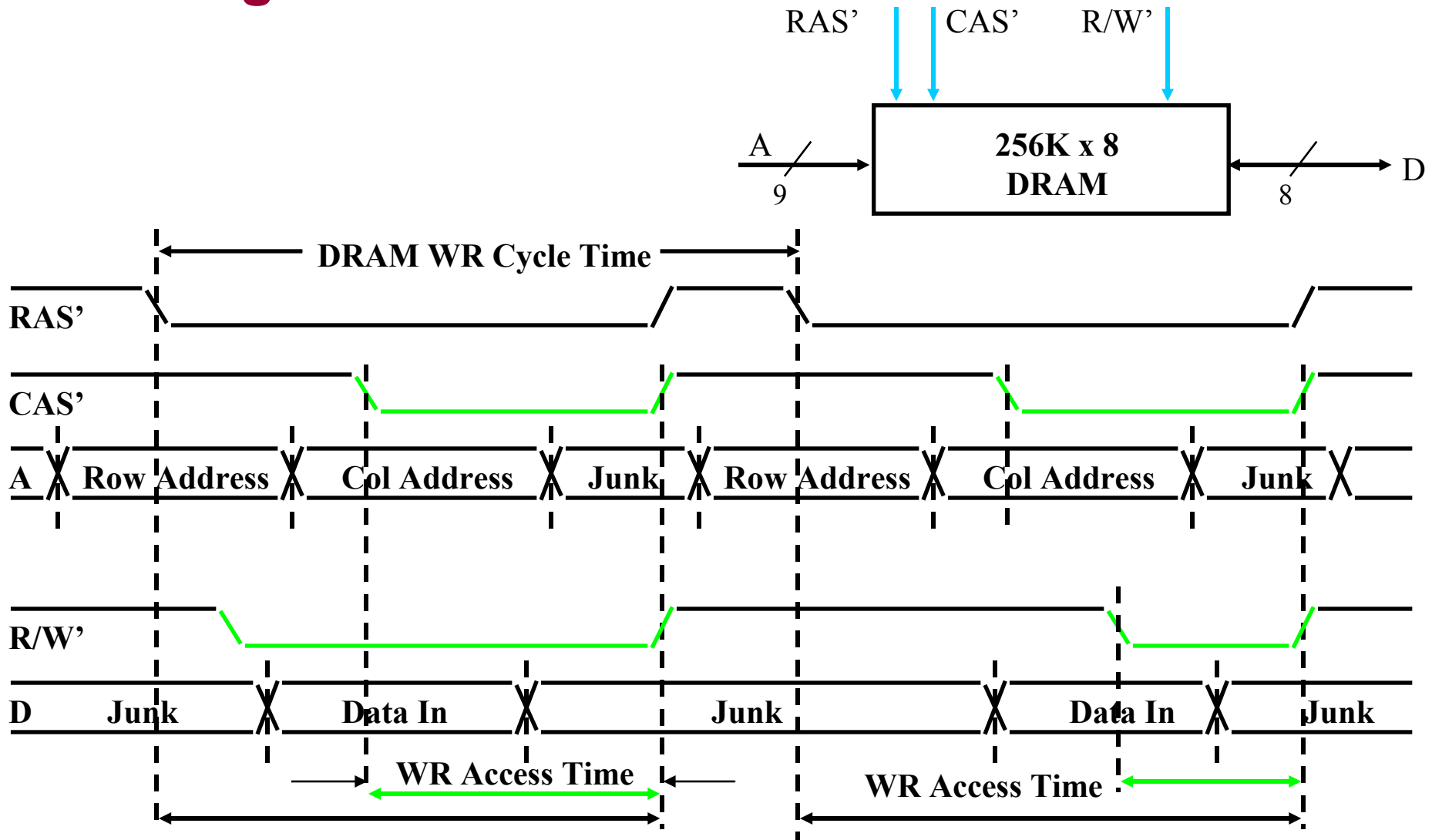
◦ Column Address (~10ns)

- Pilih Column address pada address lines & strobe **CAS**
- Jika sinyal kontrol R/W mengindikasikan :
 - **READ**: transfer from selected column latch to Dout
 - **WRITE**: Set selected column latch to Din

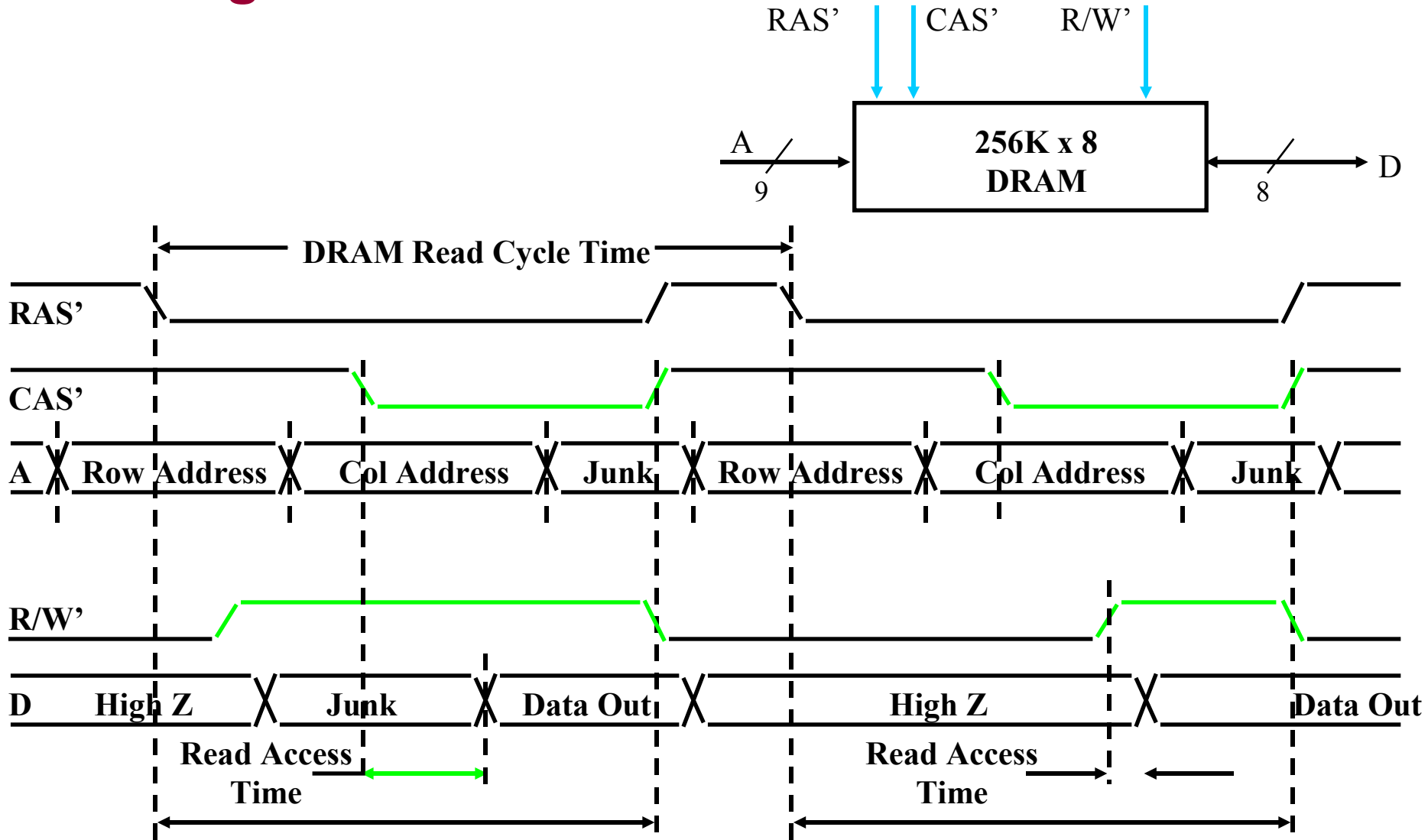
◦ Rewrite/Refreshed (~30ns)

- Write back entire row

DRAM Write Timing



DRAM Read Timing



DRAM: Kinerja

◦ Timing

- **Access time** = 60ns < **cycle time** = 90ns
- Need to rewrite row
- Model **asinkron**: operasi memori dilakukan oleh controller circuit → delay
prosesor menunggu sampai cycle time selesai lalu melakukan request lagi.

◦ Must **Refresh** Periodically

- Perform complete memory cycle for each row
- Approx. every 1ms
- Handled in background by memory controller

Perkembangan Teknologi Memori DRAM

◦ Teknologi memori: segi kecepatan akses berkembang sangat lambat

- Gap yang semakin membesar dengan kecepatan prosesor (cycle sangat kecil => 1 nsec, akses memori orde puluhan nsec).

◦ Perkembangan teknologi DRAM

- Basis tetap sama: 1-transistor memori cell (menggunakan kapasitor)
- Inovasi dilakukan dari segi: cara melakukan akses
 - memotong waktu akses (mis. CAS tidak diperlukan)
 - burst mode: sekaligus mengambil data sebanyak mungkin (seluruh word)
 - perlu tambahan rangkaian: register, latch dll

Enh

Conventional Access

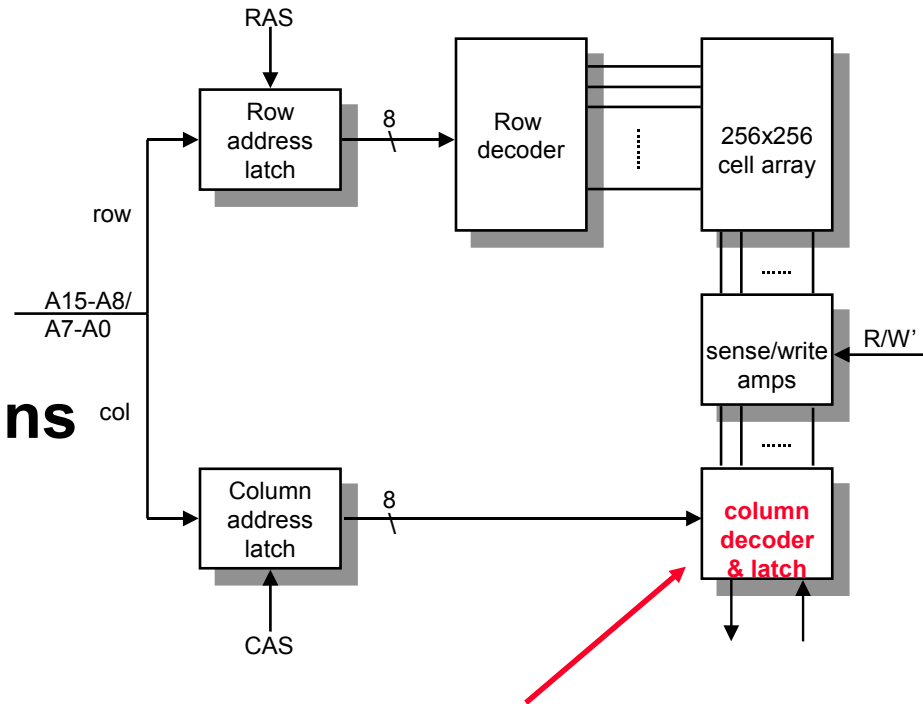
- Row + Col
- RAS CAS RAS CAS ...

Page Mode

- Row + Series of columns
- RAS CAS CAS CAS ...
- Gives successive bits

Video RAM

- Shift out entire row sequentially
- At video rate



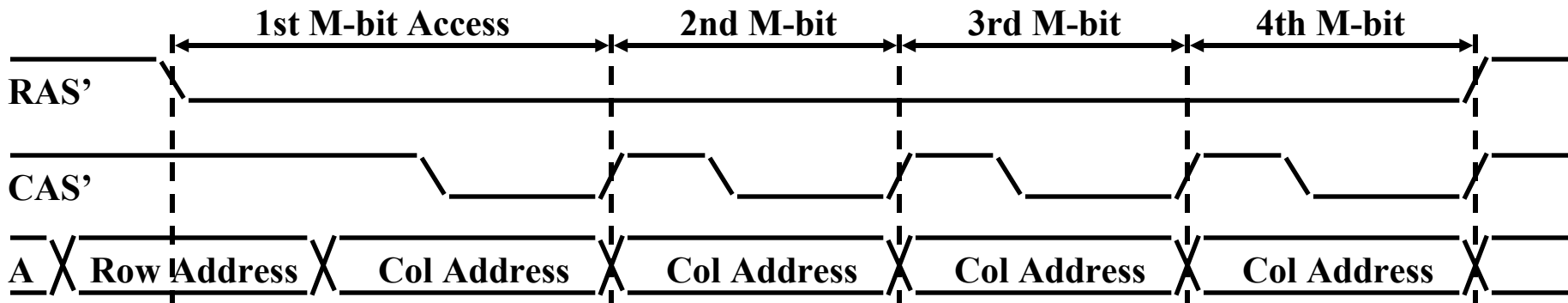
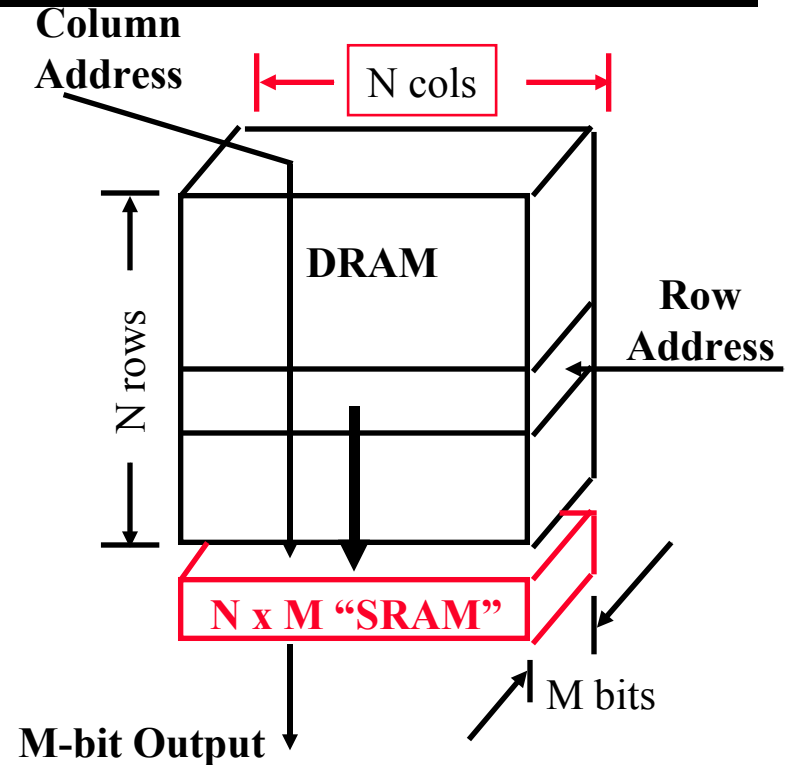
Entire row buffered here

Typical Performance

row access time	col access time	cycle time	page mode cycle time
50ns	10ns	90ns	25ns

Fast Page Mode Operation

- **Fast Page Mode DRAM**
 - $N \times M$ "SRAM" to save a row
- **After a row is read into the register**
 - Only CAS is needed to access other M-bit blocks on that row
 - RAS' remains asserted while CAS' is toggled



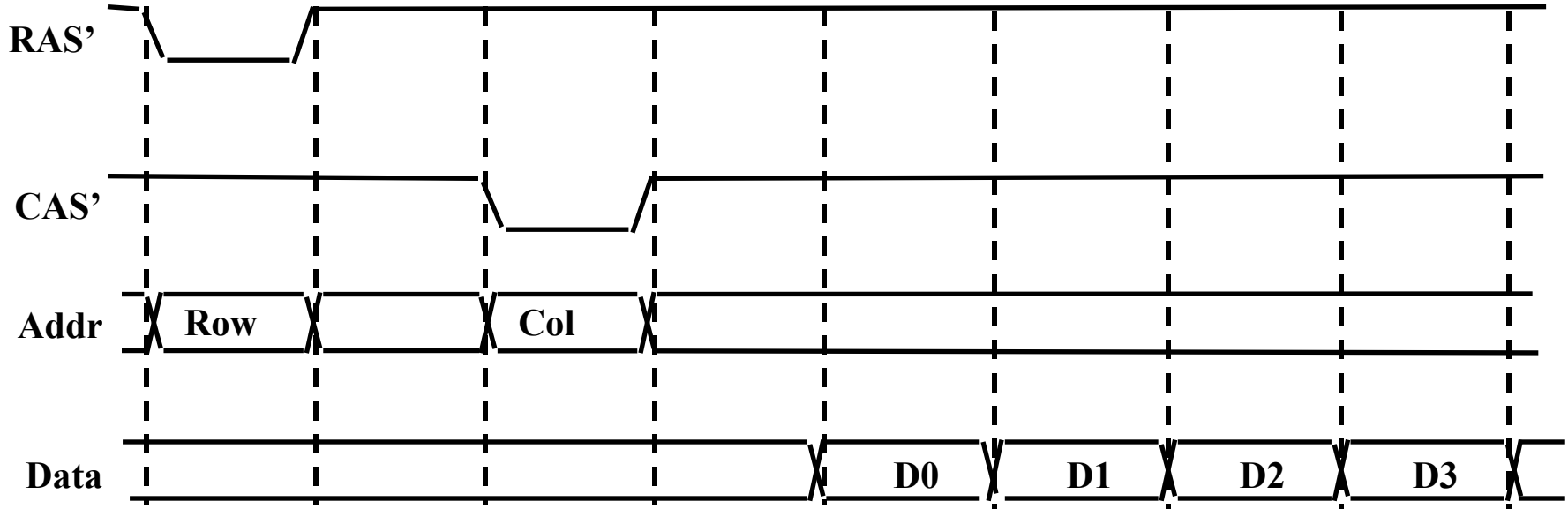
SDRAM & DDR SDRAM

- **SDRAM: Synchronous DRAM**
 - Address & Data are buffered in registers
 - Burst Mode:
 - Read/Write of different data lengths
→ **CAS signals are provided internally**
 - Standards: PC100, PC133

- **DDR SDRAM: Double-Data-Rate SDRAM**
 - Data is transferred on **both edges** of the clock
 - Cell array is organized in 2 banks
→ allows *interleaving* of word's access
 - Standards: PC2100, PC2300

- **RDRAM: Rambus DRAM**
 - High transfer rate using **differential signaling**
 - Data is transferred on **both edges** of the clock
 - Memory cells are organized in **multiple banks**
 - Standards: **proprietary** owned by Rambus Inc.

SDRAM Operation



- **Memory Latency:**

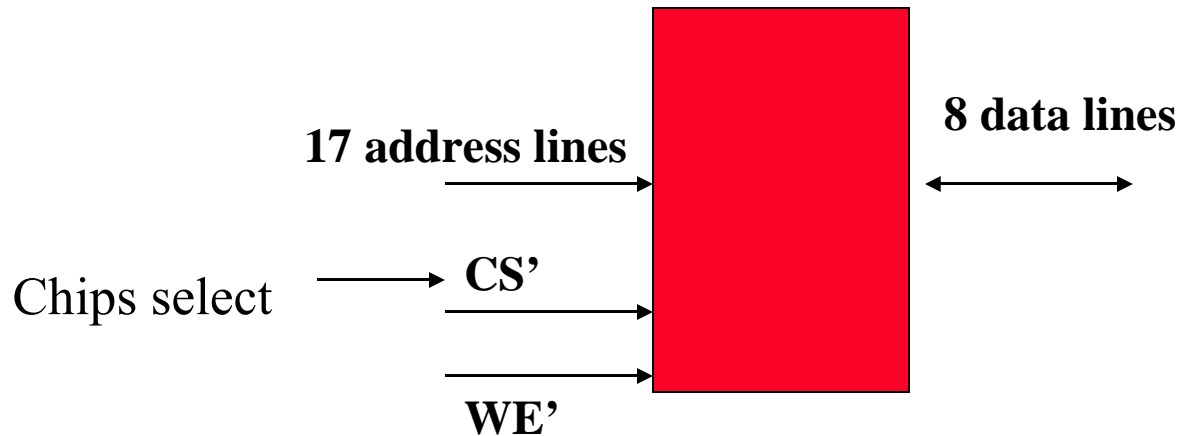
- Waktu yang dibutuhkan untuk mentransfer **word pertama**

- **Memory Bandwidth:**

- Jumlah word (byte/bit) yang dapat ditransfer per satuan waktu

Struktur Memori Besar (1/4)

Misalkan: Chip memori 128K x 8



<u>CS'</u>	<u>WE'</u>	<u>Function</u>	<u>Data Lines</u>
H	X	not selected	Hi-Z
L	H	Read	data at location on address lines
L	L	Write	write data on data lines to address on address lines

Contoh: Struktur 1 MB (2/4)

1 MB dapat dikonstruksi dengan organisasi 8 chips memori 128 KB ($8 \times 128 \times 8 = 1 \text{ MB}$)

The address space is partitioned into 128K blocks;

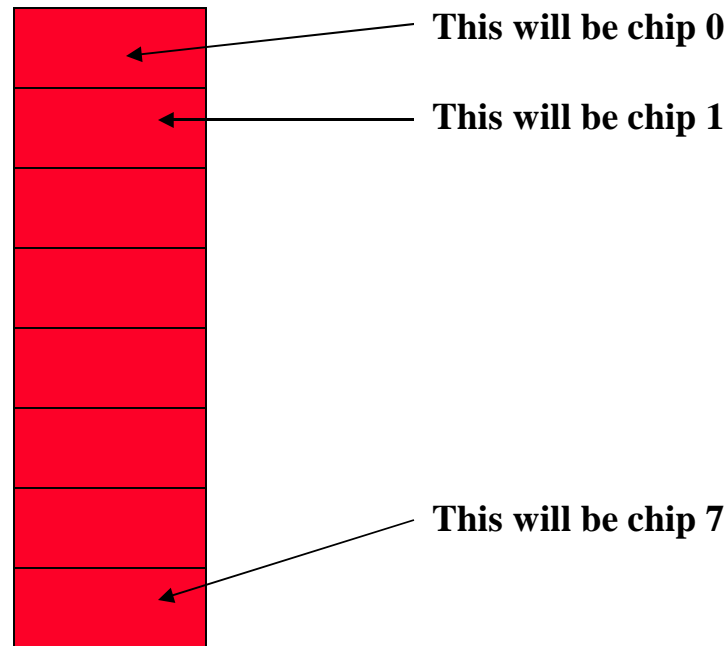
block 0 has addresses 0 -- 128K -1

block 1 has addresses 128K -- 256K-1

block 2 has addresses 256K -- 384K -1

⋮
⋮
⋮
⋮

block 7 has addresses 896K -- 1024K -1



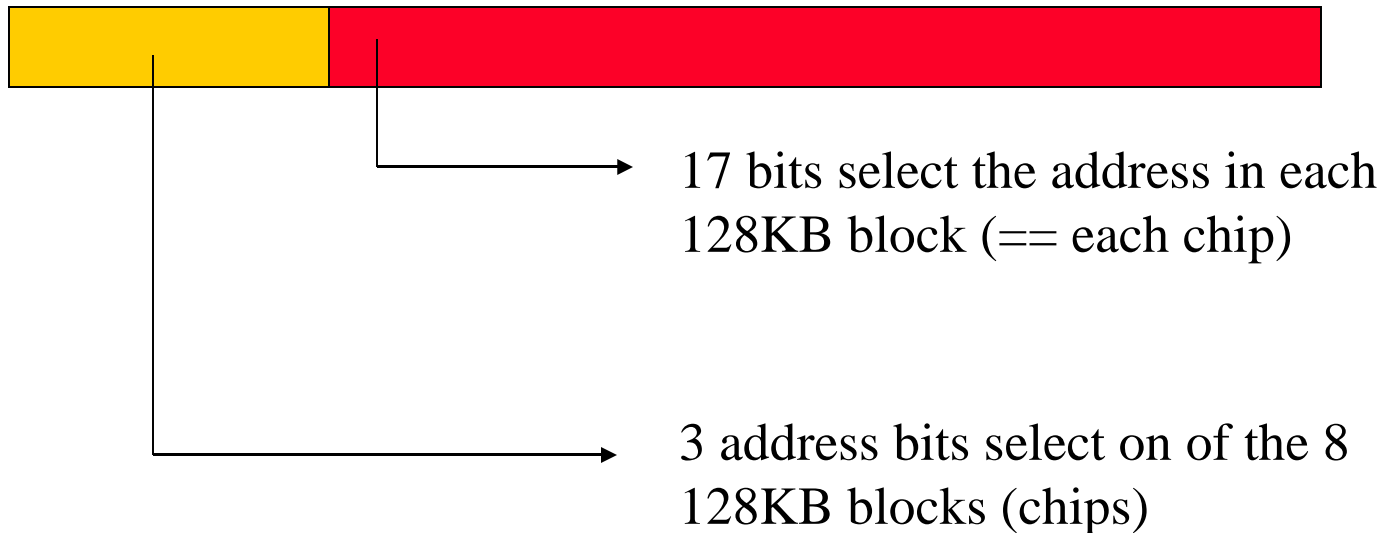
Berapa banyak bits yang diperlukan untuk alamat pada chips?
memilih chips yang mana?

Contoh: Pembagian field address (3/4)

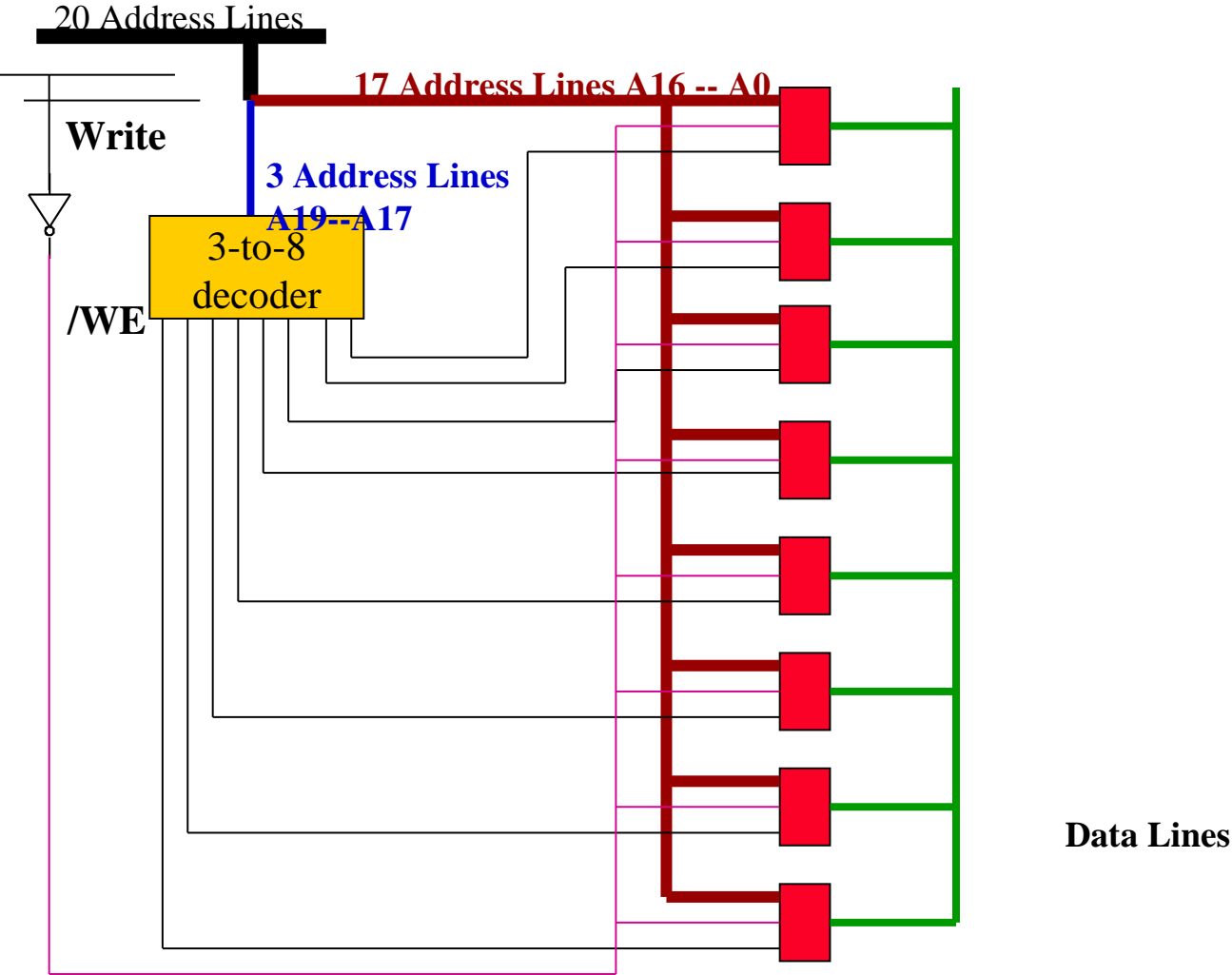
1MB membutuhkan alamat sebesar **20 bit**,
Ide: membagi field address menjadi 2 yakni:
bits untuk memilih chips dan address pada field tsb.

Bits 19 -- 17 (3 address bits)

Bits 16 -- 0 (17 address bits)



Contoh: Struktur 1MB memory (4/4)



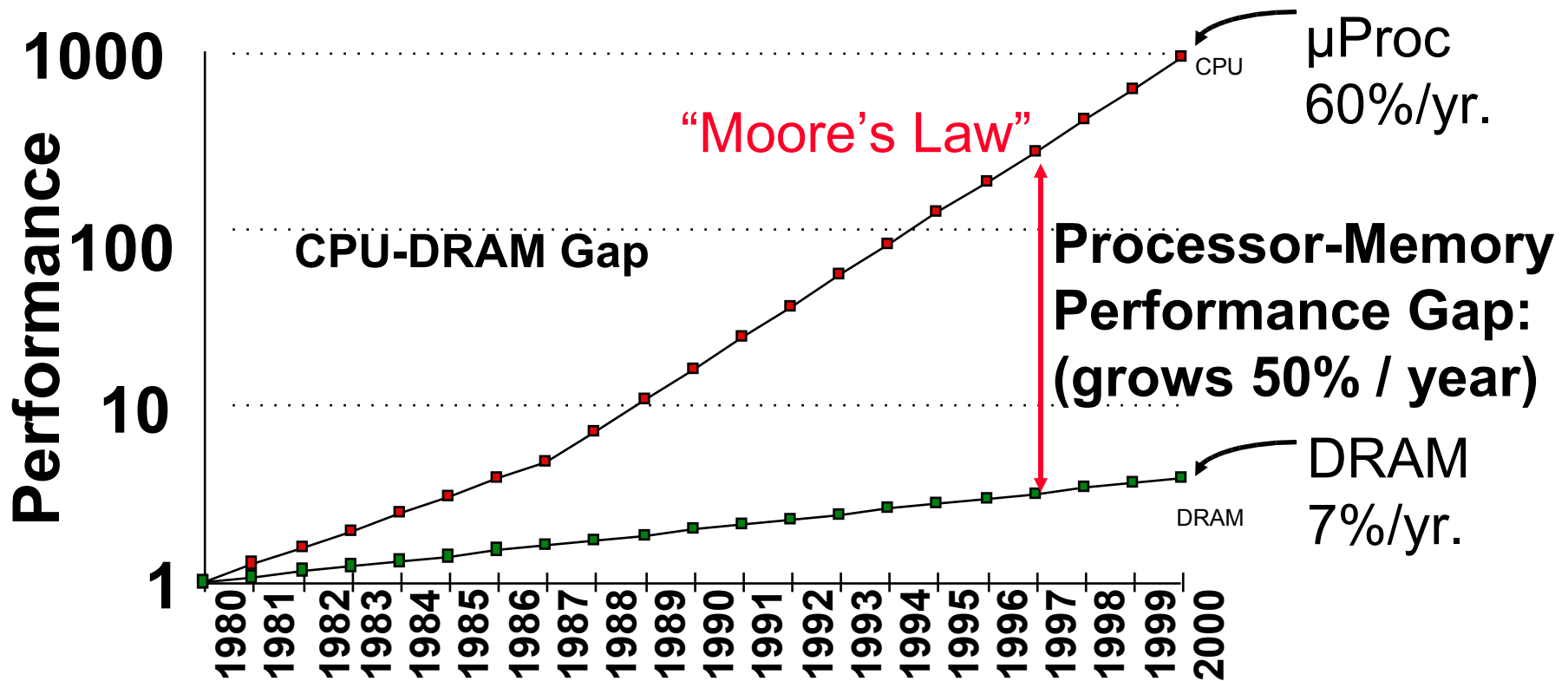
Read-Only Memory

- **ROM**
 - Write once, by manufacturer
- **PROM**
 - Write once, by user
- **EPROM**
 - Erasable PROM (by exposing it to ultraviolet light)
- **EEPROM**
 - Electrically, Erasable PROM
- **Flash**
 - ~EEPROM
 - Write in blocks
 - Low power consumption → battery driven
 - Implementation:
 - **Flash Cards**
 - **Flash Drives:**
 - Better than disk (no movable parts → faster response)

Ringkasan (.. To remember)

- DRAM **lambat** tapi murah dan kapasitas besar (densitas tinggi)
 - Pilihan untuk memberikan kapasitas **BESAR** pada sistem memori.
- SRAM **cepat** tapi mahal dan kapasitas kecil
 - Pilihan untuk menyediakan sistem memori yang waktu aksesnya **CEPAT**.
- Struktur memori besar dapat dibangun dari kumpulan chips memori kecil:
 - Field alamat **dibagi**: field address dan field untuk memilih chips/memori yang mana.
 - *Next topic: Trend teknologi memori (go to: <http://www.tomshardware.com>, search **SDRAM guide**)*

Trend Teknologi Memori (DRAM)



Prosesor sangat cepat tidak efektif => kendala “bottleneck” berada pada sumber/tujuan data yakni memori.