Ultra Small SOI DG MOSFETs
and
RF MEMS Applications

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Abstract

The continuous scaling-down process of the channel length over the last four decades is reaching its limits in terms of gate oxide thickness, short channel effects and power consumptions, all the above issues driving increased leakage currents. The dual gate SOI CMOSFET devices are expected to replace the bulk CMOSFET transistors for a better control of the entire device electrostatics. In this context, the current thesis proposes an one-dimensional analytical modeling of a novel symmetric Double-Gate SOI CMOSFET transistor, covering the dc and ac analyses, as well as its potential nano-electronics and RF MEMS applications. Our methodology offers a good characterization of the device in all regions of operation with the only assumptions of the light doping of the substrate and constant electron mobility. The silicon electrostatic potentials, inversion charge, electrical current drain and the small-signal parameters in terms of transconductance and output conductance are calculated for a silicon thickness of 20 nm, so that the volume inversion feature to be analytically proved, for 1 V voltage supply. A major contribution of the work is also, the AC analysis of an un-doped symmetric SOI MOSFET device, starting from the derivation of the small-signal circuit, continuing with the evaluation of terminal charges and capacitances and ending with the calculation of the RF figures of merits such as the cut-off frequency and the maximum frequency of oscillation. In addition, the thesis introduces the idea of the asymmetry behavior of the symmetric DG SOI MOSFET as a function of the applied channel voltage. Further, the work emphasizes the specific challenges of the analytical modeling for asymmetric DG SOI MOSFET devices, where the complexity of the mathematical equations reaches its limits.

Our entire analytical model of an un-doped symmetrical DG SOI MOSFET, is implemented in Verilog-A code in order to better support the compact device modeling and make it available for the design of the next generation of circuits. Thus, the new obtained library has been used in ”Cadence”, the typical design and modeling tool. In accordance with this goal, the operation of a common source amplifier based on the above-developed Verilog A code for the DG SOI MOSFET transistor will be shown.

Driven by the present scientific community effort to integrate the RF MEMS vibrating components and the electronic circuits for getting one chip transceiver in the near future, within this thesis we have combined the DG SOI MOSFET circuits with RF MEMS resonators for developing at the virtual level on-chip frequency generating functions. In this case, the thesis presents how the perturbation method can be applied to design a nonlinear oscillator comprising of a DG SOI MOSFET device and a RF MEMS resonator used

for the positive feedback loop.

Kurzfassung

Die stetige Reduktion der Kanallängen von MOS-Transistoren während der letzten vier Jahrzehnte erreicht aufgrund zu dünner GATEOXIDDICKEN und wegen des Vorhandenseins von KURZKANALEFFEKTEN sowie zu groβen Verlustleistungen nach und nach eine natürliche Grenze, da der Leckstrom durch diese Effekte negativ beeinflusst wird. Von den Dual-Gate SOI CMOSFET Bauteilen erwartet man, dass sie die herkömmlichen CMOSFET Transistoren ersetzen werden, da ihre elektrostatischen Eigenschaften besser kontrollierbar sind.

In dieser Arbeit wird ein eindimensionales Modell zur analytischen Beschreibung neuartiger Doppelgate SOI CMOSFET Transistoren vorgestellt, mit dem nicht nur das Gleich- und Wechselstromverhalten, sondern auch deren Anwendungsmöglichkeit für Nanoelektronik oder RF MEMS untersucht werden kann. Unsere Methode erlaubt eine genaue Charakterisierung des Bauteils unter allen Betriebsbedingungen, wobei lediglich die Annahmen leichter Substratdotierung und konstanter Elektronenbeweglichkeit gemacht wurden. Die elektrostatischen Potentiale von Silizium, die Inversionsladungen, der Verluststrom und die Kleinsignalparameter werden in Hinblick auf Leit- und Gegenwirkleitwert für Siliziumdicken von 20 nm berechnet. Ebenso enthält diese Arbeit die AC-Analyse eines undotierten symmetrischen SOI MOSFETs. Sie reicht von der Ableitung des Kleinsignal-Schaltkreises über die Auswertung von Anschlussladungen und -kapazitäten bis hin zur Berechnung der Gütefaktoren wie Grenzfrequenz oder maximaler Oszillationsfrequenz. Zusätzlich wird in dieser Arbeit die Idee des kanalspannungsabhängigen asymmetrischen Verhaltens von symmetrischen DG SOI MOSFETs eingeführt. Weiterhin werden die Herausforderungen beschrieben, die die analytische Behandlung asymmetrischer DG SOI MOSFETs mit sich bringt. Hierbei erreicht bzw. übersteigt die Komplexität der mathematischen Gleichungen die Möglichkeiten analytischer Methoden.

Um die Modellierung kompakter Bauteile bestmöglich zu unterstützen und diese für die nächste Generation integrierter Schaltkreise verfügbar zu machen, wurde das gesamte analytische Modell eines undotierten DG SOI MOSFETs in der Hardwarebeschreibungssprache Verilog-A implementiert. Die so erhaltene Bibliothek wurde in "Cadence", einem gebräuchlichen Design- und Modellierungstool verwendet.

In diesem Zusammenhang wird die Arbeitsweise eines Common-Source Verstärkers analysiert, basierend auf dem oben vorgestellten Verilog-A code des DG SOI MOSFET Transistors.

Motiviert durch den in der wissenschaftlichen Gemeinschaft gegenwärtig betriebenen Aufwand, RF MEMS Komponenten und die zugehörigen elektronischen Schaltungen in eine Ein-Chip-Lösung für Sende- und Empfangsmodule zu integrieren, wurden in dieser Arbeit DG SOI MOSFET Schaltungen zusammen mit RF MEMS Resonatoren kombiniert, um On-Chip Frequenzgeneratoren auf einer virtuellen Ebene zu implementieren. In diesem Zusammenhang wird gezeigt, wie "Pertubation"-Methoden angewendet werden können, um nichtlineare Oszillatoren mit Hilfe eines DG SOI MOSFETs und eines RF MEMS Resonators in der positiven Rückkopplungsschleife zu realisieren.

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List of Abbreviations

1D	One Dimensional
3D	Three Dimensional
AM	Amplitude Modulation
BAW	Bulk Acoustic Wave
BOX	Burried Oxide
BTBT	Band To Band Tunneling
CC	Clamped-Clamped
CMOS	Complementary Metal Oxide Semiconductor
CPU	Control Processor Unit
CSE	Charge Sharing Effect
DELTA	DEpleted Lean-channel TrAnsistor
DG	Double Gate
DIBL	Drain-Induced Barrier Lowering
DT	Direct Tunneling
FBAR	Film Bulk Acoustic Resonator
FET	Field Effect Transistor
FD	Fully Depleted
FDD	Frequency Division Duplexer
FF	Free Free
FIJ	Field Induced Junction
FN	Fowler-Nordheim Tunneling
GAA	Gate All Around
GIDL	Gate Induced Drain Leakage
GSM	Global System for Mobile Communication
IC	Integrated Circuits
IF	Intermediate Frequency
ITRS	International Technology Roadmap for Semiconductors
JFET	Junction Field Effect Transistor
LOCOS	Local Oxidation of Silicon
LO	Local Oscillation

MEMS	Micro-Electro-Mechanical-Systems
MOS	Metal Oxide Semiconductor
nMOS	N-Type MOS
pMOS	P-Type MOS
PCB	Printed Circuit Board
PD	Partially Depleted
PDA	Personal Digital Assistant
RF	Radio Frequency
SAW	Surface Acoustic Wave
SCE	Short Channel Effect
Si	Silicon
SiP	System in Package
SOI	Silicon on Insulator
SOS	Silicon on Sapphire
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency

List of Symbols

b	Damping coefficient
b_c	Critical damping coefficient
C_{DS}	Drain-source capacitance
C_G	Gate capacitance
C_{GS}	Gate-source capacitance
C_{GD}	Gate-drain capacitance
E	Energy
E_C	Conduction band energy of a semiconductor
E_F	Fermi Energy
E_g	Energy bandgap of a semiconductor
E_i	Intrinsic Fermi energy
E_V	Valence band energy of a semiconductor
f	Frequency
f_{max}	Maximum frequency of oscillation
f_T	Cut-off frequency
g_d (g_{out})	Output conductance of a $MOSFET$
g_m	Transconductance of a $MOSFET$
k_m	Mechanical Stiffness
k_e	Electrical Stiffness
I	Current
I_D	Drain current
k	Boltzmann's constant
L	Length
m	Mass
n	Electron density
n_i	Intrinsic carrier density
N_A	Acceptor doping density
p	Hole density
q	Electronic charge

Q	Electrical charge
Q_i	Interface charge density per unit area
Q_{inv}	Inversion layer charge density per unit area
R	Electrical resistance
t_{ox}	Oxide thickness
t_{Si}	Silicon thickness
T	Temperature
V	Voltage
V_D	Drain voltage
V_{DS}	Drain-source voltage
V_{FB}	Flatband voltage
V_G	Gate voltage
V_{GS}	Gate-source voltage
V_t	Thermal voltage
V_T, V_{th}	Threshold voltage of an MOS transistor
ϵ_{ox}	Dielectric constant of silicon-dioxide
ϵ_{Si}	Dielectric constant of silicon
ϵ_0	Dielectric constant of vacuum
μ_n	Electron mobility
μ_p	Hole mobility
Φ_M	Workfunction of a metal
Φ_{MS}	Workfunction difference between a metal and a semiconductor
ω	Angular frequency
Φ_S	Workfunction of a semiconductor
ω_0	Mechanical Resonant natural frequency
ξ	Damping ratio
ψ	Silicon electrostatic potential

Material and Physical Parameters

Name	**Notation**	**Silicon**
Bandgap energy at $300K$	$E_g(eV)$	1.12
Breakdown Field	$E_{br}(V/cm)$	3×10^5
Intrinsic concentration at $300K$	$n_i(cm^{-3})$	10^{10}
Mobility at $300K$ for electrons	$\mu_n(cm^2/(Vs))$	1400
Mobility at $300K$ for holes	$\mu_p(cm^2/(Vs))$	450
Relative dielectric constant for silicon	ϵ_{Si}	11.9
Boltzmann's constant	$k(J/K)$	1.38×10^{-23}
Electronic charge	$q(C)$	1.6×10^{-19}
Permittivity if vacuum	$\epsilon_0(F/m)$	8.854×10^{-12}
Thermal voltage (at $T = 300K$)	$V_t(mV)$	25.86

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Chapter 1

Introduction

1.1 Motivation

In the last decades, continuous needs of industrial process automation and people's increased desire for lifestyle, safety, security and real-time interconnectivity have been the driving force for the unprecedented development of all industrial processes and consumer electronics. In the same time, the technology of semiconductors has made an impressive progress, to respond to the above challenging market demands. As predicted by Gordon Moore, from 1965, the silicon integrated circuit (IC) technology has shown a continuous down-scaling of the $MOSFET$ transistor dimensions in order to reach higher packing density, performances improvement, faster circuit speed and lower power consumption. To attain these goals, for both consumer electronics and industrial environment, the designers have made big efforts to improve the power-efficiency, reduce the sizes and fulfill the increased integrability. Thus, the continuous efforts of chip makers to respond to market requirements and emerging new applications have lead year by year to new integrated circuits with complex functions on the same chip. After this more than four decades scaling-down journey, the bulk $CMOS$ technology will reach the end of the road-map due to the increase in short channel effects which limited the device's low power operation. Thus, the Silicon on Insulator (SOI) $CMOS$ technology appeared as a promising alternative for bulk $CMOS$ to obtain new devices with superior advantages in terms of: $1)$ light doping of the channel for mobility improvement; $2)$ good control of short channel effects by increased electrostatic control due to the voltage applied on multiple gates (dual gate-DG, three gates-TG, gates all around-GAA); $3)$ almost ideal sub-threshold slope due to the elimination of substrate doping; $4)$ increased current drive capability due to the volume inversion [6] of the entire silicon film. However, some challenges exist in terms of $3D$ technological complexity and ultra thin silicon film needed for these $SOI\ MOSFET$ devices.

On the other hand, almost in the same time with IC technology birth, the first micro-electro-mechanical systems ($MEMS$) have been developed on the silicon wafer, making

thus possible on-chip processing of non-electrical signal for sensing and actuating purposes. It was just only a matter of time, till the IC technology married with $MEMS$ technology to generate the first on-chip integrated $MEMS$, marking thus the beginning of a new technology revolution (as shown by the first integrated pressure sensors), that is bursting, now. An important branch of $MEMS$ is the $RF\ MEMS$, where many separate components, like antenna, passive and active RF components can be performed on silicon chip. This new emerging field of $RF\ MEMS$ will revolutionize the wireless electronics by the potential of the vibrating micro-mechanical circuits to operate at high quality factor, enabling the on-chip multiple signal processing and the integration of $RF\ MEMS$ on the same chip with $CMOS$ integrated circuits. It is the purpose of this thesis to open new bridges between the ultimate $SOI\ MOSFET$ technology and the emerging $RF\ MEMS$ field, trying to show by analytical methods how the new family of dual gate $DG\ SOI\ MOSFET$ devices operate in the dc and ac regime and how one can use them for developing an integrated $MEMS$ oscillator as modeling example of the future integrated $DG\ SOI$-$MOSFET$-$RF\ MEMS$ systems.

The above topic is in agreement with the research objectives of our university group in the field of the analog device and circuit modeling, as well as with the scientific target of the organization called $TICMO$ (Tunable Integrable Components in Microwave Technology and Optics). It aims the synergetic multidisciplinary interaction between many specialists and their teams working on tunable or frequency-agile components having a major and extensive operational potential in communication and sensor systems.

Very briefly speaking, within my thesis, a detailed analytical modeling of dc and ac regimes of the Double-Gate $SOI\ MOSFET$ will be realized and, then, these models will be used for developing a perturbation method-based methodology of design for a $RF\ MEMS$ based oscillator that contains the $RF\ MEMS$ resonator in its positive feedback-loop.

1.2 Research Objectives

This dissertation is focused on next generation of $SOI\ MOSFET$ devices aiming contributions to the analytical compact modeling of Dual Gate $SOI\ MOSFET$ and potential application of these new devices to wireless $RF\ MEMS$ systems. An integrated oscillator build with a $DG\ SOI\ MOSFET$ device and a $RF\ MEMS$ circuit in its positive feed-back loop is analytical modeled and designed to prove the use of these $DG\ SOI\ MOSFET$ devices for future applications. For this purpose, the state of the art in modeling and technology of $SOI\ MOSFET$ devices and the RF micro-electro-mechanical systems are thoroughly investigated. The objectives of the thesis can be summarized as follow:

- to offer a dc analytical compact modeling of a $DG\ SOI\ MOSFET$ founded on the classical physics concepts, by proposing simple and convenient methods to calcu-

late the silicon electrostatic potentials and then, the drain current, transconductance and output conductance;

- to propose an ac top-down methodology in order to derive the entire small signal equivalent circuit for a $DG\ SOI\ MOSFET$ for which, the terminal charges and capacitances are going to be calculated by using the method proposed in the previous part. The main device figures of merit such as cut-off frequency and maximum frequency of oscillation will be then calculated;
- to provide a hardware description in Verilog-A for the above-proposed model of an un-doped symmetrical $DG\ SOI\ MOSFET$;
- to offer an insight into the micro-electro-mechanical systems evolution and develop an electrical equivalent model for an $RF\ MEMS$ resonator;
- to design a common-source amplifier which contains the $DG\ SOI\ MOSFET$ device implemented in Verilog-A behavioral language;
- to propose a new Colpitts oscillator formed on a $DG\ SOI\ MOSFET$ and the equivalent RLC electrical circuit of the $RF\ MEMS$ resonator presented previously.

1.3 Thesis Outline

The thesis is organized in three main parts. The introduction consists of a motivation, problem formulation and state of the art of SOI and $RF\ MEMS$ devices. Then, the core chapters contain my original contributions to the dc and ac un-doped $DG\ SOI\ MOSFET$ modeling and its implementation in Verilog A tool. The work continues with the design of a $DG\ SOI\ MOSFET$- and $RF\ MEMS$-based oscillator. Finally, the thesis concludes with the presentation of the future work and summary of the current research. The three main parts of the thesis are described below, as follows:

I - Background Chapters 2 and 3 present the state of the art in the silicon-based devices and micro-electro-mechanical systems evolution. The goal of the chapter 2 is to present the $MOSFET$ transistor evolution by describing the gradual transition from silicon bulk technology to the silicon-on-insulator technology and emphasizing their advantages and challenges. The limiting short channel effects and the leakage currents in MOS transistors will be presented in this chapter together with their main overcoming solutions that include the silicon-on-insulator devices. Once that SOI technology environment is completed, chapter 3 poses the benefits and challenges of the new vibrating $RF\ MEMS$ devices and circuits made with the micromachining technology which can be applicable at different future portable and/or wireless communication applications. For this purpose, the $RF\ MEMS$ devices are enumerated and presented by emphasizing their main functions accomplished

when they are connected together and then describing the most important circuits used in wireless communication applications. Besides, the evolution of transceiver architectures is included, starting from the present generation where $CMOS$ integrated circuits interface at the board level with off-chip quartz-based passive components for getting transceiver architectures performed on printed circuit board (PCB) and ending up with an ultimate vision of an all-$MEMS$ transceiver in which all the above-mentioned $MEMS$ elements are located on a single silicon chip together with the electronic RF circuits.

II - Personal Contributions The chapters 4 and 5 represent the core of the work. Once the general environment of $SOI\ MOSFET$ devices is created, an important aspect is to understand and model a particular SOI transistor, called Double-Gate $SOI\ MOSFET$. Since the phenomena are more complex due to the increased number of gates that surround the silicon substrate, the chapter 4 of the thesis addresses the DC analytical modeling of un-doped double-gate $SOI\ MOSFET$ by proposing convenient and simple methods to calculate the device electrical parameters such as: electrostatic potentials, electric charges, drain current, transconductance and output conductance. Further, the AC analysis of an un-doped symmetric $SOI\ MOSFET$ device is proposed beginning with the derivation of the small-signal equivalent circuit, continuing with the evaluation of terminal charges and capacitances and ending with the calculation of the RF figures of merits such as cut-off frequency and maximum frequency of oscillation. The entire analytical model is implemented in Verilog A Language and presented in chapter 5. The efficiency of this code is shown by realizing an application in terms of a common source amplifier based on the $DG\ SOI\ MOSFET$ transistor. In addition, a Colpitts oscillator is going to be designed in the time domain, by means of a perturbation method and taking into account the electrical characteristics of novel $DG\ SOI\ MOSFET$ device and an equivalent RLC electrical circuit of a micro-mechanical resonator.

III - Forward Plan Finally, the future work and conclusions are described in the last two chapters. Since the thesis deals with two great research directions of silicon-based areas in terms of $DG\ SOI\ MOSFET$ devices and $RF\ MEMS$ components and their future linkage, the chapter 6 focuses on the next challenges in the field, where micro (like $3D\ MEMS$) and nano-technology (like CNT based nano devices and circuits) will be together on the same ultra small chip for increased functionality. Finally, in chapter 7 the dissertation presents a summary of the contributions provided by the present work.

Chapter 2

Evolution of the SOI MOSFET Devices for Integrated Circuits

During the last decades, the $MOSFET$ transistor dimensions have been in a continuous aggressive down-scaling in order to reach higher packing density, faster circuit speed and lower power consumption. The perpetual efforts of chip makers to respond to the market requirements and new applications have lead year by year to new integrated circuits with complex functions on the same chip. During this time the bulk $CMOS$ technology has shown its ability to respond to the above challenges, but in the next decade this $CMOS$ technology will reach the end of the road-map. In the shadow of the $CMOS$ big brother, the SOI (semiconductor on silicon, in the most general definition) technology has grown up steadily, proving recently its maturity when the first commercial SOI microprocessors appeared on the market. More than that, the SOI technology will be taken over as an alternative to bulk $CMOS$, when the last one is giving up in terms of scalability, material flexibility and minimum feature size of transistor.

The main objective of this chapter is to describe the smooth transition from silicon bulk technology to the silicon-on-insulator technology, by emphasizing their advantages and challenges. The current chapter begins with the history of the electron devices starting from the invention of the solid state rectifier and ending with the present devices. The scaling down rules, which have made the Moore's law to become so true for more than four decades will be described here, as well as silicon technology road-map showing the device miniaturization as a function of time in the dimension range from 10 microns to 10 nm. The limiting short channel effects and the leakage currents in MOS transistors, which have been threatening the scaling process at each new technology node, have been constantly solved by creative technologists and designers and, thus, making possible the progress we have today. Afterward, the silicon-on-insulator evolution will be described by presenting the most important devices made with this technology. The integrated circuit based on double-gate silicon on insulator $MOSFET$ transistor will be included, followed by a short description of future challenges.

2.1 The Transition from the Bulk MOSFET Devices to Multi-Gate SOI MOSFET Devices

2.1.1 History of Electron Devices

The history of semiconductor devices goes back to the year 1874, when Ferdinand Braun invented the solid state rectifier, which was based on point contact in lead sulfide [11]. By that time the solid state physics and electronics had no theoretical basis. The quantum mechanics theory and its application to solid material accelerated the progress of solid electronics. In 1900, Max Plank presented his theory of quantum energy, where the energy unit was called quanta and the energy being a multiple of quanta. According to it, the electron is not free to have every energy in the solid state, but different levels of energy. This approach helped later understanding the energy band structures in solid materials and thus, differentiate them as metals, insulators and semiconductors.

In parallel, at the beginning of 1900 year, the direction of vacuum tube was investigated. Actually, the father of vacuum technology, should be considered Thomas Edison, who has invented the light bulb which was the first vacuum tube used for the electrical applications. In 1906, Lee De Forest made the vacuum tube triode that had three terminals and amplified the audio signals, making AM radio possible. The vacuum tube or electron tube represents the first device used to amplify electronic signals and this played an important role in the development of the electronic circuits and vacuum technology as well as the system and computer science. The first computer was performed with vacuum tubes and occupied a few rooms. This is why we say today that the vacuum electronics suffered from large occupied volume, high power consumption and reliability issues, even if it was so important by that time.

Then, the final mathematical formulation of the quantum mechanic approach was developed in 1920, while its application to solid state was done by Mott and other scientists from UK. It is worth to mention that the concept of a field effect transistor (FET) was invented by Lilienfeld in 1926. He was the first who sayed that applying an electrical field on a poorly conducting material, you can change its electrical conductivity. Unfortunately, the concept was not successfully demonstrated at that time, due to the technological problems related to the control and reduction of the surface states at the interface between the oxide and the semiconductor. At the end of 1930's, Mervin Kelly from Bell Labs decided to reinforce the solid state device research and he has made a team having Robert Shockley, Russell Ohl and others, aiming to push electronics beyond vacuum tubes. Similar work was done in Germany, by Pohl and Hilsch contriving the solid amplifier based on potassium bromide, and having three metal leads. At Bells labs, the first successful decision was the selection of silicon and germanium as semiconductors crystals. Thus, in 1940, Russel Ohl investigated silicon crystals and discovered the n- and p-type silicon semiconductor, in terms of rectifying negative or positive ac signals. He, also, built a sample in which the top part constituted a p- type region and the bottom was $n-$

type. When the light shone on the pn structure, he observed a voltage drop on the terminals. After the second world war, the team from Bells included John Bardeen and Walter Brattain, among other scientists working at understanding fundamentals of surface states and its negative impact on the electrical behavior of semiconductors.

In November 1947, John Bardeen and Walter Brattain have discovered the point contact transistor using germanium as semiconductor, which was proved to Bells Labs before Christmas eve. In the next two months William Schockley, developed the theory of the transistor, introducing the concept of minority carriers. Bardeen, Bratain and Shockley won the Nobel prices for physics in 1956. The picture of the first point-contact transistor that is shown in Figure 2.1.

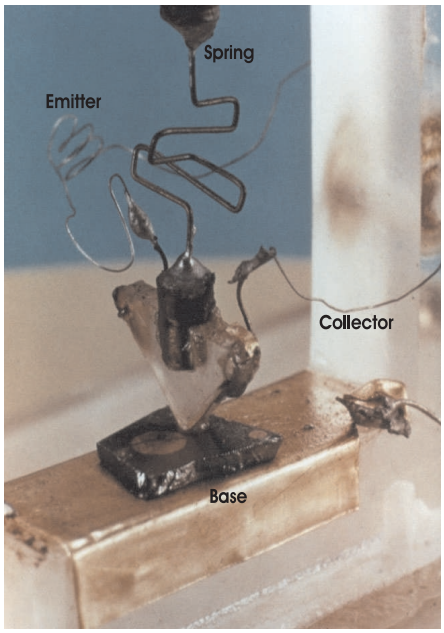


Fig. 2.1: The First Point-Contact Transistor.

Later, in 1950, Brattain, Schockley, Teal and Sparks succeeded in making the first npn bipolar device which validated the Shockley theory. Thus, they replaced the point-contact transistor by a monolithic technology, avoiding the important undesirable effects that occur at the semiconductor surface. Texas Instruments (1952) and Sony (1955) were born that time and they have been the first companies making transistors after the Bells' license. In 1952, Ian Ross and George Dacey realized a unipolar device called $JFET$ [11].

In 1957 an integrated circuit was developed by Jack Kilby from Texas Instruments [104]. Kilby solved the problem of the realization of a transistor, a resistor and capacitor on the same silicon chip, and they were interconnected by external wires. In 1959, Bob Noyce from Fairchild has "finished" the invention of Kilby, by interconnecting the on-chip components with metal thin films vapor-deposited on the surface of the SiO_2 used as dielectric above semiconductor. After this, many transistors were put on the same chip, and year by year, the technology has advanced, as predicted by Gordon Moore.

Nowadays, these chips can be seen in computers, video cameras, cellular-phones, copy machines, jumbo jets, modern automobiles, manufacturing equipment, electronic score-boards and video games.

The first field-effect transistor named $MOSFET$ was fabricated in the years of 1960 by Duane Kahng, by using Atalla's oxidation process. After the identification of sodium ions as the source of threshold voltage instability, the progress of MOS transistor technology has been accelerated.

In November 1971, the world's first single chip microprocessor, called Intel 4004, was invented by Federico Faggin, Ted Hoff and Stan Mazor from Intel company. They developed it with 2300 transistors in an area of only 3 by 4 mm.

2.1.2 Technology Roadmap from Bulk MOSFET to SOI MOSFET

Nowadays, the silicon chips and integrated circuits are everywhere, from industrial process control, till automotive and consumer electronics/wireless communication. The consumer electronics is a strong driver today, asking for smaller, faster, low power IC and with many functions implemented on the same chip, including wireless portable applications. The IC are expected to satisfy the society needs in all the fields, where health, mobility, security, communication, entertainment and education are just examples [127].

The Moore's law dates back to 19 April 1965 and it was presented in the article "Cramming more components onto integrated circuits" published in the *Electronics* magazine, by McGraw-Hill editure [104]. Its author, Gordon E. Moore predicted that the number of transistors per each integrated circuit chip (the so-called microprocessor performance) would continue to double periodically, at every 24 months. So that, a memory with a density of 65000 components was in production at Intel, ten years later, in agreement with Moore's prediction. Based on Moore's law, as the transistor number increases, the feature size is continuously shrinking until a value of 14 nm in 2020, as it is shown in Figure 2.2. As shown in the same figure, the transition from micro-technology to nano-technology and nano-electronics has already happened in 2002. Also, as predicted by Moore, the speed of the circuit increases, while the cost is drastically reduced during the down-scaling process [19, 43].

Figure 2.3 presents new features of integrated electronics after the technology node of 130 nm, where to the miniaturization process ("More Moore") obeying the Moore's law, the diversification process in terms of "More Than Moore" is added. The concept of "More than Moore" was introduced in the 2005 road-map and refers to new devices that are based on different technologies, including silicon technology and which do not compulsory follow the conventional scaling given by Moore's law. The More than Moore provides many functions as follows: wireless communication, power control, sensors, actuators, $MEMS$. However, one challenge is the integration of $CMOS$ and non-$CMOS$ based technologies within a single package. "More than Moore" consists of multi-functional

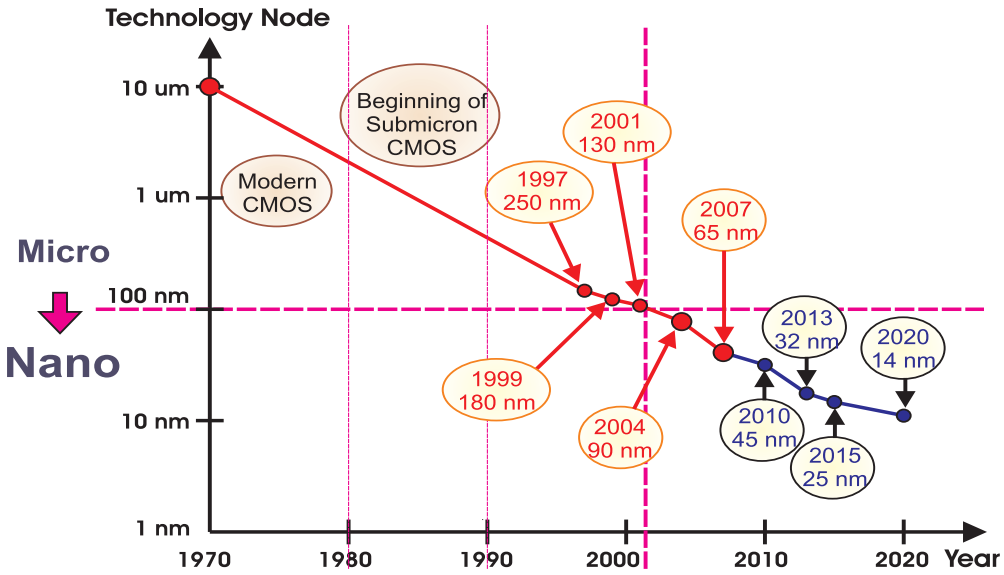


Fig. 2.2: Road-map for the Feature Size (source: $ITRS$).

system in the package (SiP) and $3D - MEMS$ technology bringing in the same package hybrid technologies for complex interaction with people and environment. The "More Moore" concept refers to a further scale down of $CMOS$ technology. Moreover, in the same time, it was possible the transition from the planar structure to non-planar three-dimensional devices such as multi-gate silicon on insulator configurations [19].

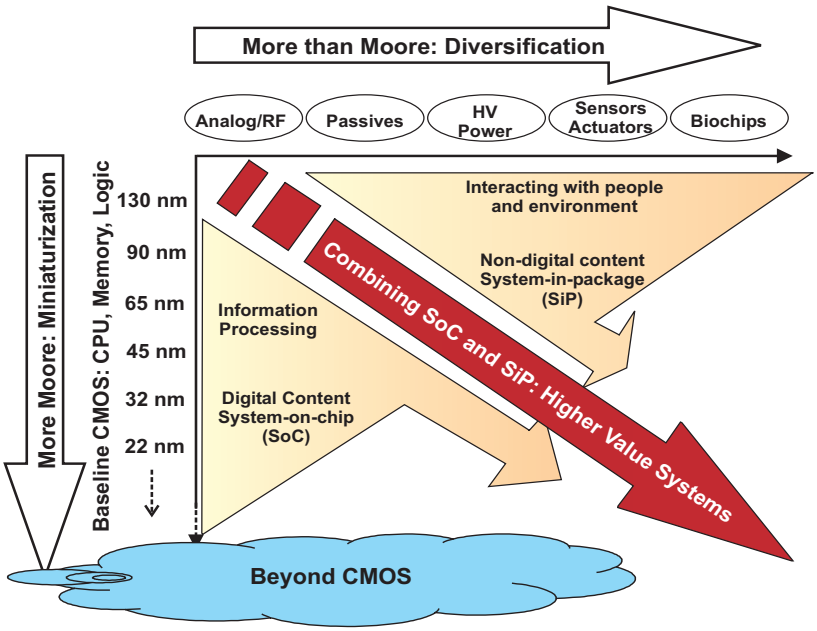


Fig. 2.3: Moore's Law and More (source: $ITRS$ 2007)

Based on Moore's Law and following the scaling rules, in Figure 2.4, it is shown the dependence of transistors number and operating frequency of the microprocessors, re-

spectively, as a function of time. An increase in transistor density results in an enhanced on-chip logic functionality. Also, the microprocessor is evolving into a "multi-core" era ($CORE\ II$) in which multiple CPU stages are integrated on the same monolithic die. On the other hand, one can see that the operation frequency has almost doubled at every 2 years and, thus, millions of instructions per second can be accomplished [4, 9].

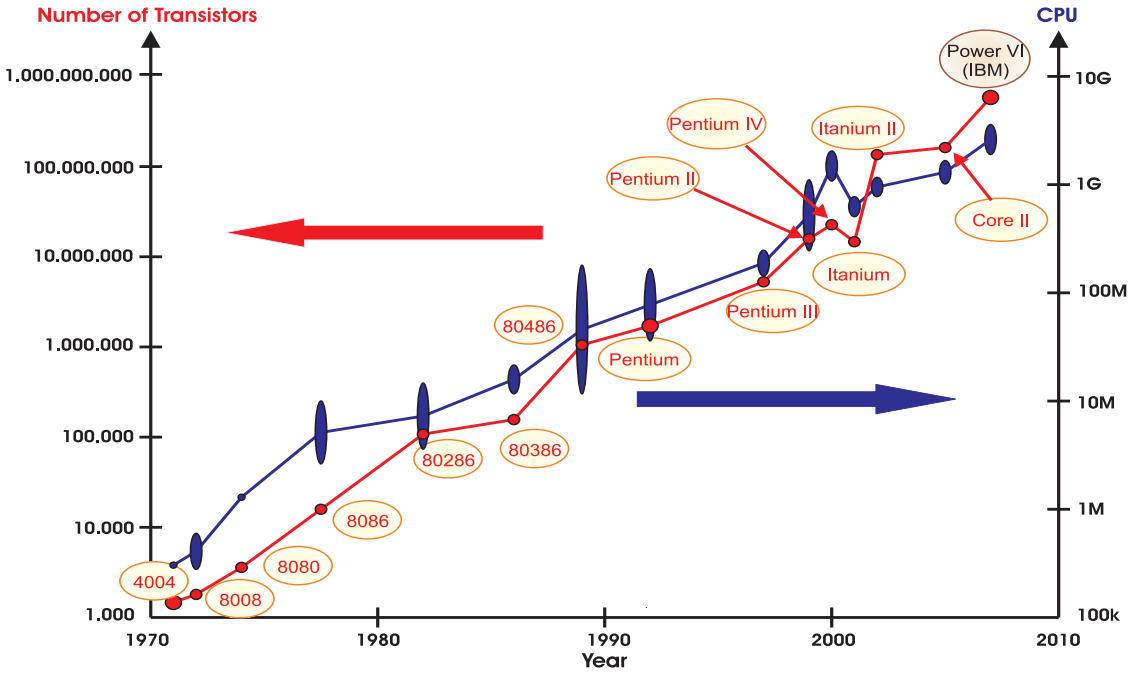


Fig. 2.4: Microprocessor and Frequency Roadmap (source: $ITRS$).

Preserving the transistor performance with scaling down was the key of microelectronics technology evolution and its success. The classification of scaling approaches and their evolution in time is presented in Table 2.1. The thumb rule of scaling consisted in the reduction of device size under constraints of keeping the electric field in the silicon or silicon dioxide to such values as to avoid increased leakage current in MOS transistors, or, in the worst case, avoiding the breakdown fields in Si or SiO_2 materials. Depending on the scaling approach, the electric field in silicon can be constant or variable [39, 42].

The first scaling law called "constant-field scaling" was developed by Robert Dennard from IBM in 1974 ($IEEE$ Journal of SSC), as presented in the third column of the Table 2.1. The electric field is kept constant, while the geometries and voltages are reduced by a scaling factor λ. The scaling lowers the current drive and switching delay time by the same coefficient λ and the power dissipation by λ^2, while the doping becomes λ times higher than th one from the previous node. Unfortunately, because of the dramatically decrease in the bias voltage, this law has not been efficient anymore for gate lengths smaller than $1\ \mu m$. Under this consideration, in 1984 Bacarani, Wordeman and Dennard [109] from IBM introduced a generalized scaling law in which the voltages are reduced by another factor k that is smaller than the geometry factor λ as shown in the fourth column of Table 2.1. The generalized scaling law determined a slower decrease in

Parameter	Notation	Constant-Field	Generalized-Field	Constant-Voltage
Physical Dimensions	W, L, t_{ox}	$1/\lambda$	$1/\lambda$	$1/\lambda$
Doping Concentration	N_B	λ	λ^2/k	$\lambda^2/1$
Voltage	V_{DD}, V_{th}	$1/\lambda$	$1/k$	1
Electric Field	E	1	λ/k	λ
On-Current	I_D	$1/\lambda$	λ/k^2	λ
Capacitance	$C_G = A \cdot \frac{\varepsilon_{ox}}{t_{ox}}$	$1/\lambda$	$1/\lambda$	$1/\lambda$
Power Dissipation	$V_{DD} \cdot I_D$	$1/\lambda^2$	$1/k\lambda$	$1/\lambda$
Gate Delay	t_{gate}	$1/\lambda$	k/λ^2	$1/\lambda^2$

Tab. 2.1: Scaling law table (source: [45]).

the value of supply voltage, which was followed by an increase in the electric fields, still in the tolerable range with respect to leakage current increase. However this generalized scaling law was not acceptable for technology nodes going below $1/4$ micrometers, due to the same reasons of imposing too low supply voltages with scaling down. Thus, the final scaling law, called scaling down at constant voltage was introduced, and this was kept down the road from $1/4$ micrometers to the present nodes of 32 nm and below, as shown in the fifth column of Table 2.1. This last scaling law determines continuous doping concentration increase and accelerates further decrease in power dissipation and gate delay time, helping the permanent increase in operation frequency of microprocessors, as described in the previous figures.

In accordance with the scaling rules, in Figure 2.5, it is illustrated the dependence of bias V_{DD} and threshold voltages V_{th} as a function of time. As shown in this figure, the bias voltage is allowed to vary slightly from $1.2\ V$ to $1\ V$, while the scaling goes on in the time interval from 2005 to 2011. Therefore, the transistor threshold voltage has to be reduced to about $0.5\ V - 0.6\ V$ to maintain a high drive current and achieve performance improvement. Till the end of the road-map, this voltage will not go below $0.45\ V$, due to the transistor control reasons. However, there is a trend towards substantially increased values of the leakage current.

In digital electronics, for a $CMOS$ circuit, the total power consumption contains both dynamic and static (leakage) components during the active mode of operation. As it was written above, as the $MOSFET$ channel length is scaled down, the power supply voltage must be reduced in accordance with Figure 2.5 in order to preserve the power density within reasonable limits. The mathematical expressions for the power components are shown below:

$$P_D = \frac{C}{2} \cdot f \cdot V_{DD}^2 \tag{2.1}$$

$$P_{LEAK} = I_{LEAK} \cdot V_{DD} \tag{2.2}$$

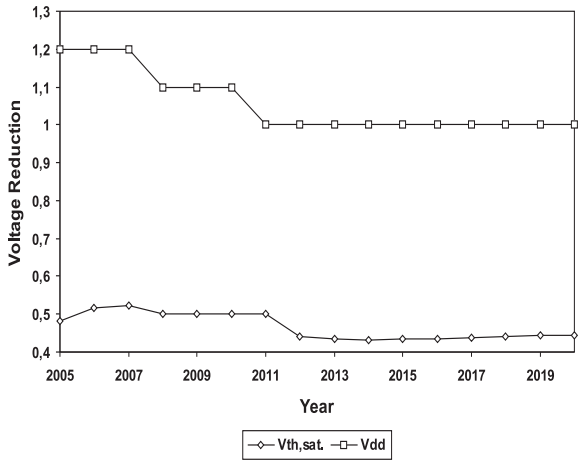


Fig. 2.5: Voltage Roadmap (source: $ITRS$).

where f is the operation frequency, C is the load capacitance and I_{LEAK} represents the total leakage current due to all the components of leakage mechanisms.

In general, the static power (or leakage power - P_{LEAK}) represents the power quantity used to hold a $CMOS$ circuit in one logic state or the other and is given mainly by leakage currents and power supply. The dynamic power (or switching power - P_D) appears every time a logic circuit changes its previous state, due to the charging and discharging of capacitance. In order to suppress the power consumption in low-voltage circuits, the static power must be reduced in both active and standby modes of operation.

In parallel with bulk $CMOS$ technology, the "surface" $CMOS\ SOI$ technology has been improved gradually. Figure 2.6 shows the silicon on insulator (SOI) $MOSFET$ family tree [26, 27].

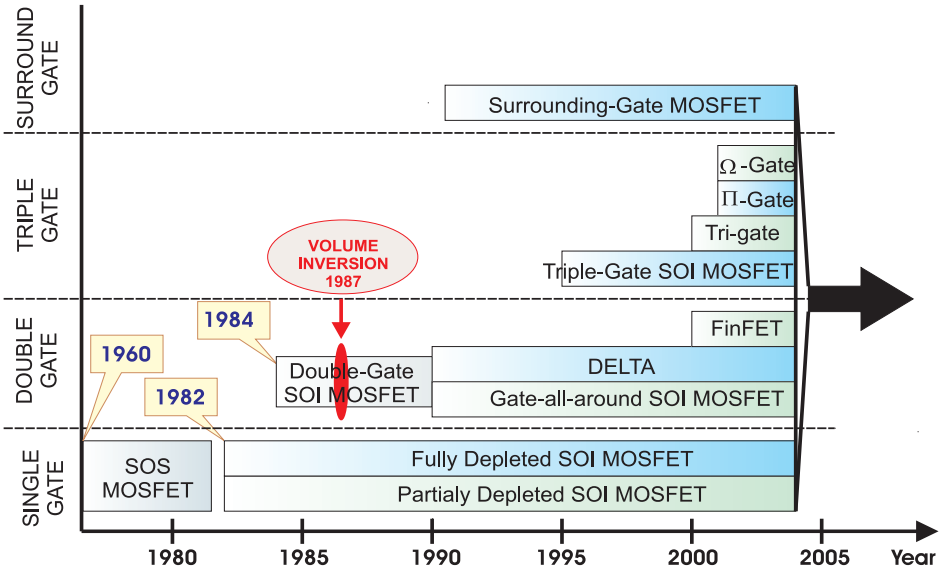
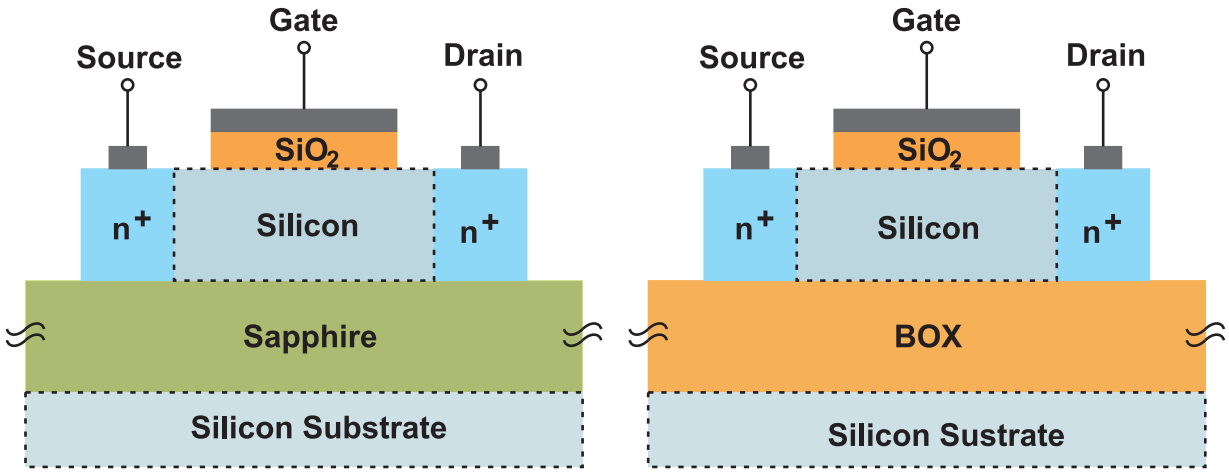


Fig. 2.6: $SOI\ MOSFET$ Roadmap (source: [27]).

One can observe that the first Silicon On Sapphire (Al_2O_3) SOS transistor dates back to 1960 (Figure $2.7a$) where sapphire stood as insulator. It was called UltraCMOS and invented at North American Aviation (now Boeing), California by Harold Manasevit and William Simpson [50]. Its first commercial application was in the late 1970 in a Hewlett-Packard 41-Series calculator.



(a) Silicon on Sapphire (source: [50])

(b) Silicon on Insulator

Fig. 2.7: A cross view of a silicon on insulator transistor.

The silicon on sapphire (SOS) presented several advantages in terms of: low power consumption and high insulating sapphire substrate. However, SOS wafers were much more expensive than bulk silicon wafer. Yet, SOS technology was used in RF wireless communications and space applications.

As shown in Figure 2.6, after $SOS\ MOSFET$ transistors worked well for about 20 years, Partially Depleted (PD) and Fully Depleted (FD) Silicon On Insulator $SOI\ MOSFET$ have been invented at early 1980 years and applied for microprocessors and memory chips and thus the sapphire (Al_2O_3) mono-crystalline substrate (Figure $2.7a$) was replaced by a silicon dioxide layer (BOX - buried oxide) grown on silicon substrate - see Figure $2.7b$. Due to the reduced area of source and drain region, the absence of depletion region under source and drain (doped silicon region touches the oxide), the $SOI\ MOSFETs$ have low leakage currents and low junction capacitances and thus, they are useful in very low-power low-voltage applications, radiation hardened circuits. The $FD\ SOI\ MOSFET$ transistors possess better characteristics than $PD\ SOI\ MOSFET$ transistors, because they have almost ideal sub-threshold slope, reduced body effect, improved current drive and further improved frequency characteristics. It was shown that fully-depleted $SOI\ MOSFET$ offered better transconductance, higher current drive and improved sub-threshold swing. Also in 1984, the era of multiple-gate silicon on insulator $MOSFET$ devices has been started.

Actually, in 1984 a double-gate (DG) $SOI\ MOSFET$ was presented in an article written by T. Sekigawa and Y. Hayashi [105]. At that time, the device had the acronym of $XMOS$ and exhibited good short-channel characteristics. The DEpleted Lean-channel

TrAnsistor ($DELTA$) was the first fabricated $DG\ SOI\ MOSFET$, with vertical silicon film and $FinFET$ appeared later in 1999. A very important feature for such fully-depleted SOI devices is the volume inversion, discovered in 1987 [6]. The improved transconductance due to the volume inversion was theoretically predicted by the team of Cristoloveanu, in 1987 [6], and proven experimentally on a planar multiple-gate $MOSFET$, named Gate-all-Around $SOI\ MOSFET$.

As shown in Figure 2.6, the surrounding gate and Gate All Around (GAA) $SOI\ MOSFET$ appeared at the beginning of 1990 for better control of short channel effects due to gate voltage applied all around the channel. In most of these cases, it is actually a single gate going on the third dimension and creating a $3D$ control of the channel voltage. In the same idea of short channel effect control, in Figure 2.6, there are shown different types of gates like Triple-Gate, Ω-gate, Π-Gate, which appeared after the year 2000. The surrounding-gate $SOI\ MOSFET$ appeared in 1991 and provided best gate control of the channel region, from theoretically point of view. During this scaling down journey of more than 40 years, many roadblocks appeared in the design and technology of bulk $MOSFET$ transistors due to leakage currents increase and short channel effects threatening the miniaturization process. As shown below, deep physical understanding of the solid state processes allowed the steadily evolution as Moore predicted, early 1965.

2.1.3 Leakage Current Effects of Down-Scaling Bulk MOSFET Devices

The key leakage currents evolution by the scaling of bulk $CMOS$ into nanometer regime are going to be shortly examined in this section. Figure 2.8 illustrates the leakage current mechanisms in a bulk $nMOSFET$, while this is scaled down to nanometer range [101]. As shown in Figure 2.8, they are in terms of: the reverse-bias pn junction leakage (I_1), the sub-threshold leakage (I_2), the gate oxide tunneling leakage(I_3), the leakage given by the injection of hot carriers from substrate to gate oxide (I_4), the gate-induced drain leakage (I_5) and the channel punch-through current (I_6). It is important to note that the off-state leakages are I_2, I_5 and I_6. I_1 and I_3 are provided in both ON and OFF states, while I_4 occurs in the transition state of transistor. Further, each mechanism will be briefly described, by emphasizing their origins and overcoming solutions.

The reverse-bias pn junction leakage (I_1):

In bulk $MOSFET$ device, the pn junctions such drain/bulk and source/bulk junctions are typically reverse biased, providing pn junction leakage current - the current I_1 from Figure 2.8. In scaled devices, both regions n and p are highly doped and thus, band to band tunneling ($BTBT$) process becomes a significant phenomena, dependent strongly on the applied drain/source voltage [17]. The depletion region is extremely thin, allowing the electrons to tunnel from the valence band of the p region to the conduction band of the n region [101].

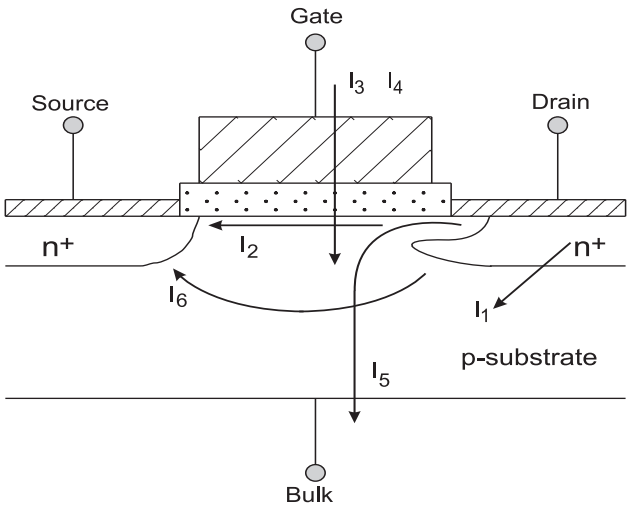


Fig. 2.8: Summary of leakage current mechanisms of deep-submicrometer transistors (source: [101]).

The sub-threshold leakage (I_2):

The quality of a MOS transistor as a digital switch can be described by the rapid drain-source current decrease when the gate voltage is set below the threshold voltage. As the threshold voltage has been continuously decreased over the years, and now this value is around $0.5\,V$, this leakage current is of paramount importance for dc power dissipation of transistor, if we think that, now, the gate voltage excursion from ON state to OFF state is low, and the current decrease should be very sharp, as we need a low power consumption in the OFF state. The sub-threshold leakage is actually the current flowing through the $MOSFET$ transistor, when its channel region is in the week inversion regime. The sub-threshold current is a diffusion current, due to the gradient in the (electron) minority carrier concentration along the source and drain, at the silicon surface, in the region of the "future" channel. This drain-source current has an exponential dependence on gate voltage, below threshold.

In order to describe the efficiency of transistor, the concept of sub-threshold swing, S, is used and defined as the inverse of the slope of the $log_{10}I_{DS}$ versus V_{GS} characteristic. The smaller the swing, the lower the voltage excursion needed to change the logic state. The ideal value of S is approximately $60\ mV/decade$. This swing tells us what is the voltage variation necessary on the gate in order to get a current variation by a decade, in the sub-threshold region. Typically, in a bulk $MOSFET$, the values are ranging from 70 $mV/decade$ to $120\,mV/decade$. In order to improve the sub-threshold swing, two solutions could be used as follows: to reduce the oxide thickness for better gate control or decrease the substrate doping [101].

This sub-threshold leakage current is present in all $MOSFET$ transistors, but due to the scaling down processes and applied voltages (drain and gate voltage), in short channel-narrow width transistors, in addition to the "old" current components given by the "Body Effect", temperature variation, new scaling-driven sub-threshold components

have been identified as affecting this leakage because of the following effects: Drain Induced Barrier Lowering ($DIBL$), "Narrow-Width", "Channel Length and V_{th} Roll-off". They are described below.

When the drain voltage can increase the carrier density in the channel, at a sub-threshold constant gate voltage, before the punch-trough appears, then the phenomenon of drain-induced barrier lowering ($DIBL$) occurs [17, 42, 70, 101, 106]. Thus, the threshold voltage is reduced due to the application of a voltage to drain which causes a lowering of the source-channel potential barrier. In a long-channel device biased in the sub-threshold regime, the source and drain are separated far enough to avoid the dependence of threshold voltage on drain bias. However, in a short channel device, as a result of the applied drain-to-source voltage, the depletion regions of the source-substrate and drain-substrate junctions will interact near the channel surface. Thus, the barrier height between the two back- to- back junctions is reduced and an increased leakage current called Drain-Induced Barrier Lowering ($DIBL$) appears. Consequently, the threshold voltage is reduced and an increase in the leakage current as a function of drain voltage increase can be observed in Figure 2.9. From this Figure 2.9, we see that the sub-threshold slope is not changed when the drain voltage is changed. As technological solutions to reduce $DIBL$, one can consider increasing surface and lowering the junctions depths.

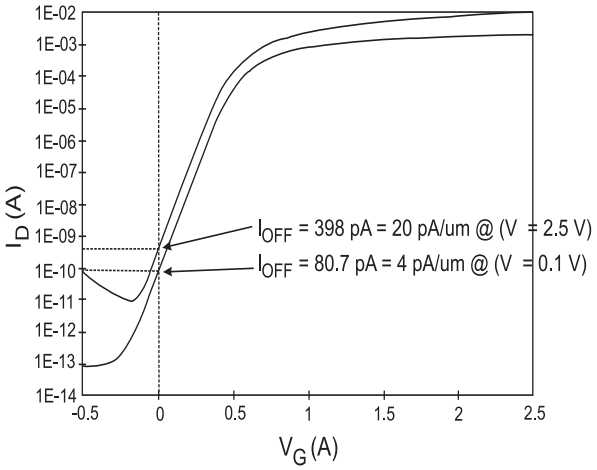


Fig. 2.9: Log(I_D) versus V_G at two different drain voltages ($0.1\ V$ and $2.5\ V$) for an $nMOSFET$. (source: [101]).

As in the case of long channel transistors, when the substrate has a potential more negative than the source, the reverse biasing substrate-to-source junction of the $MOSFET$ gives rise to a wide bulk depletion region and this will increase the threshold voltage. This is the so-called "body effect" and its influence is in the direction of decreasing the sub-threshold leakage as a function of substrate voltage [101].

A related effect of bulk $MOSFET$ miniaturization is observed in narrow-width effect [101], where the threshold voltage of transistor is modulated by the decrease of gate width. This modulation can occur in three ways for different types of MOS transistors: firstly, in terms of additional depletion charge created by the fringing field of the gate

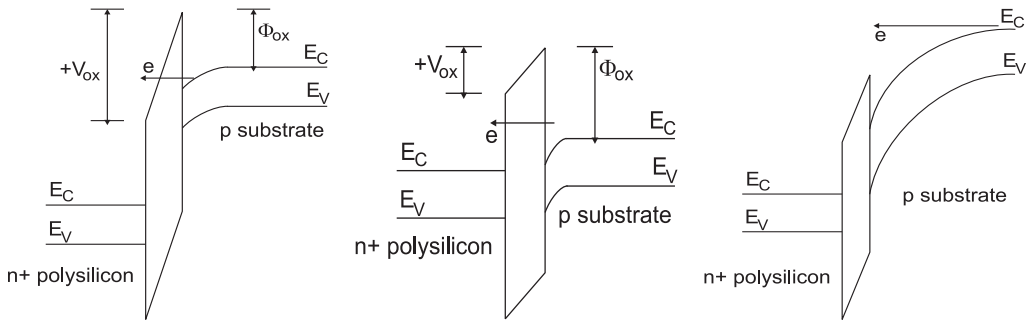
voltage, near source and drain, in the vicinity of $LOCOS$ oxides. This additional charge contribution is relevant at narrow width and thus the threshold voltage increases due to its effect. The second modulation comes from the raissed doping of silicon channel, due to the field implant (below $LOCOS$ oxide, to avoid parasitic transistors formed with thick $LOCOS$ oxides). This second component is further increasing the threshold voltage, so for the same gate voltage this part is reducing the sub-threshold current. The third modulation type is present in gates over thick oxides as in the trench isolation devices, where there is no fringing field effect, but where the oxide capacity is further extended by the gate overlapping over the thick oxide regions. An increased oxide capacity is diminishing the threshold voltage (as the C_{ox} is at the denominator of threshold voltage), and this is equivalent with sub-threshold current increase, for the same applied gate voltage.

As the channel length decreases, the threshold voltage is lowered due to the two-dimensional effects, according to which, the drain electric field is distributed through channel toward the source. Therefore, the gate voltage has a lower influence on the bulk charge inversion and the drain bias control becomes significant [101]. This reduction of threshold voltage as gate length scales down is called voltage threshold roll-off. Both voltage threshold roll-off and sub-threshold swing roll-up phenomena are known as short channel effects [20]. A common way to overcome this effect is to use super-halo implants in order to raise the channel doping [40].

The gate oxide tunneling leakage (I_3):

Due to the scale down a bulk $MOSFET$, the oxide thickness is reduced until a limit where the tunneling of electrons through the insulator from substrate to gate, or from the gate to the substrate becomes unavoidable. Therefore, the power consumption increases and leakage current becomes significant, due to the tunneling current through gate oxides. In general, there are two tunneling mechanisms through gate oxide. The first one is called the Fowler-Nordheim (FN) tunneling, in which, for example, the electron tunneling (through triangular barrier) occurs from silicon substrate to conduction band of the oxide and then the electrons will "fall down" to the conduction band of the gate electrode (Figure $2.10a$). This mechanism happens if electron energy is higher than energy barrier for electrons ($3.1\ eV$) and the electric fields in gate oxide is higher than $5-6\ MV/cm$. As such conditions are not present in short channel MOS transistors, the FN mechanism is not active in scaled down transistors.

The direct tunneling (DT) of electrons through trapezoidal energy barrier of ultra-thin gate oxide (around $2\ nm$) consists in electron trip from conduction band of one electrode to the conduction band of the other electrode, as shown in Figure $2.10b$ for DT of electrons from substrate to the gate. As can be proved from quantum mechanics theory, the DT is present at any voltage applied on the gate, if the gate oxide is thinner than $2\ nm$, which is required for scaling down process below $32\ nm$ node of silicon IC road-map. This direct tunneling current is increasing very much the current through the gate oxide and thus, reducing the input impedance of $MOSFET$ and growing the power dissipation in such



(a) Fowler-Nordheim tunneling of electrons. (b) Direct tunneling of electrons. (c) Injection of hot electrons from substrate to oxide.

Fig. 2.10: The gate oxide tunneling processes and the hot-carrier injection from substrate to oxide (source: [101]).

MOS transistors [101, 123]. The most common solution to reduce the oxide leakage is the replacement of SiO_2 by high-k dielectric (like HfO_2), which will preserve the oxide capacitance value needed from IC design reasons (threshold voltage, speed), but they will allow increasing the gate oxide thickness above $2\ nm$ so that the direct tunneling is eliminated. The equivalent oxide thickness of high-k dielectrics can be even below $2\ nm$, but with physical thickness above $2\ nm$ to avoid direct tunneling through them.

The gate current due to hot-carrier injection (I_4):

The effect of hot-carrier injection refers to the semiconductor devices where, due the high drain voltage, electrons or holes from substrate can gain enough energy (hot carriers) to overcome oxide potential barrier and, then, migrate to gate [99]. The energy band diagram of such device with high drain potential is shown in Figure $2.10c$, where electron injection to the gate is revealed. In a short-channel transistor, the electric field near the Si/SiO_2 interface is very high and provide sufficient gain for carriers to leave the substrate and they enter the oxide layer. Therefore, the "hot carriers" will generate I_4 current component and degrade the insulator causing the formation of traps and, thus, the leakage current appears [101].

The gate-induced drain leakage ($GIDL$) (I_5):

$GIDL$ current arises in silicon, below the gate, in the gate to drain overlap area due to the gate-induced high electric field from this region. Due to zero or increased negative gate voltage, an accumulated or even an inversion region (p type), respectively, can appear in the initial drain region, below the gate, which will change the electric field distribution in silicon, in that zone of $n - MOSFET$ transistors. Actually, depending on the initial drain doping level and drain voltage for an increased negative gate voltage, a field induced $p - n$ junction (FIJ) can appear below the gate, in the "old" drain region, where the electric field in the depletion area of that induced $p - n$ junction can be so high as to generate either band to band carrier tunneling in the field induced $p - n$ junction

(depending on the initial doping of the n-type drain region) or carrier multiplication in the depletion region of the FIJ. As there is a potential difference between the new born p-type surface and the substrate, the generated holes from the surface will migrate to the substrate. At initial low drain doping, the electric field appearing in the relatively large depletion region of the FIJ is not high and thus, the $GIDL$ is reduced. Similarly, if the drain doping is very high, even if the electric field in the depletion zone of FIJ is high, the overall volume of this depletion region is small and thus, the generated $GIDL$ are not considerable, which is a very good case. This is actually what happens with scaling process (the drain and substrate doping increases). In other words, the highest $GIDL$ currents are generated for intermediate doping of drain, when, at high electric field in the depletion region of FIJ, the $BTBT$ is large enough and the carrier multiplication can still happen. Further, these two above carrier generation mechanisms will run the $GIDL$ current, up to a maximum value (as the depletion area is large enough to contribute to a relevant $GIDL$). Also, the thinner oxide thickness and the higher supply voltage V_{DD} enhance the electric field and, then, give rise to $GIDL$ currents. In order to minimize this effect, it is desirable to realize a very high and abrupt drain doping [16].

The channel punch-through current (I_6):

Punch-through is a phenomenon that appears in the short channel devices where the drain is very closed to the source terminal. Because of this proximity, the depletion regions at the drain/substrate and source/substrate junctions extend into the channel. As the channel length decreases, the distance between the two above-mentioned depletion areas reduces for a constant channel doping. Therefore, a current flowing path is formed between the drain and the source below the surface, deep in the bulk, being poorly controlled by the gate terminal. Mainly, the leakage depends on the potential distribution under the channel and drain voltage. The principal effect of the punch-through leakage is in the sub-threshold regime through the degradation of sub-threshold slope. Thus, it leads to an increased of power consumption [101]. The methods used to reduce the punch-through effect are to enhance the overall substrate doping or halo implant.

In order to illustrate how the performance is influenced by the short channel effects, Figure 2.9 shows a typical curve of drain current (I_D) as a function of gate voltage (V_G) in logarithmic scale. It does worth to noticing a significant amount of drain leakage current (I_{OFF}) increase due to the $GIDL$ component, near zero V_G, which increases when V_D rises and V_G enhances, in absolute value. As it was mentioned above, the $GIDL$ leakage current is influenced by the channel doping profile, gate oxide thickness (t_{ox}), drain/source junction depth, channel physical sizes (L, W), threshold voltage (V_{th}) and bias voltage (V_{DD}). The $DIBL$ current component can be also seen as a drain current increase, in the sub-threshold region when the drain voltage grows from $0.1\ V$ to $2.5\ V$. The $nMOSFET$ transistor from Figure 2.9 presents a current I_{OFF} of $20\ pA/\mu m$ and $4\ pA/\mu m$ at the drain voltage of $2.5\ V$ and $0.1\ V$, respectively.

Over the past three decades, many improvements in circuit performance and cost per

function have been achieved when the transistor channel length reduces with each new generation of manufacturing technology. Unfortunately, the transistor scaling will not be able to follow the simple theory of down-scaling as it has been in the past, because of the above-mentioned limitations in materials and processes. So that, even if planar Si $MOSFET$ with gate length down to $10\,nm$ and SiO_2 gate oxide have been demonstrated, they do not seem to appear practical due to the direct tunneling high leakage, as already presented. Therefore, future progress can continue with new materials such as high-k dielectric [114], self-aligned silicide [18] or metal gate materials (such as Molybdenum) [17] and device structures in terms of strained silicon structures [47, 70] or non-planar multiple-gate ultra-thin body $MOSFETs$.

2.2 Multi-Gate SOI MOSFET Devices

2.2.1 SOI Technology

The silicon on insulator (SOI) technology has become a very attractive alternative to replace the bulk $CMOS$ technology, when the down-scaling process of conventional bulk $MOSFET$ transistor reached the limits in terms of device miniaturization and fabrication. The silicon wafers are still maintained to be the starting point in the fabrication of integrated circuits because of their costs compared to other semiconductors. Also, a good oxide can be already grown on silicon [52].

The main motivation for the use of SOI technology to the end of the silicon technology road-map is given by the possibility to attain increased scalability, very high operating frequency, low leakage currents and radiation hard operation in different applications due to the existence of buried oxide. It is limiting the depletion region extension to the substrate and thus, decreasing leakage current, parasitic capacitances and silicon volume where charge generation lowers considerable due to radiation specific to bulk silicon. Also, the ease and flexibility in scalability beyond the limits of the bulk $CMOS$ technology could constitute an important feature in the evolution of devices miniaturization, and this has been obtained by replacing the continuous doping of substrate as the thumb scaling rule with the scaling law based on continuous thinning of silicon film above buried oxide [29, 36]. Compared to bulk $CMOS$ processing, SOI technology provides many advantages in terms of: higher frequency operation due to a lower parasitic capacitance, lower electric power dissipation due to lower leakage currents and radiation hard capabilities. The manufacturing compatibility with the existing bulk silicon $CMOS$ technology represents a very important benefit for the SOI technology because of the need to keep the cheap silicon semiconductor as the base technology while innovating future device. On the other hand, thanks to the novel devices (like dual gate $DG\ SOI$ $MOSFET$ transistors) performed in the innovative SOI technology, the short channel effects are considerable reduced leading to a higher sub-threshold slope [35, 52].

However, due to floating body effect, where the silicon substrate below the gate is not connected to any external electrical potential, there are several undesirable effects for silicon on insulator technology, especially for partially depleted SOI devices (where a neutral region between the upper and lower silicon interface still exists). They are in terms of drain current overshoot, kink effect (at high drain voltage, for transistor operating above threshold), latch effect (for $SOI\ MOSFET$ transistor operating in the sub-threshold region), self heating phenomena (due BOX oxide making a good thermal isolation toward the Si substrate), difficulties of Si thickness control for ultra thin Si films. Also, a parasitic lateral bipolar transistor comes into being from the source-body-drain. When it is activated, extra current appears and premature breakdown might occur. This bipolar transistor effect can be reduced when the device shrinks, the silicon film becomes thinner and the channel is n-type [29]. In short channel SOI, a fringing field effect, due to the field termination on the BOX oxide and back substrate generates a virtual bias of the back gate because of the drain voltage. In addition to the $DIBL$ and charge sharing effects, this further decreases the threshold voltage. Largely due to the presence of more than one oxides and channels and an additional buried oxide, the hot carrier degradation is more complex in SOI devices than bulk $MOSFETs$.

2.2.1.1 Volume Inversion

Volume inversion was discovered in 1987 [6] and re-confirmed later in a more refined gate all around (GAA) $MOSFETs$ in 1990, by Collinge [27]. Thus, in Figure $2.11a)$, Balestra has shown a fully depleted Si film for a front gate voltage of $2\ V$ and a back gate voltage of $20\ V$, for the associated transistor data, from that figure. In Figure $2.11b)$, it is presented that a volume inversion was discovered for a slightly doped Si film thickness of $100\ nm$ and the following data: the front gate oxide thickness of $27\ nm$ and the back gate oxide (BOX) of $380\ nm$, the front gate voltage of $1\ V$, and the back gate voltage of $10\ V$. For V_G equal to $-1\ V$, the entire silicon film is accumulated, while an enhancement in gate voltage provides an increase in the electrostatic potentials at the surfaces and also in the volume of silicon film. When V_G reaches the value of $0.6\ V$, the overall film is under inversion.

The entire silicon film is under strong inversion condition when:

- $t_{Si} < 0.02\mu m$ where t_{Si} is the silicon thickness;
- low doping (a few $10^{15} cm^{-3}$).

It has been proven that the volume inversion is one of the biggest discovery of the last decades in $MOSFET$ evolution, determining the best value for the sub-threshold slope (near $60\ mV/decade$). This is due to the strong electrostatic control in the channel, the increased current drive, the absence of drain current transients and the maximum mobility values given by the shift of the channel from the surface to the Si bulk. Finally, for the

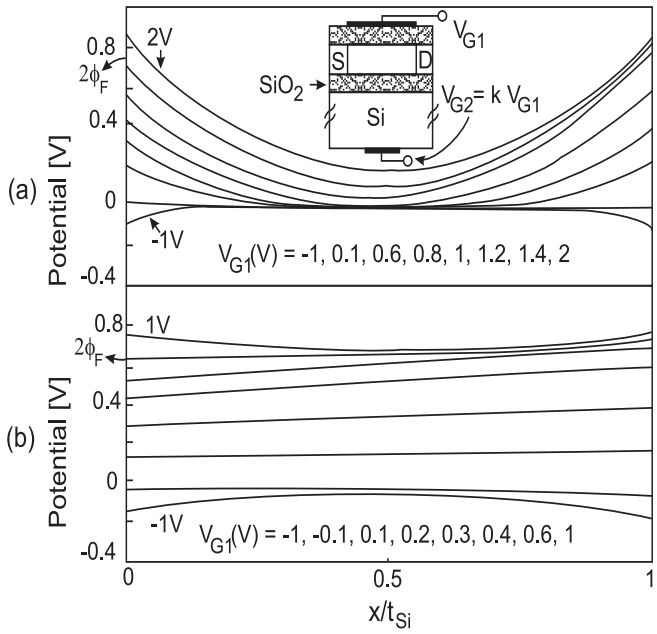


Fig. 2.11: Potential Profile inside the Silicon Film for (a) un-coupling interfaces (doping $N_A = 4 \cdot 10^{16}\ cm^{-3}$, film thickness $t_{Si} = 300\ nm$) and (b) coupling interfaces ($N_A = 3 \cdot 10^{15}\ cm^{-3}$, $t_{Si} = 100\ nm$). x is the distance from the front interface (source: [6]).

minimum thickness of Si film below $5\ nm$, a maximum transconductance is obtained in the range of impacts on carrier profile in the film, providing an indirect improvement of the effective mobility [36]. Thus, the current drive capability and outstanding transconductance gain are raised.

2.2.2 SOI MOSFET Devices

$SOI\ MOSFET$ devices can be classified as a function of the thickness of silicon layer into two big classes: partially-depleted (PD) and fully-depleted (FD) $SOI\ MOSFETs$. They are going to be described further.

2.2.2.1 Partially Depleted SOI MOSFET

Figure 2.12 shows a partially depleted silicon on insulator $MOSFET$ device. It is defined as a $MOSFET$ transistor realized with SOI technology and in which the depletion region does not extend in the whole silicon film of SOI and therefore, a neutral region of the Si layer will survive, even after biasing the device in the inversion inversion. Thus, the silicon film thickness is greater than the maximum gate depletion width. The neutral region of silicon is called ”body”.

In partially depleted $SOI\ MOSFETs$, if the body of the transistor is not connected to an external potential, then the floating body effects appear. One of these is the ”kink effects” arising at high drain to source voltage due to the majority carriers generated by

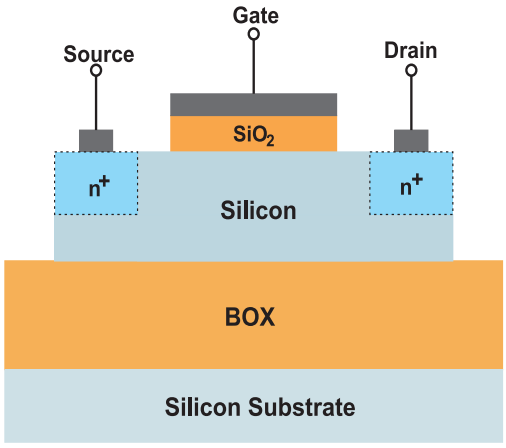


Fig. 2.12: A cross view for a partially depleted $SOI\ MOSFET$ (source [29]).

the impact ionization and collected in the body. These carriers are biasing directly the source-substrate junction and thus, the threshold voltage decreases [29]. This is depicted as a kink in the output characteristics of $SOI\ MOSFET$. Other specific parasitic effects are related to the transient drain currents (overshoot and undershoot) at transistor switching, self-heating and latching (in the sub-threshold regime).

2.2.2.2 Fully Depleted SOI MOSFET

In Figure 2.13, a fully depleted $SOI\ MOSFET$ is depicted. For it, the silicon thickness should be lower than the gate depletion width. Therefore, the entire silicon film is under depletion even before the threshold voltage drops on the gate and, thus, floating body effects are eliminated [29, 35]. The buried oxide must be very thick in order to drastically reduce the junction capacitance [108]. However, the BOX thickness is also exposed to scaling process and lowers for a better electrostatic control of the multi-gate $SOI\ MOSFET$ transistors, at the cost of increased parasitic capacitances and circuit speed decrease, anyway.

Another particularity of a $FD\ SOI\ MOSFET$ transistor refers to the channel doping which should be very light, leading to a negligible concentration of carriers. Such a device gives additional advantages in terms of reduced short channel effects and volume inversion. However, from the technology point of view, a very thin silicon film is difficult to be realized with accuracy.

2.2.3 Classification of Multi-Gate SOI MOSFET Devices

In order to reduce the short channel effects, silicon-on-insulator MOS transistors are evolving from classical planar, single-gate devices to the three-dimensional configurations with multiple gates (double, triple or quadruple gates). Thanks to the presence of more than one gate (2 to 4), these configurations have excellent electrostatic control,

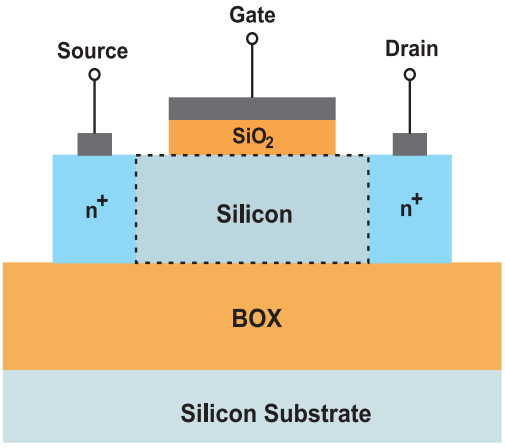


Fig. 2.13: A cross view for a fully depleted $SOI\ MOSFET$ (source [29]).

leading to reduced short channel effects and improved sub-threshold slope which reach even the ideal value of $60\ mV/decade$ as shown in Figure 2.14. Because the multiple-gate $SOI\ MOSFETs$ are fully depleted devices, the entire silicon layer is depleted and the condition of volume inversion is achieved.

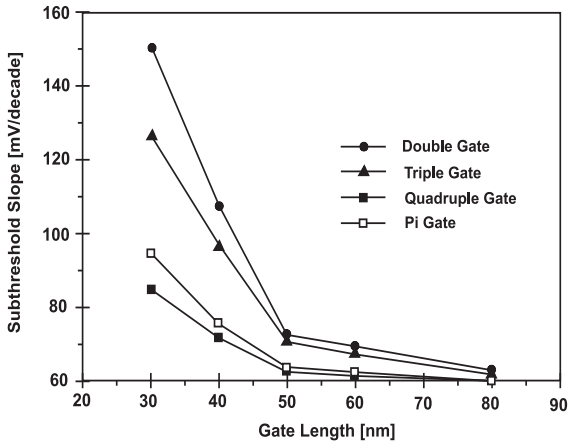


Fig. 2.14: Sub-threshold slope in a multiple-gate SOI MOSFET as a function of gate length (source: [26]).

Also, the channel is un-doped or lightly doped and thus, the fixed charge becomes negligible. Thus, no random fluctuations occur and carriers mobility improves due to the reduced impurity scattering. A solution to scale down the doping level is sustained by the adjustable silicon film thickness. For a device with a number N of gates and a channel length L, the body size should be $NL/4$ in order to obtain acceptable short channel effects [30]. In addition, they are influenced by the electric field lines from source to drain that are extremely high for a bulk device. As much as the number of gates increases, the electrostatic control is improved. In order to have a deep understanding of such a phenomenon, there is a concept of "natural length" which is defined as the length of the region of the channel controlled by drain. If the channel length of the device is 5 to 10 times larger than the natural length, the short channel effects are negligible [28].

However, the technology is very complex because of the three-dimensional technological approach. Besides, it is hard to achieve the alignment of the gates [27].

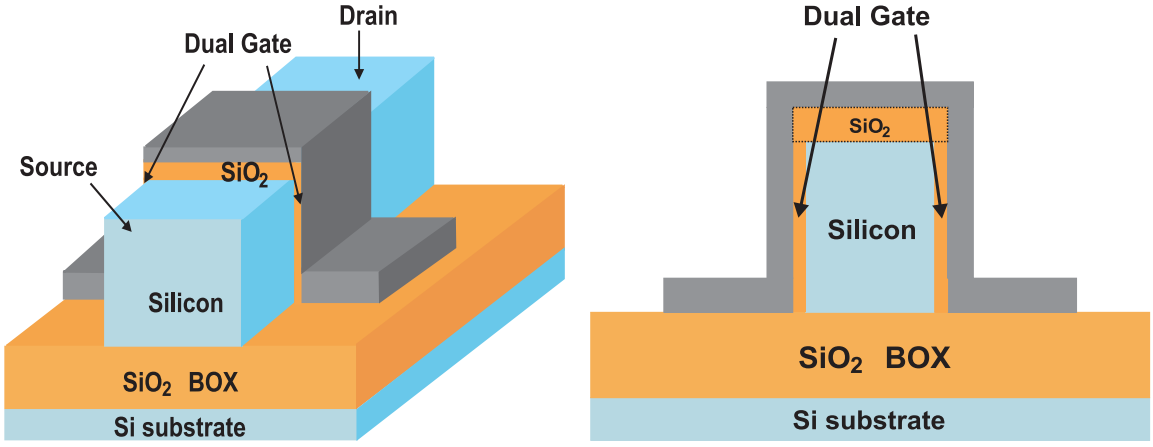
A key challenge consists of the silicon thickness that is hard to be estimated due to the quantum effects introduced for values lower the $5nm$ [36]. In order to support this idea, Monte Carlo simulations have been done for a dual-gate n-channel $SOI\ MOSFET$, with gate length of $30\ nm$ and channel thickness of $5\ nm$ [38]. It does worth to noticing that the obtained transconductance equals to $2300\ mS/mm$ and makes the device to be suitable for digital circuitry, even at Si film thickness below $5\ nm$.

In literature, many forms of multiple gate devices can be found but the most representative structures will be presented further.

2.2.3.1 Double-gate SOI MOSFET

Double gate $DG\ SOI\ MOSFET$ transistors can have either planar configuration with current flowing parallel with the surface (when the back gate transforms into the substrate or is embedded in BOX for fully depleted configuration) or $finFET\ 3D$ configuration (when the two active gates and channels are vertical).

Figure 2.15 shows the schematic view and cross section of a $finFET$, dual-gate (DG) $SOI\ MOSFET$ transistor in which the channel is vertical. The structure is built in silicon on insulator technology, where a silicon film, called "fin", is covered by poly-silicon electrode. In order to have two channels only, the top gate is not activated by growing a thicker gate on the top side of the fin.



(a) $3D$ Schematic view of a $DG\ SOI\ MOSFET$ (b) Cross-Section View of a $DG\ SOI\ MOSFET$

Fig. 2.15: A Double-Gate $SOI\ MOSFET$ (source: [27]).

In literature, it has been proven that two gates are better than one because they provide much greater control of charge in the channel, leading to a mobility enhancement and reduced short channel effects [109].

Figure 2.16 illustrates the influence of silicon doping and of the device type on the subthreshold slope. All the devices have a silicon thickness of $10\ nm$ and a channel length of

$0.05\ \mu m$. One can observe that the sub-threshold swing decreases when a second gate is in accumulation. When the $DG\ SOI\ MOSFET$ is used, the gates electrodes are linked and lead to a volume inversion in the silicon film. Therefore, the sub-threshold slope is ideal for a very low doping in the silicon as it is illustrated for $DG\ SOI\ MOSFET$.

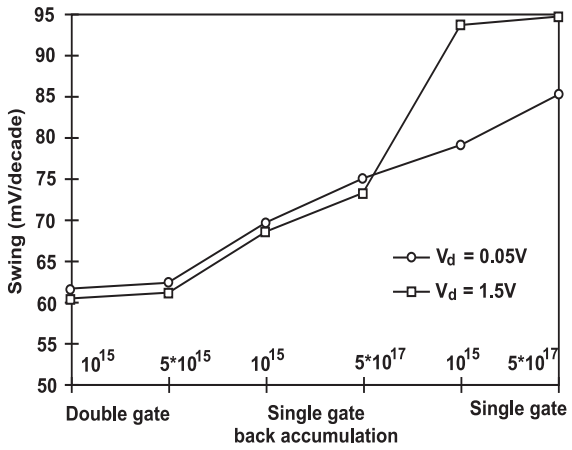


Fig. 2.16: Sub-threshold Swing for various types of extremely thin $SOI\ MOSFETs$ with ($V_{G2} = -40\ V$) and without back gate accumulation ($t_{ox1} = 3\ nm$ and $t_{ox2} = 0.38\ nm$) and with a double gate structure for various doping (source: [97]).

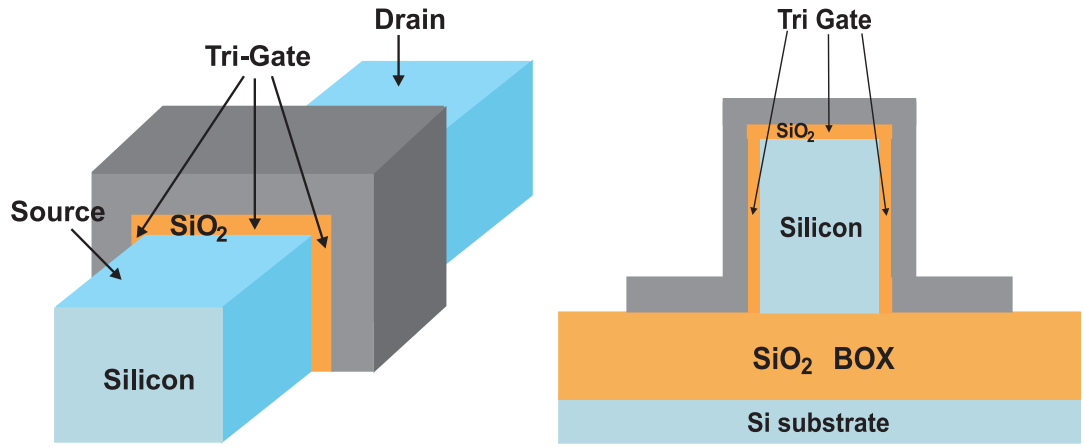
Another advantage of $DG\ MOSFETs$ consists of the ability to set the threshold voltage of the device by selecting the metal gate with the suitable work function. Beside the function of the two gates to drive more current, they can be separately biased and used independently in such a way that, they achieve increased logic function from a single FET [107, 30].

However, the manufacturing challenges make difficult the realization of a planar $DG\ SOI\ MOSFET$. Key technology aspects are in terms of the controlled thinning of the Si film and patterning the crystalline silicon film, which requires advanced lithography. The choice of gate material with mid-gap work function is hard to be accomplished. It seems that TiN gate represent the solution for mid-gap electrode keeping in a good range the threshold voltage of both $n-MOS$ and $p-MOSFET$ transistors. Another manufacturing issue is the realization of the source and drain regions while maintaining the electrical resistance low enough.

2.2.3.2 Triple-gate SOI MOSFET

Figure 2.17 shows the configuration of a triple-gate $FinFET\ TG\ SOI\ MOSFET$ device in terms of schematic view and cross section of it. One can observe that the transistor is a three dimensional structure and has similar form as $DG\ FinFET$, in which a polysilicon layer surrounds a thin silicon film, on all its sides. The gate oxide thickness is small enough to permit the current flowing on all three walls [10].

Due to its silicon on insulator technology, the structure is compatible with conven-



(a) 3D Schematic view of a Tri-Gate *SOI MOSFET* (b) Cross-Section View of a Tri-Gate *SOI MOSFET*

Fig. 2.17: A Triple-Gate *SOI MOSFET* (source: [27]).

tional silicon integrated circuit processing, but has superior performance when the transistor is scaled down into nanometer range [5]. Increasing the number of gates improves the sub-threshold swing because the control of the channel region by the gates becomes stronger. The current drive enhances and the short channel effects lower compared to the double-gate counterpart [10].

2.2.3.3 Surrounding-gate SOI MOSFET

The schematic view of a surrounding-gate *SOI MOSFET* (*SGT*) is illustrated in Figure 2.18. It is worth to noticing that this device has a vertical-channel and a non-planar form in which the gate electrode surrounds the pillar silicon island, while the source and drain are localized at different depths in the silicon film. The gate length is adjusted by the silicon height [110].

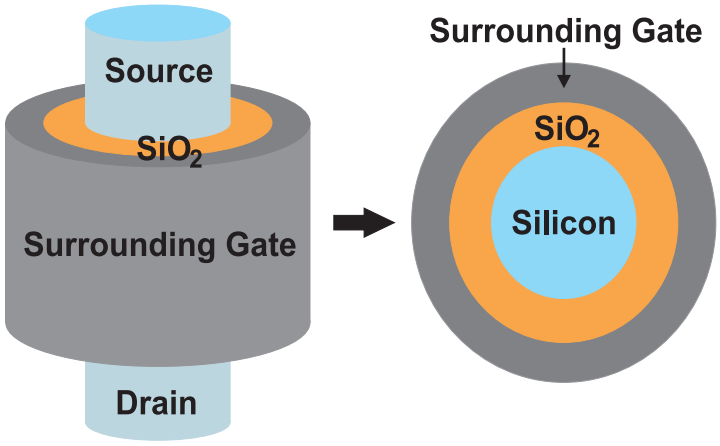


Fig. 2.18: Schematic view of a Surrounding-Gate *SOI MOSFET* (source: [27]).

Theoretically, such a transistor offers almost the best possible control of the channel

region by the gates and, thus, the short channel effects are strongly lowered, giving rise to a substantial drain current. In addition, SGT has an excellent sub-threshold slope, very small substrate effects, enhanced electron mobility and high reliabilities [76].

2.3 Integrated Circuits Design Based on Double Gate SOI MOSFET Transistor

The capability of the multi-gate (MG) SOI $MOSFET$ transistors and integrated circuits to cope with the challenging requirements of future analog and digital circuit applications is essential, if they want to become device player towards the end of the silicon road-map. For this purpose, the analog and digital performances of the non planar multi-gate devices need to be compared to those of planar bulk $MOSFET$ and single-gate SOI $MOSFETs$. Simple mixed signal circuits for RF applications have been already realized with such $3D$ SOI $MOSFET$ devices [95, 96, 98]. As it will be shown in this thesis, RF wireless technologies require high-performance transistors and low-loss (high-Q) passive devices. The high resistivity SOI substrates (larger than 2 $K\Omega-cm$) were suppose to offer high quality factor (Q) for the passive elements and hence, minimized crosstalk among analog and digital circuits. Also, an alternative approach for high-Q components is the use of the emerging the micro-electro-mechanical systems that will be presented in Chapter 3. Thus, SOI provides not only the chance to improve $MOSFET$ performance, but also opens the way towards an elegant technology platform for monolithic RF integration.

Here we show an up-dated comparison of figures of merits (FOM) for digital performances ($\frac{I_{on}}{I_{off}}$ current, saturation threshold voltage and sub-threshold slope) and analog-performances (transconductance-g_m, output conductance g_{ds}, voltage gain $(\frac{g_m}{g_{ds}})$ and cut-off frequency $(\frac{g_m}{C_{gs}})$) for planar versus non-planar SOI $MOSFET$ and bulk $MOSFET$ [57].

It is generally accepted that non-planar multi-gate SOI $MOSFET$ devices have the lowest sub-threshold slope (near $60mV/decade$) and the lowest output conductance-g_{ds} (which is also needed for the good analog-performance), due to the excellent electrostatic control of the channel, while the transconductance g_m of the planar and non-planar SOI $MOSFET$ as well as bulk $MOSFET$ is rather similar. Based on the above results, one can easily note that the voltage gain $(\frac{g_m}{g_{ds}})$ of the non-planar multi-gate SOI $MOSFET$ is much higher for the MG SOI $MOSFET$, low value of g_{ds} being responsible for this excellent analog-performance of $finFET$ [55].

It has been shown that the $finFET$ with their ultra-shallow source and drain junctions have high parasitic serial resistance, which degrades the transconductance-g_m due to voltage drop on source or drain contact, this effect being more harmful at higher operation currents, i.e. at higher overdrive voltages (for example $V_{gs} - V_{th} = 0.6V$). This last $finFET$ feature will limit the use of $finFET$ at a higher operating power.

Looking at the off currents and sub-threshold slope of $finFETs$ one can foresee a good future for these digital devices. But for having a complete answer to the above picture, we need to look at the analog-performances and mainly at the power-related frequency cut-off (f_T) behavior of these devices. The cutoff frequency of the internal device is related with both conduction properties of the device and the associated C_{gs} capacitances. Due to the increased values of the parasitic capacitances of $finFET$, the f_T of these devices can not go above the f_T value for bulk $MOSFET$ devices, at least not for the entire range current of the functional RF circuit, as follows. As a preliminary result, it appears that at around $5\ GHz$ and low overdrive voltages, the $MG\ finFET$ are attractive solutions for analog applications, while for high power higher microwave frequencies the planar $SOI\ MOSFET$ and bulk $MOSFET$ perform better than $MG\ finFET$.

The comparison of the circuit performance between $DG\ SOI\ MOSFET$ transistors and bulk $CMOS$ transistors is going to be a source of design innovation that will finally put into value the advantages and multi gate flexibility of the $DG\ FET$ structures. As an example, Figure 2.19 presents ring oscillators consisting of conventional bulk $CMOS$ and of a combination of both symmetrical and asymmetrical $DG\ SOI\ MOSFETs$, respectively [3]. One can see that stacked transistors (N_1 and N_2) are introduced to minimize the stand-by dissipation power due to the sub-threshold leakage reduction [77]. The back-bias voltage V_{BB} is applied to the lowest $NMOS$ transistor in order to dynamically change the threshold voltage.

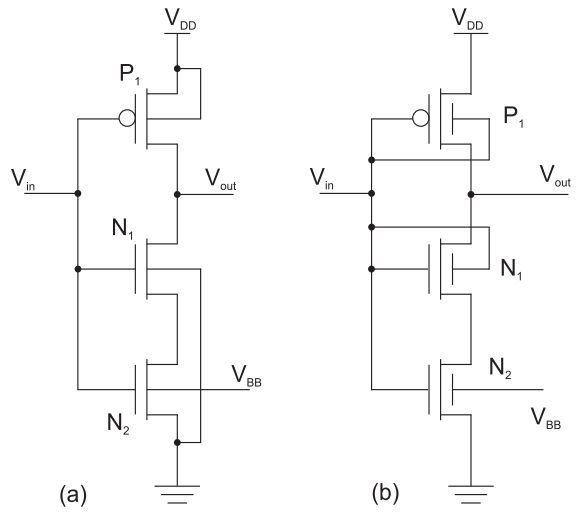


Fig. 2.19: Circuit diagram for the stacked inverters implemented with: a) Bulk and b) $Dg\ SOI\ MOSFET$ (source: [3]).

Both bulk and $DG\ MOSFET$ devices are supposed to have the same channel length of 25 nm, with the same oxide with its permittivity of 7 and the dielectric thickness of 1.62 nm, so that the gate leakage to be negligible in comparison with the total leakage current. The Dual-Gate transistors is designed with a light doping of $10^{15}\ cm^{-3}$ for a silicon thickness equal to 12 nm, in order to have a constant electron mobility, while the bulk counterpart is doped ($3 \cdot 10^{18}\ cm^{-3}$) in such a way to achieve adequate drain induced

barrier leakage and sub-threshold slope.

The simulations results indicate that the $DG\ SOI\ MOSFETs$ are consuming less power with respect to bulk $MOSFETs$ due to their stronger leakage suppression shown by the smaller sub-threshold slope for the SOI devices (78.9 mV/dec) compared to that of conventional $MOSFETs$ (89.1 mV/dec) (see Figure 2.20) [3]. This advantage is mainly provided by the threshold voltage sensitivity to the bias voltage V_{BB}. It has been also proven that the energy overhead of SOI circuits due to the switching from active to stand-by mode is decreased by more than one order of magnitude, as compared to bulk devices [3].

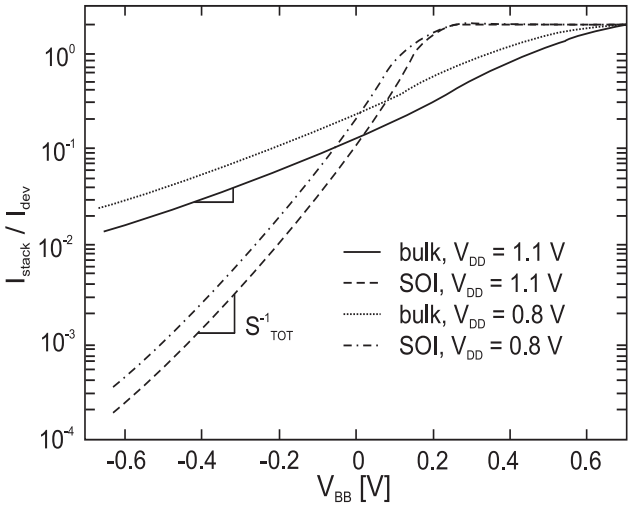


Fig. 2.20: Dependence of the leakage current reduction factor due to transistor stacking I_{stack}/I_{dev} on back-bias voltage V_{BB} (source: [3]).

This proven ability of the SOI devices to integrate both low power and high performance RF on the same platform has opened a variety of interesting areas to explore, such as the communication and the mixed-circuit applications [100]. This is only the beginning and the challenge of intensive analyses in the field for future innovative solutions operating in the range of $40 - 60\ GHz$ wireless applications.

2.4 Summary

The purpose of the current chapter is to offer a short description of the evolution of $MOSFET$ devices, by making the transition from silicon bulk technology to the silicon-on-insulator technology, with its volume inversion capability. Thus, the chapter begins with the history of electron devices starting from the discovery of the unipolar and bipolar and ending with the present devices. According to Moore's law, the scaling rules were described and then, several road-maps showed how their applicability was possible to the device miniaturization. The short channel effects, the limits and leakage currents resulted from scaling process have been illustrated in this chapter. Afterwards, the silicon-on-

insulator evolution was described by presenting the most important multi gate devices made with this technology. The integrated circuit based on double-gate, triple and Gate All Around $SOI\ MOSFET$ devices silicon on insulator $MOSFET$ transistor were briefly included.

The progress was very well predicted by Moore's law who envisioned that dimensions will decrease on an exponential curve with number of transistors doubling every two years. This scaling journey went on in the last four decades reaching the current integrated circuits state of art with more than a billion transistors and a channel length lower than $14\ nm$ by 2020. The need of smaller and high efficiency chips has led to the exploration of nanometer scale $CMOS$ alternatives, such as multiple-gate $SOI\ MOSFET$ devices.

The continuous process of down-scaling has reached its limits in terms of gate oxide thickness, short channel effects and power consumptions. This evolution gave birth to new leakage mechanisms described in this chapter and, accordingly solutions needed to overcome them. Therefore, the silicon on insulator devices were supposed to replace the bulk $MOSFET$ transistors. This chapter includes the advantages and challenges for the multi-gate $SOI\ MOSFET$ devices, together with their possible analog applications.

Chapter 3

Micro-technology Evolution Towards Large Scale Integrated RF MEMS Systems

During the last decades, the continuous miniaturization of MOS transistor dimensions has brought a tremendous increase of functional complexity of Si integrated circuits, culminating with the revolution of the microprocessors, computers and their world-wide interconnection. During the same period of time, the emerging micro-system technology has expanded the capability of micro-electronic technology by creating new functional micro-devices able to sense and control the industrial processes.

Automotive industry and consumer electronics have taken the benefits of the new on-chip sensors and actuators. Airbags containing micro-accelerometers and ink-jet heads for printers are only two success stories of Micro-Electro-Mechanical-Systems ($MEMS$) technology, culminating with integrated $MEMS$ for such applications, where both the integrated circuit and the sensors are located on the same micro-chip. Now, big expectations are for the portable RF electronic applications to take all the advantages of further micro-mechanics development. This new emerging field of $RF\ MEMS$ will revolutionize the wireless electronics by the potential of the vibrating micro-mechanical circuits to operate at high quality factor enabling on-chip multiple signal processing and integration of $RF\ MEMS$ on the same chip with $CMOS$ integrated circuits.

This chapter discusses the benefits and challenges of the new vibrating $RF\ MEMS$ devices and circuits made in this new micro-machining technology which are applicable at different portable and/or wireless communication applications. Firstly, a brief description of the most used technologies is going to be realized followed by a detailed background presentation of micro-mechanical systems. Secondly, the $RF\ MEMS$ devices will be enumerated and presented by taking into account their main functions accomplished when they are connected together and thus, obtaining important integrated micro-mechanical circuits to be used in wireless communication applications. Thirdly, the

evolution of transceiver architectures will be presented, starting from the present generation where $CMOS$ integrated circuits interface at the board level with off-chip quartz-based passive components for getting transceiver architectures, performed on printed circuit board (PCB) and ending up with an ultimate vision of an all-$MEMS$ transceiver, in which all the above-mentioned off chip elements are performed in the silicon $MEMS$ technology and located on a single silicon chip. In the end, several challenges concerning the on-going RF vibrating $MEMS$ research will be discussed and a summary will conclude the chapter.

3.1 MEMS Technology

There are several $MEMS$ micro fabrication technologies discussed over the last years. These technologies offer the possibility to construct both mechanical and electrical components with sizes down to micron and even below. Their number on the chip is continuously increasing.

Independent on the classification of $MEMS$ technologies, there are several common properties as: miniaturization, multiplicity and integrability [7, 41].

Basically, miniaturization refers to size minimization of $MEMS$ components and this conveys several advantages. As a result of size reduction, the natural resonant frequency increases and, further, the system operating frequencies. Also, the thermal time constant is shorter. However, the miniaturization is done until an operational and technological limit is reached and that is different from one application to another. The second important property, called multiplicity, has two benefits in terms of: $1)$ the possibility to fabricate 10000 or a million components at the same time as one component and $2)$ the additional flexibility in the realization of parallel interconnected electromechanical systems. The previous characteristics are not enough exploited if the microelectronics is not merged with the micro-mechanics and, thus, reaching the integrated $MEMS$ systems.

The most common processing techniques that are used to construct micro-mechanical structures are bulk and surface micro-machining [71, 74, 116].

3.1.1 Bulk Micro-machining

The bulk micro-machining [56, 74] is defined as a technology that makes micro-structures, in which the bulk silicon material is chemically etched. The etching properties are strongly dependent on the crystallographic structure of the semiconductor bulk material.

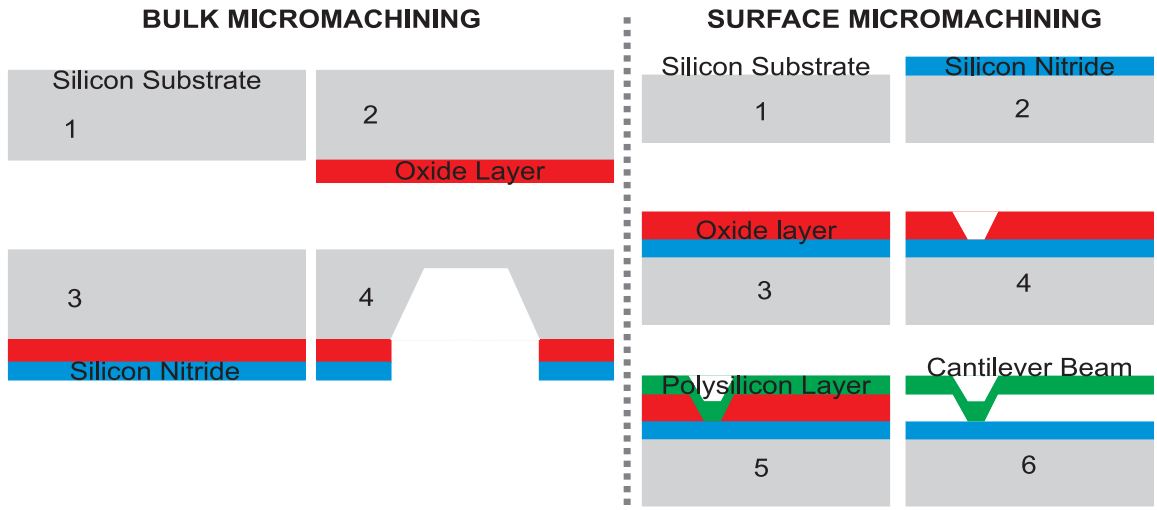


Fig. 3.1: Micro-machining technology: bulk and surface [37].

3.1.2 Surface Micro-machining

Another predominant micro-machining technology is the so-called surface micro-machining [74]. It starts with a silicon wafer which is, in this case, the silicon substrate. Then, instead of etching the bulk silicon, a thin "sacrificial layer" is removed from underneath the mechanical structure with the scope of suspending it from the substrate.

The surface micro-machining enables the fabrication of very complex micro-structures and makes realizable the constructions of systems that are impossible to be built with bulk or conventional technology. In addition, it offers the freedom for an easier fabrication of the integrated $MEMS$ with minimum compromises in materials, geometries, assembly and interconnections.

3.2 Need for a Micro-mechanical Circuit Technology

The $MEMS$ devices are seen as elements with new capabilities, extended operational performances and lifetimes of existing mechanical systems. In addition, there are many possibilities for $MEMS$ to be used in applications such as accelerometers, ink-jet print heads, hearing aids, pressure and chemical sensors, infrared imagers, gyroscopes, digital light processors, radio frequency and optical wireless communication [15, 41].

Today, the main motivation of the use of $MEMS$ technology is the miniaturization of the RF Front Ends in wireless applications. For this purpose, an ultra high quality factor (over 10000) is a paramount need of $MEMS$ usage in order to provide good selective low-loss filters and/or high-accuracy voltage controlled oscillators. Moreover, surface micro-machined $MEMS$ can be interpreted as a fabrication approach that provides the advantages of multiplicity (batch fabrication), easier monolithic fabrication with the electronics on the same chip, miniaturization (micro-scale sizes and low mass of devices)

and high reliability. On the other hand, there are a few challenges to consider: the compatibility of structural $MEMS$ technology with the $CMOS\ IC$ process, the fabrication approach, cost, time and packaging.

3.3 $MEMS$ Systems - Present and Perspectives

Recently, $MEMS$ is extending the application range from physico-chemical sensing to signal processing by exploiting the high quality factor of the vibrating micro-structures operating at the natural resonance frequency. The $MEMS$ capability to perform new functions in the field of wireless electronic application will revolutionize the next generation of communication industry. Actually, the RF integrated mechanical circuits are envisioned to grow in complexity, from low scale to medium scale and large scale integrated $MEMS$ in a similar way the integrated circuit have developed in the years $'60$ - $'90$ of the previous century. This extraordinary evolution is only possible if the basic science and technology of $MEMS$ is deeply understood and applied in market applications, at low cost and high reliability. To reach this final goal, the $MEMS$ community is trying to use the basic physics and electronics knowledge for supporting the new emerging applications of $RF\ MEMS$ devices and circuits (see Appendix A for a background presentation of time and frequency response of systems of different orders). Intensive research around vibrating $RF\ MEMS$ capacitive structures have shown that if these RF-$MEMS$ vibrating components are excited with an ac electrical signal of frequency equal to the natural mechanical resonant frequency, they can have equivalent electric circuits made of R, L, C passive components having the advantage of high quality factors, which make them very attractive for RF applications. These silicon $RF\ MEMS$ structures can be technologically integrated on the same chip with $CMOS$ electronics for getting a low size high performance integrated oscillator, and this aspect makes them a real threat to the quartz resonators used in the VCO oscillators.

Actually, such a trend of replacing quartz resonators by silicon $RF\ MEMS$ resonators is already happening today. For example a micro-electro-mechanical system ($MEMS$) oscillator ($SiT8002$) has been introduced by Discera company, in August of 2007. Such a highly reliable oscillator is completely quartz free and works in the frequency range from 1 MHz up to 125 MHz, with an excellent temperature and jitter performance. The $SiT8002$ is a factory programmable device at the customer's frequency specifications and can be used in several applications such as digital video recorder, IP-phone, scanner, IP camera [1] and this is only the beginning of a long and successful journey of $RF\ MEMS$ micro-nano structures envisaged for future RF electronics applications.

3.4 RF MEMS Devices

Increased miniaturization and performances of wireless communication systems followed by their reduced power consumption and cost are the driving forces of present progress of the field. The key challenge for today's wireless technology is the replacement of off-chip components like high-Q inductors and capacitors, ceramic and SAW filters, varactor diodes and discrete PIN diode switches, with high quality factor, new micro-mechanical vibrating $MEMS$ resonant devices that will be integrated on the same chip with electronic functions. Here we shall present different $RF\ MEMS$ components aiming not only the lay-out reduction of the application, but launching innovative ways of performing the same electronic function.

3.4.1 RF MEMS Capacitors

$RF\ MEMS$ capacitors can be used in phase shifters and voltage controlled oscillators (VCO), filters, transceiver switches and antenna. They overcome most of the disadvantages of varactor diodes which suffer from big losses, introduced by the semiconductor series resistance and leakage currents. However, their control speed is limited by the system time constant [69].

In the micro-machining technology, there are several forms of $RF\ MEMS$ capacitor as follows: transverse comb, lateral comb and parallel plates [125]. As an example, in Figure 3.2, we show a perspective view of comb $RF\ MEMS$ capacitor [125] where the electrodes are electro-statically moved with respect to one another by applying a voltage drop between them. The capacitance can be changed due to a variation in the overlapping area of the electrodes or due to the modification of the dielectric gap between electrodes.

In some of $RF\ MEMS$ capacitors, the plates are electro-statically moved with respect to one another [86, 90, 125], as it is the case of comb capacitive structure described above, while in other capacitors the dielectric is electro-statically moved between two metal stationary plates to allow the voltage control of the plate-to-plate capacitance [82, 83, 125, 126].

Thus, in Figure 3.3, we show a cross view of a parallel plates capacitor where the dielectric can move inside the electrodes due to the electrostatic forces generated by the dc-voltage V_a applied between electrodes. The movable dielectric is anchored to the substrate through a thin beam. A low resistivity metal layer is used for parallel plates electrodes in order to minimize the series resistance and maximize the quality factor Q.

3.4.2 RF MEMS Inductors

The high-performance integrated inductors are expected to be used in filters, voltage controlled oscillators (VCO) and in RF front-ends of transceivers. For these wireless com-

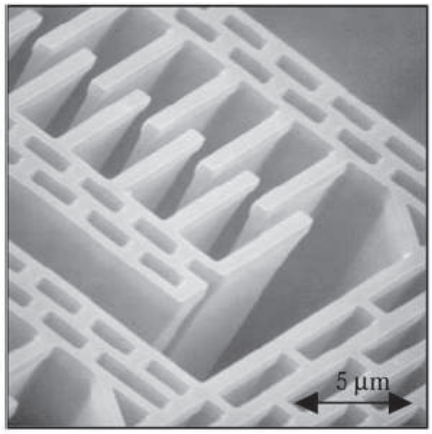


Fig. 3.2: Perspective-view of an $RF\ MEMS$ capacitor (source [125]).

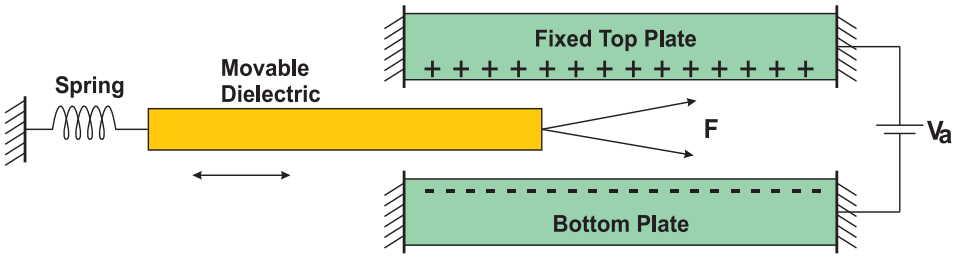


Fig. 3.3: Cross-view of an $RF\ MEMS$ capacitor with movable dielectric (source [126]).

munication applications, the tunable micro-mechanical capacitors are desired to be pair with inductors with good quality factor Q that should be larger than 20.

The most important parameter of the $RF\ MEMS$ inductors is the quality factor Q which strongly degrades when the series resistance and the substrate losses increase [69, 82, 83, 86]. Many efforts have been focused on the minimization of the unwanted effects and, thus, increasing the quality factor. Finally, by using micro-machining technology, the inductors can be integrated on the same chip together with $CMOS$ electronics. As an example, in Figure 3.4, we show a spiral inductor with a quality factor Q of 57 at a frequency of $10\ GHz$ which is obtained from a metallic layer suspended above glass substrate at about $50\ \mu m$ [125].

3.4.3 RF MEMS Switches

The $RF\ MEMS$ Switches are envisaged for: front-end transceiver switches, on-chip antenna switching, power amplifier supply switching, band/mode selection (in switchable filters), time-delay for phased-array antenna [83]. The major advantages of the micro-mechanical switches with respect to the electrical switches extensively used in the communication industry (up to now) are in terms of: the ultra low power consumption and very high isolation, the low insertion loss and the low cost.

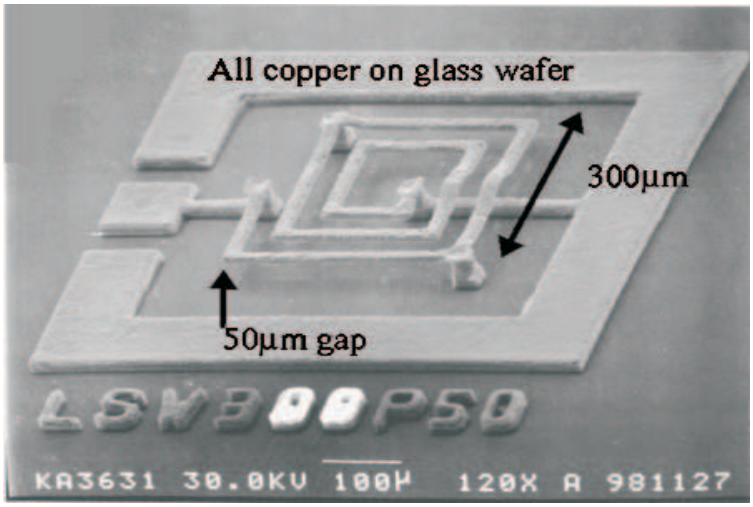


Fig. 3.4: Perspective-view of an $RF\ MEMS$ inductor (source [125]).

However, there are several challenges of $RF\ MEMS$ switches to be commented here: the limited power handling and speed due to the mechanical phenomena, the reliability and packaging.

There are two generic types of $RF\ MEMS$ switches depending on the fabrication technology and the operation principle: ohmic contact (metal - air dielectric - metal) or capacitive membrane (metal - air gap - dielectric - metal) [69, 125].

As an example, in Figure 3.5, we show a cross view of an $RF\ MEMS$ ohmic contact switch which is built from a conductive beam, suspended above a metal electrode and anchored at both ends [125]. With the metal membrane in the up-position, the switch stays in the OFF-state and, with the metal beam touching the lower electrode, the switch moves to the ON-state. The actuation of the switch from the OFF-position to ON-position is performed by a dc-voltage applied between the two electrodes. In order to come back to the previous OFF state, the electrostatic voltage is interrupted and the beam takes the initial up-position. This is the normal-opened switch operation.

The ohmic contact switch described above presents a very low ON insertion loss and high OFF isolation resistance, but their weaknesses come from a possible ON resistance enhancement due to the electric arching phenomena which can determine a decrease of its reliability.

In Figure 3.6, we present an example of an $RF\ MEMS$ capacitive switch [51] where a dielectric layer is deposited above the lower electrode. In-between the upper metal electrode and the lower electrode, we have two types of dielectric: an air-gap (g_0) and an isolator layer which is normally SiO_2. In the OFF-state, the metal electrode is in the up-position and the switch reactance has a high value, while, when the metal electrode touches the thin dielectric, the switch reactance has a low value.

The advantage of the capacitive switch comes from its realization technology where the direct metal-to-metal contact is avoided due to the presence of the isolator. Thus,

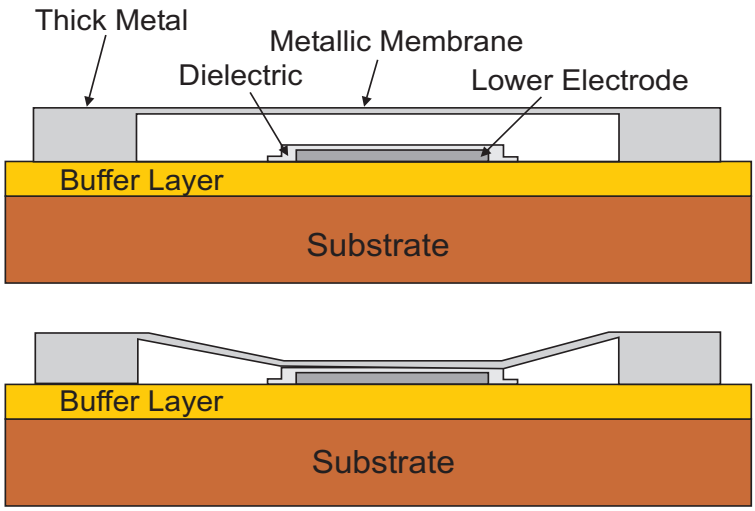


Fig. 3.5: Cross-view of an ohmic $RF\ MEMS$ switch (source [125]).

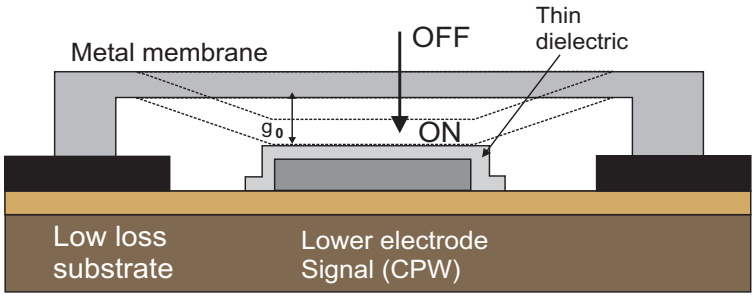


Fig. 3.6: Cross-view of a capacitive $RF\ MEMS$ switch (source [125]).

the capacitive membrane switch has a longer lifetime with respect to the ohmic contact switch. The key specification for an $RF\ MEMS$ capacitive switch is the ratio of C_{ON} to C_{OFF} which should be higher than 100 and lower actuation voltage.

3.4.4 Vibrating RF MEMS Resonators

The RF vibrating $MEMS$ resonators refer to the micro-systems in which the excitation is performed by means of external forces (piezoelectric films, thermal expansion, electrostatic forces or magneto-static forces) at their resonance frequency, while the output vibration can be detected by piezoelectric films, piezo-resistive strain gauges, optical techniques or by capacitive principle. The vibrating $RF\ MEMS$ can provide different innovative circuit functions for RF applications such as switch-able filtering, mixing, filtering and mixing, reference frequency while having very high quality factors (higher than 10000), low area and reduced power consumption for an operation frequency range of MHz to GHz. In the present wireless applications, quartz-based SAW resonators are used for the timing and frequency control.

As an example, nowadays, the quartz oscillators are widely used in cell-phones and

watches applications, where the off-chip SAW resonators having high quality factor and operation frequency are located in the positive feedback loops of silicon amplifiers. For such wireless communications, the off-chip LC passive components, SAW and quartz resonators are increasing the area of a printed circuit board (PCB).

Today, the silicon-based $RF\ MEMS$ vibrating resonators are made by the surface micro-machining technology and they are intended to replace the quartz crystals and all their functions, in cell phones and general purpose transceivers. The $RF\ MEMS$ resonators integrability with $CMOS$ silicon technology make them superior over quartz, in terms of size and, hopefully, performances, thanks to their potential high Q at high frequencies as well as their drift and their thermal stability in general. Besides, the ultimate MEMS resonators are smaller by volume, more stable and reliable and obtained with low cost technology [46]. Moreover, a micro-resonator must be designed in such a way to achieve the needed frequency with adequate linearity, tune-ability and sufficient Q.

The resonators are classified in several types, each of them being described briefly, based on their key features. The principle of operation, the technology and the modeling of $RF\ MEMS$ resonators will be described in the next sections. The choice of their topology computer aided design layout provides the frequency control and the stability of micro-resonator.

3.4.4.1 Clamped-Clamped Beam Micro-Resonators

Clamped-clamped (CC) beam micro-mechanical resonators are very attractive in the emerging reference oscillator applications due to the on-chip integrability with operational amplifiers, tiny size and expected low cost technology [49, 65].

Figure 3.7 presents a perspective view schematic of a CC-beam resonator.

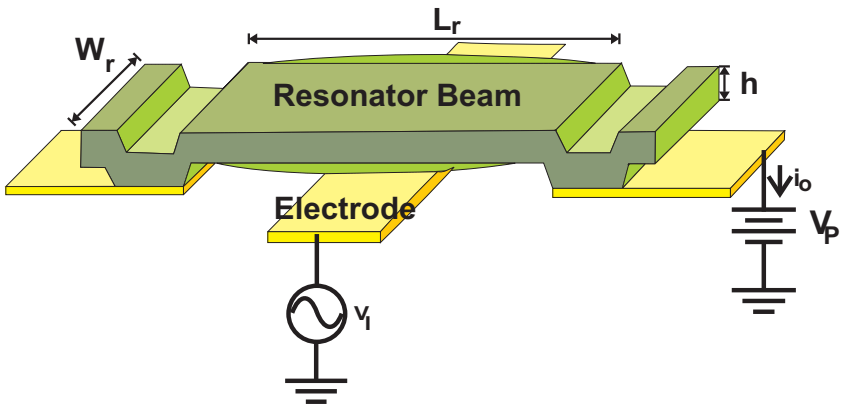


Fig. 3.7: Perspective-view of a Clamped-Clamped Beam Resonator (source [65]).

The device is mainly represented by a beam suspended above an electrode and anchored to the substrate at its ends. Electro-mechanical modeling of all types of $RF\ MEMS$ resonators will be based on the second order system theory as described in the Appendix

A. For the CC-beam resonators, the underlying input electrode is centrally located and biased at an ac voltage v_i. In the same time, a dc voltage V_P is applied on the conductive vibrating beam. The simultaneous presence of the dc and ac signals is essential for the capacitive transduction principle, specific to all $RF\ MEMS$ devices and circuits that will be described in this chapter. Briefly, this transduction principle can be explained as follows. The combination of ac and dc electrical excitations generates a time-varying electrostatic attraction force between the two electrodes, and a resonant mechanical vibration of the suspended beam is observed when the mechanical resonance frequency of the CC-resonator equals the frequency of the excitation electrical (alternative) signal. Thus, this vibration causes a time-varying gap between electrodes and generate a time-varying capacitance, which will determine a time-varying output electrical current. This motional output current flows through the vibrating capacitance and it is frequency dependent. Simple calculations coming from the second order system theory can show that, when the dc voltage, V_P is equal to zero, the equivalent motional resistance tends to infinite and the output motional current thorough the capacitive transducer is equal to zero. Thus, the entire $RF\ MEMS$ resonator enters the OFF state. Therefore, if V_P is zero, there is no dc power consumption and electromechanical coupling between the two electrodes. This observation is now extensively used for bringing a new feature to all $RF\ MEMS$ resonators, i.e., just playing with V_P value, they become $SWITCH-ABLE$ devices, no matter what function they have. So, if V_P equals to zero we have the OFF function, while if V_P is having a high enough value (determined by capacitor design and technology) we obtain the ON function (no matter what function will be, see below). They key issue with these CC resonators consists of the fact that the anchors provide losses that become stronger as frequency increases due to the energy radiated in the substrate and, therefore, the quality factor decreases. This energy loss mechanism is limiting the use of $CC-MEMS$ resonators to frequencies in the range of $10\ MHz$, where the Q is maximum 8000. At $70\ MHz$, due to this loss mechanism, the Q of CC-resonator is reduced to a value of about 30.

In order to suppress the losses, the anchoring to the substrate should be realized in some nodal points. Therefore, the resonator will become virtually isolated from the anchors and the quality factor increases.

The output of the resonator is given by the motional current that flows through the vibrating capacitance and varies as the frequency of v_i changes.

The natural resonance frequency of the resonator beam depends on the material property and geometry of the suspended electrode as given below:

$$f_0 = 1.03 \cdot \sqrt{\frac{E}{\rho}} \cdot \frac{h}{L_r^2} \cdot \sqrt{1 - (\frac{k_e}{k_m})} \tag{3.1}$$

where E and ρ are the Young's modulus and density of the structural material, respectively, L_r and h are shown in Figure 3.7, k_m and k_e represent the mechanical and electrical

stiffness, while $\frac{k_e}{k_m}$ indicates the combined electrical-to-mechanical stiffness ratio.

The vibrating clamped-clamped beam resonator interposes in the positive feedback loop of an oscillator, made in silicon. The equivalent electric circuit of the clamped clamped beam resonator is an RLC electric circuit.

As shown above, the challenges of a clamped-clamped beam resonator are in terms of the difficulty to avoid the mechanical energy loss in the anchor and the reduced operation frequency. A specific example of a clamped-clamped micro-resonator is the $8.5\ MHz$ clamped-clamped beam which provides a Q of 8000 under vacuum, where the damping effect is minimized. Unfortunately, under the atmospheric pressure, the quality factor is drastically diminished.

3.4.4.2 Free-Free Beam Micro-Resonators

Ideally, if a simple beam is suspended in space without tethers, it would have no anchor coupling and, thus, no loss due to the anchors. Such an ideal device could be called free-free (FF) beam resonator. A real free-free beam resonator is depicted in Figure 3.8 which shows a micro-mechanical beam supported at its flexural node points by several torsional thin beams, designed with quarter-wavelength dimensions to permit the great reduction of energy losses because of the anchor dissipation [32]. An underlying electrode is centrally located in order to allow the electrostatic excitation (v_i) to be applied. Its electrical operation is similar to the one of a clamped-clamped beam resonator. The output current i_o is obtained because of the action of V_P and v_i across the time-varying electrode-to-beam capacitor.

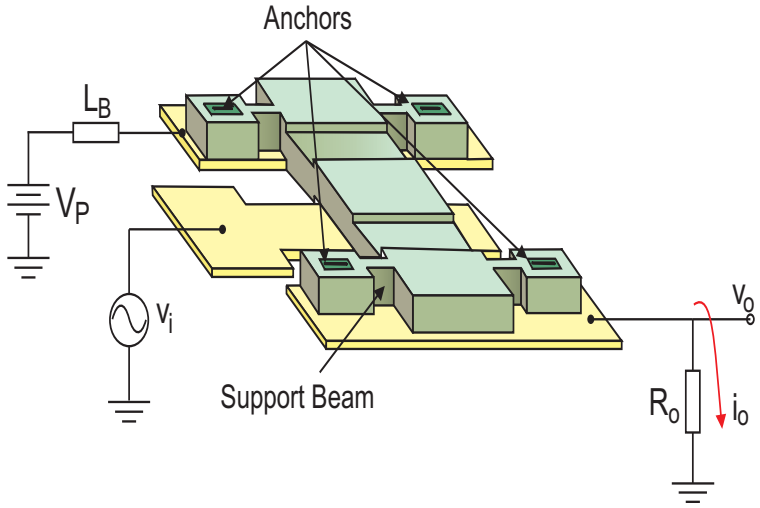


Fig. 3.8: Perspective-view of a Free-Free Beam Resonator (source [120]).

The quality factors have the values of approximately 28000 at very high frequencies (VHF) ranging from 20 to $100\ MHz$, in vacuum [120, 85]. It was proved that the free-free micro-mechanical resonators have a quality factor Q, which is an order of magnitude

higher than the Q of clamped-clamped-beam versions due to the diminished anchor dissipation.

A convenient design of a free-free beam resonator needs a good geometry which provides the desired frequency and assure a good support isolation in order to avoid any stick between beam and underlying electrode when V_P is applied. The procedure of resonator design is dependent on the range of frequency as it follows. At low frequencies, when the beam is long and thin, the Euler-Bernoulli equation is used to calculate the fundamental frequency, while the Timoshenko method is more appropriate to higher frequencies because of its ability to model the shear displacements and rotary inertias. In the same manner used in the previous CC resonator, the RLC equivalent circuit is realized. The most critical element in a micro-mechanical resonator is the motional resistance that should be low, because of the impedance matching consideration and thus, due to the maximum power transmission in and from the micro-mechanical system. An alternative to reduce it would be to use higher-mode free-free beam micro-mechanical resonators. The latter provide higher dynamic range, power handling and an improved quality factor, which did not decrease with the increase in frequency to about $100\ MHz$. They have two or three electrodes underneath the beams and centered between each adjacent node pair, and three or four torsional-mode supports attached at the nodal locations. The arrangement depends on the mode used by the designer. A higher mode involves a higher number of electrodes and support beams.

According to the above description, Figure 3.9 shows a measured spectrum of a $92.25\ MHz$ free-free beam micro-resonator for which the quality factor was found to be equal to 7450.

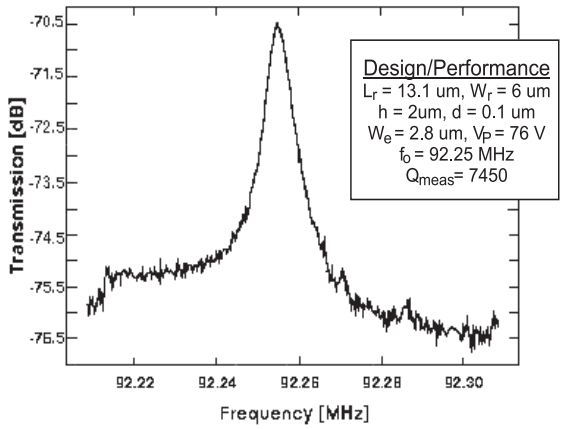


Fig. 3.9: Measured Frequency Characteristic of a Free-Free Beam Resonator (source [120]).

Despite the improvements of a higher mode free-free resonator with respect to the clamped clamped beam resonator, the performances are still weak, especially at higher frequencies than $100\ MHz$. Therefore, other types of resonators are stringent required.

3.4.4.3 n-Port Capacitive Comb Transduced Micro-Resonators

A capacitive comb transduced micro-mechanical resonator can be seen as a particularity of a free-free beam class of devices thanks to their low anchor losses. A typical comb resonator with three ports is depicted in Figure 3.10.

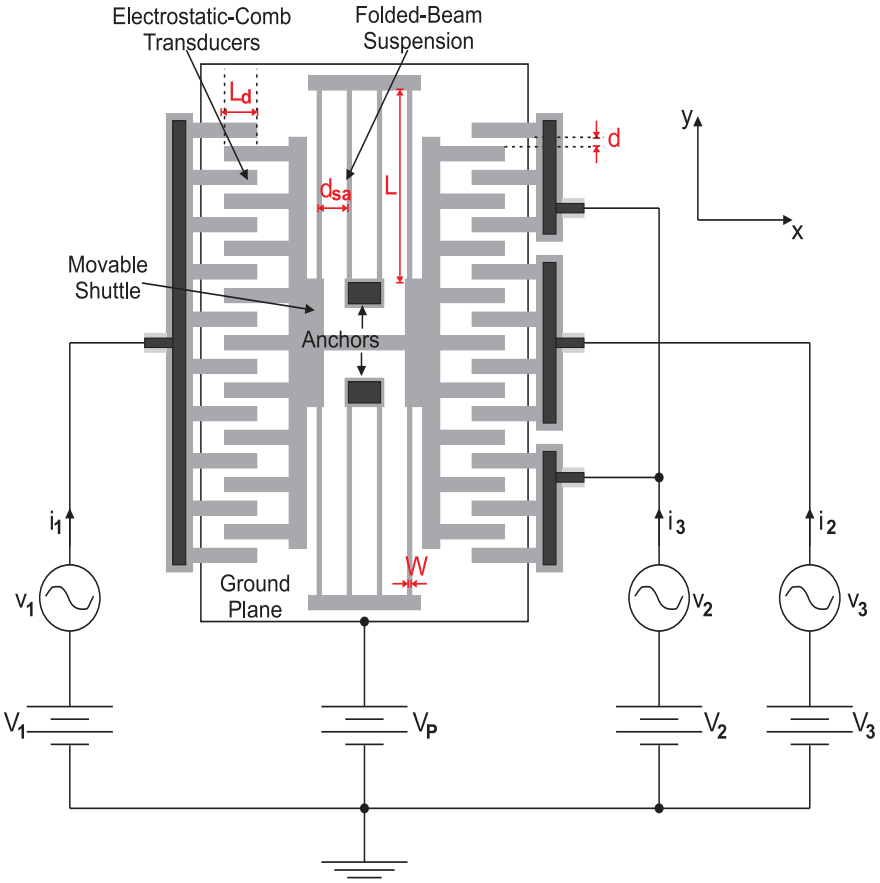


Fig. 3.10: Cross-view of a Capacitive Comb Transduced Micro-resonator (source [88]).

A finger-supporting shuttle mass is suspended above the substrate through several folded beams, which are fixed on the substrate by two anchors. The shuttle mass can move freely in the x-direction due to the dc V_P and ac v_i voltages excitation. The motion is parallel to the substrate. An alternative electrostatic force is generated between the electrodes and resonator, at the frequency of v_i, because of the alternative ac signal applied. When the resonance frequency ([79, 88]) is attained between the electrical excitation frequency and mechanical vibration frequency, the entire configuration vibrates at the maximum amplitude and a time varying comb capacitor is created at the output, where thus, a time varying current is detected.

The natural resonance frequency of the shuttle mass provided with comb structure is

given below:

$$f_0 = \frac{1}{2\pi} \cdot \sqrt{\frac{2Eh(\frac{W}{L})^3}{M_P + \frac{1}{4}M_t + \frac{12}{35}M_b}} \tag{3.2}$$

where W and L are indicated in the picture, while h is the thickness of the finger, E is the Young's modulus, M_P, M_t and M_b represent the corresponding masses of the shuttle, folding trusses and suspended beam.

The small signal equivalent circuit of a three port capacitive transduced resonator has a more complex form in comparison with other resonators [79, 88, 89]. For each port, there are several current controlled current sources that make the coupling of the given port with the others, through the ac voltage applied to all ports.

Figure 3.11 illustrates the transconductance spectra for this $MEMS$ resonator measured under a pressure of 20 mtorr and biased at a dc-voltage of 20 V. The excitation signal is assumed to be $1\ mV$ peak. For this $MEMS$ resonator, the quality factor was found to be approximately 50000.

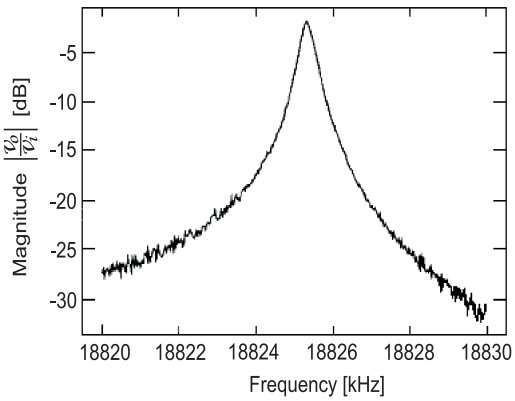


Fig. 3.11: Measured transconductance spectrum for a capacitive comb transduced mirco-resonator that operates under a vacuum pressure of 20 mtorr (source [79]).

3.4.4.4 Radial-Contour Mode Disk Resonators

A radial-contour mode disk resonator (or areal dilatation) is an alternative to attain increased-Q at very high frequency, even if the dimensions are larger than those for the flexural-modes used before. It has been tested to operate in the fundamental, second and third modes [21] reaching frequencies as high as $829\ MHz$ and quality factors of 10000.

Figure 3.12 presents the perspective view of a radial-contour disk resonator [21], with a disk suspended above the substrate and anchored only at its center. The electrodes are separated from the disk by a narrow air or a vacuum gap surrounding it.

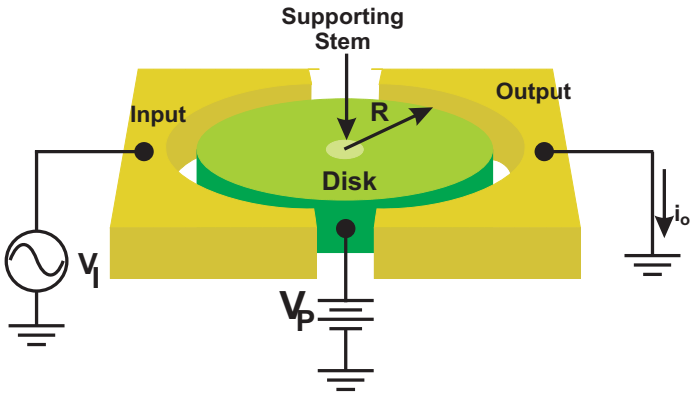


Fig. 3.12: Perspective-view of a Radial-Contour Mode Risk Resonator (source [21]).

The principle of operation is similar to that of previous resonators in which a dc voltage V_P and ac voltage v_i are applied as shown in the picture. A time varying electrostatic force is generated and acts radially on the disk, at the resonance frequency of the device. Consequently, the disk expands and contracts alternatively along the radius, while the rotational motion around the centroid is neglected. The motion gives a time-varying dc-biased capacitor between the disk and the output electrode, that generates an output current. The resonance frequency for the radial-contour mode disk coincides with the natural frequency and depends on its material properties and radius, as follows:

$$\omega_n = \omega_0 = \frac{\alpha\kappa}{R_{disk}} \cdot \sqrt{\frac{E}{\rho}} \tag{3.3}$$

where R_{disk} is the radius of the disk; E and ρ are the Young's modulus and density, respectively; κ is a constant dependent on Poisson's ratio (0.342 for poly-silicon) and α represents a constant depending on the order of the desired mode. It was proved that the resonance frequency increases when using higher mode, in the same technological conditions.

In order to complete the design, the equivalent mechanical and electrical models should be provided with the calculations of their parameters. In many applications, the series motional resistance must be minimized for impedance matching purposes, this being one of the most important issue in any resonator.

In particular, there are a few self-aligned vibrating micro-mechanical resonators that operate at the frequencies of $1.14\ GHz$ [118] and $1.156\ GHz$ [119], respectively, with Q's higher than 1500 and 2650 in both vacuum and air. For these resonators, the self-alignment of the stem to the center of the disk permits a far superior symmetrical motion of the resonator compared to the one reached by previous versions.

To analyze a disk resonator as a mechanical lumped element model, one can consider the response of a single degree of freedom system (i.e. a system which is free to move in a

single direction as it is shown in Figure $A.1$) to the harmonic excitation, as written below:

$$m \cdot \frac{d^2y(t)}{dt^2} + c \cdot \frac{dy(t)}{dt} + k \cdot y(t) = F_{el}(t) \tag{3.4}$$

where $y(t)$ is the displacement of the system as a function of time, $F_{el}(t)$ is the force exerted on the resonator, m denotes tge system mass, c is the damping coefficient and k represents the mechanical spring constant.

The equation (3.7) can be rewritten as a function of the resonant natural frequency $\omega_n = \sqrt{\frac{k}{m}}$, the quality factor $Q = \frac{\omega_n m}{c} = \frac{\sqrt{km}}{c}$ and the damping ratio $\xi = \frac{c}{2\sqrt{km_{re}}}$, as follows:

$$\frac{d^2y(t)}{dt^2} + 2\xi\omega_n \cdot \frac{dy(t)}{dt} + \omega_n^2 \cdot y(t) = \frac{\omega_n^2}{k} \cdot F_{el}(t) \tag{3.5}$$

Due to the dc voltage V_P and ac voltage v_i, a time varying electrostatic force is generated and acts radially on the disk at the resonance frequency of the device:

$$F_{el} = \frac{(V_P - v_i)^2}{2} \cdot \frac{\partial C_1}{\partial r} \tag{3.6}$$

where $\frac{\partial C_1}{\partial r}$ denotes the change in electrode-to-resonator overlap capacitance per unit radial displacement at the input port.

By applying a periodic excitation voltage v_i, of the form $V_i cos(\omega_i t)$, and by maintaining the constant dc voltage V_P, the above equation will be:

$$F_{el} = \frac{\partial C_1}{\partial r}[(\frac{V_P^2}{2} + \frac{V_i^2}{4}) - V_P V_i cos(\omega_i t) + \frac{V_i^2 cos(2\omega_i t)}{4}] \tag{3.7}$$

One can observe three terms in the equation (3.10). The first term is a dc quantity which has a small effect on high frequency oscillations. The second term shows the electrical excitation at the frequency of oscillation ω_i, being very important for filter and tank circuit applications. The third term represents an harmonic force at a frequency away from ω_i and depends only on the ac signal. Consequently, the amplitude of the harmonic is small enough to degrade the resonator performance and thus, can be neglected in the model used in our work. As a conclusion, the relation of generated force (3.10) will be simplified to:

$$F_{el} = -V_P \frac{\partial C_1}{\partial r} v_i \tag{3.8}$$

Accordingly, the disk expands and contracts alternatively along the radius, while the rotational motion around the centroid is neglected. The motion gives a time-varying dc-biased capacitor between disk and output electrode that generates an output current as

below:

$$i_{out} = -V_P \cdot \frac{\partial C_2}{\partial t} = -V_P \cdot \frac{\partial C_2}{\partial r} \cdot \frac{\partial r}{\partial t} \tag{3.9}$$

where $\frac{\partial C_2}{\partial r}$ governs the change in electrode-to-resonator overlap capacitance per unit radial displacement at the output port.

In order to have a linear model for the disk resonator, $\frac{\partial C_1}{\partial r}$ and $\frac{\partial C_2}{\partial r}$ can be written in a simple form [119]:

$$\frac{\partial C_1}{\partial r} \cong \frac{\epsilon_0 \phi_1 R_{disk} t}{d_0^2} \tag{3.10}$$

$$\frac{\partial C_2}{\partial r} \cong \frac{\epsilon_0 \phi_2 R_{disk} t}{d_0^2} \tag{3.11}$$

where R_{disk} and t are the radius and thickness of the disk, d_0 represents the electrode to resonator gap spacing, while ϕ_1 and ϕ_2 are the angles defined by the edges of the input and output electrodes. The radial displacement is:

$$\frac{\partial r}{\partial t} = \frac{Q \cdot F_{el}}{j k_{re}} \tag{3.12}$$

At this moment, the output current results in:

$$i_{out} = \omega^2 \cdot \frac{V_P}{k_{re}} \cdot \frac{\partial C_1}{\partial r} \cdot \frac{\partial C_2}{\partial r} \cdot V_P^2 \cdot v_1 \tag{3.13}$$

In order to simulate a $MEMS$ resonator with other circuit components, it is useful to provide a simple electrical model for it, by replacing the mass, spring and dash-pot elements of the mechanical model with an inductor, a capacitor and a resistor. The calculation of the electrical elements has three steps. Firstly, the mechanical transfer function is derived from the ratio of motion of the system to the generated force. In the second step, the mechanical function is transformed to the electrical transfer function which will be compared in the last step with that of the expected RLC circuit. In addition, the following electromechanical coupling factor at ports 1 and 2 are going to be used:

$$\eta_1 = -V_P \cdot \frac{\partial C_1}{\partial r} \tag{3.14}$$

$$\eta_2 = -V_P \cdot \frac{\partial C_2}{\partial r} \tag{3.15}$$

By using the Laplace transform for the equations (3.11) and (3.12) and the definition of the mechanical transfer function:

$$I_{out}(s) = \eta_2 s X(s) \tag{3.16}$$

$$F_{el}(s) = \eta_1 V_1(s) \tag{3.17}$$

$$H(s) = \frac{X(s)}{F_{el}(s)} = \frac{I_{out}}{\eta_1 \eta_2 s V_1(s)} \tag{3.18}$$

the admittance of the $MEMS$ resonator takes the following form:

$$Y(j\omega) = \frac{I_{out}(j\omega)}{V_1(j\omega))} = jeta_1\eta_2\omega \cdot \frac{\frac{1}{k_{re}}}{(1 - \frac{\omega^2}{\omega_0^2}) + j\frac{\omega}{Q\omega_0}} \tag{3.19}$$

As mentioned above, the target of this analysis is to obtain a transfer function for the resonator similar to that of a series RLC circuit. In this context, the admittance looking into a series RLC circuit can be written as:

$$Y(j\omega) = \frac{j\omega C_x}{(1 - \omega^2 L_x C_x) + j\omega C_x R_x} \tag{3.20}$$

where the resonant frequency is defined as $\frac{1}{\sqrt{L_x C_x}}$.

Comparing the equations (3.22) and (3.23), three simultaneous equations are obtained. By solving each of them, the following values for the equivalent electrical circuit are derived:

$$R_x = \frac{c_{re}}{\eta_1 \eta_2} \tag{3.21}$$

$$L_x = \frac{m_{re}}{\eta_1 \eta_2} \tag{3.22}$$

$$C_x = \frac{\eta_1 \eta_2}{f_{re}} \tag{3.23}$$

With this detailed analytical characterization of a micro-mechanical disk resonator, we can use its equivalent RLC electrical circuit in the circuit design, as it is going to prove in Chapter 5.

3.4.4.5 VHF Wine-Glass Disk Resonators

The wine-glass-mode disk resonators have been demonstrated to have much larger stiffness and, thus, a higher handling power capability. The quality factor is also very high for frequencies of GHz order [65]. These features make the disk resonator to be desired in the frequency generation and filtering applications. It has been already shown that, for such resonators, the quality factors attain values of 98000 in vacuum and 8600 in atmosphere at frequencies of $73.4\ MHz$ with [2]. The wine-glass disk resonators have the following advantages: $1.$ a smaller motional resistance and, hence, an improved impedance-matching

capability; 2. a lower dc-bias voltage can be used; 3. a higher quality factor can be obtained even in the atmosphere conditions. Also, a prototype of disk resonator, that operates at $60\ MHz$ with Q of 48000, has a 55 times higher power handling capability, a comparable series motional resistance and a 45 times higher Q compared to a wide clamped-clamped beam resonator [64]. The ever highest reported Q is on the order of 145000 at $61.373\ MHz$.

Figure 3.13 presents a wine-glass mode disk resonator in a typical bias and excitation configuration. One can see the absence of the central stem which eliminates the miss-alignment risk between the disk and central anchor. Thus, the losses in the anchor are drastically reduced. The structure consists of four electrodes surrounding the disk, being located in the opposite sides along a given axis and connected in pairs. The electrostatic force is generated on the AA'-axis and expands and compresses the disk. The output current is detected along BB'-axis. The current enters the resonator when the disk compresses and leaves when the disk expands.

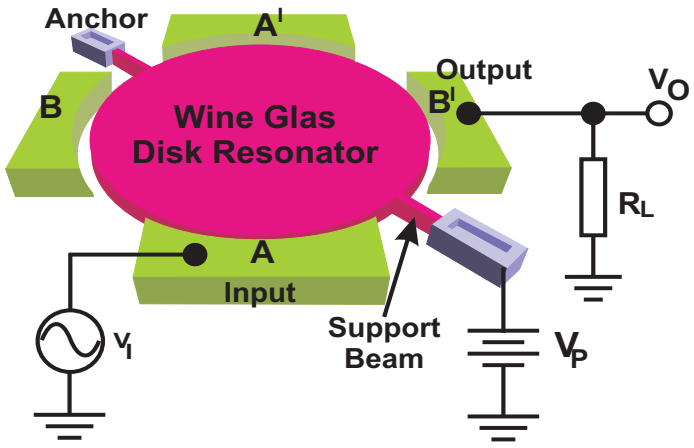


Fig. 3.13: Perspective-view of a Wine-Glass Disk Resonator (source [64]).

The excitation sources remain the applied dc and ac voltages V_P and v_i, respectively. At this configuration, the V_P is directly applied to the resonator disc without the use of any tee to separate the ac from the dc voltage. As with other resonators, the equivalent mechanical and electrical circuits of a wine-glass disk are governed by the mode shape and parameters associated with its transducer ports.

Figure 3.14 shows a measured frequency characteristics of a wine glass disk resonator, supported by only two support beams. The quality factor achieves a value of 48000, for a resonance frequency of $61.2\ MHz$.

3.4.4.6 Extensional Wine-Glass Ring Resonators

Figure 3.15 gives the perspective-view of a wine-glass ring resonator [124] which consists of a vibrating ring suspended above the substrate by four tethers connected at the nodal points. The support beam isolates the structure from the anchors in order to minimize the anchors losses and provide a high Q. Also, this configuration entails many electrodes

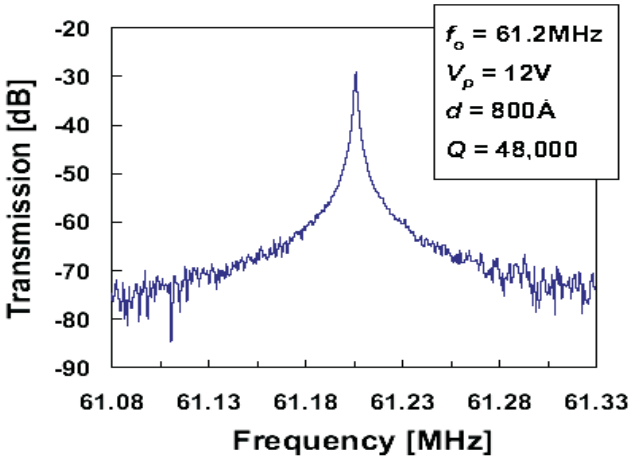


Fig. 3.14: Measured frequency characteristics of a wine glass disk resonator (source [64]).

surrounding the ring, in both inside and outside parts, with the purpose to increase the area of overlapping capacitance. The difference between wine-glass disk and ring resonators consists of the fact that the electrode-to-resonator overlap area is only on outside for the disk structure while the overlap area is formed on inside and outside part for the ring counterpart.

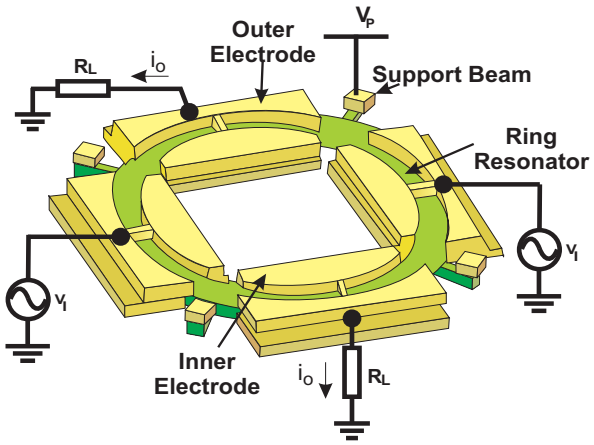


Fig. 3.15: Perspective-view of a Wine-Glass Ring Resonator (source [124]).

To excite the resonator, a dc-voltage V_P is applied to the ring, while the ac-voltage v_i drops on the two opposite electrodes. Further, a time varying electrostatic force appears at the frequency of v_i, when the device is resonating. Due to dc-biased V_P and ac-voltage v_i, at the resonance frequency, a time-varying capacitance obtained between the electrodes and resonator will generate an output current that is sensed by the other opposite electrodes. Shortly, the principle of operation is as follows: time-varying electrical input signals (voltages) are generating time-varying electrostatic forces, determining time-varying capacitances between electrodes and vibrating resonator which are giving the time-varying output currents. Mechanically, the system is modeled by a spring-mass-

dash-pot system which, from electrical point of view, is equivalent to a series-LCR tank circuit.

It has been demonstrated that the wine-glass ring resonators provide a great advantage over the disk counterpart in terms of lower motional impedance (even $2\ k\Omega$ at $1.2\ GHz$ and dc-bias of $100\ V$) that makes possible the direct coupling to antenna in RF systems, due to the good matching. Also, the benefits of high resonance frequency and quality factor are met. This design can be used at $1.2\ GHz$ and $1.47\ GHz$ with a Q of 3700 and 2300, respectively, in both vacuum and air [124]. The motional resistance is expected to have a 6 times lower value than the one of a radial-contour mode disk resonator.

3.4.4.7 Micro-mechanical "Hollow-Disk" Ring Resonators

An "all-silicon" vibrating "hollow-disk" ring resonator is obtained from a disk resonator by removing quadrants of its material as it is depicted in Figure 3.16. The ring is supported by four radial beams joining together into a central anchor stem. The radial beam length is designed with a quarter wavelength coupling so that the entire mechanical energy going towards anchors to be reflected back to the vibrating ring. For a direct contact between the radial beam and the ring, the structure can be designed to have different quality factors in the air and associated resonant frequencies as follows: $Q = 67519$ for $24.4\ MHz$, $Q = 48048$ for $72.1\ MHz$ and $Q = 5846$ for $1.169\ GHz$. If the support is notched, the losses are strongly reduced allowing the ring to have a quality factor greater than 10000 at frequencies over $1\ GHz$ [63].

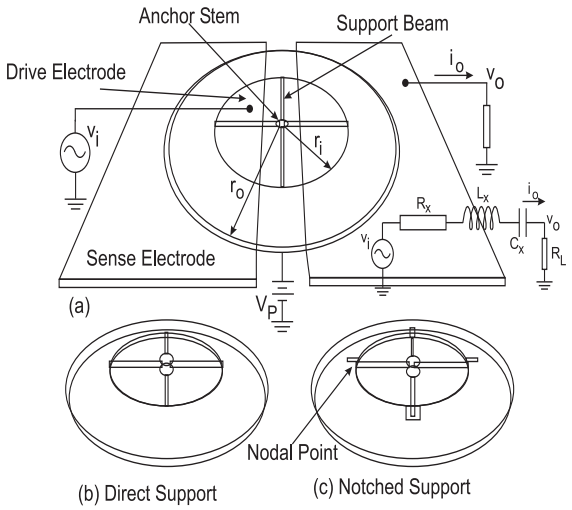


Fig. 3.16: Micro-mechanical "Hollow-Disk" Ring Resonator (source [63]).

In order to prove the above-mentioned performance for a notched hollow-disk ring resonator, Figure 3.17 presents its measured frequency characteristics, under vacuum condition. The measured quality factor is 14603 at a resonance frequency of $1.2048\ GHz$.

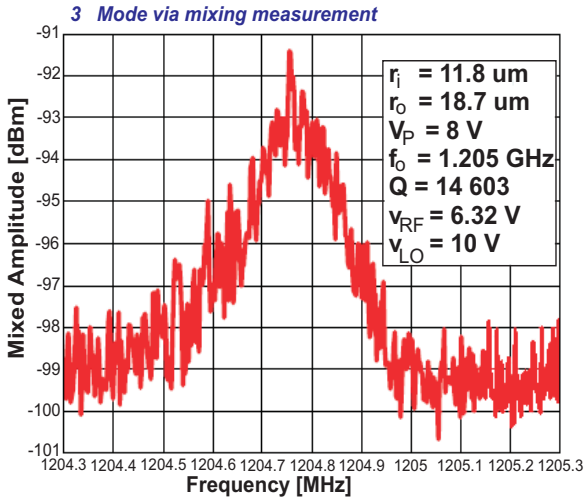


Fig. 3.17: Measured frequency characteristics for a micro-mechanical "Hollow-Disk" Ring Resonator under vacuum (source [63]).

3.4.5 Reconfigurable RF MEMS Antennas

Another generic $RF\ MEMS$ device to be mentioned here is the reconfigurable antenna, where the radiating directions can be changed being controlled by an actuation mechanism. These on-chip antennas have reasonable dimensions if the operating frequencies are in the range of GHz. In addition, the suspended antenna working in air will not benefit from the dielectric permittivity of substrate. Even if their integration is simple, there are at least two drawbacks. The antennas are very sensitive to the nearby structures and take all the interference effects.

One reported example of $RF\ MEMS$ antenna is the $17.5\ GHz\ MEMS$ reconfigurable Vee antenna shown in Figure 3.18 [69]. It contains three layers of poly-silicon realized via surface micro-machining process. The antenna arms can be rotated around a central anchor by means of a pull-push bar connected to the moving actuator.

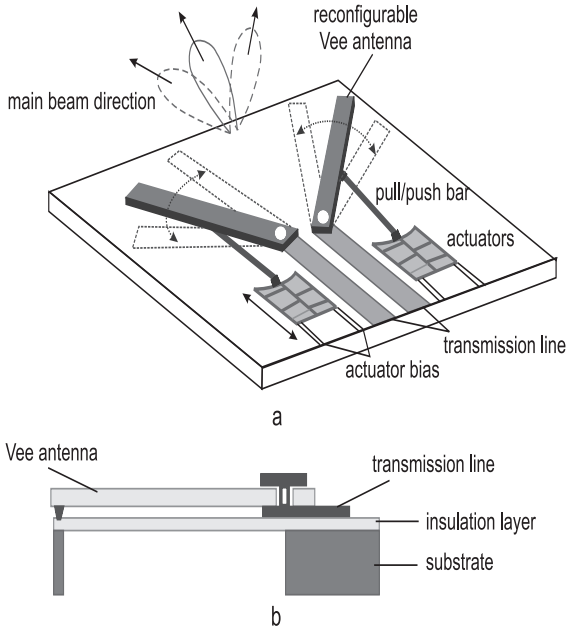


Fig. 3.18: Micro-electro-mechanical Antenna (source [69]).

3.5 RF MEMS Circuits

Within this section, we shall describe how we can use the vibrating $RF\ MEMS$ devices presented earlier for the realization of on-chip complex functions like timing and frequency control. Thus, the final goal is that passive functions like filtering and impedance matching circuits and active functions as mixing, frequency control and channel selecting will be performed by interconnecting more $RF\ MEMS$ devices and integrating them on the same chip with $CMOS$ electronics. The wide range of operation frequency and high quality factor for the $RF\ MEMS$ circuits make them very attractive for the use in the front-end band and channel selector filters of multi-mode and multi-band wireless transceiver applications.

A brief description of different $RF\ MEMS$ circuit configurations will be made by emphasizing the advantages and challenges for the specific applications.

3.5.1 Micro-mechanical Circuits for Passive Functions

The research of the last years has shown that the above $RF\ MEMS$ devices offer new perspectives and better performance when they are connected together to provide micro-mechanical circuits for mechanical signal processing, by replacing the electrical signal processing, for some future applications. The $RF\ MEMS$-based passive circuits that will be described below are the bandpass filters with greatly reduced insertion losses and micro-mechanical array filters that allow the impedance matching with antenna.

3.5.1.1 Filters

Usually, any transceiver contains in its structure many filters that hold the role to select the desired frequencies while blocking those which drop outside the band. In order to have enhanced performances and functional flexibility, a stringent requirement of front-end RF section is a very high quality factor determining very low insertion loss. Unfortunately, in the present transceivers, the filters are off-chip components being performed with quartz-based surface acoustic wave devices. Today, the $MEMS$ research is promoting the vibrating resonant $RF\ MEMS$ filters realized in the silicon technology as the next best alternative to the quartz devices in order to obtain excellent insertion loss, small frequency bandwidth and convenient rejection of undesirable interferences [48, 49, 78, 87]. However, their high impedance versus poor power handling capability constitutes the major challenge for such vibrating $MEMS$ circuits. The vibrating $RF\ MEMS$ filters could be used in the transmit/receive duplexer (FDD), RF band-select filters, IF channel filters, VCO stabilization and image rejection circuits [80, 81, 86].

The on-chip micro-mechanical filters consist of several identical resonators connected to each other by conductive or non-conductive beams at very specific locations of the resonators [49]. The central frequency is given by the frequencies of its constituent resonators. Several silicon filter configurations are shortly presented here. Figure 3.19a shows two suspended clamped-clamped micro-mechanical resonators coupled mechanically by a conductive beam located at the flexural nodes [49, 90]. The capacitive transducer electrodes underlie the central parts of each resonator to make the entire structure to vibrate.

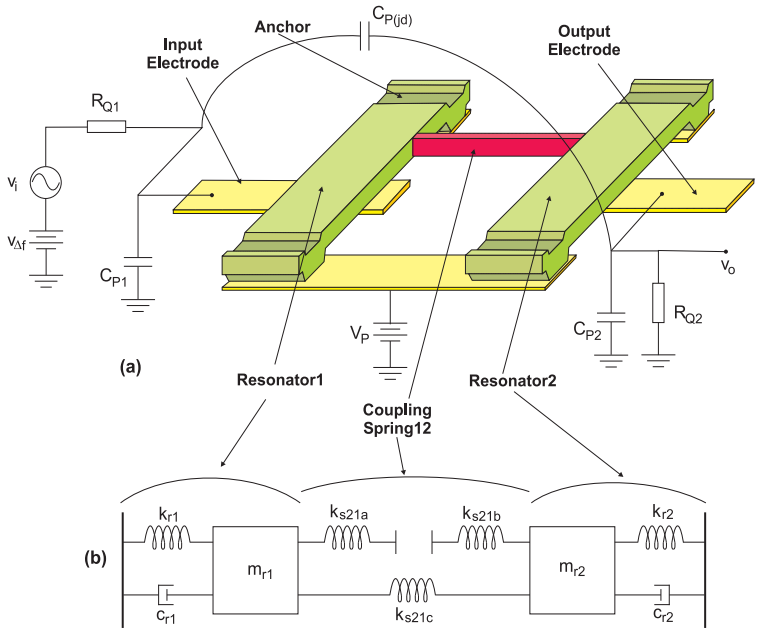


Fig. 3.19: a. Perspective-view of a Clamped-Clamped Micro-mechanical Filter; b. Equivalent Mechanical Circuit (source [49, 90])

Considering the theory of second order systems, an equivalent mechanical circuit of the filter with the above lay-out is shown in Figure $3.19b$. Each resonator is replaced by a mass-spring-damper system and the coupling beam is represented by a network of mechanical spring. The bandwidth is determined by the stiffness of the coupling spring, while the center frequency is given, especially, by the frequencies of the two clamped-clamped beam resonators. The equivalent electrical circuit is depicted in Figure 3.20, where, each resonator is replaced by a series RLC circuit and the coupling beam is modeled via a capacitive T-network.

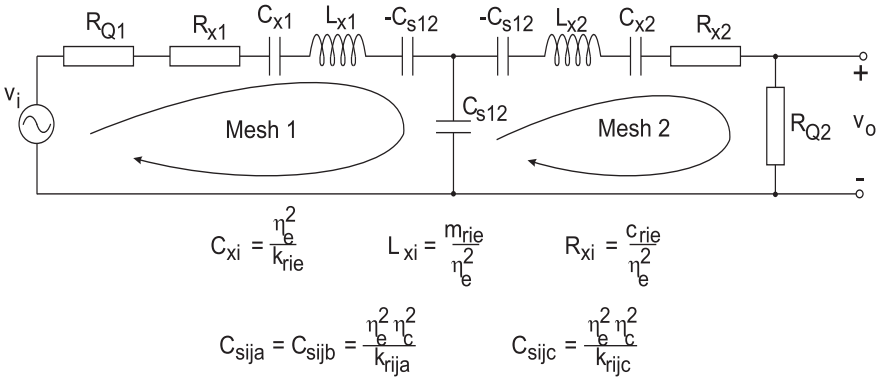


Fig. 3.20: Equivalent Electric Circuit (source [49, 90]).

The measured and simulated spectrum for a terminated $7.81\ MHz$ two-resonator micro-mechanical filter is illustrated in Figure 3.21. One can observe that the bandwidth equals to $18\ kHz$ and the insertion loss has an impressive low value of $1.8\ dB$. Also, the quality factor is 435. The simulated spectra are obtained by using the above equivalent circuit of such a filter.

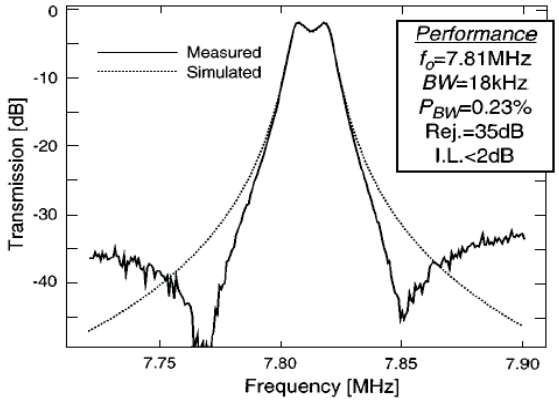


Fig. 3.21: Measured spectrum for $7.81\ MHz$ micro-mechanical filter. (source [49]).

Figure 3.22 shows the perspective-view of a bridged micro-mechanical filter [59, 85], operating as a higher order filter with sharper roll-offs and larger stop-band rejection compared to the previous counterparts. This configuration is constituted from three clamped-clamped micro-mechanical resonators connected by soft flexural mode mechan-

ical beams, where the non-adjacent resonators are bridged in order to improve the filter bandwidth shape. The entire vibrating structure is suspended above the substrate.

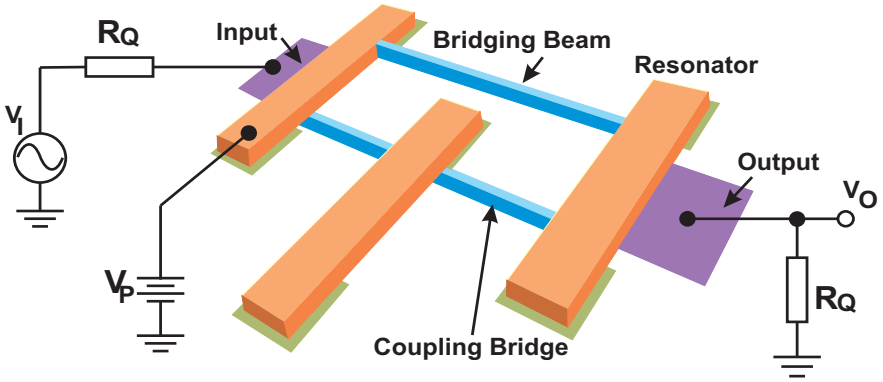


Fig. 3.22: Perspective-view of a Bridged Micro-mechanical Filter (source [59]).

The capacitive transducer electrodes are positioned in the central parts of each beam and induce the filter into vibration. It uses three-quarter-wavelength ($\frac{3\lambda}{4}$) couplers. In this way, a feed-forward path generates the loss poles in the filter transfer function to provide a very steep slope for the filter's characteristics.

The last circuit can be used as a self-switching vibrating micro-mechanical filter [61], the main purpose being to eliminate the need of lossy series switches. Therefore, they achieve zero-loss filters with on/off filter switching capabilities.

3.5.1.2 Micro-mechanical Array Filters

It has been proved that the capacitive transduced micro-mechanical filters achieve the lowest insertion loss and excellent frequency characteristics with impressive on-chip miniaturization and integrability properties. However, their impedances seem to be very large leading to the undesired mismatch with the conventional antenna impedances. Therefore, new filter architectures [33, 60, 62] have been proposed to replace the previous forms, being constituted from mechanically coupled arrays of N-resonators. Thus, the termination resistance of the filter is N-times reduced, while the stiffness increase by N-times compared to a single resonator. Also, the bandwidth decreases N-times and the insertion loss are drastically reduced.

3.5.2 Micro-mechanical Circuits for Active Functions

The most representative configurations of micro-mechanical active circuits are mixer-filter ("mixler") devices, voltage controlled oscillators and channel selector filter networks. The mixlers are translating and filtering the input frequencies, and they represent a unique feature of mechanical signal processing circuits. In the following sections, all the above active functions performed with passive micro-mechanical circuits are described.

3.5.2.1 Mixer-Filters ("Mixler")

Present generations of wireless communication receivers are comprised of filters for channel selection and mixers to realize the down-conversion process. These blocks are implemented as separated stages that interface with one another at the board level. Several drawbacks may arise from large size, high power consumption and the need for impedance matching between the mixer output and filter input. Therefore, the use of the micro-machining technology seems to be a good alternative to overcome the above-mentioned weaknesses, by linking into a single passive micro-mechanical circuit both mixing and filtering functions. Because of that, the structure is called "mixer-filter" or "mixler" [81, 122]. In Figure 3.23 we present a perspective view of a mixler. In fact, such a mixler is a micro-mechanical switch-able filter, consisting of two clamp-clamp resonators connected by a non-conductive beam, each resonator having its own dc biasing. On the input resonator the input RF signal and the local oscillator signal are applied on separate electrodes for mixing, while on the output terminal, the time varying current is obtained at the output.

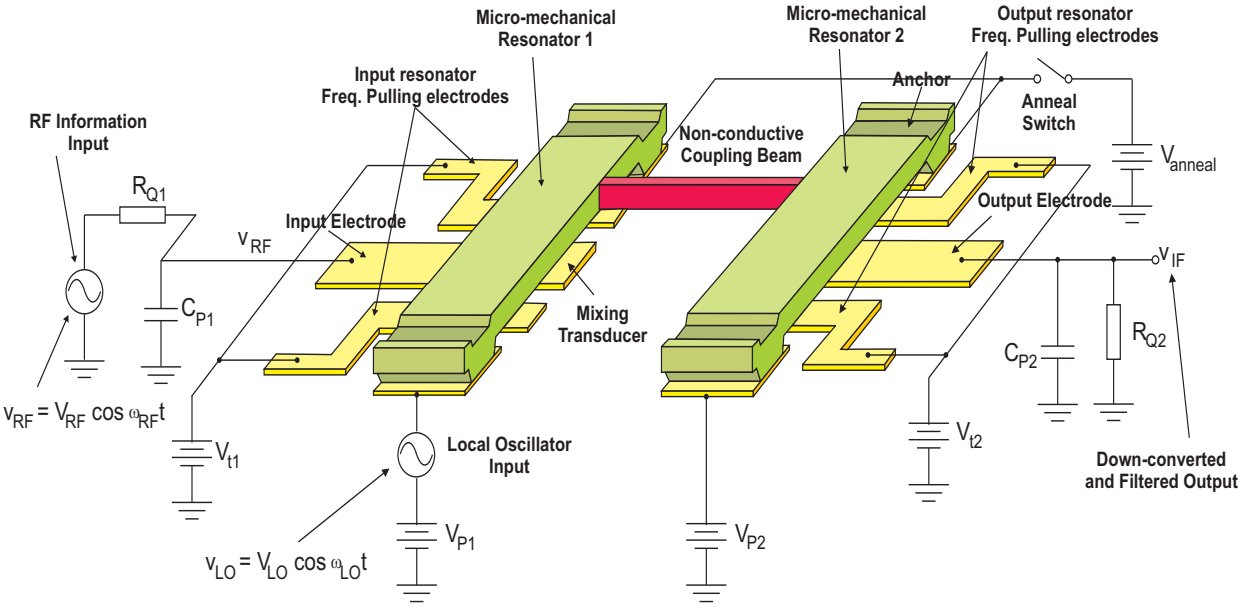


Fig. 3.23: Perspective-view of a Mixer-Filter (source [122]).

The above reported mixler down-converts the radio frequency signals from $233 - 242$ MHz to an intermediate frequency in a range of $33 - 42$ MHz and performs a high-Q filtering with low insertion loss and zero dc power consumption. The spectrum of such a mixler is shown in Figure 3.24.

A mixler converts the two ac electric signals (RF and LO frequencies) into a mechanical force proportional to the frequency difference (RF-LO) via its first clamped-clamped beam resonator, then the mechanically processed signal is transmitted through the non-conductive beam and further filtered in the second resonator, where the output electrical current is obtained through capacitive transduction. The mixing function is accomplished

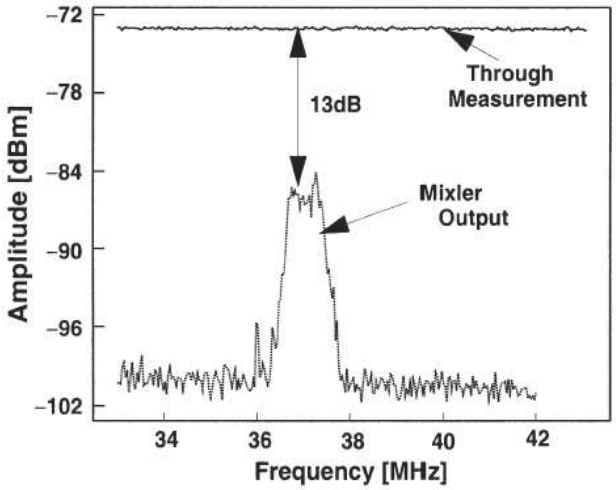


Fig. 3.24: Mixler Spectrum (source [122]).

through the capacitive transducer that achieves the voltage-to-force conversion described by an approximately linear law transfer function:

$$F_{mix} = ... - \frac{1}{2} V_{RF} VLO \frac{\delta C}{\delta x} \cdot \cos(\omega_{RF} - \omega_{LO})t + ... \tag{3.24}$$

where $\omega_{RF} - \omega_{LO}$ is the intermediate frequency ω_{IF}. If the above-mentioned capacitive transducer is coupled to a micro-mechanical filter centered at ω_{IF}, a mixler function is achieved.

3.5.2.2 MEMS Oscillators

Today, the voltage controlled oscillators (VCO) consist of an amplifier and an off-chip LC tank in the positive feed-back, the last one being responsible for the temperature stability of the VCO. The voltage controlled oscillator represents one of the most important source of noise and non-linearity in RF applications, mainly, due to the LC tank. The evolution towards micro-machined tunable capacitors and inductors offer a big improvement in linearity and quality factor, while the losses are minimized and the noise performance improved.

The emerging on-chip local oscillators consisting of an amplifier and an on-chip vibrating $RF\ MEMS$ will bring not only miniaturization due to the on-chip $MEMS$ resonators but high performance in terms of rather decreased low power for a GSM accepted phase noise, as well as long-term and short-term high temperature stability, because of Q much higher than 1000 for the vibrating resonators. Figure 3.25 shows the generic schematic of a series resonant oscillator circuit in which the vibrating micro-mechanical resonator is represented by the series LCR circuit embedded in the positive feedback loop of the amplifier.

The temperature stability of these $MEMS$ based LO as well as the phase noise are al-

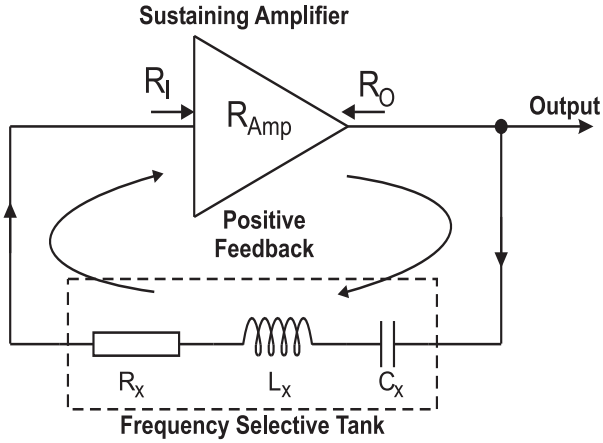


Fig. 3.25: Schematic-view of a Series Resonant Oscillator Circuit (source [65]).

ready equal to the present quartz-based LO. A specific example of an integrated LO that includes an on-chip vibrating $MEMS$ resonator (replacing LC off chip tank) is depicted in Figure 3.26, where a capacitive comb transduced micro-resonator is integrated on the same chip with the amplifier. For this local oscillator, a trans-resistance amplifier is used for a better impedance match to the large motional resistance exhibited by the micro-mechanical resonator. This is an on-chip high performance LO with low losses, obtained from good matching of series resistance, low substrate coupling and parasitic capacitances [65, 66]. However, there are still some disadvantage arising from the superposed noise, which degrades the frequency stability and, thus, affects the phase-noise. Another example of $MEMS$ oscillator is the $61\ MHz$ wine-glass oscillator or with single free-free beam μresonator [65]. This high Q (48000) LO fulfilled the GSM cell phone requirements in terms of phase noise for a power consumption of only 950 micro-watts. However, an unexpected $1/f^3$ noise component appeared from the resonator non-linearity involved in the oscillation amplitude limiting process.

The conditions governing the start-up and sustenance of the oscillation for these $MEMS$-based LO are as follows:

- Start-up: $R_{amp} > R_x + R_i + R_o$;
- Steady-state: $R_{amp} = R_x + R_i + R_o$;
- The total loop phase around the positive feedback loop must be 0^0

where R_{amp}, R_i, R_o are the gain, input resistance and output resistance of the trans-resistance amplifier and R_x is the series motional resistance of mechanical resonator. The functionality of a $MEMS$-based oscillator will be described in detailed in the Chapter 5.

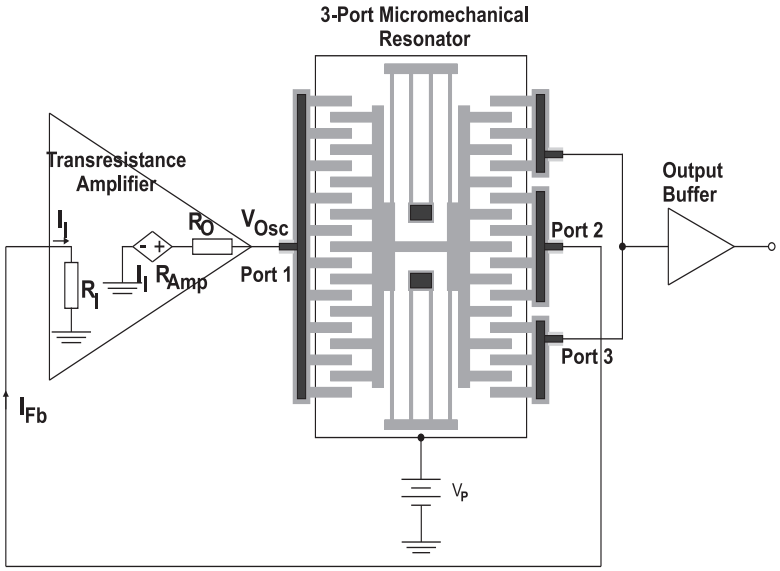


Fig. 3.26: Perspective-view of a Micro-mechanical Oscillator (source [88]).

3.5.2.3 Channel Selector Filter Networks

In wireless communications systems, multiple access techniques are used to permit many mobile users to share simultaneously a radio spectrum. Therefore, it is necessary to design a stage responsible for channel selection. Even if the RF designers have shown a high demand for (front-end) RF channel selector, due to the absence of a big number of high Q (> 10000) tunable resonators, this requirement was difficult to realize with today's technologies. Under these constrains, (only) a band selection is possible and only at IF or baseband, not at the front-end RF level. Under these conditions, the front-end RF stages (LNA, mixer, RF filter) need to handle the un-wished alternate channels interferer, and this will increase the dynamic range and power consumption of the front-end stage. On the other hand, today, there is an increased demand for higher functionality of wireless applications, where multi-mode multi-band reconfigurable devices are strongly required. Such new multi-mode applications would require an increased number of off-chip passive components, which will enhance the size and cost of portable applications. These "trendy" functional requirements have created an excellent opportunity for the high-Q RF vibrating $MEMS$ to show their capability of frequency processing at the front end, by using a high number of $MEMS$ based RF channels. To select an individual RF channel, one can use a single switch-able high-Q RF $MEMS$ filter operating in a non-tunable manner. Such a filter is switched ON by an electronic block, like a decoder [80, 81, 84, 90].

Figure 3.27 shows a schematic of a micro-mechanical RF channel-selector which replaces the above-mentioned off-chip structure.

The new architecture based on the integrated micro-mechanical circuits comprises a bank of on chip micro-mechanical filters, where one switch-able RF $MEMS$ filter is used for selecting a specific frequency channel. In order to select a specific channel, the dc

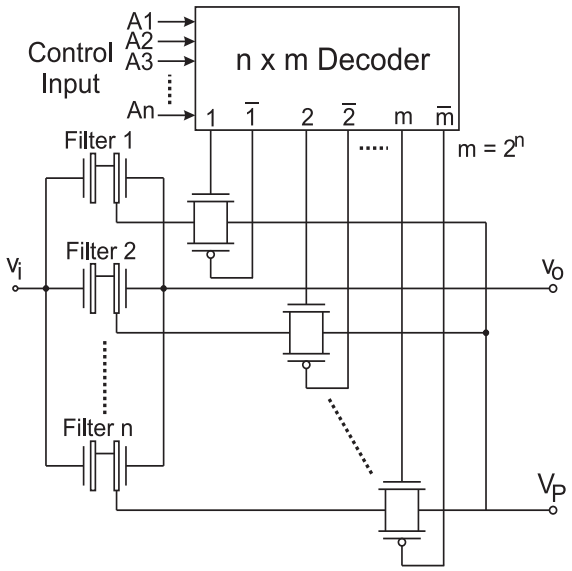


Fig. 3.27: Schematic-view of a Channel Selector Filter Network (source [81]).

voltage is applied by the n x m decoder only to the corresponding $RF\ MEMS$ filters, which will be thus, in the ON state, while all the other $RF\ MEMS$ filter specific to the remaining channels are set on the OFF state (not being dc biased). Consequently, lower dynamic range, low power consumption, higher gain, smaller noise figures are all possible for LNA block. Thus, the overall receiver linearity requirements are relaxed.

3.6 Ultimate RF MEMS Application: Fully Integrated Transceiver

The ultimate trend in wireless applications (cellular handsets, PDA's, low-power networked sensors, ultra-sensitive radar) is to increase functionality by adding multi-mode, multi-band reconfigurability features, simultaneously taking care to minimize the size and power consumption in transceivers. To reach such goals, the main interest is to eliminate the off-chip passive components needed for filtering and frequency generation/processing in wireless communication circuits. In the present receivers, the high Q off-chip elements are the SAW/BAW crystals filters and LC tanks used in voltage controlled oscillators due to their good thermal stability and aging performances. Unfortunately, the LC tanks are still difficult to be on-chip integrated together with $CMOS$ technology, especially at frequencies below $1\ GHz$, while the piezoelectric thin films-based SAW/BAW devices are still hardly to be integrated on silicon chips. Therefore, it is desirable to get the same performance with on-chip, $CMOS$-compatible $RF\ MEMS$ devices. In accordance with this target, a very high integrability arises from the use of the integrated micro-mechanical communication circuits and transistor circuits all integrated onto a single silicon chip. Therefore, the $MEMS$ devices are expected to be used as potential replacements for the high-Q passives (ceramic filters, SAW filters, quartz crystals, $FBAR$ filters) because of their favorable properties: high-Q at GHz frequencies, ther-

mal stabilities, encouraging aging characteristics, antenna-matchable impedances [80, 81]. The already proved functions of $MEMS$ circuits in terms of low-loss filtering, mixing, switching and frequency generation are the driving force for the emerging highly integrated, multi-functional wireless communication applications.

Figure 3.28 shows the present receiver that still contains a size-able number of the off-chip components:

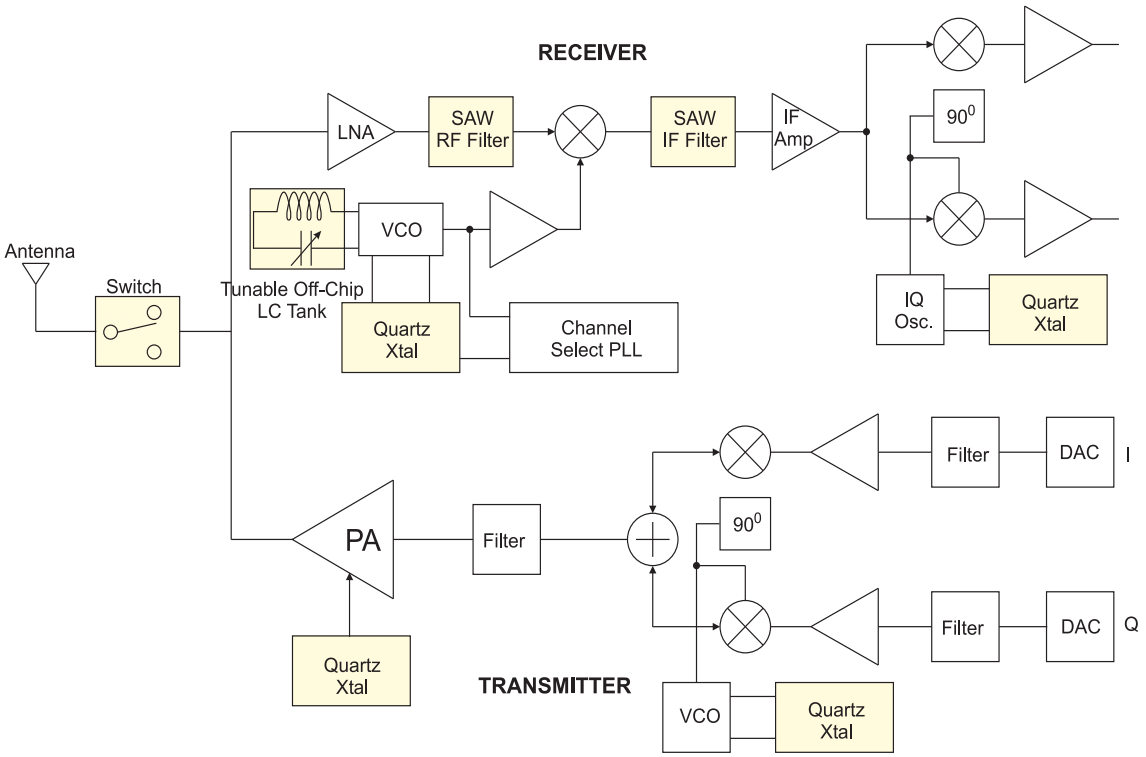


Fig. 3.28: Schematic-view of a Transceiver that uses Off-chip Components (source [90]).

Considering the above potential advantages of $RF\ MEMS$ vibrating devices, the colored stages are those desired to be replaced by $MEMS$ components. To address the value added by $MEMS$ devices, there are several aspects to be solved: 1. The type of the starting material for $MEMS$ technology (silicon, glass etc); 2. The method of micro-machining (surface, bulk, etc); 3. The application space (optical $MEMS$ etc). The literature survey suggests that surface micro-machining on silicon substrate is the selected candidate for the on-chip vibrating $RF\ MEMS$-$CMOS$ technology solution. Thus, $C.T. - C.$ Nguyen et al. have proposed a gradual transition from present transceivers with many off chip passive components to single chip transceiver where all MEMS front end transceivers represent the end of the road map. This evolution is based on the incorporating the vibrating $MEMS$ circuits and devices into wireless communication transceivers [81]. Their approaches will be described briefly below, by means of several evolution stages, as follows: direct-replacement of off-chip high-Q passives, multi-band RF-channel select architecture, all $MEMS\ RF$ Front-End receiver architecture. Their main advantages stand in tiny size, zero dc power dissipation and ultra high quality factor, even in the GHz fre-

quency range. Also, the performance gains are maximized and the trade-off between Q and power is enormously alleviated.

3.6.1 Direct-Replacement of Off-Chip High-Q Passives

In this case, the off-chip ceramic, SAW and crystal resonators are directly replaced by $MEMS$ resonators, inductors or capacitors for voltage controlled oscillators and matching networks, $MEMS$ filters and switches in order to provide enhanced antenna diversity and enormous power savings, as it is shown in Figure 3.29. Therefore, the size is reduced considerably and the integrability is greatly enhanced, moving as many RF $MEMS$ vibrating components as possible on a single silicon chip. By performing the impedance matching between $CMOS$ FET-based LNA and VCO electronic circuits and micro-mechanical vibrating circuits it will open the gate towards increased performances in gain, low power and figure of merit of improved transceiver [80, 81, 82].

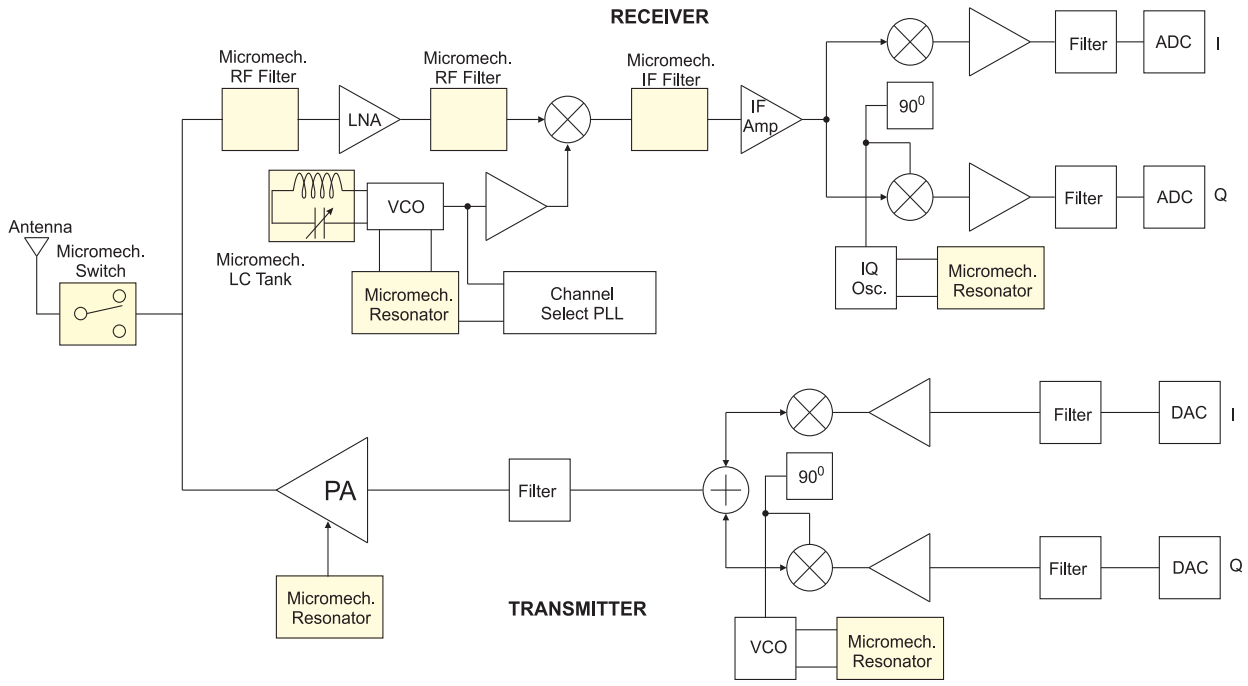


Fig. 3.29: Schematic-view of a Transceiver that uses On-chip Components.

3.6.2 RF-Channel Select Architecture

The direct replacement of off-chip components of present transceiver is a step forward but not the end of the road. Thus, further changes have been made and a new configuration appears as in Figure 3.30. The major benefit of such a structure is the replacement of the active functions like mixers with RF $MEMS$-based passive approach, and this change will give more power reduction because of the use of complex integrated $MEMS$

circuits that are similar to transistor circuits, but operating at zero dc power. Thus, the performance gain is maximized, the size is decreased and no dc power consumption is observed. In this transceiver, three complex features are introduced in the RF front end, as well as at IF: switch-able RF channel select filter, switch-able micro-mechanical resonator synthesizer and micro-mechanical mixer-filter, all of them being explained in the previous subsections [80, 81, 82].

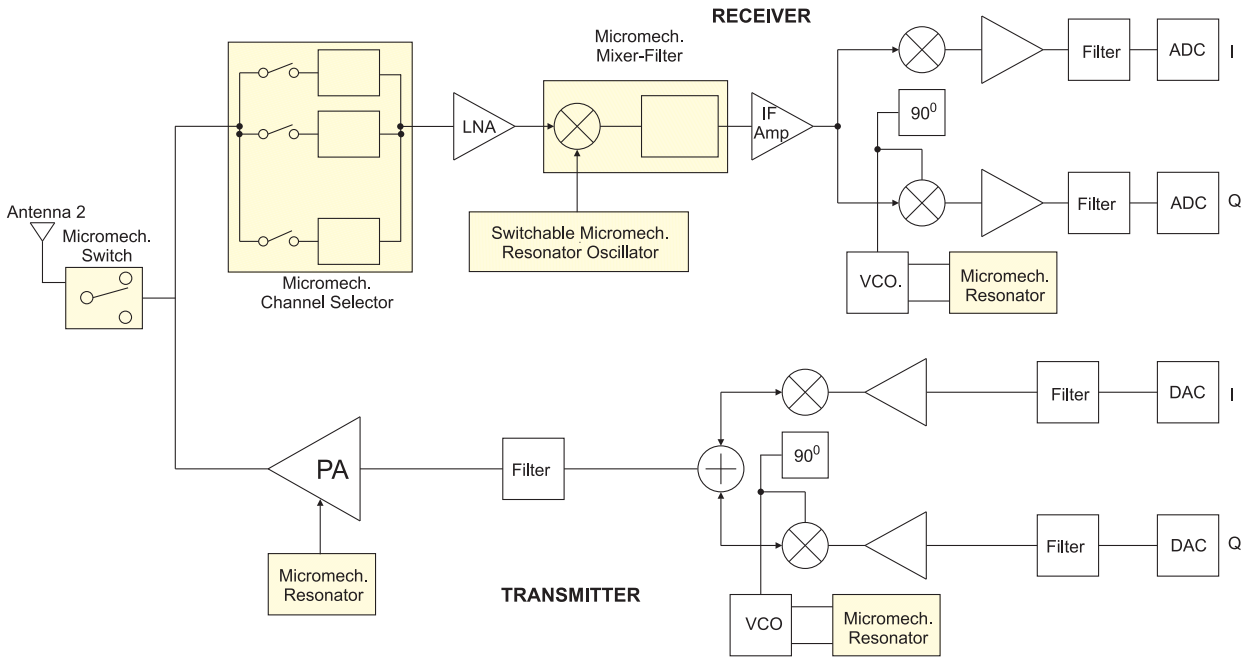


Fig. 3.30: Schematic-view of a Transceiver with Switch-able RF Channel Select Filter, Switch-able Micro-mechanical Resonator Synthesizer and Micro-mechanical Mixer-Filter.

According to the transceiver's structure, the first stage after antenna is allocated to RF filter. Its great advantage is to select the channel at radio frequencies and, thus, the succeeding stages of the receiver (Low Noise Amplifier, mixer) do not need to handle the power of alternate channel interferers. The dynamic range of LNA would be greatly relaxed giving a further power reduction. On the other hand, by realizing the selection of the desired channel immediately after antenna, the adjacent channel interferers are rejected providing a reduction in the phase noise of the local oscillator (VCO). Therefore, the power further decreases, as less electronics is needed to fulfill the noise requirements. Due to the technological difficulty to have tunable LC tanks on RF front end, an alternative is to incorporate low-loss, non-tunable micro-mechanical RF filters in the front end. Actually for multi-band applications, it is desirable to assign a switch-able RF filter to each channel, each filter being selected by a decoder controlling the dc voltage that makes the ON function of the micro-mechanical filter.

In addition, another $MEMS$ stage used in the proposed receiver architecture is the switchable micro-mechanical resonator synthesizer that saves more power when implemented together with the above mentioned RF filter. Moreover, a micro-mechanical mixer-filter can be further used in order to eliminate the dc power consumption assigned

to the normal active mixer. Therefore, an extra power saving of approximately $10 - 20$ mW is established.

3.6.3 All MEMS RF Front-End Transceiver Architecture

Figure 3.31 illustrates a receiver where $MEMS$ components have been inserted within all. Consequently, the use of LNA is eliminated due to the localization of the micro-mechanical RF filter immediately before the micro-mechanical mixer-filter. The new structure can be renamed as an all-$MEMS$ RF front-end receiver. The only active electronics used at RF front-end are those introduced in the local oscillator where the introduction of a μmechanical resonator in the positive loop of the oscillator further saves power.

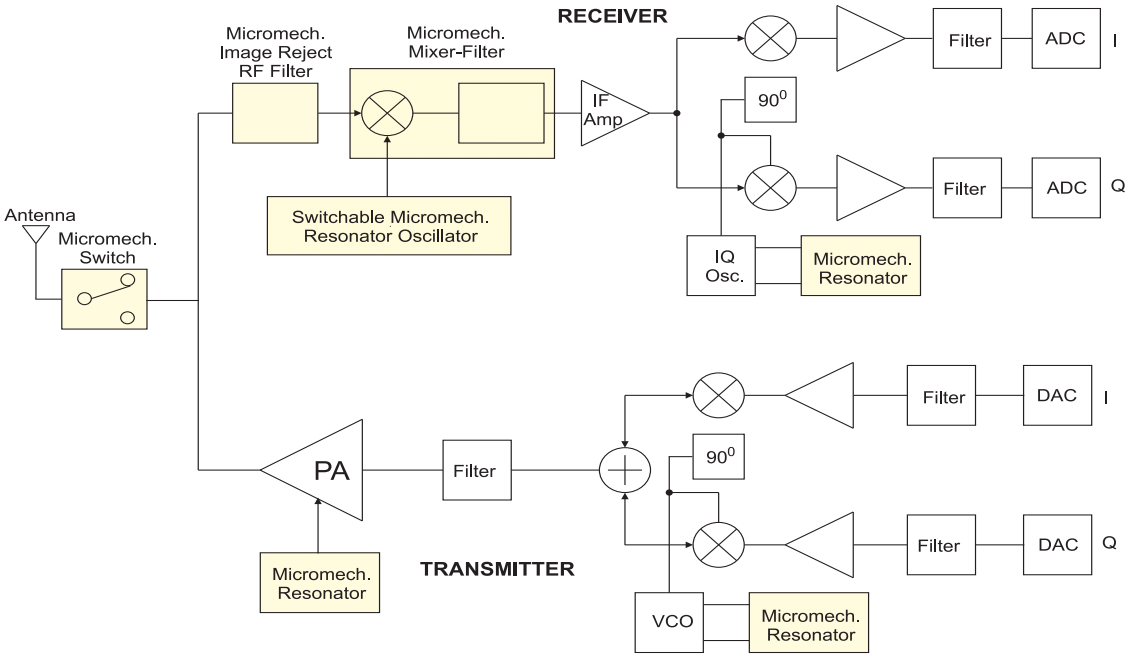


Fig. 3.31: Schematic-view of a $MEMS$ RF Front-End Transceiver.

3.7 Research and Challenging Issues in RF MEMS

The designers face an ultimate challenge to make an on-chip mobile phone that can fulfill at least the same functions of the current counterparts, at higher speed, with lower noise and size. The radio frequency micro-electro-mechanical systems have a lot of potential for replacing the previous configurations. The micro-machining technology matches perfectly with the conventional technology and, thus, the on-chip circuits become realizable. The large off-chip components are going to be eliminated in the future, determining the development of new market application, with increased functionality, mainly in the portable domain.

Wireless communication applications are dealing with new challenges in the field of extra large carrier frequencies in order to provide good performances and accuracy. Therefore, the on-going research deals with the replacement of off chip passive components, as well as new all $MEMS\ RF$ architectures while increasing the carrier frequency up to many GHz. It is worth to noticing that the ultimate trend is to put more than tens of micro-mechanical components on the same chip with $CMOS$ circuits, for obtaining more complex integrated electro-mechanical circuits that can function in the mentioned environment. On the other hand, the devices realized in micro-machining technology provide larger input and output impedances, making more difficult the realization of a good match to antenna impedance. Hence, big effort is focusing on new solutions to optimize the above issues.

3.8 Summary

This chapter consisted in a general overview on the state-of-the-art in micro-electro-mechanical systems. The survey covered the most important high-$Q\ RF\ MEMS$ vibrating devices made in surface micro-machining technology and the functions fulfilled by them when they are put together in emerging new RF architectures for wireless communication applications. The main target is to miniaturize and make possible the integration of the vibrating $RF\ MEMS$ devices together with the $CMOS$ technology on the same chip, to obtain low power, low size, low noise requirements of the next generations of transceivers.

Chapter 4

Contributions to the DC and AC Analytical Modeling of an Un-doped Double Gate SOI MOSFET

In the last few decades, the bulk $CMOS$ devices and their technologies have been scaling down continuously until the short channel effects, already described in the Chapter 2, increased and threatened the performance and further size reduction of the transistor. Thus, the double-gate $SOI\ MOSFET$ appeared as a promising alternative with some important advantages in terms of: $1)$ light doping of the channel, reducing the mobility degradation due to elimination of impurity scattering; $2)$ good control of the short channel effects because of the reduced influence of the drain voltage on the channel charge; $3)$ ideal sub-threshold slope due to the thinning of the silicon film above buried oxide; $4)$ increased electrostatic control due to the gate voltage applied on both sides; $5)$ increased current drive capability due to the volume inversion [6] of the entire silicon film. However, some challenges still exist in terms of $3D$ technological complexity and ultra thin silicon film needed for these $SOI\ MOSFET$ devices.

Another important aspect concerning the development of $CMOS$ devices consists of the efforts devoted to the understanding and modeling of the behavior of $DG\ MOSFET$ devices. The device physics and technology are more complex, since the number of gates is increased and the silicon substrate is very thin and $3D$ processed. There are numerical and analytical models in the literature trying to explain the electrical behavior of the emergent multi-gate devices, but some of them are considering the fitting parameters without physical meaning for explaining the experimental results, while other theoretical approaches are showing a single (isolated) result and not a clear presentation of the transistor characteristics [67, 68, 73, 92, 112]. It is the purpose of this chapter to show a compact analytical modeling of an un-doped double-gate $SOI\ MOSFET$ by proposing convenient and simple methods to calculate the device dc and ac electrical parameters such as: electrostatic potentials, electric charges, drain current, capacitances, cut-off frequency and maximum frequency of oscillation.

In the beginning of the chapter, we are proposing simple mathematical methods needed to perform a compact analytical model of the DC behavior of an Un-doped Double Gate $SOI\ MOSFET$ device. The main target is to explain theoretically the dc characteristics of a symmetric transistor by calculating the silicon electrostatic potentials, inversion charge, electrical current drain and the small-signal parameters in terms of transconductance and output conductance. Besides, it is the purpose of this section to present detailed results and the limitations of the one-dimensional analytical modeling of an un-doped asymmetric $DG\ SOI\ MOSFET$. Finally, the AC analysis of an un-doped symmetric $SOI\ MOSFET$ device will be proposed by starting from the derivation of the small-signal circuit, continuing with the evaluation of terminal charges and capacitances and ending with the calculation of the RF figures of merits such as the cut-off frequency and the maximum frequency of oscillation.

4.1 Contributions to the DC Analytical Modeling of a Symmetric Un-doped DG SOI MOSFET

4.1.1 Background of the DC Analysis for a Symmetric Un-doped DG SOI MOSFET

For the first time, Y. Taur [111] has proposed the analytical calculation of Poisson's equation in the silicon film of an un-doped symmetric $DG\ SOI\ MOSFET$, where only one type of mobile charge (inversion charge) is present. Thus, he has solved the Poisson's equation, considering only the mobile electrons in the channel. According to it, Figure 4.1 shows an un-doped symmetric double gate $SOI\ nMOSFET$ structure which will be one-dimensional ($1D$) analytically analyzed, in this chapter. As it is depicted in the picture, the current flows only on the y direction, the one on the x direction being neglected. As shown in this figure, the $DG\ SOI\ MOSFET$ device presents the symmetry property, according to which both gates have the same work function, oxide thickness and the same applied voltage on the gate terminals.

The corresponding energy bands diagram of $DG\ SOI\ nMOSFET$ is represented in Figure 4.2. Because of the lack of contact in the silicon body of $DG\ SOI\ MOSFET$, the Quasi-Fermi level is constant along the vertical direction (x axis) and the energy levels are referred to the electron quasi-Fermi level of the n^+ source/drain [112]. On the left side (Figure $4.2a$)), the energy bands diagram at thermodynamic equilibrium in the structure is shown, while on the right side (Figure $4.2b$)) the band bending in the presence of an applied voltage on the gates is presented. In addition, this figure proves intuitively also the volume inversion [6] specific to this $DG\ SOI\ MOSFET$, as due to the applied gate voltage, the Fermi level is above the intrinsic Fermi level within the entire volume of an initially p-type substrate.

The silicon thickness is thick enough so that the quantum confinement effects are not

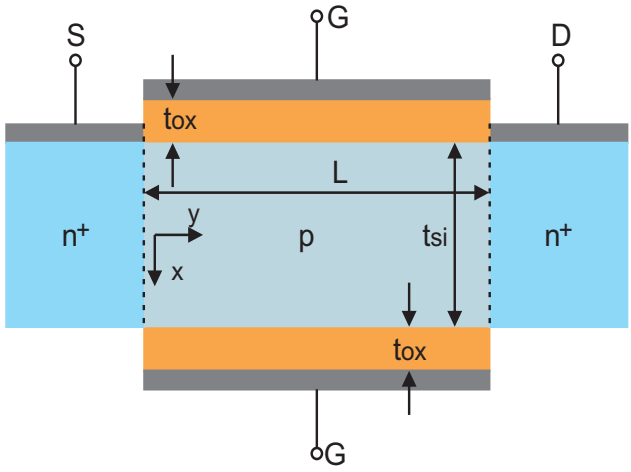


Fig. 4.1: Schematic-cross section of a Double Gate $SOI\ MOSFET$ structure.

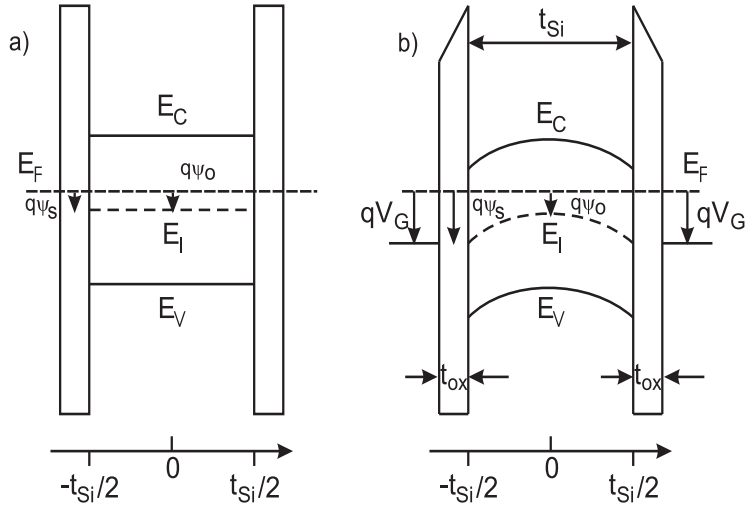


Fig. 4.2: Schematic energy bands diagram for a Double Gate $SOI\ MOSFET$, at thermodynamic equilibrium.

taken into account. As shown in the literature, for thin silicon films of the SOI, the substrate can be very lightly doped, as the channel charge control is performed by the two gate voltages, which are thus reducing the $DIBL$ effects described earlier. So, it can be easily understood that the fix charge in the depletion and channel region can be ignored when solving the Poisson equation. Actually, we can simply prove that. If we want to neglect the mobile carriers and the fix charge of substrate of about $N_B = 10^{15}\ cm^{-3}$, then from simple calculation it is obtained that the applied gate voltage should be higher than 0.37 V. Another assumption in the thesis consists of the Maxwell-Boltzmann statistics for the charge carriers in silicon. Within this general description of the model, we are also considering the drain voltage, V, applied on the drain terminal. Such an approach is useful for the drain current calculations that will be shown later. However, for the calculation of the electrostatic potential and charges at the thermal equilibrium, the drain voltage will not be considered initially. In agreement with the above SOI considerations and assump-

tions, the starting point of the analytical model consists of the calculation of the Poisson's equation as in [67, 73, 111] by using only the inversion charge, i.e., the electrons:

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \cdot (e^{\frac{q(\psi - V)}{kT}} - e^{-\frac{q\psi}{kT}}) \tag{4.1}$$

with the following boundary conditions:

$$\frac{d\psi}{dx}|_{x=0} = 0 \tag{4.2}$$

$$V_{GS} - V_{FB} = \psi|_{x=\frac{t_{si}}{2}} + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} \cdot \frac{d\psi}{dx}|_{x=\frac{t_{si}}{2}} \tag{4.3}$$

where: Ψ represents the electrostatic potential in the silicon body, V_{FB} is the flat-band voltage, V_{GS} - gate to source voltage, t_{Si} - silicon thickness, t_{ox} - oxide thickness ($2nm$ throughout the thesis), V is the channel voltage, when the V_{DS} voltage is applied on the device, ε_{si} - electrical permittivity of the silicon, ε_{ox} - electrical permittivity of the silicon dioxide, k - Boltzmann constant, T - temperature, n_i - intrinsic charge carrier concentration of silicon. Because we consider the mid-gap electrodes, the work function difference between gate and silicon is zero, and for simplicity, we ignore the effect of the interface charges on the flat-band voltage, and thus we take an ideal $V_{FB} = 0\,V$ throughout the thesis. An alternative approach would be to operate everywhere in the thesis with $V_{GS} - V_{FB}$ as term instead of our V_{GS} term.

The boundary condition (4.2) shows the idea of the maximum electrostatic potential present in the central part of silicon film, while the boundary condition given by relation (4.3) denotes the continuity of the normal electrical displacement at the interface between silicon and SiO_2.

From the first integration of Poisson's equation, one can derive the electric field in the silicon film:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{si}} \cdot e^{-\frac{qV}{kT}} \cdot [e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}}]} \tag{4.4}$$

and the electrostatic potential is computed by making the second integration of it:

$$\psi(x) = \psi_0 - \frac{2kT}{q} \cdot ln[\cos(b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot x)] \tag{4.5}$$

while the amount b is: $b = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}$ and ψ_0 represents the electrostatic potential at the central point of the silicon body.

When $x = \pm\frac{t_{si}}{2}$ and by using the relation (4.5), the electrostatic potential at the silicon film surface (ψ_s) is derived:

$$\psi_s = \psi_0 - \frac{2kT}{q} \cdot ln\{\cos[b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot \frac{t_{si}}{2}]\} \tag{4.6}$$

Also, at the surface of the silicon body, the electric field, is given by (4.4) by replacing x with $\pm\frac{t_{si}}{2}$. Thus, from the second boundary condition (4.3), an important equation related to the applied gate voltage and the electrostatic potential is computed:

$$V_{GS} - V_{FB} = \psi_s + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} \cdot \sqrt{\frac{2kTn_i}{\varepsilon_{si}} \cdot e^{-\frac{qV}{kT}} \cdot [e^{\frac{q\psi_s}{kT}} - e^{\frac{q\psi_0}{kT}}]} \tag{4.7}$$

Further, we are proposing original, simple and efficient methods to solve the above transcendental equation that will allow us to develop a compact analytical modeling of an un-doped $DG\ SOI\ nMOSFET$.

4.1.2 Original Calculation Method for the Electrostatic Potentials at Thermo-dynamic Equilibrium

The main target of this section of the thesis is to introduce our simple method for the calculation of the surface electrostatic potential in the silicon film of an un-doped symmetric $DG\ SOI\ nMOSFET$. Thus, our approach consists of the extending of the calculation of the silicon electrostatic potentials until a transcendental equation is obtained. By using our method, the electrostatic potential in the center of the silicon film can be derived and then the surface silicon electrostatic potential. In the first step, for the simplicity's purpose, the device is assumed to operate at the thermodynamic equilibrium according to which no voltage is applied on the drain terminal ($V = 0\ V$).

4.1.2.1 Graphical Method for the Calculation of the Electrostatic Potential from the Center of the Silicon Film, at Thermo-dynamic equilibrium

Our method consists of the determination of the electrostatic potential in the center of silicon body by means of the relations (4.6) and (4.7) as follows. We introduce the potential ψ_s in the relation (4.7) and then, get a transcendental equation that relates the applied gate-to-source voltage and the electrostatic potential in the middle of the silicon film as it is written below:

$$V_{GS} - \psi_0 = a \cdot e^{\frac{q\psi_0}{2kT}} \cdot |\tan(y)| - \frac{2kT}{q} \cdot ln\{\cos(y)\} \tag{4.8}$$

where the amounts a and y are:

$$a = \frac{t_{ox} \cdot \sqrt{2\varepsilon_{si} kTn_i}}{\varepsilon_{ox}}; \quad y = b \cdot e^{\frac{q\psi_0}{2kT}} \cdot \frac{t_{si}}{2} \tag{4.9}$$

By analyzing the relation (4.8), one can see that there are some limitations in the variation of ψ_0 electrostatic potential introduced by the definition domain of the functions involved in that transcendental equation. Thus, from the condition of the existence for the logarithm function ($cos(y) > 0$) we get the variation domain for y amount which is $y \in [-\frac{\pi}{2}; +\frac{\pi}{2}]$. From the definition of the amount y, one can easily observe that the variation of y is in the range of $[0; +\frac{\pi}{2}]$. If we consider the fact that we work with positive electrostatic potentials (n channel DG SOI MOSFET), then we obtain the following variation range for ψ_0:

$$\psi_0 \in (0; \psi_{0m}]; \tag{4.10}$$

where ψ_{0m} is derived for $y = +\frac{\pi}{2}$. Making these calculations, we obtain the following equation for the maximum limit (ψ_{0m}) of the central silicon electrostatic potential:

$$\psi_{0m} = \frac{2kT}{q} \cdot ln(\frac{\pi}{t_{si} \cdot b}) \tag{4.11}$$

As an example, for $t_{si} = 20\ nm$ and the room temperature $T = 300\ K$, we get $\psi_{0m} = 0.462\ V$, while for $t_{si} = 5\ nm$, we obtain $\psi_{0m} = 0.5341\ V$.

It is worth to note that the maximum value of electrostatic potential in the center of the silicon body depends only on the thickness of the silicon film. Thus, according to the miniaturization process of devices, ψ_{0m} increases when silicon thickness decreases until a value of about $5\ nm$ where the quantum effects can not be neglected anymore.

By solving the equation (4.8), we can obtain the value of the electrostatic potential at the middle of silicon film for each applied gate-to-source voltage. By considering the variation domain for ψ_0 in the range $(0; \psi_{0m}]$, from equation (4.8) one can obtain the variation domain for V_{GS}. In our case, we have chosen for V_{GS} value ranging from $0.2\ V$ to $1.5\ V$ in order to assure that only electrons play a role in Poisson's equation, on one hand, and, on the other hand, to let V_{GS} to be much higher than the threshold voltage for a good current drive of the $DG\ SOI\ MOSFET$ transistor.

At this point, because the limits of both gate-to-source voltage and electrostatic potential in the middle of the silicon film are found, the transcendental equation (4.8) is solved with graphical method, as described in our published paper [129]. Starting from the relation (4.8), we have defined two functions: f and g, both of them depending on V_{GS}, and ψ_0 and the difference between them is denoted h as follows:

$$f = V_{GS} - \psi_0 \tag{4.12}$$

$$g = a \cdot e^{\frac{q\psi_0}{2kT}} \cdot |\tan(y)| - \frac{2kT}{q} \cdot ln\{\cos(y)\} \tag{4.13}$$

$$h = f - g \tag{4.14}$$

The definition domain of the two functions f and g is thoroughly analysed, so that to be able to solve the above transcendental equation. For each value of V_{GS} in the above domain, ψ_0 is allowed to vary from 0 to the ψ_{0max} and, when h tends to zero, we obtain the ψ_0 corresponding to that input V_{GS} value. The above described algorithm is implemented in Matlab tool. In order to prove its efficiency and applicability, an example is given in Figure 4.3, where the two functions f and g are represented in respect to ψ_0 for $V_{GS} = 0.5$ V, $V_{FB} = 0$ V and $V_{DS} = 0$ V. One can conclude that the intersection point of both functions f and g represents the solution of the transcendental equation (4.8) or a given set of values. Therefore, for an applied gate-to-source voltage of 0.5 V, a central silicon electrostatic potential of 0.4353 V was obtained and this solution fits perfectly with the condition introduced by (4.10).

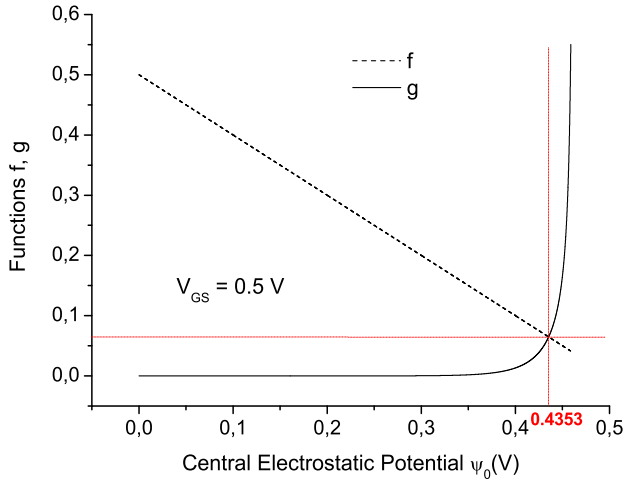


Fig. 4.3: Graphical method for the calculation of the electrostatic potential drop in the center of the silicon body ψ_0, when $V_{GS} = 0.5$ V. The functions f and g are dependent on ψ_0 and V_{GS}.

By using our method described above and varying the applied voltage on the gate terminal, a range of solutions for the central silicon electrostatic potential is derived. Then the electrostatic potential at the surface of the silicon film is obtained from relation (4.6). Thus, we show in Figure 4.4 the dependence of ψ_0 and ψ_s as a function of V_{GS} for different silicon thicknesses: 5 nm and 20 nm. The results for the electrostatic potential in the center of the silicon film obtained with our graphical method in Matlab (see Appendix B.1) are in good agreement with the results presented in the literature [112].

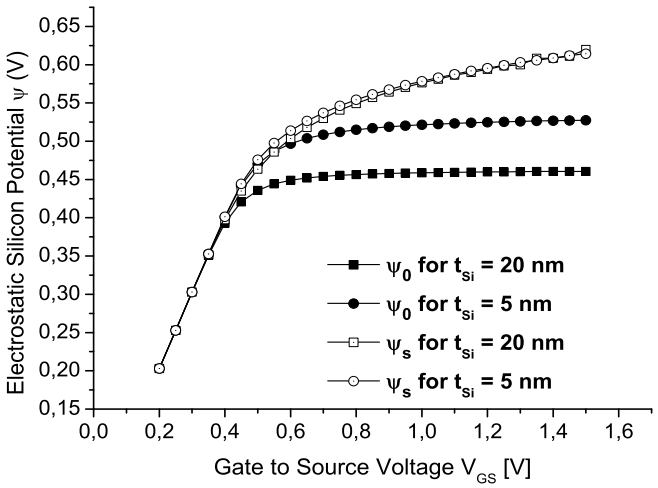


Fig. 4.4: The electrostatic potentials ψ_s and ψ_0 as a function of V_{GS} voltage. This result was obtained with our graphical method for silicon thickness of $5\ nm$ and $20\ nm$.

4.1.3 Original Methods for the Calculation of the Electrostatic Potentials at Thermodynamic Non-Equilibrium

An important step in the analytical modeling of the un-doped symmetric $DG\ SOI\ MOSFET$ has been done by S. Malobabic et.al. [73] where the influence of the applied voltage along the channel on the mobile charge in the silicon film has been introduced. In their paper, the Lambert function has been used for the calculation of the surface electrostatic potential in the silicon. Unfortunately, their approach is mathematically very complicated and uses smoothing parameters without physical meaning. Therefore, this section is going to introduce our two simple methods for the calculation of that surface electrostatic potential in the silicon film and, thus, making unnecessary the application of Lambert function in a symmetrical $DG\ SOI\ MOSFET$ device. The first approach is the above-mentioned graphical method extended for different potentials applied on the drain terminal of the transistor, while the second procedure relates with the bisection method used for the general case of device's operation, as described in our published paper [133].

4.1.3.1 Graphical Method for the Calculation of the Electrostatic Potential from the Center of the Silicon Film

Within this subsection, for the calculation of the electrostatic potential at thermodynamic non-equilibrium we extend our method presented before and in the paper [129], by including the effects of the applied V_{DS} voltage as shown below. From (4.3), (4.4) and (4.5), the following transcendental equation is obtained:

$$V_{GS} - \psi_0 = a \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot |\tan(z)| - \frac{2kT}{q} \cdot ln\{\cos(z)\} \tag{4.15}$$

where the amounts a is the same from equation 4.9 and z is:

$$z = b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot \frac{t_{si}}{2} \tag{4.16}$$

By analyzing the relation (4.15), we can determine the permitted values of the central electrostatic potential in agreement with the definition domain of the functions involved in the transcendental equation. Thus, from the existence condition for the logarithmic and tangent functions, we get the following accepted values for ψ_0:

$$\psi_0 \in (0; \psi_{0m}]; \tag{4.17}$$

where

$$\psi_{0m} = V + \frac{2kT}{q} \cdot ln(\frac{\pi}{t_{si} \cdot b}) \tag{4.18}$$

At this point, by taking into account the dependence of ψ_0 as a function of voltages applied on drain and gate terminals, the transcendental equation (4.15) is solved with our graphical method. According to it, the expression (4.15) is divided into two functions f and g, both being dependent on V and V_{GS}.

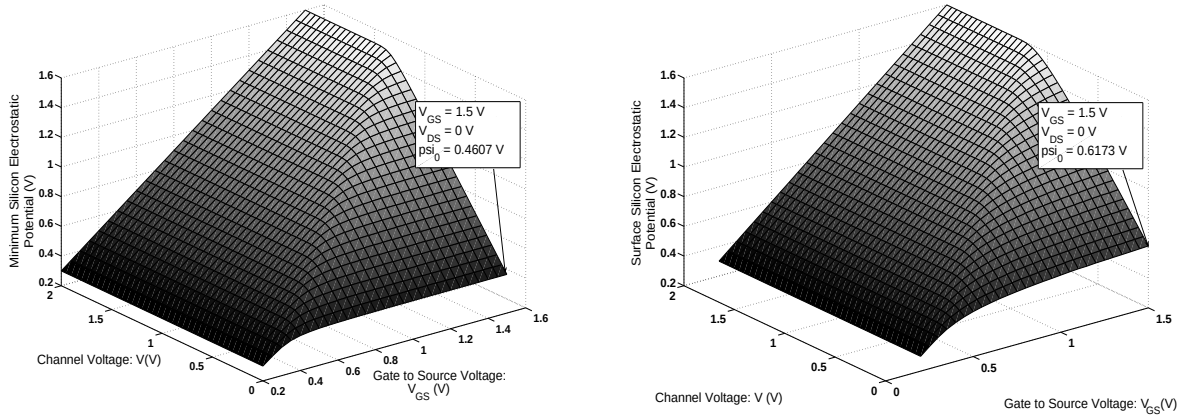
$$f = V_{GS} - \psi_0 \tag{4.19}$$

$$g = a \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot |\tan(y)| - \frac{2kT}{q} \cdot ln\{\cos(y)\} \tag{4.20}$$

$$h = f - g \tag{4.21}$$

Our graphical method developed in the Matlab code (see Appendix B) allows the determination of ψ_0 for each V_{GS} between $0.37\ V$ and $1.5\ V$ and V channel values being in the range of $[0; 2]\ V$. The solution ψ_0 is obtained when h is equal to zero for a set of values V_{GS} and V, as the input points. For each calculated value of ψ_0 one can compute the electrostatic potentials in the bulk and at the surfaces $(x = \pm\frac{t_{Si}}{2})$ as shown in the equation (4.5). In Figure $4.5a$ we show the calculated dependence of the electrostatic potential from the central part as a function of channel and gate to source voltages (when $V_{GS} > 0.37\ V$, in order to keep only the electrons in the Poisson equation, as explained above) while in the Figure $4.5b$ it is depicted the dependence of the surface electrostatic

potential as a function of the same parameters. One can observe that, for small values of channel voltage and the gate to source voltage in the whole variation domain, the electrostatic potential at the surface is higher than the one from the silicon center while at higher channel and gate to source voltages the two electrostatic potentials have similar values. One can thus conclude that the entire silicon film is under the volume inversion and it becomes a solid body having the same electrostatic potential.



(a) ψ_0 (b) ψ_s

Fig. 4.5: The electrostatic potentials as a function of gate to source and channel voltages.

Figure 4.6 shows the dependence of the electrostatic silicon potential as a function of the channel voltage when different voltages are applied on both gates - see Appendix B.1.

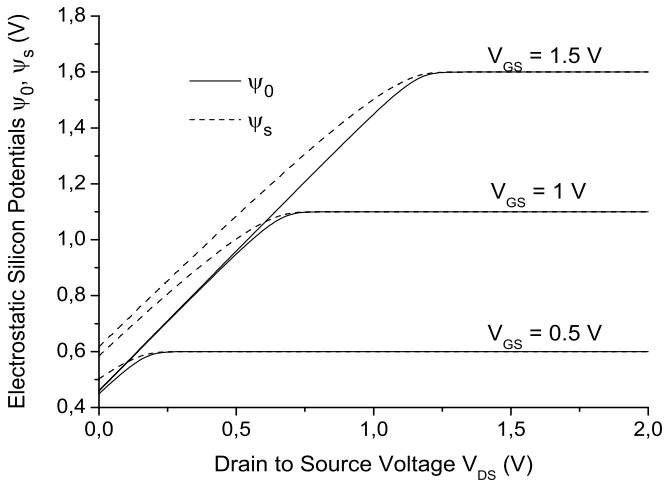


Fig. 4.6: The silicon electrostatic potential as a function of the channel voltage when the gate voltage takes the values of $0.5\ V$, $1\ V$ and $1.5\ V$.

We remark that when the channel voltage is situated in a range with small values, the minimum electrostatic potential has different values compared with the surface electro-

static potential. When this channel voltage increases, both minimum and surface electrostatic potentials are pinned together. Consequently, when the drain voltage is applied, the electrostatic potentials in silicon are different only for small values of the channel voltage, while at channel voltage higher than a certain value, the entire silicon film being under the same potential.

In order to enforce the above-mentioned explanations, Figure 4.7 shows the dependence of the electrostatic potential with the position in the silicon body for different applied gates and drain voltages.

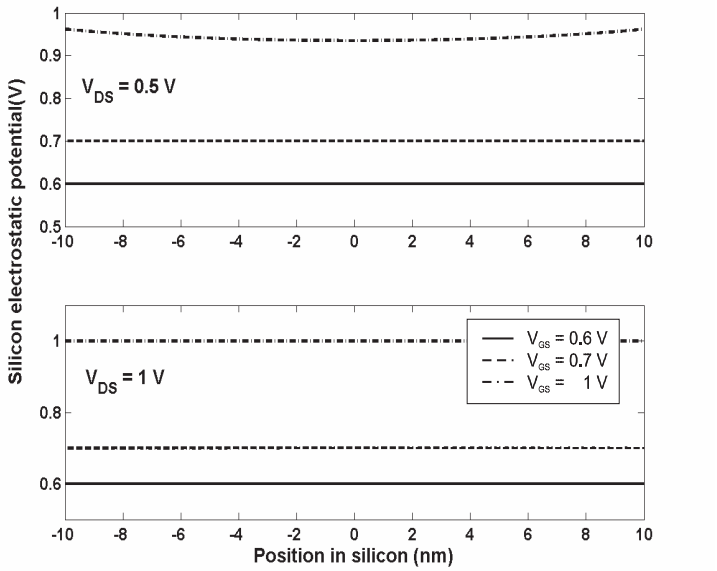


Fig. 4.7: The variation of the electrostatic potential with the position in the silicon film for the drain voltage equal to $0.5\ V$ and $1\ V$. The gate voltage takes the values of $0.6\ V$, $0.7\ V$ and $1\ V$.

If no voltage is applied on the drain terminal, the electrostatic potential presents a minimum in the middle of the silicon layer and the surface electrostatic potentials are very well emphasized when gates voltages increases. In the same time, one can be observed that the position of the minimum potential falls in the middle of silicon film. Further, by considering a drain voltage different from zero, (which means a channel voltage higher than zero at any y position between source and drain), at zero (and low) channel voltages the electrostatic potential has a clear parabolic shape. This shape is even more evident at higher gate voltages, while at higher channel voltages the electrostatic potential in the silicon is perfectly flat, even when higher gate voltages are applied. The same effect can be observed for a high channel voltage, independent on the applied gate voltage. This flattening effect of the channel voltage on the electrostatic potential in the whole silicon body was seen for the first time by us. Actually, one can say that the concept of the minimum electrostatic potential in the silicon in the presence of higher channel potential is no longer valid, as the potential is almost constant in the entire silicon body.

4.1.3.2 Bisection Method for the Calculation of the Electrostatic Potential from the Center of the Silicon Film

Earlier, S. Malobabic et al. [73] has shown a method for solving the above transcendental equation to obtain the values of ψ_0 by using the Lambert function together with a set of smoothing functions, as can be seen below.

$$\psi_0 = U - \sqrt{U^2 - (V_{GS} - V_{FB}) \cdot V_{FB}} \tag{4.22}$$

$$U = \frac{1}{2} \cdot [(V_{GS} - V_{FB}) + (1 + r) \cdot \psi_{0max}] \tag{4.23}$$

$$r = (At_{ox} + B)(\frac{C}{t_{si}} + D)e^{-EV} \tag{4.24}$$

where the following parameters were found in order to model ψ_0 from the above authors: $A = 0.0267\, nm^{-1}$, $B = 0.0270$, $C = 0.4526\, nm$, $D = 0.0650$, $E = 3.2823\, V^{-1}$, $V_{FB} = 0$ V for simplicity, r is the shoulder smoothing parameter and equation (4.24) is empirical.

As the smoothing parameters have no physical meaning, we have developed a simple mathematical method for solving the same transcendental equation, as shown in our published paper [133]. This is an alternative approach to our method presented above. Thus, for the non-equilibrium conditions, our second proposed approach, the so-called bisection method, solves a transcendental equation in which the surface electrostatic potential is determined as a function of the gate-to-source voltage V_{GS} and drain-to-source voltage V_{DS} as shown below.

When the relation (4.4) is introduced in (4.3), a transcendental equation is obtained and then rearranged in order to have the following form:

$$\psi_S - V_{GS} + a \cdot \sqrt{\mathrm{e}^{-\frac{qV}{kT}} \left(\mathrm{e}^{\frac{q\Psi_S}{kT}} - \mathrm{e}^{\frac{q\psi_0}{kT}} \right)} = 0 \tag{4.25}$$

The next step is to define a function, f, where its domain and co-domain are related by the following expression:

$$f(\psi_S) = \psi_S - V_{GS} + a \cdot \sqrt{\mathrm{e}^{-\frac{qV}{kT}} \left(\mathrm{e}^{\frac{q\Psi_S}{kT}} - \mathrm{e}^{\frac{q\psi_0}{kT}} \right)} \tag{4.26}$$

Now, one can easily remark that the solution of the equation (4.25) is obtained for $f(\psi_S) = 0$, i.e., the solution is given by the intersection of the function f with the horizontal axis, which is represented by ψ_S in this case. If the function keeps the same monotony in a given interval $[c, d]$ and goes through a zero value inside that interval, then the following condition $f(c) * f(d) < 0$ is fulfilled.

In our case, the searched value of ψ_S must be in the range of $[0, V_{GS}]$, because the electrostatic potential in the n-channel DG SOI MOSFET is positive and cannot exceed the applied V_{GS} voltage.

For the application of the bisection method in order to determine the solution ψ_S, we have to consider an interval $[c, d]$ and the median point $m = \frac{c+d}{2}$. Then, we have to calculate the values of the f, in the following points: $f(c)$, $f(m)$ and $f(d)$. If the product $f(c) * f(m) < 0$, then the desired value of ψ_S is in the interval [c,m]. If the product $f(m) * f(d) < 0$, then the searched solution of transcendental equation (4.25) is in interval $[m, d]$. After the identification of the reduced interval where the solution is located ($[c, m]$, $[m, d]$) we shall continue the procedure in the same way until we find the solution ψ_S with the desired accuracy.

4.1.4 Channel Potential Asymmetry Effects on the Electrical Current in a Symmetric Un-doped DG SOI MOSFET

In this subsection, we investigate the effect of the drain voltage on the value and localization of the minimum electrostatic potential. Thus, we want to analyze the asymmetry introduced by the channel voltage in an un-doped symmetric $DG\ SOI\ MOSFET$. Because we assumed that the minimum electrostatic potential will not be maintained in the middle of the silicon layer as the channel voltage increases, the equation that presents the silicon electrostatic potential function with position will be slightly changed as it follows:

$$\psi(x) = \psi_0 - \frac{2kT}{q} \cdot ln[\cos(b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot (x - x_0))] \tag{4.27}$$

Due to the asymmetry induced by the drain voltage, the boundary conditions (4.2) and (4.3) are transformed in the following relations corresponding to both the bottom and the top interfaces as follows:

$$\frac{d\psi}{dx}|_{x=x_0} = 0 \tag{4.28}$$

$$\frac{\varepsilon_{ox}(V_{GS} - \psi|_{x=\frac{t_{si}}{2}})}{t_{ox}} = \varepsilon_{si} \cdot E|_{x=\frac{t_{si}}{2}} \tag{4.29}$$

$$\frac{\varepsilon_{ox}(V_{GS} - \psi|_{x=-\frac{t_{si}}{2}})}{t_{ox}} = \varepsilon_{si} \cdot E|_{x=-\frac{t_{si}}{2}} \tag{4.30}$$

where expressions (4.29) and (4.30) illustrate the continuity of the normal electrical displacement at the front and back interfaces between silicon and oxide. The equation (4.28) from above relates to the position of the minimum electrostatic potential which is not automatically considered to be in the central part of the silicon layer, but x_0 may be located somewhere in the silicon film. Considering the relations (4.4), (4.27), (4.28), (4.29) and (4.30) and combining them, one can obtain an explicit system of two transcendental equations that provides the minimum electrostatic potential (ψ_0) and its location (x_0). Both parameters are dependent on the channel potential and the gate voltage as shown below in the equations (4.31) and (4.32):

$$V_{GS} - \psi_0 = a \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot |\tan(y_1)| - \frac{2kT}{q} \cdot ln\{\cos(y_1)\} \tag{4.31}$$

$$V_{GS} - \psi_0 = a \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot |\tan(y_2)| - \frac{2kT}{q} \cdot ln\{\cos(y_2)\} \tag{4.32}$$

where the parameters y_1 and y_2 are given below:

$$y_1 = b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot (\frac{t_{si}}{2} - x_0) \tag{4.33}$$

$$y_2 = b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot (-\frac{t_{si}}{2} - x_0) \tag{4.34}$$

Looking at the two transcendental equations (4.31) and (4.32), one can see that the logarithmic and tangent functions restrict the domains of definitions of both parameters ψ_0 and x_0. Therefore, by using the mathematical definitions for the above-mentioned functions, the upper end of the range of variation for the minimum silicon electrostatic potential will be limited by one of the following relations:

$$\psi_0 < V + \frac{2kT}{q} \cdot ln(\frac{\pi}{2b \cdot (\frac{t_{si}}{2} + x_0)}) \tag{4.35}$$

$$\psi_0 < V + \frac{2kT}{q} \cdot ln(\frac{\pi}{2b \cdot (\frac{t_{si}}{2} - x_0)}) \tag{4.36}$$

According to the previous expressions and accepting here, for the simplicity of calculations, that the maximum value of ψ_0 is placed in the central point of the silicon film, we can calculate the upper limit of the range for the electrostatic potential, which is: $(V + 0.4643)\ V$. In order to know the domain of definition for ψ_0, the low end must be computed, too. For this purpose, we have to find the working gate voltages which will allow solving the Poisson equation with only inversion carriers, i.e. neglecting the fix charge and the mobile minority carriers. If we want to neglect the mobile carriers and the fix charge of substrate of about $N_B = 10^{15}\ cm^{-3}$, then, from simple calculation it is obtained that the applied gate voltage should be higher than $0.37\ V$. Therefore, according to our model, we conclude that the minimum silicon electrostatic potential should vary in the range of $0.37\ V$ up to $(V + 0.4643)\ V$. At the same time, we assume that x_0 is located within the silicon layer, since the electrostatic potential may have an extreme value inside of it. At the same time, for finding an accurate definition domain, we need to eliminate those values of (x_0, ψ_0) that provide infinite value of the tangent function. Therefore, we transform the inequalities (4.35) and (4.36) into two equalities that determine the points which do not belong to the domains of ψ_0 and x_0, denoted by $(x_0, \psi_0)_{tan}$. As a conclusion, the definition domain for the functions involved above is the $2D$ domain of the form $(((-\frac{t_{Si}}{2}, \frac{t_{Si}}{2}) \times (0.37\ V, (V + 0.4643)\ V)) - (x_0, \psi_0)_{tan})$.

Now, after having obtained the definition intervals for each parameter, the graphical method can be applied and the minimum electrostatic potential together (ψ_0) with its position (x_0) are calculated with transcendental equations (4.31) and (4.32) as it was shown in our work [132]. For this, each relation is divided into two functions: f and g, both of them being dependent on the channel voltage V and gate to source voltage V_{GS} and the difference between them is called h as it is shown below:

$$f_1 = f_2 = V_{GS} - \psi_0 \tag{4.37}$$

$$g_1 = a \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot |\tan(y_1)| - \frac{2kT}{q} \cdot ln\{\cos(y_1)\} \tag{4.38}$$

$$g_2 = a \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot |\tan(y_2)| - \frac{2kT}{q} \cdot ln\{\cos(y_2)\} \tag{4.39}$$

$$h_1 = f_1 - g_1 \tag{4.40}$$

$$h_2 = f_2 - g_2 \tag{4.41}$$

For each value of V_{GS} in the domain of $[0; 1.5]\ V$, ψ_0 varies from $0.37\ V$ up to $V + 0.4643$ V while its position is allowed to move from $-\frac{t_{Si}}{2}$ up to $\frac{t_{Si}}{2}$ in both equations and, when h_1 and h_2 tend to zero, we obtain the ψ_0 and x_0 for that channel voltage. In this manner, we calculate both minimum electrostatic potential and its position for the entire range. Figure 4.8 shows the dependence of the minimum, front surface and back surface electrostatic potentials as a function of gate to source voltage for different channel voltages when the silicon thickness equals to $10\ nm$ and oxide thickness is $2\ nm$.

One can see that, for small channel voltages, the front and back surface potential dependencies are split and the hypotheses with x_0 different from zero makes sense. It is worth to noticing, for high channel voltages, that the entire silicon layer has the same electrostatic potential in each point of it. The result where the entire silicon body has the same potential for high channel voltage was also obtained for the pure symmetric approach, as described in the previous section.

In order to strongly emphasize, that an un-doped symmetric $DG\ SOI\ MOSFET$ introduces asymmetry effects, Figure 4.9 presents the variation of the silicon electrostatic potentials with the channel voltage when the gate to source voltage equals to $0.6\ V$ - see the software program developed for this in the Appendix B.2.

Figure 4.10 depicts the distribution of the electrostatic potential in the silicon film when the drain and gate voltages are those written in the graphics. We observe that the position of the extremum is not in the central part of the silicon layer and the minimum is shifting as a function of the applied channel voltages. When the drain voltage is different from zero, one can notice that the shapes depend on the gate voltage and when those channel voltages values are high enough, the overall silicon presents the same electrostatic potential. This figure also shows the difficulties in finding the minimum potential, for higher values of channel voltage or gate voltage, when the dependence is almost flat in the entire silicon body.

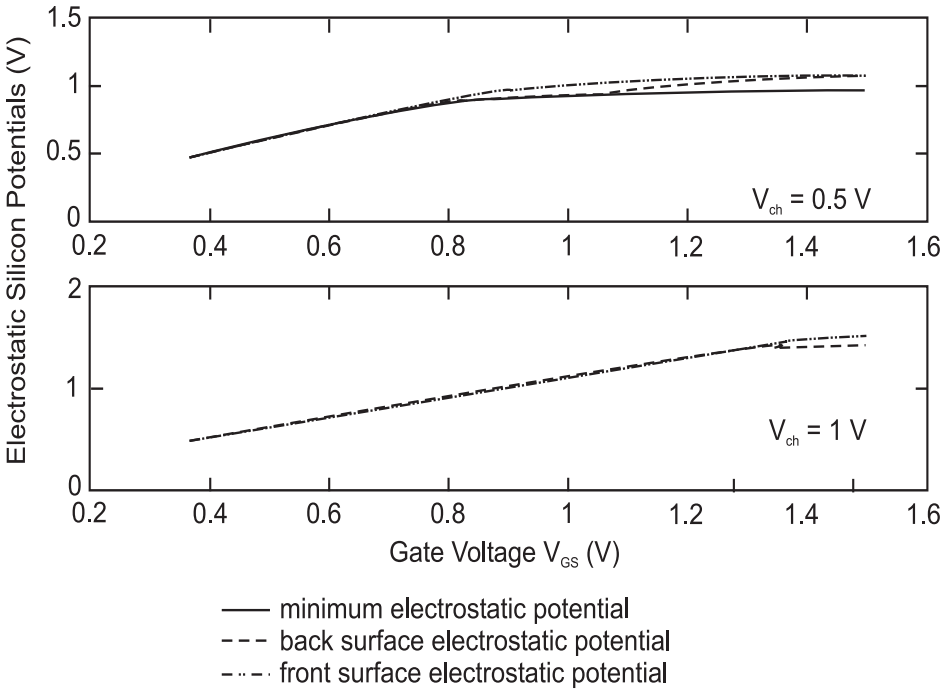


Fig. 4.8: The silicon electrostatic potentials as a function of gate to source voltage V_{GS} when the channel potential has different values, for asymmetric $DG\ SOI\ MOSFET$ transistor.

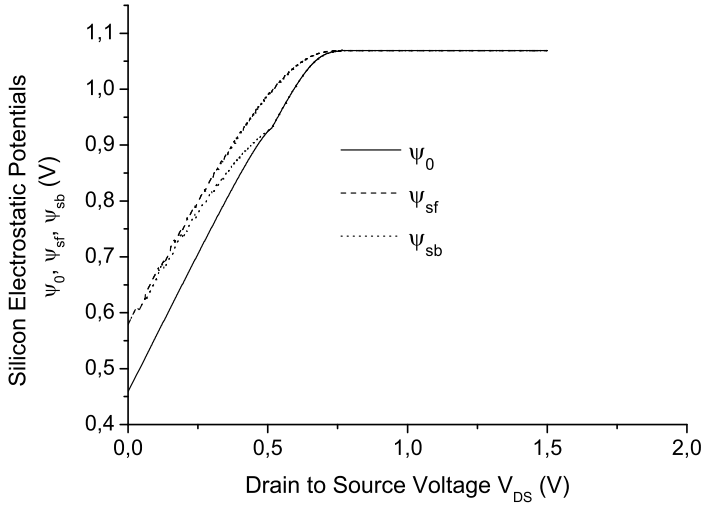


Fig. 4.9: The silicon electrostatic potentials as a function of channel voltage V_{ch} when the gate to source potential is $0.6\ V$.

Figure 4.11 depicts how the position of the minimum for the electrostatic potential is shifted when a voltage is applied on the drain terminal.

Thus, despite of the symmetric property of the device, we observe a slight asymmetry in its electrical characteristics introduced by the distribution of potential in the channel, when a voltage is applied on the drain terminal. As a consequence of such phenomenon,

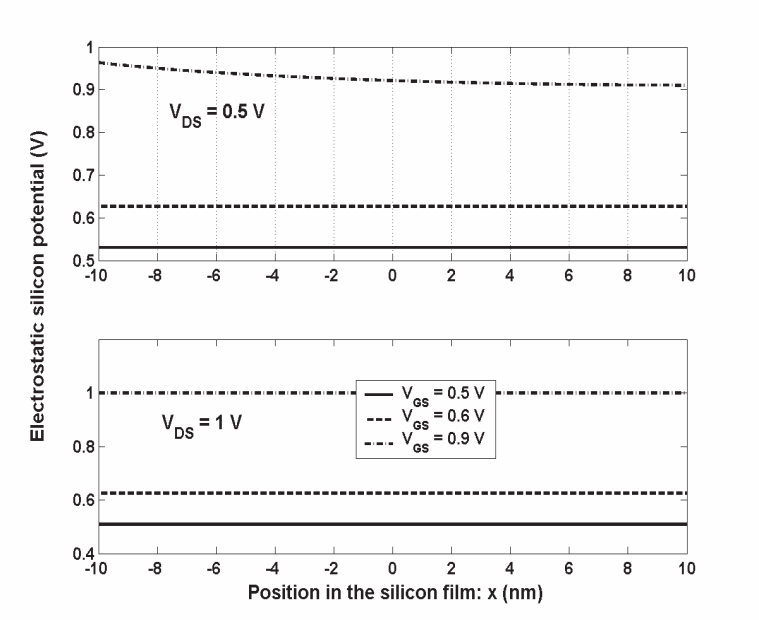


Fig. 4.10: The variation of the electrostatic potential with the position in the silicon film, when the drain voltage is $0.5\ V$ and $1\ V$, respectively. The gate voltage is assumed to be equal to $0.5\ V$, $0.6\ V$ and $0.9\ V$.

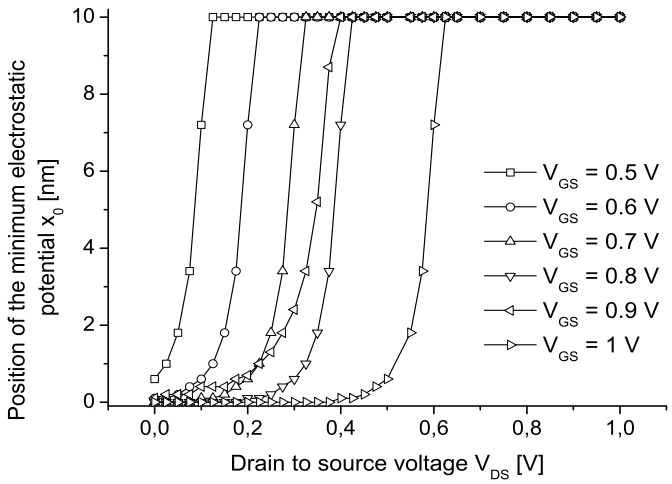


Fig. 4.11: The position of the minimum silicon electrostatic potential as a function of drain voltage when V_{GS} varies in the range of $[0.5; 1]\ V$.

the localization (x_0) of the minimum silicon electrostatic potential will not be in the central part of the silicon layer anymore. One explanation for such a behavior would be the one that takes into account the effects appeared in the device on "y" direction. In the same time, Figure 4.11 proves that the description of the novel device may be further refined with a two-dimensional model in order to include all the effects given by both voltages dropped on gates and drain, too.

4.1.5 Compact Analytical Model of the Drain Current for a Symmetric Un-doped DG SOI MOSFET

In this section, we derive the expression of the drain current for an un-doped symmetric $DG\ SOI\ MOSFET$ which is valid for all regions of operation. The current in the channel is caused by both drift and diffusion phenomena. Starting from the general $MOSFET$ theory proposed by Pao and Sah [94], there are several surface potential and charge based models able to calculate the drain current for a $DG\ SOI$ device [44, 91, 103, 113].

Our $DG\ SOI\ MOSFET$ approach is included in the category of surface potential based model and offers a great simplicity for the calculation of the drain current. Our model is using only the drift current component, which is largely accepted, as the diffusion component, proposed for the first time by Pao and Sah, represents only a few percents from the total drain current [94]. Our electrical current model has its foundation built on the electrostatic calculations from the previous sections. Therefore, it starts from the electrostatic potential results provided by Poisson's equation and continues with the steps below for the electrical current analytical calculation.

Neglecting the diffusion component, and considering a constant electron mobility, of approximately $0.03\ m^2/(Vs)$ in the whole silicon film, the drain current can be computed as shown below.

$$I_D = \mu \cdot \frac{W}{L} \cdot \int_0^{V_{DS}} Q_{inv}(V)dV \tag{4.42}$$

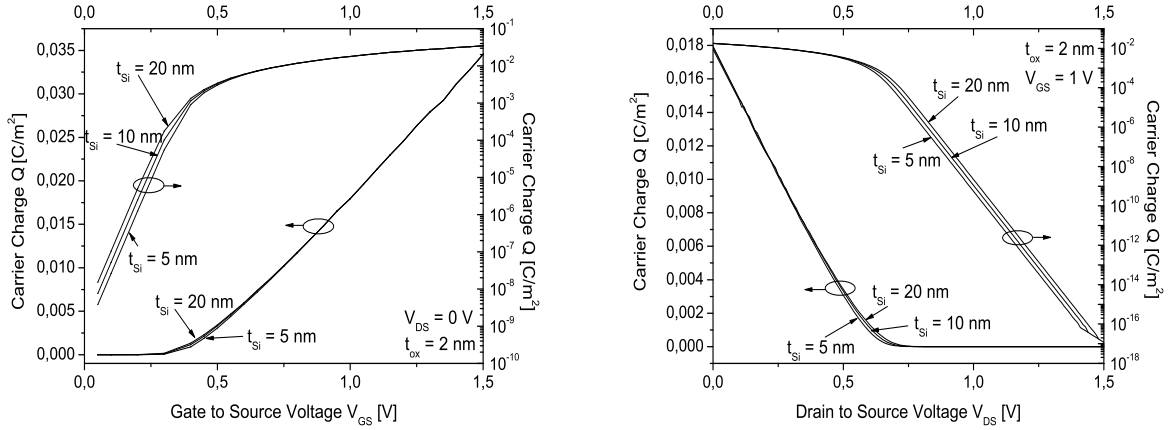
Because the symmetric $DG\ SOI\ MOSFET$ device is un-doped, the charge induced in the channel is practically the total charge in the semiconductor. Therefore, by applying the Gauss's law at the interfaces and taking into account the symmetry characteristic, the inversion charge is as follows:

$$Q_{inv} = 2 \cdot \varepsilon_{si} \frac{d\psi}{dx}|_{x=\frac{t_{si}}{2}} \tag{4.43}$$

By substituting the electric field into equation (4.43), the expression of the inversion charge will become:

$$Q_{inv} = \sqrt{8\varepsilon_{Si} n_i kT} \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot \left| \tan(be^{\frac{q(\psi_0 - V)}{2kT}} \cdot \frac{t_{Si}}{2}) \right| \tag{4.44}$$

Figure 4.12 shows the dependence of the mobile charge carriers (electrons) induced in the channel as a function of the gate to source voltage V_{GS} and the drain to source voltage V_{DS}, respectively, for different silicon thicknesses as calculated in (4.44).



(a) $V_{DS} = 0V$ (b) $V_{GS} = 1V$

Fig. 4.12: The carrier charge as a function of gate voltage and drain voltage, for silicon thicknesses of $5\ nm$, $10\ nm$ and $20\ nm$.

From Figure $4.12a$, the sub-threshold slope can be derived as being the inverse of semi-logarithmic charge-gate voltage characteristics slope and its value is about $62.5\ mV/decade$ which is very close to the ideal case of $60\ mV/decade$. Besides, one can observe that the silicon thickness has an influence on the inversion charge in the sub-threshold region, while in the saturation regime the film thickness has no influence on the inversion charge, which is also validated by the experimental results published in the literature [97].

At this point, two drain current expressions can be derived by using the equations (4.42) and (4.44):

$$I_D = \mu \cdot \frac{W}{L} \cdot \sqrt{8\varepsilon_{Si} n_i kT} \cdot \int_0^{V_{DS}} e^{\frac{q(\psi_0 - V)}{2kT}} \cdot \left| \tan(be^{\frac{q(\psi_0 - V)}{2kT}} \cdot \frac{t_{Si}}{2}) \right| dV \tag{4.45}$$

$$I_D = 2\mu \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot [V_{GS} \cdot V_{DS} - \int_0^{V_{DS}} \psi_s(V) dV] \tag{4.46}$$

The above equations are applicable in all regions of operation of the $DG\ SOI\ MOSFET$ device. Figure 4.13 presents the drain current - drain voltage output characteristics for various values of gate to source voltage. A simple numerical method, starting from Riemann summation was used for the calculation of the above integral in the equation (4.45) and implemented in Matlab - see Appendix B.2.

4.1.6 Calculation of the Transconductance and Output Resistance for a Symmetric Un-doped DG SOI MOSFET

This section is aiming to study the effect of a very small change of the bias voltages (V_{GS} and V_{DS}) on the dc-steady state value of the drain current I_D. It refers to the situation

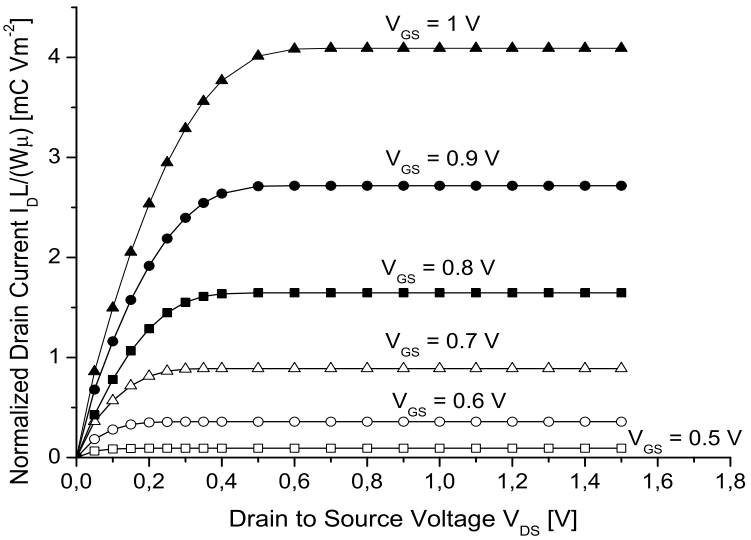


Fig. 4.13: Output characteristics of the $DG\ SOI\ MOSFET$ with V_{GS} varying from $0.5\ V$ to $1\ V$.

when the drain current is constant before and after any change in V_{GS} and V_{DS}, which means the drain current reaches the dc-steady state, after any voltage change. By definition, the transconductance is the variation of the drain current when the gate voltage is changed at a constant drain voltage, while the output conductance of $MOSFET$ transistor is the variation of the drain current as function of drain voltage, when the gate voltage is kept constant. Mathematically, the two parameters are written below, as follows:

- The small-signal gate transconductance g_m that is defined as follows:

$$g_m = (\frac{\partial I_D}{\partial V_{GS}})_{V_{DS}=constant} \tag{4.47}$$

- The small-signal drain-source conductance g_{out}, known as the output conductance which is defined as below:

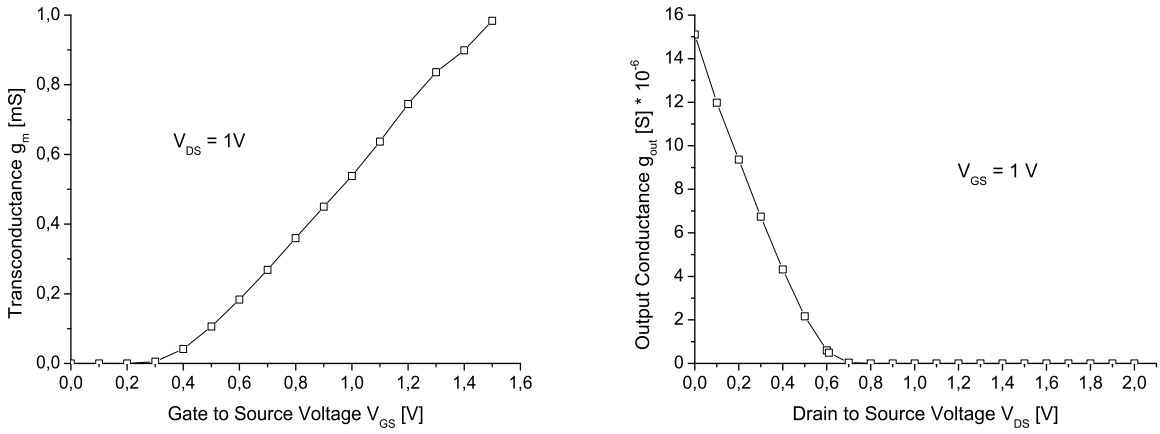
$$g_{out} = (\frac{\partial I_D}{\partial V_{DS}})_{V_{GS}=constant} \tag{4.48}$$

By substituting our analytical expression of the drain current in the above equations, the transconductance and output conductance will have the following analytical forms:

$$g_m = 2\mu \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot [V_{DS} - \frac{\partial}{\partial V_{GS}}(\int_0^{V_{DS}} \psi_s(V)dV)] \tag{4.49}$$

$$g_{out} = 2\mu \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot [V_{GS} - \frac{\partial}{\partial V_{DS}}(\int_0^{V_{DS}} \psi_s(V)dV)] \tag{4.50}$$

Figure 4.14 illustrates the dependence of the above-mentioned parameters g_m and g_{out} as a function of gate to source and drain to source voltages for an un-doped symmetric $DG\ SOI\ MOSFET$ device, calculated with our model. The Matlab tool was used to obtain the graphics - see Appendix B.



(a) Transconductance versus gate to source voltage (b) Output conductance versus drain to source voltage

Fig. 4.14: Transconductance and Output Conductance for an un-doped symmetric $DG\ SOI\ MOSFET$.

The theoretical results obtained from our model, which are showing an increase of the transconductance as a function of gate voltage enhancement are in good agreement with other similar results from literature [6]. However, our modeling shows only the increasing part of the transconductance as function of gate voltage increase, and this might be due to the limited range of the voltage gate variation, in our simulation process. For a constant gate voltage of 1 V, the output conductance (Figure $4.14b$) presents a continuous decrease when the drain voltage increase. In other word, the electric current has a small variation with the drain voltage dependence. When the drain voltage exceeds 0.6 V, the output conductance becomes zero, which means the current plateau is reached in the output characteristics.

4.2 Contributions to the DC Analytical Modeling of an Asymmetric Un-Doped DG SOI MOSFET

It is generally accepted that the dual-gate (DG) $SOI\ MOSFET$ device represents a reliable solution of the scaling down of the $SOI\ ULSI$ circuits to the lowest technological sizes. On the other hand, this DG concept removes the short channel effects and gives a good electrostatic control of the channel charge by the gate voltages. For the same type of the gates materials, doping and dielectric layers, a symmetric $DG\ SOI\ MOSFET$ is ob-

tained, while any technology differences at the gate and/or the dielectric level will imply the asymmetry of the device. In the last years, 1D analytical modeling of both symmetric and asymmetric $DG\ SOI\ MOSFET$ has been used for the description of their DC electrical behavior and the understanding of the device physics.

The analytical approach of the Poisson's equation was possible by using only the inversion charge and ignoring the fixed charge due to the lightly silicon doped film specific to this $DG\ SOI$ technology. One of the important results of the above modeling assumptions was the demonstration of the volume inversion in the ultra-thin silicon film of $SOI\ MOSFET$ devices. However, only a few modeling results were presented for the asymmetric transistors, without the description of the used procedure and a clear presentation of the validity domain. It is the purpose of our work to present detailed results and limitations of the $1D$ analytical modeling of the asymmetric $DG\ SOI\ MOSFET$ and to show its differences compared to the symmetric case.

This section will present the background and the assumptions of the analytical modeling, followed by our detailed mathematical approach which includes the identification of the definition domain for the involved model parameters and the limitations of the calculation of the electrostatic potential as a function of the applied V_{GS} voltage.

4.2.1 Background of the 1D Analytical Modeling for an Asymmetric DG SOI MOSFET

The analytical modeling will be related to the n-channel $DG\ SOI\ MOSFET$, where the silicon thickness of the p-type silicon substrate (t_{Si}) is equal to 20 nm, while the SiO_2 gates dielectric thicknesses (t_{ox}) are equal to 2 nm. The geometry and the energy band diagram of the asymmetric $DG\ SOI\ MOSFET$ are presented in Figure 4.15, where one can see that, due to the p and n type dopings of the two gates at the thermal equilibrium, one silicon surface is already in inversion (see Figure $4.15a$), while the other becomes accumulated because of the differences in the work functions of gates materials and the silicon substrate (see Figure $4.15b$).

For lightly doped silicon film of the asymmetric $DG\ SOI\ MOSFET$, the analytical approach was similar to the symmetrical case, where a minimum of the electrostatic potential, ψ_0, was assumed to be located in the silicon body, at the position x_0, but not exactly located in the center of the silicon layer as in the case of the symmetrical $DG\ SOI\ MOSFET$. Thus, the calculation of the electrostatic potential was done by means of Poisson's equation and the specific boundary conditions as shown below:

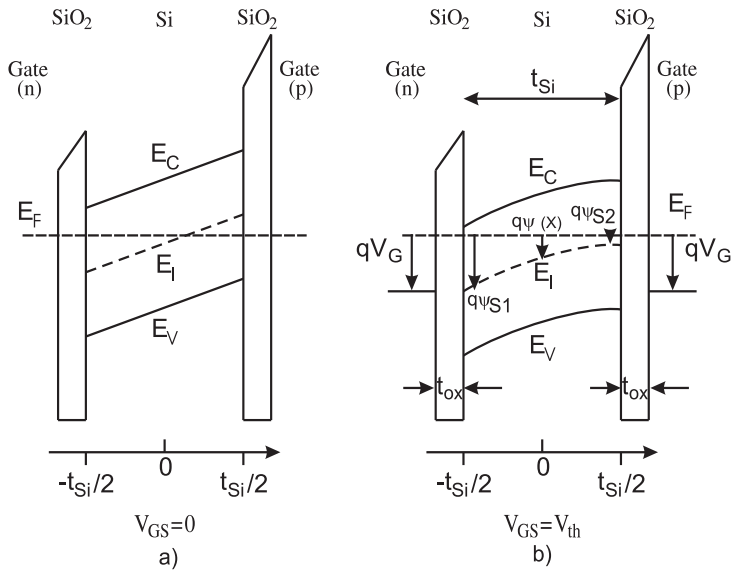


Fig. 4.15: Schematic energy bands diagram of an asymmetric, un-doped $DG\ SOI\ MOSFET$.

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \cdot e^{\frac{q\psi}{kT}} \tag{4.51}$$

$$\frac{d\psi}{dx}|_{x=x_0} = 0 \tag{4.52}$$

$$\varepsilon_{si} \cdot \frac{V_{GS} - \psi_{s1} - \Delta\phi_1}{t_{ox}} = \varepsilon_{ox} \cdot E_{si}|_{x=-\frac{t_{si}}{2}} \tag{4.53}$$

$$\varepsilon_{si} \cdot \frac{V_{GS} - \psi_{s2} - \Delta\phi_2}{t_{ox}} = \varepsilon_{ox} \cdot E_{si}|_{x=\frac{t_{si}}{2}} \tag{4.54}$$

In the above equations, $\Delta\phi_1$ and $\Delta\phi_2$ are the work function differences of the n doped gate and the p doped gate, respectively, while E_{si} represents the electric field at the corresponding Si/SiO_2 interfaces.

The equations (4.53) and (4.54) represent the continuity of the normal component of the electrical displacement at the two interfaces between the silicon and dielectrics. We also assume the presence of the minimum electrostatic potential in the silicon layer at relatively higher V_{GS} voltages.

By the integration of the Poisson's equation with its boundary conditions giving a minimum electrostatic potential (ψ_0) at the position x_0, one obtains the solution for the electrostatic potential as follows:

$$\psi(x) = \psi_0 - \frac{2kT}{q} \cdot ln[\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (x - x_0)] \tag{4.55}$$

where $b = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}$.

At low applied gate voltages, Taur has assumed a constant electrostatic field in silicon,

while at higher applied voltages a minimum electrostatic potential of $0.462V$ was found and this was located near the center of the Si layer [112].

4.2.2 Clarifications and New Results of 1D Analytical modeling

An important limitation of $1D$ analytical modeling of the $DG\ SOI\ MOSFET$ is given by the use of only electron mobile inversion charge in the Poisson's equation. This assumption is valid for very low substrate doping and by neglecting the hole mobile charge. In our case, for a better validation of the model assumption, we have used the p-type substrate doping equal to $N_B = 10^{15}\ cm^{-3}$ which is a much lower value than the one described in the literature. Based on our calculations [131], the electrostatic potentials higher than $0.3\ V$ will make negligible the influence of (mobile) holes and fixed depleted charge in the above Poisson's equation. For our N_B value, the Fermi level is located below the intrinsic Fermi level, E_i, and at $0.24\ eV$ above E_v.

From the equations (4.53) and (4.54) and the dependence given by the relation (4.55), we have derived the explicit system that provides the minimum electrostatic potential (ψ_0) and its location (x_0) in silicon body:

$$\begin{aligned} V_{GS} - \psi_0 - \Delta\phi_1 = \\ = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\frac{t_{si}}{2} - x_0)) - \\ - \frac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\frac{t_{si}}{2} - x_0))\} \end{aligned} \tag{4.56}$$

$$\begin{aligned} V_{GS} - \psi_0 - \Delta\phi_2 = \\ = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\frac{t_{si}}{2} - x_0)) - \\ - \frac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\frac{t_{si}}{2} - x_0))\} \end{aligned} \tag{4.57}$$

where $a = \frac{t_{ox} \cdot \sqrt{2\varepsilon_{si} kT n_i}}{\varepsilon_{ox}}$.

From the equations (4.56) and (4.57), one can see that the solutions ψ_0 and x_0 should be in the definition domains of the natural logarithmic function and the tangent function. Thus, the conditions for the existence of the logarithm function and tangent function are:

$$\psi_0 < \frac{2kT}{q} \cdot ln\{\frac{\pi}{2b(\frac{t_{si}}{2} + x_0)}\} \tag{4.58}$$

$$\psi_0 < \frac{2kT}{q} \cdot ln\{\frac{\pi}{2b(\frac{t_{si}}{2} - x_0)}\} \tag{4.59}$$

From the relations (4.58) and (4.59), one can estimate an upper limit value of the minimum electrostatic potential (ψ_0), by assuming the localization (x_0) of this minimum in

the center of the silicon body. For this case, we calculated an upper limit value of ψ_0, equal to $0.4643\ V$. Thus, according to our model, device geometry and above assumption, we prove that the minimum electrostatic potential should be in the range from $0.37\ V$ to $0.4643\ V$.

In the same time, for finding the definition domain of the tan function, we need to eliminate those values of (x_0, ψ_0) which determine an infinite value of the function. Such (x_0, ψ_0) pairs are obtained by transforming the inequalities (4.58) and (4.59) into equalities and solving the corresponding system. Based on this approach, in Figure 4.16, we present the two plots with the data points which do not belong to the definition domain for x_0 and ψ_0.

Therefore, the final value of the two-dimensional definition domain of our $1D$ analytical modeling and chosen geometry is considered as follows: $(x_0; \psi_0) \in (((-10\ nm, 10\ nm) \times (0.37\ V, 0.4643\ V)) - (x_0; \psi_0)_{plot})$ where $(x_0; \psi_0)_{plot}$ represents the data points located in the two plots in Figure 4.16.

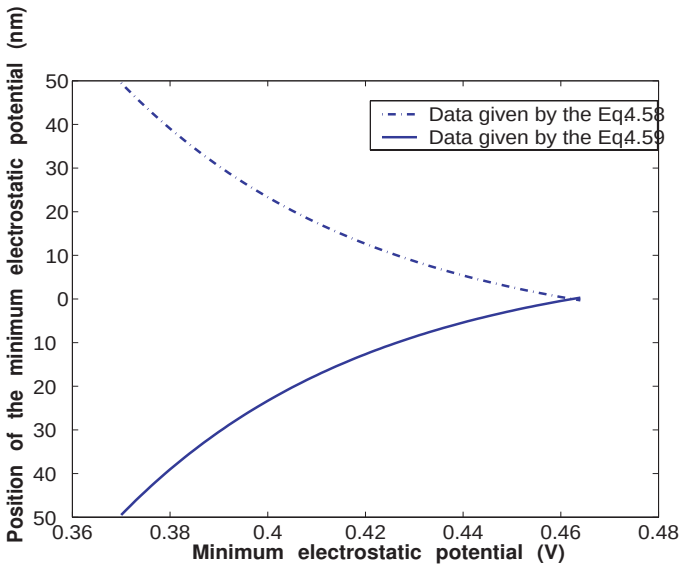


Fig. 4.16: Domain of definition for both minimum electrostatic potential and its localization.

Now, after we have found the definition domain, we have solved the system of equations (4.56) and (4.57) in the Matlab code, by means of an iterative method which provides the x_0, ψ_0 solutions. Firstly, we introduce the following notations:

$$f_1 = V_{GS} - \psi_0 - \Delta\phi_1 \tag{4.60}$$

$$g_1 = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\frac{t_{si}}{2} - x_0)) - \\ - \frac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\frac{t_{si}}{2} - x_0))\} \tag{4.61}$$

$$f_2 = V_{GS} - \psi_0 - \Delta\phi_2 \tag{4.62}$$

$$g_2 = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\frac{t_{si}}{2} - x_0)) - \\ - \frac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\frac{t_{si}}{2} - x_0))\} \tag{4.63}$$

Based on the above relations, the system formed on the equations (4.56) and (4.57) becomes:

$$h_1 = f_1 - g_1 = 0 \tag{4.64}$$

$$h_2 = f_2 - g_2 = 0 \tag{4.65}$$

The above system of equations is solved by considering the work function differences $\Delta\phi_1 = -0.56\ eV$ (between the $n-$type gate electrode and the intrinsic silicon) and $\Delta\phi_2 = 0.56\ eV$ (between the p- type gate electrode and the intrinsic silicon). As the system has no analytical solutions, we have solved it by using a numerical approach . For each applied V_{GS} voltage in the range of $(0.5, 0.95)\ V$ and x_0 values in the domain $(-10, 10)\ nm$, we calculate the values of h_1 and h_2 for ψ_0 ranging from $0.37\ V$ to $0.4643\ V$. The solution of the system given by relations (4.64) and (4.65) is found for those $(x_0; \psi_0)$ values that satisfy the conditions written below:

$$abs(h_1) < 10^{-6} \tag{4.66}$$

$$abs(h_2) < 10^{-6} \tag{4.67}$$

According to the previous system, for V_{GS} variation in the range from $0.5\ V$ to $0.95\ V$, we obtain a minimum electrostatic potential dependence as shown in Figure 4.17. The solutions x_0 of the positions of the minimum electrostatic potentials were found closed to the center of silicon film, but the difficulty associated with their extraction will be commented later.

From Figure 4.17, one can see for the first time a pinning effect of the minimum electrostatic potential as a function of the applied V_{GS} voltage for asymmetric $DG\ SOI\ MOSFET$ devices. If we consider the minimum electrostatic potential dependence in Figure 4.17 and look at the qualitative energy band diagrams in Figure 4.15, it is easy to understand that, at V_{GS} higher than $0.5\ V$, the Fermi level in the silicon layer is closed to

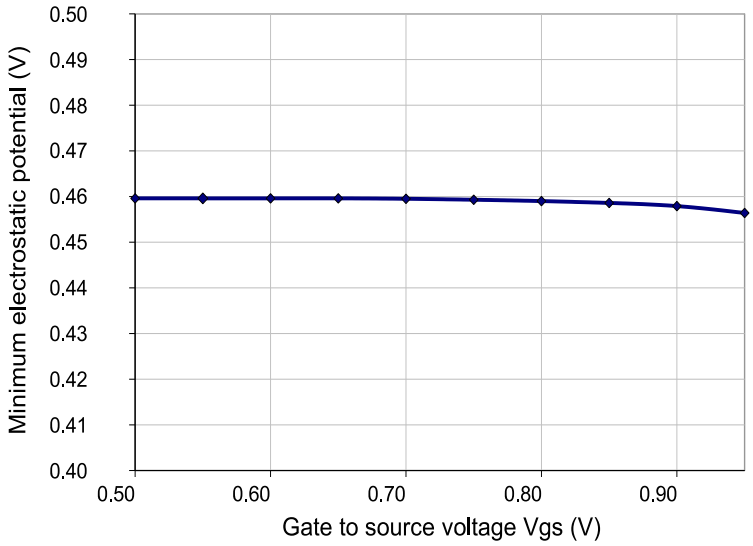


Fig. 4.17: The minimum electrostatic potential as a function of the applied gate-to-source voltage.

bottom of the conduction band for the whole silicon body which demonstrates the presence of the volume inversion even in the case of asymmetric $DG\ SOI\ MOSFET$. This volume inversion can also be demonstrated by representing the electrostatic potential profile as a function of the position in the silicon film of the $DG\ SOI\ MOSFET$. Such result is presented in Figure 4.18 by means of the equation (4.55), where we show the dependence of the electrostatic potential as a function of the position in silicon body for an applied V_{GS} voltage equal to $0.95\ V$. That plot was obtained for a $\psi_0 = 0.4564\ V$ and $x_0 = 0.878\ nm$.

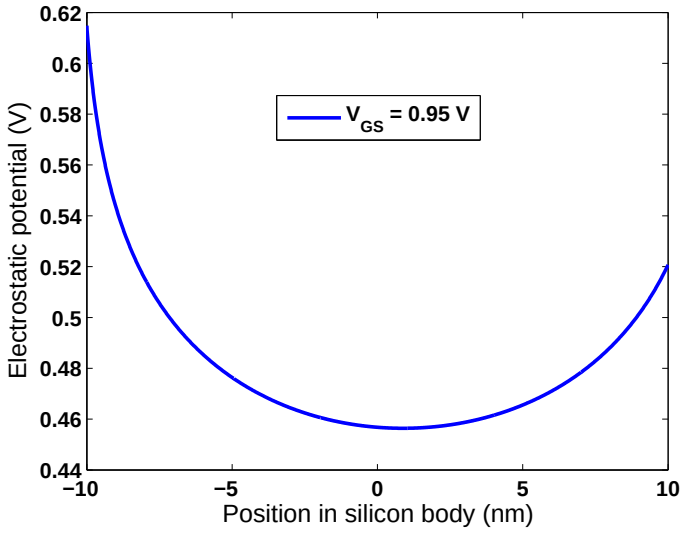


Fig. 4.18: Electrostatic potential profile in the silicon body for $V_{GS} = 0.95\ V$.

From Figure 4.18, one can notice that the electrostatic potential is much higher at the interface with the $n-$doped poly-silicon gate, which can be understood from the initial

bands bending of the silicon layer due to the work function differences at the thermal equilibrium. This figure, also, shows a wide sink shape of the electrostatic potential in the middle of the silicon body, which makes its minimum location to be a difficult numerical task. In his paper, Taur has presented a calculation of the electrostatic potential only for an applied voltage $V_{GS} = 1.4\ V$ and he obtained the minimum electrostatic potential of $0.462\ V$ located at $0.425\ nm$, far from the center of silicon layer. Unfortunately, the paper was not focused on the description of more details about the method used to obtain the results. If we make an analysis of our and Taur's results, we can deduce that the minimum electrostatic potential is further maintained up to a rather constant value of $V_{GS} = 1.4\ V$. Actually, due to a flat profile of the electrostatic potential in the central region of silicon body as shown in Figure 4.18, one can understand the difficulty of extracting the position of the minimum electrostatic potential. Thus, the coordinates of the minimum electrostatic potential are very critical for the calculation of the electrostatic potential distribution in the entire silicon body.

In order to prove the sensitivity of the electrostatic potential distribution to the location of its minimum, in Figure 4.19, it is presented the effect of a slight variation in x_0 position on the shape of the entire distribution. In this example, we have considered three arbitrary values in the position of minimum electrostatic potential in the range from -0.5 nm to $+0.5$ nm around the center of the silicon layer, but we kept constant the value of the minimum electrostatic potential equal to $0.46\ V$.

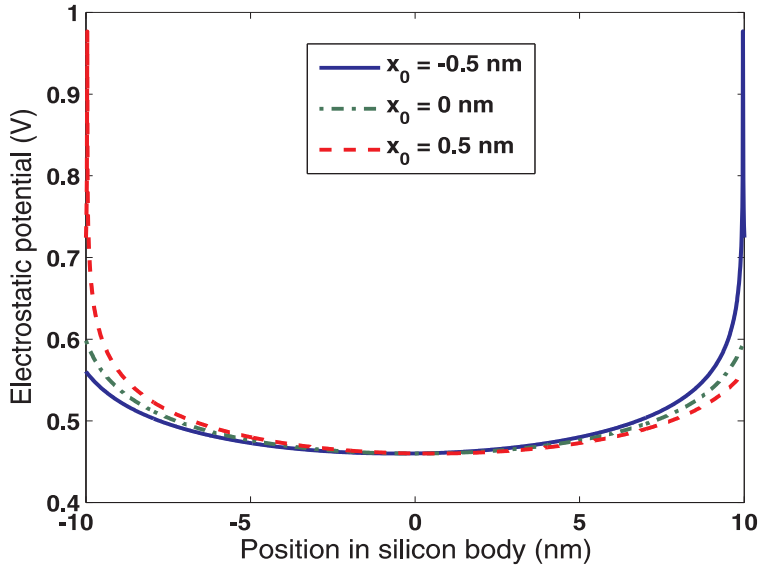


Fig. 4.19: Electrostatic potential profile in the silicon body for three arbitrary values of the position of minimum electrostatic potential in the range from -0.5 nm to $+0.5$ nm around the center of silicon layer, but with constant ψ_0.

From this figure, one can see high differences for the electrostatic potential at the two interfaces in the three cases, where some of the interface potential values are not even having a physical meanings. In the same time, in the central silicon region, the effect of different locations on the electrostatic distributions is very weak.

Overall, despite the sensitivity of the results to the accuracy of the numerical calculations, our approach has shown the capability of the $1D$ modeling to provide a good understanding of the physics of the asymmetric $DG\ SOI\ MOSFET$ devices, where the volume inversion is found for a typical defined geometry and biasing.

4.3 Contributions to the AC Analysis for a Symmetric Un-doped DG SOI MOSFET

In order to offer a comprehensive picture of the $DG\ SOI\ MOSFET$ modeling, this section deals with the description of our proposed ac analytical model, which is benefiting from the quasi-static approximation up to an upper frequency limit of validity. Beyond that upper frequency limit, non-quasi static models should be developed, but this is not the goal of our thesis. Initially a large signal modeling is developed for the $DG\ SOI\ MOSFET$ transistor, adapted from the bulk $MOSFET$ theory ([115]) and then a small signal modeling is shown, able to work for low and medium frequency range. Then, an original equivalent small-signal circuit will be provided along with the calculation of the device capacitances, making possible the theoretical study of the frequency response of the asymmetric $DG\ SOI\ MOSFET$ for understanding the frequency behavior of these new emerging devices. Finally, a preliminary model for a small signal equivalent circuit of a symmetric un-doped $DG\ SOI\ MOSFET$ is derived considering the analytical modeling results of the above novel $MOSFET$ transistor that is going to continue the scaling "race" beyond the bulk $MOSFET$ technology capabilities.

4.3.1 The Large Signal Dynamic Modeling of a DG SOI MOSFET

Within this section, we shall start with our large signal dynamic modeling of the $DG\ SOI\ MOSFET$, adapted after the bulk $MOSFET$ theory. Here, at large ac signals, there will be no restrictions about the magnitude of the dynamic signal superposed on the dc signal. The final goal of this section is to build an ac complete model used to provide the equivalent small signal electric circuit for a symmetric un-doped $DG\ SOI\ nMOSFET$ device. This model should be able to describe the medium and high frequency operation of the symmetric un-doped $DG\ SOI\ nMOSFET$ device, as long as the approximation of quasi-static operation is valid, as presented above. As known from the basic electron device theory, at small ac signals, the magnitude of the dynamic excitation and response is very small compared with dc bias, and the magnitude of the small signal (dynamic) response is linear with respect to the small dynamic excitation. Here, the term complete model refers to two aspects. Firstly, to obtain a complete model, the dc and low frequency components are also included in the final equivalent circuit to describe the transport current through transistor. As this is well known from the bulk $MOSFET$ theory, here we shall present the results without demonstration. Secondly, the dynamic effect of any ter-

minal voltage variation to any terminal charge change and associated charging currents is also incorporated in the $DG\ SOI\ MOSFET$ model so that the resulting charging currents (specific only to dynamic regime of $MOSFET$ transistors) will have corresponding physical circuit elements for an enhanced validity of the ac model when compared with experimental results. According to the quasi static approximation, even if the terminal voltages are varying in time, the charges per unit area at any time are assumed identical to those obtained if dc voltages are used instead. Consequently, the dc models for electric charges and transport current are transferred to the ac regime modeling. This is the big advantage of the quasi static approximation for modeling. However, as mentioned above, one can not transfer any charging currents models from dc regime from the simple reason that these charging currents do not exist, in the dc operation. The entire modeling from here is considering only the intrinsic transistor (i.e, only the region of gate, dielectric and inversion region from silicon are considered) ignoring the source and drain regions and associated parasitic contributions, like series resistances and capacitances specific to them.

We consider an intrinsic $DG\ SOI\ MOSFET$ transistor with the total time varying voltages that consist of a dc bias part and ac (dynamic) large signal part as follows:

$$v_{G1}(t) = v_{g1}(t) + V_{G1} \tag{4.68}$$
$$v_{G2}(t) = v_{g2}(t) + V_{G2} \tag{4.69}$$
$$v_S(t) = v_s(t) + V_S \tag{4.70}$$
$$v_D(t) = v_d(t) + V_D \tag{4.71}$$

In the above formulas, we do not put any restrictions on the magnitude of the ac signal, as announced. The rules of capital and lowercase letters and subscripts are those well known to the electronic circuit designers for total, ac and bias signals to be used for dynamic modeling of circuits. In accordance to all the mentioned assumptions, Figure 4.20 presents an intrinsic asymmetric $DG\ SOI\ nMOSFET$ transistor with four terminal voltages consisting of a dc bias and a time varying signal. The schematics from Figure 4.20 will be used for either large and small signal modeling. For simplicity, in the above figure we have introduced an original symbol for the asymmetric $DG\ SOI\ nMOSFET$ transistor, where we have shown the two separate biased gates and gate oxides, as well as source, drain and silicon film of SOI. For the $DG\ SOI\ nMOSFET$ transistor symbol, we did not consider the BOX oxide and substrate effect, and its biasing. The floating silicon film (p type in Figure 4.20), where the volume inversion can take place, is well represented.

In addition, let us consider the currents I_D, I_{G1}, I_S and I_{G2} defined as entering the device. From the previous sections, we remember that the current flow is given by the transport of electrons in the silicon (volume) inversion layer. Following the same steps used in the conventional bulk $MOSFET$ device, the transport current is defined as flow-

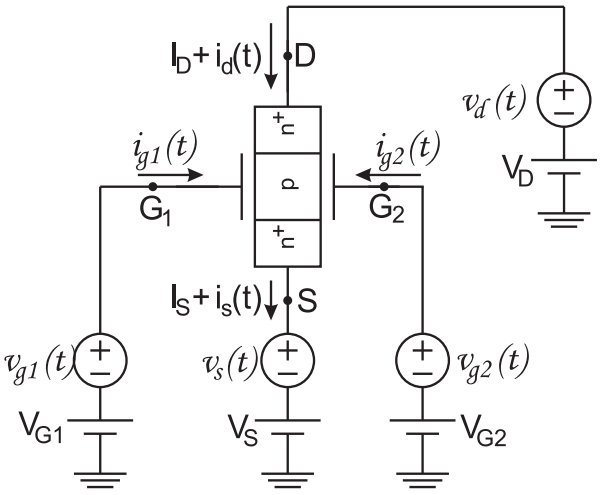


Fig. 4.20: An asymmetric $DG\ SOI\ nMOSFET$ with terminal voltages consisting of a dc bias plus a time-varying signal. The same schematic can be used for both large and small signal approaches.

ing from the drain to the source, through the channel (which is the entire silicon body) and denoted by I_T as follows:

$$I_D = I_T \tag{4.72}$$

$$I_{G1} = I_{G2} = 0 \tag{4.73}$$

$$I_S = -I_T \tag{4.74}$$

Within this section, all the current entering the device is considered with positive sign, as a convention.

Assuming that there are no gates leakages and, thus, no gates transport currents, the gates currents are displacement currents and associated with charge changing on the two gates. In addition, the sum of the drain and source currents represents the total electrical current that enters the channel and changes the inversion layer charge as follows:

$$i_{Gj}(t) = \frac{dq_{Gj}}{dt}; j = 1; 2 \tag{4.75}$$

$$i_D(t) + i_S(t) = \frac{dq_{INV}(t)}{dt} \tag{4.76}$$

It is important to noticing that in the dc regime, $i_D(t) = -i_S(t) = i_T(t)$. Introducing it in the equation (4.76), the following relation is obtained:

$$\frac{dq_{INV}(t)}{dt} = 0 \tag{4.77}$$

and thus, the inversion charge is constant along the channel (which can be the entire silicon volume for $DG\ SOI\ MOSFET$) during the dc device operation: $q_{INV} = constant$.

If the voltages are time varying as it is in the ac regime, the charge becomes variable ($q_{inv} \neq constant$). Then, the first derivative in time of the total inversion charge is not zero anymore and then, the sum of the drain current from the above definitions and equation (4.76) is not zero providing a small difference between the source current ($-i_S(t)$) and drain current ($-i_D(t)$) [115], as shown below.

$$\frac{dq_{inv}(t)}{dt} \neq 0 \Rightarrow i_d(t) \neq -i_D(t) \tag{4.78}$$

Therefore, it is assumed that in the general case of time-varying voltages, both drain and source currents contain the transport current from dc regime, to which one adds an ac component. In the literature, there was much confusion about dynamic modeling of these ac drain and source currents. Now, as shown below, the things are clear and the ac model is well understood after making the analogy of the dynamic MOS transistor behavior with a dynamic fluid system consisting of two liquid tanks (source tank and drain tank) communicating between them by a piston-controlled reservoir with variable volume (corresponding to the inversion channel volume controlled by gate voltage). For liquids, flowing in the tank system in the dc conditions, with the piston in a fix position, the same amount of liquid per minute enters the source tank in the reservoir and then flows away in the drain tank. This is exactly what happens to the MOS transistor at dc regime, when drain and source currents are equal. When the valve piston is moved down very fast and the reservoir is increasing its volume, a part of the liquid coming from the source tank will remain "stored" in the increased-volume reservoir, and during a transient regime, the liquid flow entering the source tank will be higher than the liquid flow arrived at drain tank (due to the additionally remained or "stored" liquid in the reservoir with increased volume), even if it is a serial system. This is exactly what happens in the ac regime of MOS transistor, when the gate voltage is rapidly increased, and for a short transient time, the drain current is decreasing with respect to the source current, due to a kind of an additional 'stored' charge in the inversion layer, associated to gate voltage enhancement. With this dynamic fluid analogy in mind, now, it may be easier to understand that in dynamic regime, the absolute value of source current cannot be equal to the total drain current and that some charging currents ($i_{SA}(t)$ at source end and $i_{DA}(t)$ at drain end) will appear for expressing this difference with respect to dc regime ($i_T(t) = I_D$). These charging current components cannot be found in the dc regime. Those total dynamic drain and source currents containing the dc transport current (expressed by $i_T(t)$) and the two charging currents $i_{SA}(t)$ and $i_{DA}(t)$ for source and drain, respectively, as shown above, are written as mathematical expressions as follows.

$$i_D(t) = i_T(t) + i_{DA}(t) \tag{4.79}$$

$$i_S(t) = -i_T(t) + i_{DA}(t) \tag{4.80}$$

From these equations and (4.76), we get:

$$i_{DA}(t) + i_{SA}(t) = \frac{dq_{INV}(t)}{dt} \tag{4.81}$$

Therefore, one can conclude that the total transport current $i_T(t)$ is responsible for the dc transport process, while the quantities $i_{SA}(t)$ and $i_{DA}(t)$ give the changing in the inversion charge $q_{INV}(t)$, to comply with the total value of the gate voltage, specific to the dynamic regime. It is obvious that for an increased value of gate voltage, in the dynamic regime, an external observer can not distinguish any difference between the electrons entering the source and charging the channel (like a reservoir with increased volume, due to piston enlarging the volume of reservoir) and those leaving the drain, i.e., cannot make a distinction between electrons contributing to charging current and transport current. By introducing two dynamic fictitious charges from the source and the drain, to comply with different values and mathematical expressions of the total source and drain currents, one gets the following expression for the (large signal) total drain and source currents:

$$i_{DA}(t) = \frac{dq_D}{dt} \tag{4.82}$$

$$i_{SA}(t) = \frac{dq_S}{dt} \tag{4.83}$$

For example, if $i_{DA}(t)$ is negative, it means that the total drain current is smaller than the transport value, due to the less charge flowing at the drain with respect to the dc regime, when a change appears in the gate voltage, becoming higher for an $nMOS$ transistor ("piston effect on the reservoir which will increase its volume"). From these expressions, one can also see that, for the modeling purposes, we need to know only the first derivative of the functions describing the fictitious charges from source and drain with respect to time, and not the functions itself. The two functions expressing the sum of the two fictitious charges have a constraint: the sum of the two fictitious charges should be equal to the total inversion charge, as shown below.

By including the relations (4.82) and (4.83) in (4.81), one can obtain:

$$q_D(t) + q_S(t) = q_{INV}(t) \tag{4.84}$$

If the terminal voltages are varying very slow, the quasi-static operation is maintained and, thus, the evaluation of the two quantities denoted by $q_S(t)$ and $q_D(t)$ in the dynamic regime can be given as a function of the electrical potentials applied on the $DG\ SOI\ MOSFET$, as modeled in the dc regime. The dc voltages are now replaced by the dc value corresponding to the total voltage, as described in the equations (4.68) - (4.71). It is worth to know, that, indeed, in the dc regime the sum of the two charge amounts from above is equal to the total inversion charge, and therefore one can use the analytical

expression already obtained in the dc modeling for the calculation of the q_D and q_S from below:

$$q_D(t) = f_D(v_D(t), v_{G1}(t), v_{G2}(t), v_S(t)) \tag{4.85}$$
$$q_S(t) = f_S(v_D(t), v_{G1}(t), v_{G2}(t), v_S(t)) \tag{4.86}$$

where f_S and f_D represent functions that show the dependence of the q_S and q_D as a function of the voltages applied on all four terminals of a $DG\ SOI\ nMOSFET$ as it is depicted in the Figure 4.20. Considering the device as a single node where all the electrical currents are entering as presented in Figure 4.20, from Kirchhoff's current law we get:

$$i_D(t) + i_{G1}(t) + i_{G2}(t) + i_S(t) = 0 \tag{4.87}$$

It is important to note that the Kirchhoff's current law holds also for the ac regime where we have introduced the charging currents for source and drain, as shown above and thus, the equation (4.87) becomes:

$$i_{DA}(t) + i_{G1}(t) + i_{G2}(t) + i_{SA}(t) = 0 \tag{4.88}$$

By using the above equation, the following definitions for the current and capacitances [115] and considering all the terminals of the device as voltage excitation points, we get the following equations:

$$i(t) = \frac{dq}{dt} \tag{4.89}$$
$$C_{KK} = \frac{\partial q_K}{\partial v_K}|_{Q-point} \tag{4.90}$$
$$C_{KL} = -\frac{\partial q_K}{\partial v_L}|_{Q-point}; L \neq K \tag{4.91}$$

and by having the general condition:

$$C_{KL} \neq C_{LK} \tag{4.92}$$

the expressions for the small-signal charging currents (and thus explaining the small letters for the electric currents from below) are derived as below:

$$i_{DA}(t) = C_{DD} \cdot \frac{dv_D}{dt} - C_{DS} \cdot \frac{dv_S}{dt} - C_{DG1} \cdot \frac{dv_{G1}}{dt} - C_{DG2} \cdot \frac{dv_{G2}}{dt} \tag{4.93}$$

$$i_{SA}(t) = -C_{SD} \cdot \frac{dv_D}{dt} + C_{SS} \cdot \frac{dv_S}{dt} - C_{SG1} \cdot \frac{dv_{G1}}{dt} - C_{SG2} \cdot \frac{dv_{G2}}{dt} \tag{4.94}$$

$$i_{G1}(t) = -C_{G1D} \cdot \frac{dv_D}{dt} - C_{G1S} \cdot \frac{dv_S}{dt} + C_{G1G1} \cdot \frac{dv_{G1}}{dt} - C_{G1G2} \cdot \frac{dv_{G2}}{dt} \tag{4.95}$$

$$i_{G2}(t) = -C_{G2D} \cdot \frac{dv_D}{dt} - C_{G2S} \cdot \frac{dv_S}{dt} - C_{G2G1} \cdot \frac{dv_{G1}}{dt} + C_{DG2} \cdot \frac{dv_{G2}}{dt} \tag{4.96}$$

It does worth to noticing that the capacitance parameters used in the above equations are not associated to the intrinsic physical capacitors at this moment, but simply quantities defined as in (4.90) and (4.91). For the theoretical calculation of the above charging currents and capacitances, analytical functions for the charges should be known, and this is the advantage of the quasi-static operation, that will allow us to "import" them from the dc models, under circumstances described previously. It is also worth to mention that the above equations can define the right environment for the realization of the equivalent small-signal circuit of the asymmetric and symmetric $DG\ SOI\ nMOSFET$. In the next section, we shall describe what the electrical requirements are, for the transformation of the above large signal equations into small signal equations.

4.3.2 The Small Signal Dynamic Modeling of a DG SOI MOSFET

According to the charging currents model described above for the dynamic regime of $DG\ SOI\ MOSFETS$ and the general theory of small signals applied in the electronic circuits, one can admit that if the dc terminal voltages of $DG\ SOI\ MOSFETS$ transistor are all increased with small ac amounts, as in the equations (4.68) - (4.71), then the total currents can be expressed as follows:

$$i_T(t) = I_T + i_t(t) \tag{4.97}$$

$$i_D(t) = i_T(t) + i_{DA}(t) = I_T + i_t(t) + i_{DA}(t) = I_T(t) + i_t(t) + i_{da}(t) = I_D + i_d(t); \tag{4.98}$$

as explained before, we have no dc component for $i_{DA}(t)$, being a charging current specific only to the dynamic regime:

1. $i_S(t) = -i_T(t) + i_{SA}(t) = -(I_T + i_t(t)) + i_{SA}(t) = -I_T - i_t(t) + i_{sa}(t) = I_S + i_s(t)$ (similarly, we have no dc component for $i_{SA}(t)$);

2. $i_{G1}(t) = i_{g1}(t)$ (no dc gate current component as long as the gate oxide leakage is almost zero);

3. $i_{G2}(t) = i_{g2}(t)$ (no dc gate current component as long as the gate oxide leakage is almost zero).

In this environment, $i_d(t)$, $i_s(t)$, $i_{g1}(t)$, $i_{g2}(t)$ are all small signal current components. From the above equations, we find the following relations for small signal current of the drain and the source:

$$i_d(t) = i_t(t) + i_{da}(t) = i_t(t) + \frac{dq_d}{dt} \tag{4.99}$$

$$i_s(t) = -i_t(t) + i_{sa}(t) \tag{4.100}$$

From the equation of small signal drain current, one can easily understand that for a complete equivalent circuit, the circuit elements associated to the small-signal transport current component ($i_t(t)$) specific to low frequency operation should be included in the final circuit, as will be presented further. According to the definition of the small signal regime, we have the following conditions that should be fulfilled:

$$i_d(t) << I_D \tag{4.101}$$

$$i_s(t) << I_S \tag{4.102}$$

The mentioned two conditions should be accomplished in the quasi-static regime where the drain and source charge variations with time are slow enough, so that those charging currents superpose to the small signal transport currents to remain much smaller than the dc bias current for source and drain. Such a comment could help us to determine the upper limit of the operation frequency where the quasi-static regime is still applicable. In addition, specific for a small signal regime, it should remain the fact that, if we apply small signal excitation voltages superposed to dc bias, the two current components we obtain should be linear functions of the small signal excitation voltage.

Based on the above observations, the Kirchoff's law of current becomes :

$$i_{DA}(t) + i_{G1}(t) + i_{G2}(t) + i_{SA}(t) = i_{da}(t) + i_{g1}(t) + i_{g2}(t) + i_{sa}(t) \tag{4.103}$$

Considering the presented approach of the small signal dynamic regime, the mentioned charging current expressions become:

$$i_{da}(t) = C_{dd} \cdot \frac{dv_d}{dt} - C_{ds} \cdot \frac{dv_s}{dt} - C_{dg1} \cdot \frac{dv_{g1}}{dt} - C_{dg2} \cdot \frac{dv_{g2}}{dt} \tag{4.104}$$

$$i_{sa}(t) = -C_{sd} \cdot \frac{dv_d}{dt} + C_{ss} \cdot \frac{dv_s}{dt} - C_{sg1} \cdot \frac{dv_{g1}}{dt} - C_{sg2} \cdot \frac{dv_{g2}}{dt} \tag{4.105}$$

$$i_{g1}(t) = -C_{g1d} \cdot \frac{dv_d}{dt} - C_{g1s} \cdot \frac{dv_s}{dt} + C_{g1g1} \cdot \frac{dv_{g1}}{dt} - C_{g1g2} \cdot \frac{dv_{g2}}{dt} \tag{4.106}$$

$$i_{g2}(t) = -C_{g2d} \cdot \frac{dv_d}{dt} - C_{g2s} \cdot \frac{dv_s}{dt} - C_{g2g1} \cdot \frac{dv_{g1}}{dt} + C_{dg2} \cdot \frac{dv_{g2}}{dt} \tag{4.107}$$

Very useful relations between the capacitances can be obtained if we consider some general observations related to the nature of the small signal generators and the way we apply them to the circuit from Figure 4.20, as follows:

1. Assume that $v_d(t) = v_{g1}(t) = v_{g2}(t) = v_s(t) = v(t)$ in Figure 4.20. The obtained configuration is shown in Figure 4.21.

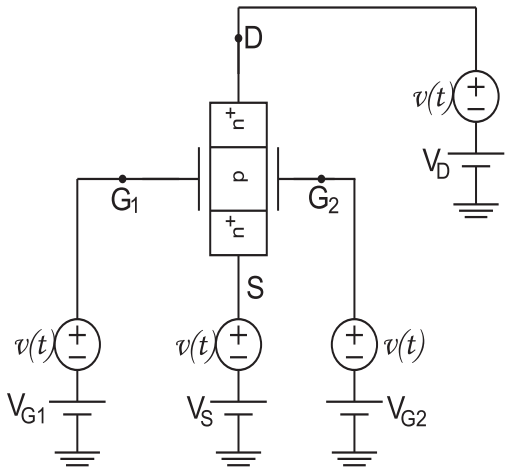


Fig. 4.21: An asymmetric $DG\ SOI\ nMOSFET$ with all four terminal-to-ground small signal voltages equal.

From (4.104), we get:

$$i_{da}(t) = (C_{dd} - C_{ds} - C_{dg1} - C_{dg2}) \cdot \frac{dv}{dt} \tag{4.108}$$

- There is no small-signal voltage across any two of the terminals and thus, all terminal small signal currents must be zero even for nonzero $\frac{dv}{dt}$. This conclusion implies that: $C_{dd} - C_{ds} - C_{dg1} - C_{dg2} = 0$ and then:

$$C_{dd} = C_{ds} + C_{dg1} + C_{dg2} \tag{4.109}$$

- If we consider: $\frac{dv_s}{dt} = \frac{dv_{g1}}{dt} = \frac{dv_{g2}}{dt} = 0$, nonzero $\frac{dv_d}{dt}$ and equations (4.103), (4.104) - (4.107) - from which the sum of small signal charging currents must equal zero - we will have:

$$C_{dd} = C_{sd} + C_{g1d} + C_{g2d} \tag{4.110}$$

Similarly, the same steps are applied further and, thus, the following expressions for the unknown capacitance parameters are obtained:

$$C_{ss} = C_{sd} + C_{sg1} + C_{sg2} = C_{ds} + C_{g1s} + C_{g2s} \tag{4.111}$$

$$C_{g1g1} = C_{g1d} + C_{g1s} + C_{g1g2} = C_{dg1} + C_{sg1} + C_{g2g1} \tag{4.112}$$

$$C_{g2g2} = C_{g2d} + C_{g2s} + C_{g2g1} = C_{dg2} + C_{sg2} + C_{g1g2} \tag{4.113}$$

2. Another important observation says that if three of the small-signal charging currents are known, the forth can be calculated from:

$$i_{da}(t) + i_{g1}(t) + i_{g2}(t) + i_{sa}(t) = 0 \tag{4.114}$$

This final observation coming from Kirchhoff's law of current will simplify the approach for building the small signal equivalent circuit, telling us that only i_{da}, i_{g1} and i_{g2} can be used without loosing any information, as long as the effect of $i_{sa}(t)$ on the circuit elements has been already included in the above capacitance relations. Also, if we assume that terminal voltages of drain and gates are referenced to source, we obtain the small signal biasing from the Figure 4.22 from which we can write:

$$v_D = v_{DS} + v_S = V_{DS} + v_{ds} + V_S + v_s \tag{4.115}$$
$$v_{G1} = v_{G1S} + v_S = V_{G1S} + v_{g1s} + V_S + v_s \tag{4.116}$$
$$v_{G2} = v_{G2S} + v_S = V_{G2S} + v_{g2s} + V_S + v_s \tag{4.117}$$

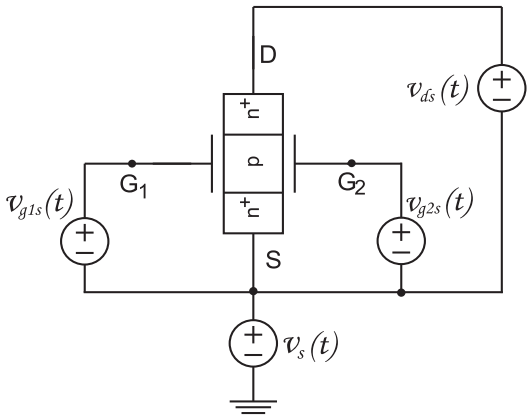


Fig. 4.22: A $DG\ SOI\ nMOSFET$ with terminal voltages referenced to source.

With this condition and the equations (4.104) - (4.107), the following current expressions are derived:

$$i_{da} = C_{dd} \cdot \frac{dv_{ds}}{dt} - C_{dg1} \cdot \frac{dv_{g1s}}{dt} - C_{dg2} \cdot \frac{dv_{g2s}}{dt} \tag{4.118}$$
$$i_{g1} = -C_{g1d} \cdot \frac{dv_{ds}}{dt} + C_{g1g1} \cdot \frac{dv_{g1s}}{dt} - C_{g1g2} \cdot \frac{dv_{g2s}}{dt} \tag{4.119}$$
$$i_{g2} = -C_{g2d} \cdot \frac{dv_{ds}}{dt} - C_{g2g1} \cdot \frac{dv_{g1s}}{dt} + C_{dg2} \cdot \frac{dv_{g2s}}{dt} \tag{4.120}$$

As it was mentioned previously, by knowing three currents, the fourth current can be easily calculated by using the equation (4.114):

$$i_{sa} = -i_{da}(t) - i_{g1}(t) - i_{g2}(t) \tag{4.121}$$

At this point, the complete small-signal circuit can be derived for an asymmetric $DG\ SOI\ nMOSFET$ device with two gates independently biased, as shown in Figure 4.23. This circuit is obtained from the relations (4.118) - (4.121) and the small signal low frequency equivalent circuit of any MOSFET transistor equivalent circuit (not described here).

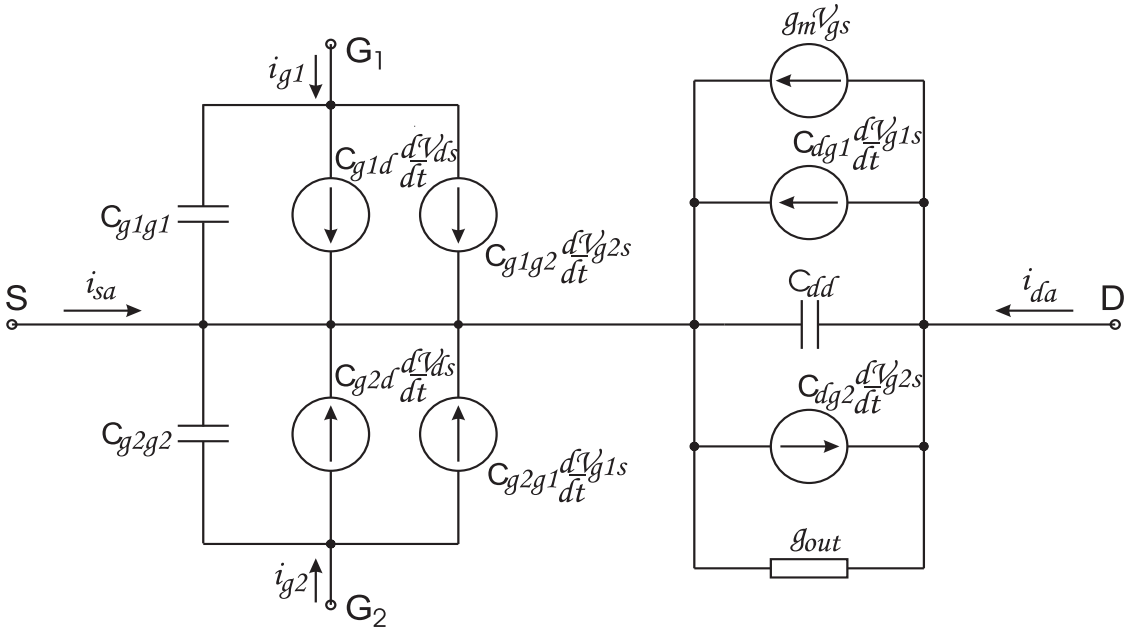


Fig. 4.23: The complete small signal circuit for an asymmetric $DG\ SOI\ nMOSFET$ device.

When the $DG\ SOI\ nMOSFET$ is a symmetric device, both gates are technologically and electrically connected together and have the same type and thickness of gate oxide. Thus, it can be shown that the equivalent small signal circuit of the symmetric $DG\ SOI\ MOSFET$ can be characterized by three terminals and thus, simpler equations will be obtained here, from the above asymmetric case. It is worth to mention that, because of the two gate oxides, the C_{dg} capacitance from below has a value which is two times higher than the one of a single gate transistor. Also, as the two gates are connected together, the last term in the equation of first gate current from asymmetric becomes equal to zero, and the equations become:

$$i_{da} = C_{dd} \cdot \frac{dv_{ds}}{dt} - C_{dg} \cdot \frac{dv_{gs}}{dt} \tag{4.122}$$

$$i_g = -C_{gd} \cdot \frac{dv_{ds}}{dt} + C_{gg} \cdot \frac{dv_{gs}}{dt} \tag{4.123}$$

If we express the terminal voltages with respect to the gate voltage of the symmetric DG transistor, then the equivalent circuit has a new form, where capacitances C_{dd} and C_{gg} will be replaced by capacitances with physical meaning, as shown below:

$$C_{dd} = C_{ds} + C_{dg} = C_{sd} + C_{gd} \tag{4.124}$$

$$C_{gg} = C_{gd} + C_{gs} = C_{dg} + C_{sg} \tag{4.125}$$

The complete equivalent circuit at small signal for the symmetric $DG\ SOI\ nMOSFET$, at quasi-static operation can be obtained after considering the final forms of the current equations as shown in Figure 4.24.

$$i_g = C_{gd} \cdot \frac{dv_{gd}}{dt} + C_{gs} \cdot \frac{dv_{gs}}{dt} \tag{4.126}$$

$$i_{da} = C_{ds} \cdot \frac{dv_{ds}}{dt} + C_{dg} \cdot \frac{dv_{dg}}{dt} \tag{4.127}$$

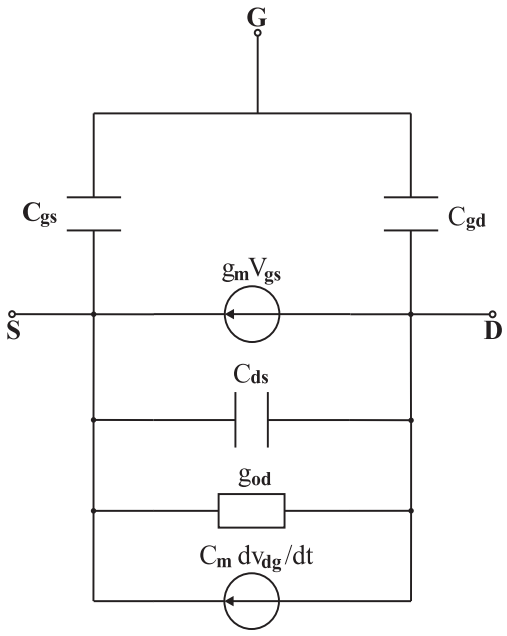


Fig. 4.24: The complete small signal circuit for a symmetric $DG\ SOI\ nMOSFET$ device, at quasi-static operation.

where $C_m = C_{dg} - C_{gd}$.

4.3.3 Evaluation of Charges and Capacitances

This section is assigned to evaluate the charges associated with each terminal for a symmetric $DG\ SOI\ nMOSFET$ operating in the dynamic regime at small signal, under the quasi-static approximation. Under these conditions, the total time-varying charges can be calculated with the same analytical functions derived for the dc regime, as shown above. Thus, here we show how we can calculate these small signal terminal charges by means of the expressions we have obtained in the previous sections for our compact DG

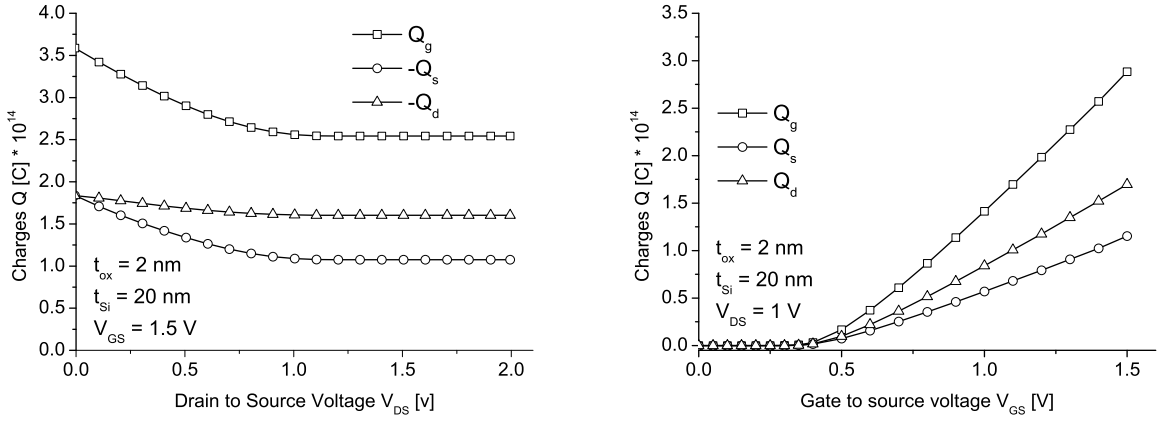
$SOI\ nMOSFET$ dc analytical model. As we work with symmetric $DG\ SOI\ nMOSFET$, there are only three terminals because the two gates are connected together and switched simultaneously. The dc total gate charge, Q_G, is calculated by integrating the inversion charge along the channel. Following the Ward and Dutton's linear channel charge partition method [121] which is widely accepted for the bulk $MOSFET$, the drain (Q_D) and source (Q_S) charges are computed as below:

$$Q_G = -W \int_0^L Q_{inv}(y)dy = -\mu W^2 \int_0^{V_{DS}} \frac{Q_{inv}^2(V)}{I_D} dV \tag{4.128}$$

$$Q_D = W \int_0^L \frac{y}{L} Q_{inv}(y)dy = \frac{WLt_{ox}}{2\epsilon_{ox}} \int_0^{V_{DS}} \frac{Q_{inv}^2(V)}{V_{GS}V - \int_0^V \psi_s(v)dv} dV \tag{4.129}$$

$$Q_S = -Q_G - Q_D \tag{4.130}$$

For these charge calculations, for the case of $DG\ SOI\ MOSFET$ at small signal and quasi-static operation, we have used the results of our compact modeling, as previously demonstrated. The numerical integration of terminal charges for a symmetric $DG\ SOI\ nMOSFET$ is implemented in Matlab code. In accordance with it, Figure 4.25 shows the calculated dependence of the three charges Q_G, Q_D and Q_S as a function of drain to source voltage (a) and gate to source voltage (b), respectively. From Figure $4.25a$, one can note that, for a zero drain voltage, Q_S is equal to Q_D as expected. These dc results can be transferred to the dynamic model for the small signal quasi-static operation.



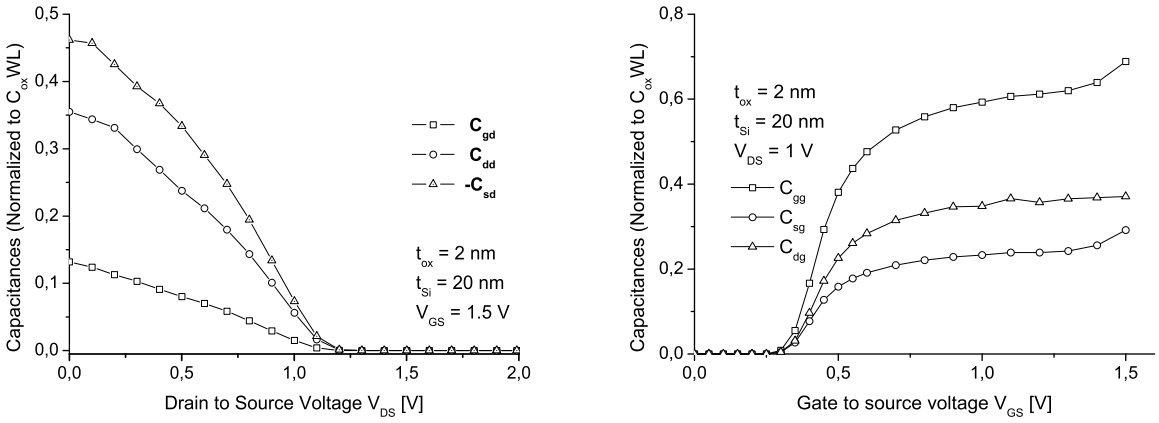
(a) The terminal electric charges as a function of V_{DS} (b) The terminal electric charges as a function of V_{GS}

Fig. 4.25: Terminal electric charges of a symmetric $DG\ SOI\ nMOSFET$, derived with our analytical model.

Generally speaking, a device with three terminals needs nine non-reciprocal capacitances for small-signal simulation as it has been specified in the previous section. According to the Tsividis's model [115] adapted by us for the DG SOI MOSFET under quasi-static functionality, these nine capacitances are defined in (4.90) and (4.91). Due to the charge

conservation law and further calculations, only four capacitances are independent: C_{gd}, C_{dd}, C_{dg} and C_{gg}, as shown in the equations (4.124) - (4.125). The other capacitances can be calculated from the independent capacitances and by using equations derived from the charge-conservation equation.

Figure 4.26 illustrates the capacitances of a $DG\ SOI\ nMOSFET$ calculated by our compact analytical model as a function of drain to source voltage (a) and gate to source voltage (b), respectively. The results are in excellent agreement with the generalized theory of the $MOSFET$ devices.



(a) The normalized capacitances as a function of V_{DS} (b) The normalized capacitances as a function of V_{GS}

Fig. 4.26: Normalized capacitances of a symmetric $DG\ SOI\ nMOSFET$, derived with our analytical model.

4.3.4 Cut-off Frequency

For the complete device, including extrinsic elements, we need to calculate a transition frequency called cut-off frequency (f_T). It is defined as the value of frequency at which the current gain of the symmetric $DG\ SOI\ nMOSFET$ device drops to one ($|\frac{i_{out}}{i_{in}}| = 1$). In order to obtain the frequency response, we propose to apply to our novel device the method used for the bulk $nMOSFET$ transistor. For this, we consider to have the transistor in saturation regime, where the drain is terminated in an incremental short circuit, while the gates are driven by the same ideal current source due to its symmetry property - see the Figure 4.27.

The Kirchhoff's law is applied at the two nodes represented in the Figure 4.27 and, thus, we obtain:

$$i_{in} - v_{gs} \cdot j\omega C_{gs} - v_{gs} \cdot j\omega C_{gd} = 0 \tag{4.131}$$

$$i_{out} - g_m v_{gs} - C_m C_{ds} \cdot \frac{dv_{dg}}{dt} + v_{gs} \cdot j\omega C_{gd} = 0 \tag{4.132}$$

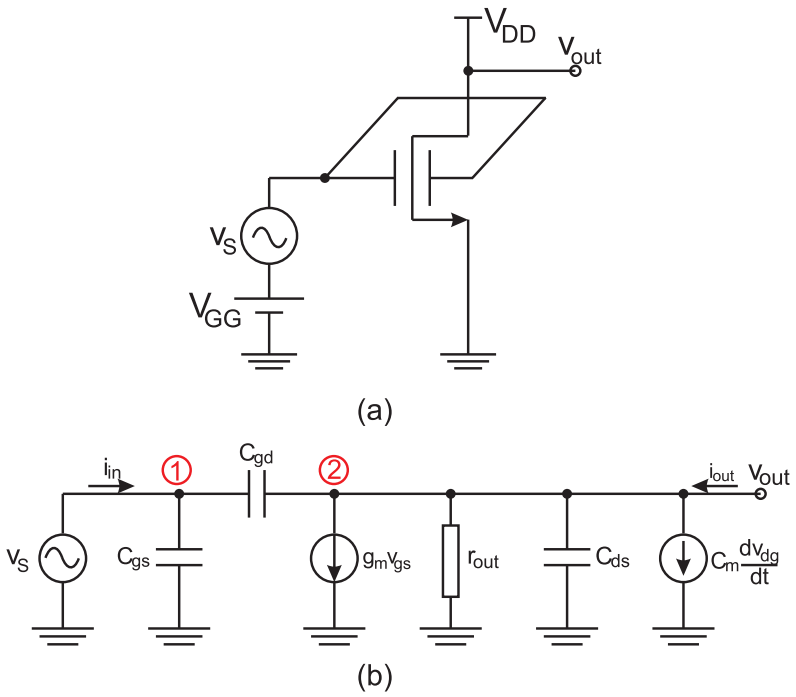


Fig. 4.27: a. The $DG\ SOI\ nMOSFET$ used in a common source configuration; b The small-signal circuit for the $DG\ SOI\ nMOSFET$ used as a circuit.

Assuming that $C_m = 0$ for low frequency operation and the current gain is defined as $h_{21} = \frac{i_{out}}{i_{in}}$, we have:

$$h_{21} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})} \tag{4.133}$$

By using the definition and the previous equation, the cut-off frequency will have the following form

$$f_T = \frac{g_m}{2\pi \cdot \sqrt{C_{gs}^2 + 2C_{gs}C_{gd}}} \tag{4.134}$$

Figure 4.28 shows the dependence of the cut-off frequency as a function of the gate to source voltage. It is important to noticing that the frequency can enhance by increasing V_{GS} and it might reach values of $15\ GHz$ for V_{DS} equal to $1\ V$.

4.3.5 Maximum Frequency of Oscillation for a DG SOI MOSFET-based Common Source Amplifier

The maximum frequency of oscillation (f_{max}) represents another figure of merit for a $RF\ MOSFET$ device due to its use in the analog circuits design. It is defined as the frequency at which the power gain is extrapolated to fall to unity [115]. In order to compute this frequency for a symmetric $DG\ SOI\ nMOSFET$, we make an attempt to analytically

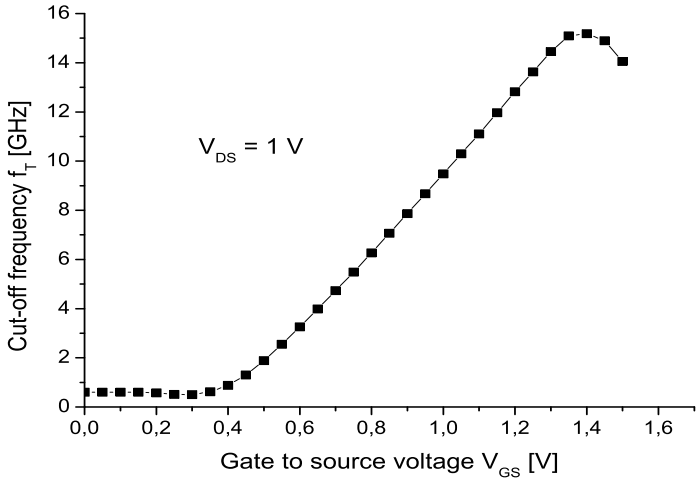


Fig. 4.28: The variation of cutoff frequency as a function of V_{GS}, calculated with the analytical model.

derive it by using the well-known approach from the conventional $MOSFET$ device. For this purpose, several assumptions have to be done. Firstly, the input impedance is computed with shorted drain and by neglecting C_{gd}, while the output impedance is derived by taking into account the capacitance C_{gd}. Secondly, the maximum power gain requires conjugate-matching between the signal generator and the input impedance of transistor, as well as between the output impedance of transistor and load.

In accordance with the definition, the maximum frequency of oscillation is given by the equation:

$$\frac{P_L}{P_{in}} = 1 \tag{4.135}$$

where, P_L represents output power and P_{in} is input power.

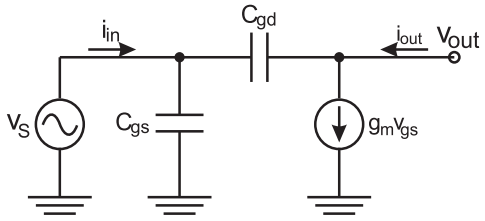


Fig. 4.29: Simplified Small-Signal Circuit of the common source configuration from Figure $4.27a$.

The formula from below can show that the maximum frequency is sensitive to the generator resistance:

$$f_{max} = \frac{f_T}{2 \cdot \sqrt{2r_g \cdot (g_{out} + 2\pi f_T \cdot C_{gd})}} \tag{4.136}$$

4.4 Summary

The continuous scaling down of the channel length as well as the necessity of increasing performances while short channel effects are maintained at the lowest level were the driving force for the development of new devices based on silicon on insulator technology. The so-called multiple-gate $SOI\ MOSFETs$ are seen as one of the best possibilities to replace the bulk $MOSFET$ device, at the end of the road map. To receive large acceptance, simple and efficient static and dynamic models of the multi-gate SOI devices should be developed and validated by experimental results. It has been the purpose of this chapter to show our contribution to the analytical modeling of un-doped asymmetrical and symmetrical $DG\ SOI\ MOSFET$ devices in the static and dynamic regime.

An original, simple and efficient analytical approach has been proposed in this thesis for the calculation of the electrostatic potential from the central part of the silicon layer in the symmetric and asymmetric $DG\ SOI\ MOSFET$ starting from the analytical approach of Poisson's equation. Then, the distribution of the electrostatic potential in the silicon film was derived for both cases. Our procedure is based on mathematical computations implemented in the Matlab code - see the Appendix B. Our method could replace other complex approaches based on Lambert function and smoothing factor without physical meaning which were previously used for the same electrostatic potential computation. Continuing on the same direction, the electric inversion charge and drain current could be calculated by using our analytical model in the symmetrical $DG\ SOI\ MOSFET$ device, in order to obtain a complete DC view.

Also, this chapter has shown the results and limits of a $1D$ analytical modeling for the electrostatic potential distribution in the very slightly doped silicon body of the asymmetric $DG\ SOI\ MOSFET$ devices, where the asymmetry was given by the different p or n type doping of the polysilicon gate electrodes. For the applied V_{GS} voltages higher than $0.5V$, the Poisson's equation was analytically solved by using only the electrons as charge carriers, the boundary conditions given by the continuity of the electric displacement at the two interfaces and the presence of a minimum electrostatic potential in the silicon body. The analytical approach was done in two steps. In the first step, the coordinates of the minimum electrostatic potential were derived, while in the second step the electrostatic potential distribution was obtained. The analytical functions involved in the modeling have restricted the coordinates of the minimum potential value to a well-defined $2D$ existence domain. An iterative method performed in the Matlab code was used for the calculation of the coordinates of the minimum electrostatic potential. At the end of this process, we have demonstrated for the first time that, when the applied V_{GS} voltage varied from $0.5\ V$ to $1\ V$, the minimum electrostatic potential was pinned at a value of about $0.459\ V$ rather similar with the pinning phenomenon shown in the analytical modeling of symmetric $DG\ SOI\ MOSFET$. The coordinates of the above minimum has allowed us the calculation of the electrostatic potential distribution in the whole silicon body.

Despite the sensitivity of the electrostatic potential solution to the accuracy of its min-

imum localization, our theoretical study described in this chapter has shown that the $1D$ analytical modeling is a powerful tool to understand the physics of the asymmetric $DG\ SOI\ MOSFET$ devices and to prove a volume inversion for a typical geometry and biasing.

In order to have a complete evaluation of a $MOSFET$ device, it is necessary to offer an AC view of it. Therefore, a small signal circuit for a symmetrical $DG\ SOI\ MOSFET$ has been proposed, starting from the assumption of the quasi-static operation. According to it, even if the terminal voltages are varying in time, the charges per unit are assumed to be identical at any time to those obtained if the dc voltages are used instead. In this environment, the intrinsic small signal circuit has been constructed and the terminal charges and capacitances were calculated by using the proposed analytical approach in order to complete the AC description. At the end of the chapter, new models have been used to compute the RF figures of merits in terms of the cut-off frequency and maximum frequency of oscillation.

Chapter 5

Contributions to the Modeling and Design of Circuits Based on DG SOI MOSFET and MEMS

During the last few decades, the bulk $MOSFET$ transistors have been continuously scaling down, and today they are reaching deep sub-100 nm sizes, where the limitations due to the short channel effects (SCE) are more and more challenging. This SCE threatening has driven to a high demand for the development of new devices in silicon on insulator technology such as double-gate $SOI\ MOSFET$. The IC designers have put a great effort to investigate the potential of these novel devices for their use in the next generation of digital and analog applications [55, 100]. Excellent analog performances of SOI devices in terms of low leakage, high frequency operation, high voltage gain and transconductance have been already electrically proven. However, the simulation of analog/digital circuits based on multiple-gate SOI devices is still at the beginning since the existing compact models for new transistors have not been accessible for market applications.

It is the purpose of this chapter to present a library created in Verilog A tool for the compact analytical modeling of the symmetrical un-doped double-gate $SOI\ MOSFET$ given in Chapter 4 and to use this library for the design of circuits based on $DG\ SOI\ MOSFET$ devices. The main reason for using the Verilog A programming consists of its incorporation within Cadence Virtuoso Design environment where the new device can be further introduced in the structure of analog circuits. The chapter comprises of two big parts. The first section of the chapter is assigned to the design of a common source amplifier based on a $DG\ SOI\ MOSFET$ transistor described with Verilog A tool. The second section is proposing a procedure to design a configuration of future integrated Colpitts oscillator consisting of a $DG\ SOI\ MOSFET$ device and a $RF\ MEMS$ resonator as the positive feedback loop. The analytical behavioral model is based on an iterative perturbation method, which is helping us to systematically analyze the transient and steady state oscillations in the above-mentioned oscillator and finally, to design such a novel circuit with a deep understanding of it.

5.1 DC Operation of a Common Source Amplifier Based on DG SOI MOSFET

Chapter 4 from this thesis has been dealing with the analytical modeling of both symmetrical and asymmetrical un-doped $DG\ SOI\ MOSFET$ device in the static and dynamic regimes. The proposed $DG\ FET$ analytical model gives a good perspective for understanding the physical phenomena occurring in such a new transistor and facilitates the calculation of the drain current, specific conductances, charges and capacitances. The overall characteristics have been obtained by using the powerful Matlab tool. However, the Matlab programming does not make the device accessible for analog or/and digital circuit design and, thus, the entire behavior of a symmetrical un-doped $DG\ SOI\ MOSFET$ transistor should be implemented in Verilog A tool.

Verilog A represents a high-level language used to create behavioral models of RF blocks such as mixers or amplifiers as well as device models for bulk $MOSFETs$, $SOI\ MOSFETs$ etc. This tool allows the designer to build Verilog A compact models within the Cadence Virtuoso Design environment where the circuit simulations can be subsequently performed.

This section of the chapter proposes a Verilog A approach (see Appendix C) for the entire model of a symmetrical un-doped $DG\ SOI\ MOSFET$ device proposed in Chapter 4. Figure 5.1 illustrates the output characteristics of the above-mentioned transistor obtained with Matlab and Verilog A tools.

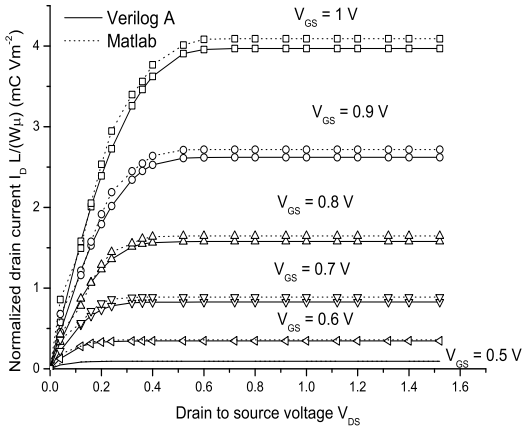


Fig. 5.1: Comparison of the Output Characteristics for an Un-doped Symmetric $DG\ SOI\ MOSFET$ performed with Matlab and Verilog A.

One can observe that the $I - V$ output characteristics resulted from Verilog A have very similar values to those obtained with the Matlab code. The small difference might come from the less accurate calculation of Verilog A tool. However, Verilog A presents

the advantage of incorporating the analytical compact device modeling into a library to be further used for $DG\ SOI\ MOSFET$- based circuit simulations. As an example, we have designed a simple analog circuit that contains the above-mentioned library. Thus, in Figure 5.2, we show a common source amplifier based on a $DG\ SOI\ MOSFET$ transistor that has its analysis implemented in Verilog A as written above.

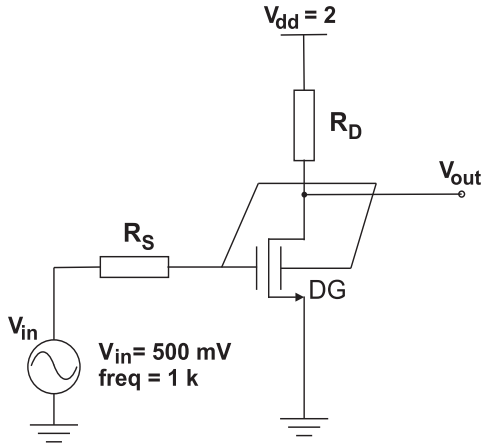


Fig. 5.2: Common Source Amplifier Based on $DG\ SOI\ MOSFET$ implemented in Verilog A.

The rectangular symbol from Figure 5.2 represents the novel transistor for which the library comes from the Verilog A code (see Appendix C) and has three terminals in terms of gate, drain and source. Note that the symbol has only one gate because of the symmetry property of the transistor. The resistances R_S and R_D were chosen to provide dc biasing and a proper voltage transfer characteristic for the common-source amplifier that is illustrated in Figure 5.3.

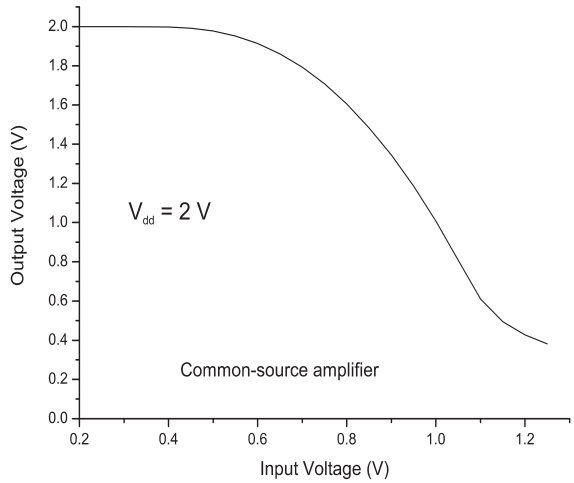


Fig. 5.3: Transfer Characteristic ($V_{out} = f(V_{in})$) for a Common Source Amplifier Based on $DG\ SOI\ MOSFET$ implemented in Verilog A based on our developed models.

The inverter-type transfer characteristic can be easily noticed from Figure 5.3. Thus,

one can remark that the output voltage is equal to V_{dd} when the input voltage is smaller than threshold voltage, i.e., the $DG\ SOI\ MOSFET$ transistor is in OFF state. As the input voltage (V_{in}) increases above the threshold voltage, the drain current begins to flow and the output voltage starts to fall below V_{dd} as shown in Figure 5.3. By further increasing the input voltage, the output voltage rapidly falls toward a low voltage. Further, as the input voltage is much beyond the threshold voltage, the transistor enters the triode region and the output voltage is closed to zero.

5.2 Colpitts Oscillator Based on RF MEMS and DG SOI MOSFET

The electronic oscillators represent one of the most common functional blocks used in the communication systems, where they act as local oscillators in order to up- and down-convert the signal frequency or to provide a clock signal as a time reference signal for the synchronization in the operation of transmitters and receivers. Since the trend is to standardize and exploit the digital cellular phone systems or to replace the cables by wireless links, a great demand of high frequency of approximately several GHz has emerged and thus, the clock signal has to be very accurate and a high performance oscillator is needed. On the other hand the oscillator integration is a strong demand, needed for the low cost-low size chips in many applications including next generations of cell phones. The present solution consists of tuned oscillators class that contains off-chip components, like passive resonator LC tank [8, 31, 128], quartz crystal [34, 75, 117] or surface acoustic wave resonator in its positive feed-back loop. It is well known that the tuned oscillators have a poor integrability because of a low quality factor for inductors and their large area. The off-chip quartz crystal oscillators consume a lot of PCB area but they present really huge crystal quality factors ($Q > 100000$ at 10 MHz [53]). The current research offers a possibility to reduce the PCB size issue by replacing the off-chip quartz crystal resonators with on-chip $MEMS$ silicon resonators which should preserve high quality factor [54, 93].

The evolution of the integrated circuit technology has also increased the transistor performances making them faster with every new generation, which determine high performances of both analog and digital circuits. Thus, the use of $DG\ SOI\ MOSFET$ in circuits is envisioned for the ultimate miniaturization which is pushing the operation frequencies to its limits, too.

Accordingly, in this chapter, a methodology to analytical design a configuration of an integrated Colpitts oscillator formed on a $DG\ SOI\ MOSFET$ device with a $RF\ MEMS$ resonator in the positive feedback loop is proposed, for the first time. It is anticipated to have much smaller size than the present oscillators and at least the same performances, if not better. In this thesis, we are going to analytically design the oscillator in the time domain, by means of the perturbation method proposed by Buonomo et al. [12, 13] for clas-

sical oscillator circuits. The method is able to predict the duration of transient regime and the characteristics of the steady state oscillations, in terms of amplitude and frequency evolution from the start-up time till the stable regime is reached. As detailed in the annex D, the Lyapunov's stability criteria for the differential equations characterizing the time-domain behavior of the oscillator will provide a reliable design method for the integrated passive/active component, and the dc biasing of the circuit, so that to get the needed instability of oscillation at the start-up time as well as the stability operation after reaching steady state regime.

In this context, Figure 5.4 shows an $RF\ MEMS$ and $DG\ SOI\ MOSFET$ based oscillator in which the RLC series circuit represents the functional equivalent electrical circuit of the micro-mechanical disk resonator characterized in Chapter 3. As a reminder, a micro-electro-mechanical ($MEMS$) device is mechanically analyzed as a mass-spring system which is moving in the presence of a damping force, when an external force acts. In addition, it is also electrically characterized by finding an equivalent electric circuit in terms of a series RLC for which the resistance, inductance and capacitance depend on the mechanical components (m, c and k).

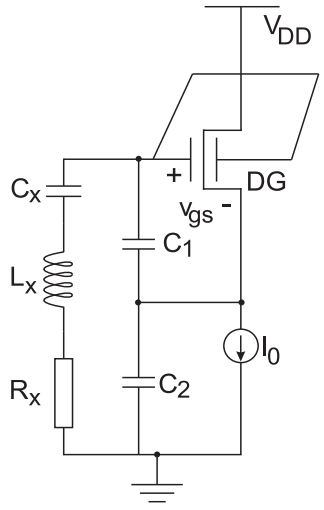
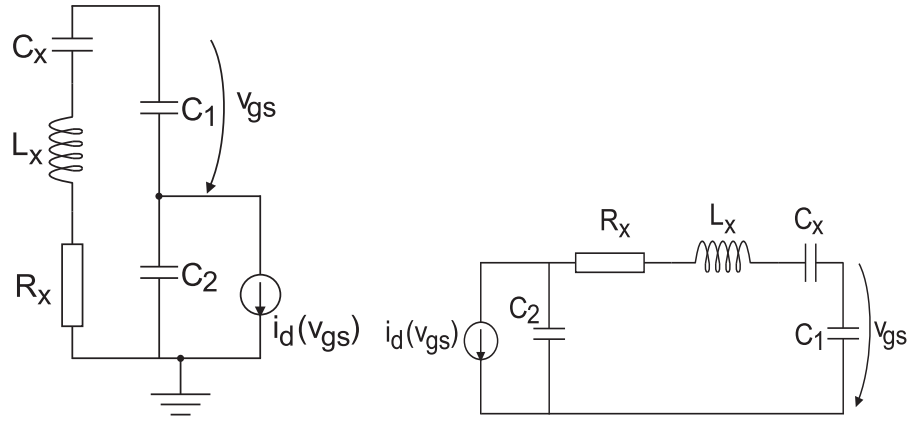


Fig. 5.4: Integrated $RF\ MEMS$ and $DG\ SOI\ MOSFET$ Based Oscillator.

Figure $5.5a.$ illustrates the small signal circuit of our Colpitts oscillator, while Figure $5.5b.$ presents the equivalent scheme, consisting of the amplifier and its integrated RLC positive feedback loop called incremental circuit.

The dynamic equation describing the time-domain evolution of our oscillator around the equilibrium point [12] is derived by considering the feedback loop circuit previously presented and the small signal equivalent circuit of the MOSFET transistor, in terms of the voltage-controlled current-source $i_d(v_{gs})$ shown in Figure $5.5b$. Here, v_{gs} and i_d are the incremental quantities superposed on the static operation Q-point. The AC analysis is based on the DC characteristics and the associated DC equations are further summarized,



(a) Small Signal Equivalent Circuit of the integrated Colpitts oscillator

(b) Incremental Circuit

Fig. 5.5: Small signal equivalent circuit and incremental circuit for an $RF\ MEMS$ and $DG\ SOI\ MOSFET$ based oscillator.

below.

$$I_0 = 2\mu\frac{W}{L}\frac{\epsilon_{ox}}{t_{ox}}(V_{GS}V_{DS} - \int_0^{V_{DS}} \psi_s(V)dV) \tag{5.1}$$

The oscillator has a $DG\ SOI\ MOSFET$ transistor as an active device which was accurately modeled in Chapter 4. For simplicity, the equation (4.46) has been re-written above. It is also assumed that the silicon central electrostatic potential is pinned to its maximum value for a channel voltage higher than a certain value (see Chapter 4). The dependence law of the maximum central electrostatic potential as a function of the channel potential is the following:

$$\psi_0 = \frac{2kT}{q} \cdot ln(\frac{\pi}{t_{si} \cdot b}) + V = 0.462 + V \tag{5.2}$$

By introducing the equation (5.2) in (4.6), the surface electrostatic potential of the $DG\ SOI\ MOSFET$ transistor used for the proposed oscillator can be calculated, as below:

$$\psi_s = 0.462 + V - \frac{2kT}{q} \cdot \ln[\cos(b\exp(\frac{0.462 \cdot q}{2kT})\frac{t_{Si}}{2})] \tag{5.3}$$

For the simplicity's reason, we make some notations:

$$D = \frac{2kT}{q} \cdot \ln[\cos(b\exp(\frac{0.462 \cdot q}{2kT})\frac{t_{Si}}{2})] \tag{5.4}$$

$$E = 0.462 - D \tag{5.5}$$

For further analysis, the output resistance of the current mirror (current source) and the one of the $DG\ SOI\ MOSFET$ transistor are neglected. The capacitances C_{gd}, C_{gs}

and C_{ds} are neglected for the equivalent incremental circuit, due to the small associated reactances at the RF frequencies. The active device is assumed to always operate in the pinch-off region ($V_{DS} \geq V_{GS} - V_{th}$ where V_{th} represents the threshold voltage).

In the design of oscillator circuits, it is necessary to find relationships between the circuit parameters and the oscillator characteristics in order to satisfy the design requirements. It is the purpose of the further analysis to establish the relation between the specifications and the design constraints.

From the small signal circuit of the oscillator (Figure $5.5b$.), the ac currents flowing through the circuit and the voltages dropped on the elements can be calculated as follows:

$$i_{C_1} = C_1 \frac{dv_{gs}}{dt} \tag{5.6}$$

$$v_{C_x} = \frac{C_1}{C_x} \cdot v_{gs} \tag{5.7}$$

$$v_{R_x} = C_1 R_x \frac{dv_{gs}}{dt} \tag{5.8}$$

$$v_{L_x} = C_1 L_x \frac{d^2 v_{gs}}{dt^2} \tag{5.9}$$

By applying Kirchhoff's laws on the circuit, the following equations are obtained:

$$v_{C_2} = C_1 L_x \frac{d^2 v_{gs}}{dt^2} + C_1 R_x \frac{dv_{gs}}{dt} + (\frac{C_1}{C_x} + 1) v_{gs} \tag{5.10}$$

$$i_d(v_{gs}) + i_{C_2} + i_{C_x} = 0 \tag{5.11}$$

By introducing the equations (5.6) - (5.10) in the equation (5.11), a third order differential equation is derived. Even if apparently we have four components able to store energy (C_x, C_1, C_2 and L_2), one can easily see that C_x and C_2 can be replaced by a single equivalent capacitance, and thus, finally, we get a circuit with three elements able to store energy (and thus a third order system is justified for our oscillator). The equation (5.11) governs the functionality of the oscillator in the time domain and can be interpreted as a time-domain "transfer function" of the oscillator because of the output voltage related with the input voltage (see Figure 5.4).

$$\frac{d^3 v_{gs}}{dt^3} + \frac{R_x}{L_x} \cdot \frac{d^2 v_{gs}}{dt^2} + \frac{1}{L_x C} \cdot \frac{dv_{gs}}{dt} = -\frac{1}{L_x C_1 C_2} \cdot i_d(v_{gs}) \tag{5.12}$$

The notations used in the previous equation are as follows:

$$i_d(v_{gs}) = g_m v_{gs} + i \tag{5.13}$$

$$i = 2\mu \frac{W}{L} \frac{\epsilon_{ox}}{t_{ox}} (\frac{v_{gs}^2}{2} - E \cdot v_{gs} + V_{th}(E - \frac{V_{th}}{2})) \tag{5.14}$$

$$g_m = 2\mu \frac{W}{L} \frac{\epsilon_{ox}}{t_{ox}} (v_{gs} - V_{th}) \tag{5.15}$$

$$\frac{1}{C} = \frac{1}{C_x} + \frac{1}{C_1} + \frac{1}{C_2} \tag{5.16}$$

$$F = 2\mu \frac{W}{L} \frac{\epsilon_{ox}}{t_{ox}} \tag{5.17}$$

Note that the above small-signal analysis is performed with respect to the real time t variable.

One can see that the non-linear circuit behavior is characterized by the third-order differential equation (5.12), which, if numerically solved, this can provide the transient and the steady state oscillation signal, for a proper designed circuit. The methodology used here will help us to design the active and/or passive components of the oscillator components so that to get the desired oscillation functionality. In addition, based on the perturbation theory (presented in detail in the Appendix D), one can demonstrate that the above equation (5.12) describes an oscillator with shifting bias, which means that the final steady state oscillation will end up with a dc signal component superposed to the initial dc biasing of the oscillator, as treated in Buonomo [12], which can trigger the oscillator in the class-C operation. Thus, one can predict the operation region of the amplifier, based on this perturbation modeling. This iterative perturbation method is used in order to analyze the transient evolution and steady-state oscillations for our proposed oscillator based on $RF\ MEMS$ and $DG\ SOI\ MOSFET$ devices. In accordance with it, a small dimensionless perturbation parameter ϵ is introduced and assumed to be related to the circuit losses. Thus, this perturbation parameter is defined as the inverse of the circuit quality factor Q as follows:

$$\epsilon = \frac{R_x}{\omega_0 L_x} \tag{5.18}$$

and $\omega_0 = \sqrt{\frac{1}{L_x C}}$. Here, it is important to emphasize, that the omega zero represents the natural resonance of the RLC circuit, which coincides with the oscillation frequency of the ideal oscillator, where no losses are present in the circuit. In the presence of the losses, the perturbation theory can predict a solution asymptotically closed to the experimental result, in terms of both amplitude and frequency of oscillation, which are both shifted from their corresponding values for the ideal oscillator. The higher the order of approximation used for deducing the oscillation solution, the more accurate fit between the theoretical and experimental value of the oscillation frequency and the oscillation amplitude of real oscillator is obtained. By further processing the equation (5.12), a normalized equation is

derived, in terms of dimensionless time, t' and input voltage, v_{gs}/V_{th}. Thus, a dimensionless time $t' = \omega_o t$ and a dimensionless variable $x = \frac{v_{gs}}{V_{th}}$ are used in the equation (5.12) and the following normalized perturbation equation is derived:

$$(\frac{d^3}{dt'^3} + \epsilon \cdot \frac{d^2}{dt'^2} + \frac{d}{dt'})x = \epsilon \frac{F(V_{th}+E)}{R_x C_1 C_2 \omega_0^2} \cdot (x + \alpha V_{th} x^2 + \frac{\beta}{V_{th}}) \tag{5.19}$$

where $\alpha = -\frac{3}{2(V_{th}+E)}$ and $\beta = -V_{th} \cdot \frac{2E-V_{th}}{2(v_{th}+E)}$.

On the other hand, as written in the Annex D, the general equation describing the third order oscillator with shifting bias has the following form: $(\frac{d^3}{dt^3} + \epsilon a \frac{d^2}{dt^2} + b\frac{d}{dt} + \epsilon c)x = \epsilon(k_2 \frac{d^2}{dt^2} + \epsilon k_1 \frac{d}{dt} + k_0) f(x)$. By making the identification between the above-mentioned two equations, the constants a, b, c, k_0, k_1 and k_2 and the non-linear function $f(x)$ (which describes the behavior of the active device around the equilibrium point) are obtained as follows:

$$a = b = 1 \tag{5.20}$$

$$c = k_1 = k_2 = 0 \tag{5.21}$$

$$k_0 = \frac{F(V_{th}+E)}{R_x C_1 C_2 \omega_0^2} \tag{5.22}$$

$$f(x) = x + \alpha V_{th} x^2 + \frac{\beta}{V_{th}} \tag{5.23}$$

If the oscillator is correctly designed, at the level of both feed-back loop and amplifier, then the numerical solution of the equation (5.19) will provide the oscillation waveform $x(t)$, in terms of oscillation frequency and amplitude for both the transient and the steady state regime. Within the thesis we shall learn how to design the circuit parameter for obtaining a stable oscillation and we shall determine the oscillation characteristics by means of the perturbation method, where both x and $f(x)$ values, which are specific to active device, will be expressed as complex functions (i.e., functions written in the imaginary domain) of perturbation parameter and the multitude of signal harmonics. The advantage of the perturbation method is the fact that the theoretical solution can be designed to fit asymptotically the experimental oscillation result by adding an increased number of perturbation terms, by going to higher approximation orders, as shown below. Therefore, the key aspect of the perturbation method applied for the analysis and design of the electronic oscillators is that the solution $x(t)$, the transfer function of active device, $f(x)$ and the oscillation frequency can be forced to be expressed as complex polynomial expressions (see the Annex D) depending on the perturbation parameter as below:

$$x(t) = x_0 + \epsilon x_1 + \epsilon^2 x_2 + ... \tag{5.24}$$

$$\omega = \omega_0(\tau) + \epsilon \omega_1 + \epsilon^2 \omega_2 + ... \tag{5.25}$$

$$x_0 = B_0(\tau(t)) + A_0(\tau(t)) cost \tag{5.26}$$

In the above equations, τ is representing what it is called "slow time scale", which reflects the fact that the time variation of the dc component of the emerging oscillation, as well as its amplitude envelope are slower with respect to the rapid variation with the time of the oscillation, itself , x(t). Mathematically the relation between the two time scales is expressed by : $\tau = \epsilon * t$.

The detailed description of the oscillation solution is presented in the Annex D.

Here, it is worth to emphasize that B_0 is the dc component of the emerging oscillation and A_0 is the amplitude of oscillation, both of them being slowly variable with time in the transient regime, if we compare their time variation with respect to the period of oscillation. For a more detailed description of the perturbation method, one can study the Annex D of the thesis, where characterization of the circuit up to the second order approximation is developed.

The first order approximation methodology is enough for designing the oscillator. Anyway, the second order approximation was also used here, but only for an accurate description of the frequency deviation from the ideal value of the oscillation signal.

5.2.1 Analysis and design of integration of a Colpitts oscillator by means of perturbation method based on first order approximation

According to this approximation, only the terms in epsilon at the first power and free terms will be kept from the calculation. Following the entire procedure described in the Annex D, for the first order approximation methodology and considering that only the fundamental harmonic is present in the circuit, we get the following general final form of our normalized perturbation equations:

$$e^{j\nu}(-3\omega^2\frac{dA_0}{d\tau} - 3\omega\frac{d\omega}{d\tau}A_0 - j\omega^3 A_1 - a\omega^2 A_0 + b_0\frac{dA_0}{d\tau} + j\omega b_0 A_1 + j\omega b_1 A_0 + cA_0) + b_0\frac{dB_0}{d\tau} + cB_0 = e^{j\nu}(k_0 - k_2\omega^2)F_{1,0} + k_0 F_{0,0} \quad (5.27)$$

Balancing the real and imaginary part of the amplitude of fundamental harmonic (A_0) and the DC component (B_0) of the general first order equation, we get the following system of equations:

$$\frac{dB_0}{d\tau} = k_0 F_{0,0} - cB_0 \quad (5.28)$$

$$\frac{dA_0}{d\tau} = \frac{1}{2}[(k_2 - k_0)F_{1,0} + (c - a)A_0] \quad (5.29)$$

where, as shown in the Annex D, the expressions for the above amounts $F_{0,0}$ and $F_{1,0}$ specific to first order approximation approach for our oscillator are given below:

$$F_{0,0} = B_0 + \alpha V_{th}(B_0^2 + \frac{A_0^2}{2}) + \frac{\beta}{V_{th}} \tag{5.30}$$

$$F_{1,0} = A_0(1 + 2\alpha V_{th} B_0) \tag{5.31}$$

In order to find the time evolution for the dc and the ac component of the "potential" oscillation of our Colpitts circuit, as expressed by B_0 and A_0, in the above equations, we need to replace k_0, k_2, "a" and "c" constants by their specific expressions from the relations $(5.20$ - $5.23)$, and thus we obtain the equations from below:

$$\frac{dB_0}{d\tau} = k_0 F_{0,0} \tag{5.32}$$

$$\frac{dA_0}{d\tau} = \frac{1}{2}[-k_0 F_{1,0} - aA_0] \tag{5.33}$$

The first order nonlinear differential equations (5.28) and (5.29) from above offer us the possibility to understand and hopefully predict under which conditions we can get a successful transition of the system from an unstable transient regime to the steady-state stable oscillations. The above two equations characterize an electronic system, i.e., an oscillator, which can be either stable or unstable. Moreover, as we want to design an electronic oscillator, we need to force the system to behave unstable at the origin of time, so that an initial small oscillating signal coming from noise, to be able to grow and become a stable oscillation, at the end of the transient time. As shown in the Annex D, the key idea is that the mathematical stability of the above equations will characterize also the stability of the oscillator, as it was described above. Actually, within this thesis, the mathematical stability is studied by means of Liapunov' first method of stability. The approach of Lyapunov can be also used for finding the opposite condition, i.e. the instability condition needed to the start-up time. Lyapunov demonstrated the following stability statements:

1. If a "daughter " linearized system of differential equations is stable, than the "mother" non-linear system of differential equations (that generated the linearized system) is also stable. A similar logic conclusion can be drawn for the instability condition.

2. The stability of the linearized system of differential equations is assured if the eigenvalues of the Jacobian matrix of the linearized differential equations are negative real numbers. Starting from this, one can easily derive the instability condition of the same system, in terms of having positive eigenvalues of the Jacobian matrix.

Having this background in mind, one can find the conditions for system instability in the time origin, and its stability in the steady state condition followed by robust design of the oscillator in order to find amplitude, frequency of oscillation as well as the transient regime. The system of linearized equations, obtained from the above theory is given below, as follows :

$$\frac{dB_0}{d\tau} = k_0 \frac{\partial F_{0,0}}{\partial B_0} B_0 + k_0 \frac{\partial F_{0,0}}{\partial A_0} A_0 \tag{5.34}$$

$$\frac{dA_0}{d\tau} = -k_0 \frac{1}{2} \frac{\partial F_{1,0}}{\partial B_0} B_0 + \frac{1}{2}[-k_0 \frac{\partial F_{1,0}}{\partial A_0} - a] A_0 \tag{5.35}$$

With all these equations from above we can now derive the stability and instability needed for a robust design of our Colpitts oscillator.

The stability conditions, as per Lyapunov method applied to our oscillator are given below:

$$k_0 \frac{\partial F_{0,0}}{\partial B_0} - \frac{k_0}{2} \frac{\partial F_{1,0}}{\partial A_0} - \frac{a}{2} < 0 \tag{5.36}$$

$$k_0 \frac{\partial F_{0,0}}{\partial B_0} (-\frac{k_0}{2} \frac{\partial F_{1,0}}{\partial A_0} - \frac{a}{2}) > -k_0 \frac{k_0}{2} \frac{\partial F_{0,0}}{\partial A_0} \cdot \frac{\partial F_{1,0}}{\partial B_0} \tag{5.37}$$

After doing further calculations and arrangements the conditions of stability become:

$$a > k_0 \frac{F_{1,0}}{A_0} \tag{5.38}$$

$$a > k_0 (\frac{F_{1,0}}{A_0} - 2\alpha^2 V_{th}^2 A_0^2 \frac{A_0}{F_{1,0}}) \tag{5.39}$$

Similarly, following the Lyapunov theory and doing all calculations, the instability condition for our oscillator, specific to time origin operation will bring the following result:

$$\frac{W}{L} > \frac{t_{ox}}{\epsilon_{ox}} \cdot \frac{1}{2\mu} \cdot \frac{R_x C_1 C_2 \omega_0^2}{v_{th} + E} \tag{5.40}$$

If the mentioned stability and instability conditions are fulfilled, then by solving the nonlinear system of differential equations, in the time domain, one can get the amplitude envelope evolution in the transient (start-up) and the steady state regime of the first order approximated solution.

Thus, the system of first-order equations ($D.46$) and ($D.47$), formed on the particular coefficients obtained for our proposed $RF\ MEMS$ and $DG\ SOI\ MOSFET$ based oscillator, will show the transition of the circuit to the steady-state oscillation and provides a way to calculate the steady-state values for A_0 and B_0. In order to get the stationary values, their derivatives, as provided from the equations (5.27 - 5.28) are assumed to be zero and the steady state expressions for B_0 and A_0 result in:

$$B_0 = -\frac{1+k_0}{2\alpha k_0 V_{th}} \tag{5.41}$$

$$A_0 = \frac{\sqrt{\frac{k_0^2(1-4\alpha\beta)-1}{2}}}{\alpha k_0 V_{th}} \tag{5.42}$$

One can see that they strongly depend on the elements of the $RF\ MEMS$ resonator from the positive loop (R_x, L_x and C_x) and on the $DG\ SOI\ MOSFET$ device used in the oscillator.

With regard to the transient evolution of the oscillator, our interest is in the determination of the envelope for the oscillation amplitude until the steady-state regime is reached, as follows. First of all, as the oscillation solution provided by the first order analysis has the form: $x(\tau) = B_0(\tau) + A_0(\tau)cos(\tau)$, then it is easy to understand that not only during the transient, but also at the steady state, the amplitude envelopes (maximum and minimum values of $x(\tau)$) of the oscillation are obtained by performing the sum and subtraction of A_0 and B_0. Their dependencies on time are calculated by solving the system of first-order nonlinear equations (5.27) and (5.28) as follows:

$$\frac{d^2A_0}{d\tau^2} = -\frac{dA_0}{d\tau} + (\frac{k_0^2-1}{4} - \alpha\beta k_0^2)\cdot A_0 - \frac{\alpha^2 V_{th}^2 k_0^2}{2}\dot{A}_0^3 \tag{5.43}$$

$$B_0 = -\frac{1}{\alpha k_0 V_{th}}\cdot(\frac{k_0+1}{2} + \frac{1}{A_0}\frac{dA_0}{d\tau}) \tag{5.44}$$

The above system of non-linear equations was solved numerically, based on the known circuit values for both amplifier and feed-back loop components, in our case the $DG\ SOI\ MOSFET$ transistor and RLC circuit associated to the integrated $RF\ MEMS$ resonator. So in order to have a practical application of the above-described $RF\ MEMS$ and $DG\ SOI\ MOSFET$ based oscillator, we take into account the micro-mechanical disk resonator described in detail in Subsection 3.4.4.4 from Chapter 3, for which the values of the behavioral RLC series circuit obtained experimentally ([119]) are: $R_x = 745\ \Omega$, $L_x = 0.523\ mH$ and $C_x = 36.6\ aF$. We also assume that: $C_1 = C_2 = 0.6\ pF$, $V_{th} = 0.4\ V$, $I_0 = 1.7\ mA$ and $W/L = 1500$. The constant quantities used to describe the $DG\ SOI\ MOSFET$ transistor are those from Chapter 4, where the entire dc and ac analyses were done. We also neglect the term of $\frac{\beta}{v_{th}}$ in the equation (5.21) because it is very small related to the other terms of the function $f(x)$.

In Figure 5.6 we show the asymmetric amplitude envelopes of v_{gs} which are obtained by following the procedure presented above. The preliminary numerical results show that the steady-state oscillation is reached in a very short time of $1.5\ ns$ which, if confirmed by further modeling could prove the superior performance of an Colpitts oscillator formed on $MEMS$ resonator and $DG\ SOI\ MOSFET$ device over the bulk Colpitts oscillators.

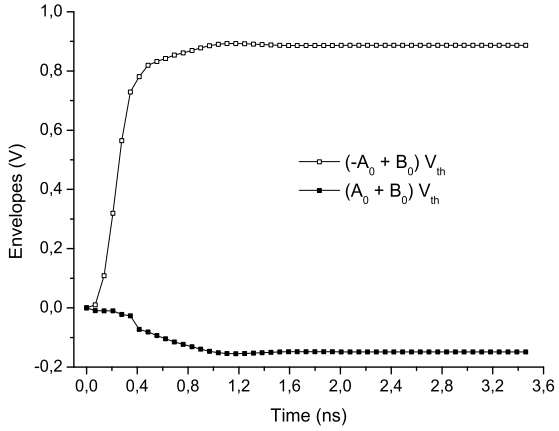


Fig. 5.6: Amplitude Envelope of the fundamental harmonic as a function of time for the case of first order approximation of the integrated Colpitts oscillator based on $RF\ MEMS$ resonator..

5.2.2 Analysis and design of integration of a Colpitts oscillator by means of perturbation method based on second order approximation

The design of the integrated oscillator based on the perturbation method, where the second order approximation is used can provide a further improved accuracy of the fit between the theoretical solution and the experimental one, but the improvement is not essential, at least when the amplitude envelope of fundamental harmonic is concerned. Much higher motivation for the use of the second order approximation in the design of oscillator comes from the need of theoretical evaluation of the oscillation frequency deviation from the natural resonance frequency of the fee-back loop circuit. As shown in the previous sub-section, within this second order approximation, the time evolution of the oscillation frequency with the slow time scale is: $\omega = \omega_0 + \epsilon\omega_1 + \epsilon^2\omega_2$. Actually, the frequency will have a small deviation from the natural frequency of the oscillator because of the losses and the nonlinear effects which are treated with the perturbation method. For this purpose, the second order approximation has been developed by keeping only the terms assigned to the ϵ^2 in all the terms of the general equation of the third order differential equation, and the term ω_2 is obtained as presented below - see Appendix D.

$$\omega_2 = \frac{1}{2A_0}[(k_2 - k_0)Im(R_{1,1}) - k_1F_{1,0} + b_2A_0 - 2k_2\frac{dF_{1,0}}{d\tau} + 3\frac{d^2A_0}{d\tau^2}] \tag{5.45}$$

By taking into account the particular values for the proposed oscillator based on $DG\ SOI\ MOSFET$ transistor and $RF\ MEMS$ resonator, the frequency deviation ω_2 becomes:

$$\omega_2 = \frac{1}{2A_0}(2\frac{dA_0}{d\tau} + 3\frac{d^2A_0}{d\tau^2}) \tag{5.46}$$

The value of ω_0 is derived from the zero order approximation and is a constant value which is given by the natural resonance circuit of RLC series circuit (and it is associated with ideal oscillator, when epsilon is almost zero), while the frequency deviations ω_1 and ω_2 come from the first and second order approximation, respectively. These amounts ω_1 and ω_2 are varying slowly with the time, being dependent on the slow time τ, as described in the Annex D.

For our oscillator, considering the numerical values from below for the $DG\ SOI\ MOSFET$ transistor and the $RF\ MEMS$ disk resonator, we can obtain explicit frequency deviations. Thus, for the micro-mechanical disk resonator described in detail in Subsection 3.4.4.4 from Chapter 3 the values of RLC series circuit obtained experimentally ([119]) are: $R_x = 745\ \Omega$, $L_x = 0.523\ mH$ and $C_x = 36.6\ aF$. In Figure 5.7 we show an example of calculation of the variation of the normalized frequency (ω/ω_0) as a function of transient time under the following conditions: $C_1 = C_2 = 0.6\ pF$, $V_{th} = 0.4\ V$, $I_0 = 1.7\ mA$, $W/L = 1500$. The parameters of the $DG\ SOI\ MOSFET$ transistor are those from Chapter 4 and the term of $\frac{\beta}{v_{th}}$ in the equation (5.21) is neglected , due to its very small value when related to the other terms of the function $f(x)$.

It is obvious that the frequency deviation $\epsilon^2\omega_2$ is not negligible because of the losses and the nonlinearity effects given by the $MEMS$ positive feed-back loop.

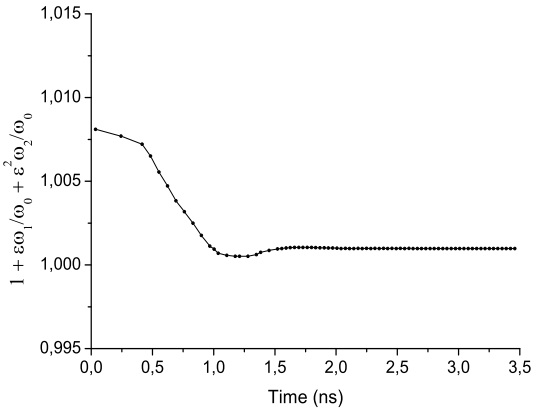


Fig. 5.7: Variation of the normalized oscillation frequency as a function of time during transient regime, as predicted by the second order approximation.

5.3 Summary

The purpose of this chapter has been to model and design several circuits applications based on double-gate $SOI\ MOSFET$ device and $MEMS$ resonator. Thus, at the beginning of the chapter we showed the operation of a common source amplifier based on $DG\ SOI\ MOSFET$ transistor, where a code written in Verilog A tool was developed for building a library that contains the proposed compact model of a symmetric un-doped $DG\ SOI\ MOSFET$ device (see Chapter 4). As a case study, this library was then used to simulate a common source amplifier based on the previous library for $DG\ SOI\ MOSFET$ transistor. It was shown that the Verilog A library-based static transfer characteristics of the common source amplifier using the $DG\ SOI\ MOSFET$ looks similar to that obtained for the same circuit, but where the Matlab code was used for solving the static equations of the circuit.

Then, in the second part of the chapter, the feasibility of the realization of an integrated oscillator containing the $DG\ SOI\ MOSFET$ transistors and $RF\ MEMS$ resonators performed in the SOI technology platform has been predicted at the modeling analysis by using the first and the second order approximation of the perturbation theory. This encouraging result might support the experimental research towards ultra small consumer electronics wireless applications. The chapter has shown, for the first time, how the perturbation method can be applied to design a non-linear oscillator comprising of a $DG\ SOI\ MOSFET$ device and a $RF\ MEMS$ resonator used for the positive feedback loop. The developed procedure showed the operation and design of the oscillator in time domain determining what are the conditions for start-up and for the stability in the steady state oscillations, as per Lyapunov' stability theory. The evolution with the time of the amplitude envelope of the fundamental harmonic and of the oscillation frequency deviation was theoretically predicted for the first time for an integrated Colpitts oscillator built with $DG\ SOI\ MOSFET$ and $RF\ MEMS$ disk resonator.

Chapter 6

Future Research Challenges in the Micro/Nano Technology Era

The micro/nano-electronics field is characterized by the translation of research from the well-known $CMOS$ down-scaling process to a more complex domain, where the innovation going beyond the limits of CMOS technology is accompanied by More-than-Moore technology diversification for reaching new system functionality like intelligent analog/RF, (bio)sensing, actuation micro/nano systems on chip (SoC) or in the package (SiP), that will benefit from the low power consumption, new smart (nano)materials and heterogeneous existent in the systems exploiting nano-technology. In this context, following the Moore's law for the miniaturization purpose will not be the only technology target in the near future, but adding new materials and new technologies in the package, containing $2D$ or $3D$ technologies for increased on-$2D/3D$ chip functionality at low cost-low power-high performance IS challenge, that deserves to be addressed.

In the general accepted framework of the micro- and nano-electronics, Figure 6.1 illustrates three main research domains that will co-exist in the near future: (1) More Moore, (2) Beyond CMOS and (3) More than Moore.

As it is described in chapter 2, Figure 6.1 shows that the More Moore domain is mainly dealing with technologies that obey the Moore's law, while the concept of "More than Moore" refers to new complex systems that combine different technologies and do not compulsory follow the conventional scaling law. The "More than Moore" also gives particular importance to $MEMS/NEMS$ and sensor technologies that are integrated with $CMOS$-based technology within a single chip. It consists of multifunctional system in the package (SiP) and $3D-MEMS$ technology. The Beyond $CMOS$ domain presented in Figure 6.1 exploits novel technologies such as nanowires and carbon nanotubes, as well as the molecular electronics that are expected to be used as an alternative when semiconductors are getting harder to scale. Taking into account the three research directions around Moore's law and more than that, here we show briefly the main challenges associated to each of them.

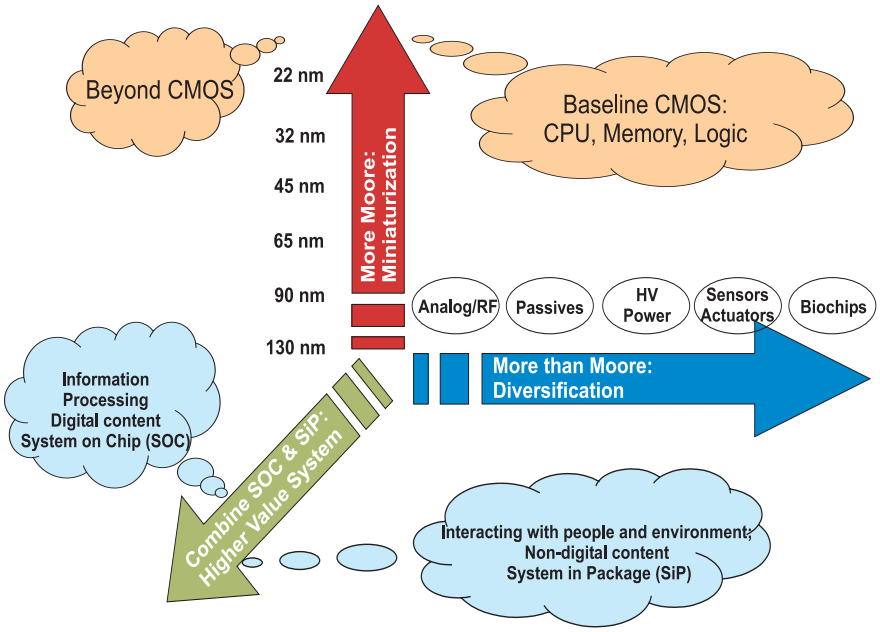


Fig. 6.1: Moore's Law and More (source: $ITRS$ 2007).

6.1 Quantum Effects in SOI Devices Specific to More Moore Domain

The topic is quite broad, with many implications at the level of device performance, like electric current capabilities in nano $MOSFET$ transistors, but here we shall mention just a basic quantum effect of electron concentration in silicon channel for such devices. As device miniaturization continues down to nm range, quantum effects will become relevant for the silicon-based nano devices. In the SOI devices, the quantum effects are important for the silicon film thickness and width decreasing below 5 nm, due to mainly the carriers confinement in such nano-scale layers. In comparison with the classical model, from quantum mechanics calculation (as it is shown in Figure 6.2 [72]) one can show that the electron concentration in the silicon channel has a maximum far from surfaces, and not at the surfaces as it is the case for the classical model of $MOSFET$ transistor. Such result can explain the increase of the threshold voltage observed in the ultra thin SOI $MOSFET$ transistors, due to the channel formation below the surface.

One can observe that the quantum effects give peaks of the electron concentration distributions at a distance of few nanometers from the surfaces. If the silicon thickness is very small (lower than 10 nm) the two surface regions will overlap and provide an electron concentration maximum in the middle of the semiconductor layer.

The entire analytical modelling of such a small SOI device that includes the quantum effects starts from the calculation of the Schrödinger and Poisson equations system as follows:

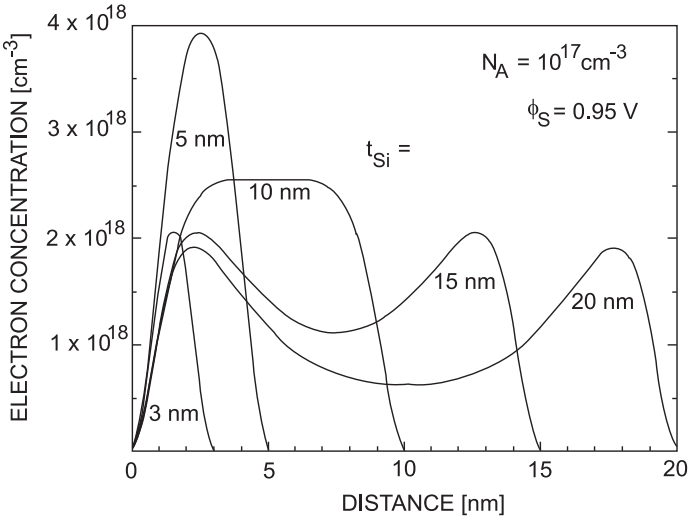


Fig. 6.2: Influence of the silicon thickness on the electron concentration distribution at the surface potential constant, according to the quantum model (source: [72]).

$$\frac{d^2\psi_{ij}(x)}{dx^2} + \frac{2m_{xj}}{\bar{h}^2}[E_{ij} - V(x)]\psi_{ij}(x) = 0 \tag{6.1}$$

$$\frac{d^2V}{dx^2} = \frac{q^2}{\epsilon_s}[N_A^-(x) + n(x) - p(x)] \tag{6.2}$$

where $\psi_{ij}(x)$ represents the normalized wave function of electrons occupying energy levels E_{ij}, $n(x)$ is the local concentration of electrons, $p(x)$ is the local concentration of holes, $V(x)$ gives the electrostatic potential energy and m_{xj} is the electron effective mass that describes the dynamics of the motion in direction perpendicular to the surface.

The Schrödinger equation gives the energy eigenstates and the corresponding eigenfunctions that contribute to the derivation of the electron concentration that will be used in the Poisson equation for the electrostatic potential distribution in silicon layer in the perpendicular direction to the surface. In accordance with the "quantum" model, the electron energies are quantized with a larger gap between two accepted energy levels for electrons because of a quite strong bending of the energy bands (see Figure 6.3) and, further, the effective mobility degrades and decrease the drain current. Besides, the transfer characteristics of the SOI transistor seems to be worse.

One can conclude that the agressive down-scaling process of the SOI devices touches a limit where the classical physics is insufficient to explain the behaviour of the transistor. At this point, a quantum mechanical model becomes necessary to provide an assessment of the device performance. The current and future research is concentrated on the understanding and modeling of the quantization effects in the semiconductor devices.

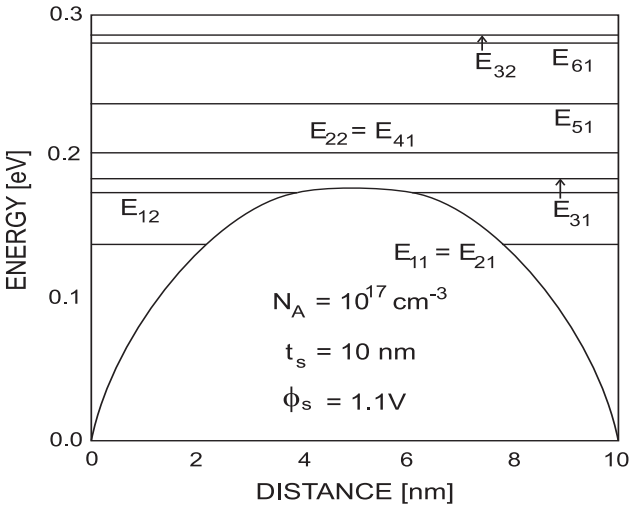


Fig. 6.3: Discrete energy levels E_{ij} of electrons in the semiconductor conduction band for a symmetrical $DG\ SOI\ MOSFET$ structure (source: [72]).

6.2 Carbon Nanotube Resonators Specific to Beyond CMOS Domain

The future technology is paved by new functional nano-materials such as the carbon nanotubes (CNT) expected to be used in many applications, including high frequency-electronics because of their large mobility, high transconductance and long mean-free paths. There are several applications like CNT based detectors, mixers and amplitude-modulated (AM) demodulator for modulation frequencies up to 100 kHz due to its non-linear current-voltage characteristics. The latter stage was involved in an AM radio receiver that operates at a carrier frequency of 1 GHz as it is shown in Figure 6.4 [102].

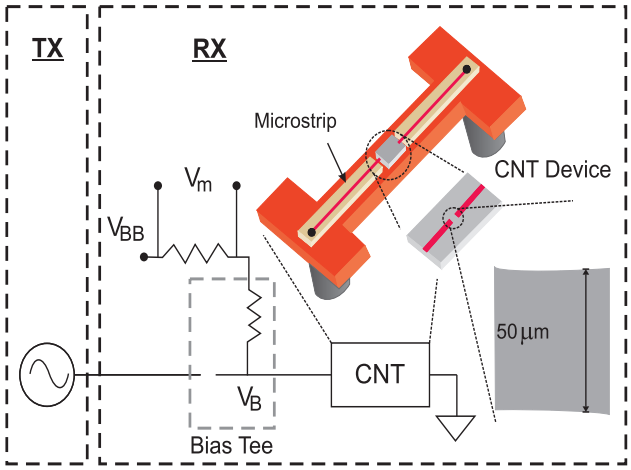


Fig. 6.4: Schematic of the CNT-based AM demodulator (source: [102]).

One can observe that the future receivers can have in their structure, CNT-based circuits instead/or in addition to silicon-based technology. This evolution is a promising improvement in performances and area even if the formation of low resistance contacts for $CNTs$ is a big challenge due to its influence on the device properties. The dynamical characteristics of nanotubes are functionally suitable for both active and passive elements such as: nanotube transistors, nanotube interconnects and resonators. Thus, Figure 6.5 presents the LC equivalent circuit for a nanotube LC tunable resonator that works at frequencies of GHz orders [58].

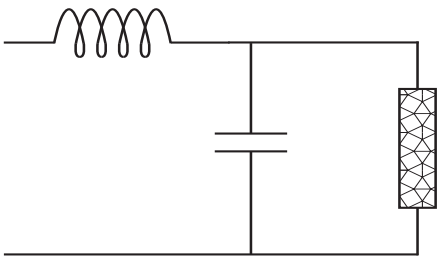


Fig. 6.5: Equivalent circuit for the CNT resonator (source: [58]).

Furthermore, carbon nanotubes is one of the most promising materials for interconnects in $3D$ integration, electronic devices (field emission sources, transistors, nano- transmission lines), nano-antenna, low-noise analog microwave amplification circuits [14].

In this context, the exploitation of $CNTs$ is a promising future alternative of silicon $CMOS$ under the nanoelectronics umbrela. So that, high speed and telecom devices and circuits operating at very high frequencies of hundreds of GHz and reaching even the THz regime will be essential for providing More than Moore and Beyond Moore system solutions. Co-existence of silicon-based analog ICs with CNT devices will be important for aproaching both very high frequency and low power operation.

6.3 3D MEMS Technology Specific to More Than Moore Domain

The technology trend for the future systems is given by the three-dimensional ($3D$) $MEMS$ technology which brings in the same package hybrid technologies for complex interaction (by means of wireless and autonomous $3D-MEMS$ micro-nano systems) with people and environment. It also provides thick and robust sensor structures that are very sensitive to inertial forces and pressure, but immune to other external factors. The $3D$ $MEMS$ is a novel technology that implies a combination of bulk and surface $MEMS$ technology for sensor realization, in addition to the IC technology for sensor signal processing in order to offer compatibility with the demands of the three-dimensional world. The thickness of the micro-structures may decrease and the thinned wafers are gathered to each

other to build multi-wafer stacks. Also, every $MEMS$ device for sensor and actuator applications has to be hermetically encapsulated. Besides, this innovative technology offers very accurate sensors, small unit size and low power consumption, becoming ideal for wireless applications, including on-chip energy harvesting for powering the $3D-MEMS$ system.

Figure 6.6 presents different generations of silicon-based RF System in Package (SiP) that use $3D$ die stacking and packaging. Replacing wire bonding by flip chip technology for on-chip area saving, combined with wafer to wafer bonding and through the silicon vias for new electrical interconnection methods are the technology steps for building $3D-MEMS$ systems in package (SiP) for future wired and wireless applications. Their great advantage consists of the integration of high-quality passive components onto a silicon wafer which serves as a substrate for the realization of active component dies, $MEMS$ dies etc.

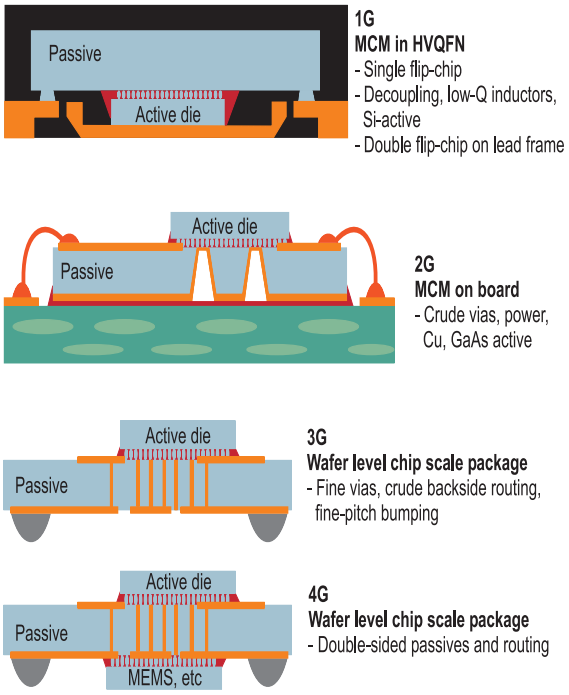


Fig. 6.6: Different generations of silicon-based SiP modules using $3D$ die stacking and packaging (source: Solid State Technology).

6.4 Summary

The current chapter has offered big future research challenges for the thesis advancement since the micro/nano-electronics area has been developed in such a way that the research from the well-known $CMOS$ down-scaling process could be translated to a more complex domain, in which the More-than-Moore technology diversification counts in order

to reach new system functionality like intelligent analog/RF, (bio)sensing, actuation micro/nano systems on chip (SoC) or in the package (SiP). In this context, following the Moore's law, the quantum effects in SOI devices ($DG\ SOI\ MOSFET$ in this thesis) have constituted a relevant research topic for the future work since they become significant as device miniaturization continues to scale down to several nm range. The system formed on Schrödinger equation and Poisson equation has created the possibility to build a quantum mechanical model which describes the quantization of the electron energy levels going to a new shape for the electron concentration distribution. The effort should be focused on the understanding and modeling the quantum effects in the silicon on insulator devices in order to obtain a pretty accurate analyses.

In addition, the trend given by "More than Moore" brings the three-dimensional $MEMS$ technology which gathers on the same chip hybrid technologies that realize complex interaction with people and environment. Also, the carbon nanotubes are expecting to be utilized in many applications due to their superior performances over the $MEMS$ devices.

Chapter 7

Conclusions

This dissertation has presented an one-dimensional compact analytical modeling of a novel symmetric Double-Gate $SOI\ MOSFET$ transistor, covering the dc and ac analyses. The adopted methodology offers a good characterization of the device in all regions of operation with the only assumptions of the light doping of the substrate and constant electron mobility. The model has been implemented in Verilog-A code and then, used in the circuits simulation. In addition, this work has emphasized the specific challenges of the analytical modelling for asymmetric $DG\ SOI\ MOSFET$ devices, where the complexity of the mathematical equations reaches its limits. Driven by the present scientific community effort to integrate the $RF\ MEMS$ vibrating components and the electronic circuits for getting one chip transceiver in the near future, within thin thesis we have combined the $DG\ SOI\ MOSFET$ circuits with $RF\ MEMS$ resonators for developing on-chip frequency generating functions. In this case, a disk $MEMS$ resonators acting as an RLC series circuit has been located in the positive feed-back loop of an amplifier in order to get an on-chip oscillator for GHz applications for future transceivers.

7.1 Results of Research Work

The continuous scaling-down process of the channel length over the last four decades is reaching its limits in terms of gate oxide thickness, short channel effects and power consumptions. The basic aspects of short channel effects and leakage mechanisms were described in Chapter 2 for a better understanding of the technology and design solutions envisaged by the scientific community to overcome them. Now, when we are closed to the end of $ITRS$ road-map, the dual gate $SOI\ MOSFET$ devices are expected to replace the bulk $MOSFET$ transistors for a better control of the entire device electrostatics. In parallel, Chapter 3 has offered a general overview on the state-of-the-art in the RF micro-electro-mechanical systems focusing on new frequency processing functions of the integrated micro-mechanical circuits. It has been shown that one of the long term targets of the $MEMS$ domain is the miniaturization of cell phones and other wireless applica-

tions, by integrating the expensive off-chip passive components. To make this happen, on-chip high Q components and functions which can be obtained with vibrating capacitive $RF\ MEMS$ are emerging, even in the GHz range. Within this thesis, it is for the first time when a model for designing an $RF\ MEMS$-based oscillator has been developed starting from an amplifier with a $DG\ SOI\ MOSFET$ transistor and an $RF\ MEMS$ resonator located in its positive feed-back loop. Such a design can be the starting point for the future ultra wide band oscillators serving to the realization of the next generation of low size/power/noise, fully integrated $DG\ SOI\ MOSFET$ transceivers for wireless applications.

To receive large acceptance, simple and efficient static and dynamic models of the multi-gate SOI devices should be developed and validated by experimental results. It has been the purpose of this thesis to show our contribution to the analytical modeling of un-doped asymmetrical and symmetrical $DG\ SOI\ MOSFET$ devices in the static and dynamic regime.

An original, simple and efficient analytical model has been proposed in this thesis for the calculation of the electrostatic potential from the central part of the silicon layer in the symmetric and asymmetric $DG\ SOI\ MOSFET$, starting from the analytical approach of Poisson's equation. Then, the distribution of the electrostatic potential in the silicon film was derived for both cases. Our procedure is based on original mathematical computations implemented in the Matlab code for solving the transcendental equation providing the minimum electrostatic potential in the middle of the silicon film. Our method could replace other complex approaches based on Lambert function and smoothing factor without physical meaning which were previously used for the same electrostatic potential computation. The mechanical quantum effects and short channel effects appeared in even this novel device were not studied in our analytical work. Continuing on the same direction, the electric inversion charge and drain current have been calculated by using our analytical model in the symmetrical $DG\ SOI\ MOSFET$ device, in order to obtain a complete DC behavior. It is necessary to mention that the silicon thickness of our novel device is of 20 nm, so that the volume inversion feature was analytically proved.

The thesis has introduced for the first time the idea of the asymmetry behavior of the symmetric $DG\ SOI\ MOSFET$ as a function of the applied channel voltage. The chapter 4 has shown that when the drain voltage is very small, the potentials at the front and back surfaces are distinct and, thus, the minimum electrostatic potential is not located anymore in the middle of the silicon film. Then, as the drain voltage increases, the entire silicon body is under the same potential in both situations considered above: pure symmetrical and asymmetrical behavior.

Another aspect treated in this work is the $1D$ analytical modeling for the electrostatic potential distribution in the very slightly doped silicon body of the asymmetric $DG\ SOI\ MOSFET$ devices. The asymmetry was supposed to be given by the different p or n type doping of the polysilicon gate electrodes. According to our model, the Poisson's equation could be analytically solved for the applied V_{GS} voltages higher than $0.5V$, by using

only electrons as charge carriers and boundary conditions given by the continuity of the electric displacement at the two interfaces and the presence of a minimum electrostatic potential in the silicon body. The proposed analytical methodology was fulfilled in two steps. In the first step, the coordinates of the minimum electrostatic potential were calculated, while in the second step the electrostatic potential distribution was obtained in the entire silicon film. We have demonstrated for the first time that, when the applied V_{GS} voltage varied from 0.5 V to 1 V, the minimum electrostatic potential was pinned at a value of about 0.459 V rather similar with the pinning phenomenon shown in the analytical modeling of symmetric $DG\ SOI\ MOSFET$. The coordinates of the above minimum allowed us to calculate the electrostatic potential distribution in the overall silicon body.

The dissertation has also proposed a small signal equivalent circuit for an un-doped symmetrical $DG\ SOI\ MOSFET$, starting from the assumption of the quasi-static operation. In this way, the device was completely evaluated in order to be further used in the circuits simulation. In accordance with the quasi-static operation, even if the terminal voltages are varying in time, the charges per unit area at any time are assumed to be identical to those obtained, if the dc voltages are used instead. In this context, the terminal charges and capacitances were calculated with our proposed analytical approach in order to complete the AC description.

The entire analytical model of an un-doped symmetrical $DG\ SOI\ MOSFET$, proposed in this thesis, was implemented in Verilog-A code in order to better support the compact device modeling and make it available for the circuits design. Our developed tool is seen as an extension of Spice code. The results obtained in this way are fitting perfectly those got by using Matlab program. Thus, the new obtained library has been used in Cadence.

An important result of this thesis is the pioneering work done for modeling and simulation a $RF\ MEMS$ based oscillator, where the amplifier was realized with $DG\ SOI\ MOSFET$ devices. A case study was defined where a $MEMS$ disk resonator has been described analytically and implemented in Matlab and its equivalent RLC-series electrical circuit has played the role of positive feedback in a $DG\ SOI\ MOSFET$-based oscillator. The perturbation method has been used in this dissertation in order to design the transient behavior of the oscillator and provide the stability conditions for it. Thus we could integrate our entire $DG\ SOI\ MOSFET$ analytical modeling into an original transistor libraries to be accessed by Cadence, as a starting point to define design tools for GHz applications. The static behavior of a common source amplifier has been designed by using the above constructed library of the novel $DG\ SOI\ MOSFET$ device.

7.2 Directions for DG SOI MOSFET Future Work at Device level

The analytical $DG\ SOI\ MOSFET$ model within the thesis provides a robust device description to be used in the design of future analog and digital circuits where the advantages of SOI devices over the bulk $MOSFET$ transistor can be exploited. Also, the $DG\ SOI\ MOSFET$ can be further developed as a technology platform for integrating electronics and $RF\ MEMS$ devices and circuits in order to obtain ultra small multifunctional systems on chip (SoC) or in the package (SiP) for the next generation of one-chip transceivers, as an example of market application.

Short Channel Effects in DG SOI MOSFET: The proposed analytical method of an un-doped symmetric and/or asymmetric $DG\ SOI\ MOSFET$ can be extended to include the short channel effects components. Even if they are drastically reduced by adopting a multiple-gate $SOI\ MOSFET$ as an alternative to replace the bulk $MOSFETs$, they are not completely eliminated, the $DIBL$ component providing the strongest leakage in such a novel device.

Quantum Effects in DG SOI MOSFET: The mechanical quantum effects that appeared, when the silicon thickness decreases below 10 nm, can be also assessed during the realization of an accurate method to model the dc and ac behavior of the $DG\ SOI\ MOSFET$. As it was explained in the chapter 6, the Schrödinger equation must be used besides the Poisson equation in order to begin the analytical modeling.

The entire model can be implemented in Verilog-A in order to make it accessible for the circuit design with Cadence.

Implementation of RF MEMS Devices in Verilog-A: Another research direction could be the implementation of the analytical model of more complex configuration of a $RF\ MEMS$ device and circuits in Verilog-A in order to provide an improved accuracy in the design of an $DG\ SOI\ MOSFET$- based oscillator and other frequency processing electro-mechanical blocks.

Phase Noise for a DG SOI MOSFET- and RF MEMS- based Oscillator: Since an oscillator presents the phase noise as its figure of merit, the thesis should be continued in the direction of a complete design of the used oscillator. This work gave a methodology to obtain the transient response for a $DG\ SOI\ MOSFET$- based oscillator that has an $RF\ MEMS$ disk resonator in its positive loop.

Appendix A

Micro-mechanical Systems

For a better understanding of the electrical behavior of the $RF\ MEMS$ vibrating resonators a brief background presentation of the time and frequency response of the systems of different orders is described below, where the order of the system is given by the number of elements able to store energy in that system, as follows.

A.1 Zero-Order Systems

These are the systems that are not able to store energy. This is the case of an electrical system represented by a simple electrical resistance. It is generally agreed that a zero order system represents an ideal situation, as even such a zero-order system may have parasitic components around them able to store energy, and this will happen mainly at a higher operation frequency.

A.1.1 Time Response for a Zero-Order System

A zero-order system is defined, mathematically, as a simple model which has $N = M = 0$. From the physics point of view, there is no element able to store energy in the system. In the case of the electrical system, a good example is a pure resistance, which may operate as a zero order system at low frequencies.

From equation 3.1, we obtain the following specific expression:

$$y(t) = \frac{b_0}{a_0} \cdot x(t) \tag{A.1}$$

where $k = \frac{b_0}{a_0} = constant$ is the gain or the sensitivity of the system. As shown in the equation $A.1$, for zero-order systems, in the time domain, the output signal is following the input signal without any distortion or delay. This is an ideal system.

A.1.2 Frequency Response for a Zero-Order System

The transfer function of zero-order system is obtained from the above expression, by applying the Laplace transform and is given below:

$$H(s) = \frac{Y(s)}{X(s)} = \frac{b_0}{a_0} = constant \tag{A.2}$$

From the above equation, we obtain a constant magnitude as a function of frequency which provides an infinite frequency bandwidth. Similarly, the argument of this transfer function is zero which means there is no phase delay between the output and the input.

A.2 First-Order Systems

A.2.1 Time Response for a First-Order System

From the physics point of view, a first-order model corresponds to a system which has only one element able to store energy. From the equation 3.1, when $N = 1$ and $M = 0$, we get the equation from below:

$$a_1 \cdot \frac{dy}{dt} + a_0 \cdot y(t) = b_0 \cdot x(t) \tag{A.3}$$

From simple calculations, we obtain the model equation as follows:

$$\tau \cdot \frac{dy}{dt} + y(t) = k \cdot x(t) \tag{A.4}$$

where $\tau = \frac{a_1}{a_0} = constant$ is the time constant of the system and $k = \frac{b_0}{a_0} = constant$ represents the dc gain or the sensitivity of the system.

If $x(t)$ is a step unit function, the response $y(t)$ of the first order-system is given below:

$$y(t) = k \cdot [1 - \exp(-\frac{t}{\tau})] \tag{A.5}$$

A.2.2 Frequency Response for a First-Order System

By applying the Fourier transform to the equation $A.5$, we obtain the frequency behavior as given by the following transfer function:

$$H(s) = \frac{Y(s)}{X(s)} = \frac{k}{1 + \tau \cdot s} \tag{A.6}$$

The magnitude and argument of the transfer function of the first-order system are given below:

$$|H(j\omega)| = \frac{k}{\sqrt{1 + (\tau \cdot \omega)^2}} \tag{A.7}$$

$$\phi(\omega) = -\arctan(\tau\omega) \tag{A.8}$$

As an example of first-order systems, we have an electrical circuit containing a capacitance and a resistance. Similarly, we might have a circuit consisting of an inductance and a resistance.

A.3 Second-Order Systems

A.3.1 Time Response for a Second-Order System

From the physics point of view, a second order system is modeled by a circuit which contains two elements able to store energy. For example, a second order mechanical system consists of a mass suspended by a spring to a fix point as shown in Figure $A.1$, while a second-order electrical system can be represented by an RLC series circuit.

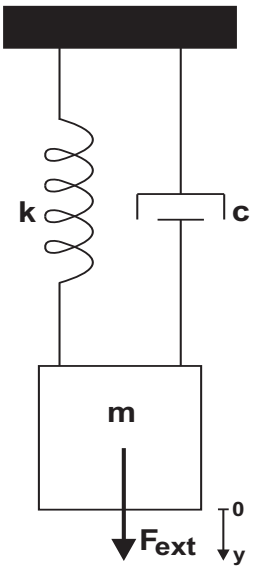


Fig. A.1: MEMS Resonator.

From the equation 3.1, where $N = 2$ and $M = 0$ one can obtain the expression that describes the dynamic behavior of a second order system.

$$a_2 \cdot \frac{d^2y}{dt^2} + a_1 \cdot \frac{dy}{dt} + a_0 \cdot y(t) = b_0 \cdot x(t) \tag{A.9}$$

The physical significance of the constants a_2, a_1 and a_0 can be calculated from Newton's law of motion applied to the system mass m spring from Figure $A.1$, in the presence

of damping force (equal to $c \cdot \frac{dy}{dt}$), when an external force F_{ext} acts in the y direction. Thus, we obtain the equation from below:

$$m \cdot \frac{d^2y}{dt^2} + c \cdot \frac{dy}{dt} + k \cdot y = F_{ext} \tag{A.10}$$

where k is the mechanical spring constant and c represents the damping coefficient.

The above equation can be written as a function of the resonant natural frequency $\omega_0 = \sqrt{\frac{k}{m}}$, the quality factor $Q = \frac{\omega_0 m}{c} = \frac{\sqrt{km}}{c}$, the critical damping coefficient $c_c = 2\sqrt{km}$ and the damping ratio $\xi = \frac{c}{c_c}$.

By solving the above equation, one can obtain the displacement of the inertial mass as a function of time for different values of damping ratio as follows:

Undamped oscillatory regime : $\xi = 0$

$$y(t) = A\cos(\omega_0 t) + B \cdot sin(\omega_0 t) + \frac{F_{ext}}{k} \tag{A.11}$$

Under-damped regime : $0 < \xi < 1$. In this case, the system is oscillating at a damped natural frequency $\omega_d = \omega_0 \cdot \sqrt{1-\xi^2}$ and with a decaying rate of $\exp(-\xi\omega_0 t)$.

$$y(t) = \exp(-\xi\omega_0 t)(C_1\cos(\omega_0\sqrt{1-\xi^2}t) + C_2 \cdot sin(\omega_0\sqrt{1-\xi^2}t)) + \frac{F_{ext}}{k} \tag{A.12}$$

Critically damped regime : $\xi = 1$. Its response makes the transition from the non-oscillatory over-damped response to the oscillatory motion.

$$y(t) = (M + N \cdot t) \cdot \exp(-\omega_0 t) + \frac{F_{ext}}{k} \tag{A.13}$$

Over-damped regime : $\xi > 1$. The response exhibits no overshoot or oscillation.

$$y(t) = P\exp(\lambda_1 t) + R\exp(\lambda_2 t) + \frac{F_{ext}}{k} \tag{A.14}$$

A.3.2 Frequency Response for a Second-Order System

From the equation $A.10$, by applying the Laplace transform, we obtain the transfer function and its components.

$$H(s) = \frac{Y(s)}{F_{ext}(s)} = \frac{1/k}{\frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1} \tag{A.15}$$

$$|H(j\omega)| = \frac{1/k}{\sqrt{(1-\frac{\omega^2}{\omega_0^2})^2 + (\frac{\omega}{Q\omega_0})^2}} \tag{A.16}$$

$$\phi(\omega) = -\arctan(\frac{\frac{\omega}{Q\omega_0}}{1-\frac{\omega^2}{\omega_0^2}}) \tag{A.17}$$

Appendix B

Matlab Code Support for Deriving Electrical Behavior of DG SOI MOSFET Device Related to Gate and Drain Voltage

The analytical modelling of a symmetric un-doped $DG\ SOI\ MOSFET$ device has been done in Chapter 4 from thesis and this approach started from the calculation of the Poisson's equation and, then, has continued with the derivation of its electrical static and dynamic characteristics. The entire procedure has depended on the following transcendental equation:

$$V_{GS} - \psi_0 = a \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot |\tan(z)| - \frac{2kT}{q} \cdot ln\{\cos(z)\} \tag{B.1}$$

from which the central silicon electrostatic potential was obtained. In this context, the surface electrostatic potential, inversion charge, drain current, transconductance, output conductance, terminal charges and capacitances were calculated as follows:

$$\psi_s = \psi_0 - \frac{2kT}{q} \cdot ln\{\cos[b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot \frac{t_{si}}{2}]\} \tag{B.2}$$

$$Q_{inv} = \sqrt{8\varepsilon_{Si} n_i kT} \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot \left|\tan(be^{\frac{q(\psi_0 - V)}{2kT}} \cdot \frac{t_{Si}}{2})\right| \tag{B.3}$$

$$I_D = \mu \cdot \frac{W}{L} \cdot \sqrt{8\varepsilon_{Si} n_i kT} \cdot \int_0^{V_{DS}} e^{\frac{q(\psi_0 - V)}{2kT}} \cdot \left|\tan(be^{\frac{q(\psi_0 - V)}{2kT}} \cdot \frac{t_{Si}}{2})\right| dV \tag{B.4}$$

$$g_m = 2\mu \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot [V_{DS} - \frac{\partial}{\partial V_{GS}}(\int_0^{V_{DS}} \psi_s(V)dV)] \tag{B.5}$$

$$g_{out} = 2\mu \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot [V_{GS} - \frac{\partial}{\partial V_{DS}}(\int_0^{V_{DS}} \psi_s(V)dV)] \tag{B.6}$$

$$Q_G = -W\int_0^L Q_{inv}(y)dy = -\mu W^2 \int_0^{V_{DS}} \frac{Q_{inv}^2(V)}{I_D}dV \tag{B.7}$$

$$Q_D = W\int_0^L \frac{y}{L}Q_{inv}(y)dy = \frac{WLt_{ox}}{2\epsilon_{ox}} \int_0^{V_{DS}} \frac{Q_{inv}^2(V)}{V_{GS}V - \int_0^V \psi_s(v)dv}dV \tag{B.8}$$

$$Q_S = Q_G - Q_D \tag{B.9}$$

$$C_{KK} = \frac{\partial q_K}{\partial v_K}|_{Q-point} \tag{B.10}$$

$$C_{KL} = -\frac{\partial q_K}{\partial v_L}|_{Q-point}; L \neq K \tag{B.11}$$

At this point, one can see that the numerical methods must be applied in order to obtain the dependencies of the above-mentioned coefficients as a function of gate and drain voltages and thus, Matlab codes were used for this purpose.

The appendix has two sections where the previous electrical parameters are going to be extracted from. Each program is providing the dependencies on gate and drain voltages, respectively. The used notations are as follows:
- minimum electrostatic potential in the central part of silicon film: $psi_{ovf} = f(V_{GS}, V_{DS})$;
- silicon surface electrostatic potential: $psi_s = f(V_{GS}, V_{DS})$;
- inversion charge: $Qi = f(V_{GS}, V_{DS})$;
- drain current: $Id = f(V_{GS}, V_{DS})$;
- trans-conductance: $g_m = f(V_{GS})$;
- output conductance: $god = f(V_{DS})$;
- terminal charges: $Q_g = f(V_{GS}, V_{DS})$, $Q_d = f(V_{GS}, V_{DS})$, $Q_s = f(V_{GS}, V_{DS})$;
- capacitances: $Cgg = f(V_{GS})$, $Csg = f(V_{GS})$, $Cdg = f(V_{GS})$, $Cdd = f(V_{DS})$, $Cgd = f(V_{DS})$, $Csd = f(V_{DS})$.

B.1 Matlab Code Support for Deriving Electrical Behavior of DG SOI MOSFET Device Related to Gate Voltage

```
%%%%%  The Calculation of the Silicon Central and Surface  %%%%%
%%%%%  Electrostatic Potentials, Inversion and Terminal  %%%%%
%%%%%  Charges, Drain Current, Transconductance and  %%%%%
%%%%%  Capacitances as a Function of Gate Voltage  %%%%%
```

```
%%%%%%%%   Constants:   %%%%%%%%

q = 1.6 * 10^-19; % Electric charge [C]
k = 1.3807 * 10^-23; % Boltzmann's constant [J/K]
T = 300; % Temperature [K]
eps_o = 8.8542 * 10^-12; % Vacuum permitivity [F/m]
eps_rsi = 11.7; % Relative permitivity of silicon
eps_si = eps_o * eps_rsi; % Silicon permitivity
eps_rox = 4; % Relative permitivity of $SiO_2$
eps_ox = eps_o * eps_rox; %Permitivity of $SiO_2$
t_si = 20 * 10^-9; % Silicon thickness [m]
t_ox = 2  * 10^-9; % Oxide thickness [m]
ni = 1.45 * 10^16; % Intrinsic concentration [m^3]
mu = 300 * 10^-4; % Electrons mobility [m^2/Vs]
W = 1e-6; % Channel's width [$\mu m$]
L = 1e-6; % Channel's length [$\mu m$]

a = t_ox/eps_ox * sqrt(2*k*T*eps_si*ni);
b = sqrt(q*q*ni/(2*eps_si*k*T));

const = sqrt(8 * eps_si * ni * k * T);
Qg_constant = -2*mu * W*W;
Qd_constant = mu*mu * W*W*W/(L);
ct = mu * W/L;
Cox = eps_ox/t_ox; % Oxide capacitance per unit area

%%%%%%%%   Code:   %%%%%%%%

Vg=0:0.05:2; % Gate to source voltage [V]
Vds=0:0.01:1.5; % Drain to source voltage [V]

for l = 1:length(Vg)
   Vgs = Vg(l);
   for i = 1:length(Vds)
   if (i==1)
      % Calculation of psi_o for a Vds = 0 V and Riemann's
      % sum for the first iteration:

      V = 0;
      psi_omax_0 = V + (2*k*T/q)*log(pi/(b*t_si)); % Maximum
        % value of the silicon central electrostatic potential
      psi_ox = 0:0.0001:psi_omax_0 ;
      deltaVds = 0.1; % The rate for Riemann sum
```

```
    for j = 1:length(psi_ox)
       z = psi_ox(j);
       f1(j) = Vgs - z;
       g1(j) = a*exp(q * (z-V)/(2*k*T)).* abs(tan(b*exp(q*(z-V)
               /(2*k*T))*t_si/2))-2*k*T/q*log(abs(cos(b*exp(q
               *(z-V)/(2*k*T))*t_si/2)));
       h1(j) = f1(j) - g1(j);
       if abs(h1(j)) <= 0.05
          psi_ov = z; % Minimum electrostatic potential obtained
                      % for the first iteration
       end
    end

    % Drain current for the first iteration:
    Id(l,i) = ct*deltaVds*exp(q*(psi_ov-V)/(2*k*T)).*abs(tan(b
              *exp(q*(psi_ov-V)/(2*k*T))*t_si/2))*const;

    % Silicon surface electrostatic potential for the first
    % iteration:
    psi_s(l,i) = psi_ov-(2*k*T/q)*log(cos(b*exp(q*(psi_ov-V)
                 /(2*k*T))*t_si/2));

    funct(l,i) = exp(q*(psi_ov-V)/(2*k*T)).*abs(tan(b*exp(q
                 *(psi_ov-V)/(2*k*T))*t_si/2));

    % Inversion charge for the first iteration:
    Qi(l,i) = const * funct(l,i);

    % Gate charge for the first iteration:
    Qg_num(l,i) = (Vgs-psi_s(l,i))*Qi(l,i)*deltaVds;
    Qg(l,i) = Cox * Qg_num(l,i)/Id(l,i);

    % Drain charge for the first iteration:
    F(l,i) = Qi(l,i) * deltaVds;
    Qd_num(l,i) = F(l,i)*Qi(l,i)*Qi(l,i) * deltaVds;
    Qd(l,i) = Qd_num(l,i)/(Id(l,i)*Id(l,i));

    % Source charge for the first iteration:
    Qs1_num(l,i) = Qi(l,i)*Qi(l,i) * deltaVds;
    Qs1(l,i) = Qg_constant * Qs1_num(l,i)/(2*Id(l,i));
    Qs(l,i) = Qs1(l,i) + Qd_constant * 2 * Qd(l,i);

else
    t = Vds(i);
    psi_omax = t + (2*k*T/q)*log(pi/(b*t_si));
```

```
psi_o = 0:0.0001:psi_omax;
for j = 1:length(psi_o)
   z = psi_o(j);
   f = Vgs - z;
   g = a*exp(q*(z-t)/(2*k*T))*abs(tan(b*exp(q*(z-t)
       /(2*k*T))*t_si/2))-2*k*T/q*log(cos(b*exp(q
       *(z-t)/(2*k*T))*t_si/2));
   h = f - g;
   if abs(h) <= 0.06
      psi_ovf(l,i) = z;
      V_ds(l,i)=t;

      % Silicon surface electrostatic potential:
      psi_s(l,i) = psi_ovf(l,i)-2*k*T/q *log(cos(b*exp(q
                  *(psi_ovf(l,i)-V_ds(l,i))/(2*k*T))
                  *t_si/2));

      % Drain current:
      funct(l,i)=exp(q* (psi_ovf(l,i)-V_ds(l,i))/(2*k*T))
                 *abs(tan(b*exp(q*(psi_ovf(l,i)-V_ds(l,i))
                 /(2*k*T))*t_si/2));
      Id(l,i) = Id(l,i-1)+funct(l,i)*deltaVds*const*ct;

      % Inversion Charge:
      Qi(l,i)= const *funct(l,i);

      % Gate charge:
      Qg_num(l,i) = Qg_num(l,i-1)+(Vgs-psi_s(l,i))*Qi(l,i)
                   *deltaVds;
      Qg(l,i) = Cox * Qg_num(l,i)/Id(l,i);

      % Drain charge:
      F(l,i) = F(l,i-1) + Qi(l,i) * deltaVds;
      Qd_num(l,i) = Qd_num(l,i-1)+F(l,i)*Qi(l,i)*Qi(l,i)
                   *deltaVds;
      Qd(l,i) = Qd_num(l,i)/(Id(l,i)*Id(l,i));

      % Source charge:
      Qs1_num(l,i) = Qs1_num(l,i-1)+Qi(l,i)*Qi(l,i)*deltaVds;
      Qs1(l,i) =Qg_constant * Qs1_num(l,i)/(2*Id(l,i));
      Qs(l,i) = Qs1(l,i) + Qd_constant * Qd(l,i);

      Q_g(l,i) = Qg_constant * Qg(l,i);   % Gate Charge
      Q_d(l,i) = Qd_constant * Qd(l,i);
   end
```

```
      end
   end
   end

Q_g = Qg_constant * Qg(:,101);
Q_d = Qd_constant * Qd(:,101);
Q_s = Qs(:,101);
end

%%%%%     Capacitances     %%%%%

for i=1:length(Q_g)
   if ( i==1 || i==2 )
      Cgg(i)=-(-Q_g(i+2)+4*Q_g(i+1)-3*Q_g(i))/(2*deltaVds);
   elseif( i>=3 & i<(length(Q_g)-1))
      Cgg(i)=-(-Q_g(i+2)+8*Q_g(i+1)-8*Q_g(i-1)+Q_g(i-2))/(12*deltaVds);
   elseif (i>=length(Q_g)-1)
      Cgg(i)=-(3*Q_g(i)-4*Q_g(i-1)+Q_g(i-2))/(2*deltaVds);
    end
end

for i=1:length(Q_d)
   if ( i==1 || i==2 )
      Cdg(i)=-(-Q_d(i+2)+4*Q_d(i+1)-3*Q_d(i))/(2*deltaVds);
   elseif( i>=3 & i<(length(Q_d)-1))
      Cdg(i)=-(-Q_d(i+2)+8*Q_d(i+1)-8*Q_d(i-1)+Q_d(i-2))/(12*deltaVds);
   elseif (i>=length(Q_d)-1)
      Cdg(i)=-(3*Q_d(i)-4*Q_d(i-1)+Q_d(i-2))/(2*deltaVds);
   end
end

for i=1:length(Q_s)
   if ( i==1 || i==2 )
      Csg(i)=-(-Q_s(i+2)+4*Q_s(i+1)-3*Q_s(i))/(2*deltaVds);
   elseif( i>=3 & i<(length(Q_s)-1))
      Csg(i)=-(-Q_s(i+2)+8*Q_s(i+1)-8*Q_s(i-1)+Q_s(i-2))/(12*deltaVds);
   elseif (i>=length(Q_s)-1)
      Csg(i)=-(3*Q_s(i)-4*Q_s(i-1)+Q_s(i-2))/(2*deltaVds);
   end
end

%%%%%    Representation of figures:    %%%%%

figure
   plot(Vg, psi_ovf(:,1), '-ks', Vg, psi_s(:,1), '-ko',...
```

```
                'LineWidth',1.25,...
                'MarkerEdgeColor','k ',...
                'MarkerFaceColor','r',...
                'MarkerSize',5); grid on
   xlabel('Gate voltage: V_{gs}(V)');
   ylabel('Electrostatic silicon potentials (V)');
   legend('Central silicon potential: psi_{o}(V)',
          'Surface silicon potential: psi_s(V)', 2);

figure
   plot(Vg, Qi(:,1), Vg, Qi(:,51), Vg, Qi(:,101), Vg, Qi(:,151));
   grid on
   legend('V_{DS} = 0 V','V_{DS} = 0.5 V','V_{DS} = 1 V',
          'V_{DS} = 1.5 V', 0);
   xlabel('Voltage to Source Voltage V_{DS} [V]');
   ylabel('Inversion Charge Q [C]');

figure
   plot(Vg, Id);
   xlabel('Gate voltage: V_{gs}(V)');
   ylabel('Electric drain current (A)');

figure
   plot(Vg, -Q_g, Vg, Q_d, Vg, -Q_s); legend('Qg','Qd','Qs',0);
   grid on
   xlabel('Gate to Source Voltage V_{DS} [V]');
   ylabel('Terminal Charge Q [C]');

figure
plot(Vg,Cgg/(10*Cox*W*L), Vg,-Cdg/(10*Cox*W*L), Vg,Csg/(10*Cox*W*L));
legend('C_{gg}','C_{dg}','C_{sg}',0);
xlabel('Gate to Source Potential V_{GS} (V)');
ylabel('Normalized Capacitances to C_{ox}WL');
```

B.2 Matlab Code Support for Deriving Electrical Behavior of DG SOI MOSFET Device Related to Drain Voltage

```
%%%%%  The Calculation of the Silicon Central and Surface  %%%%%
%%%%%  Electrostatic Potentials, Inversion and Terminal  %%%%%
%%%%%  Charges, Drain Current, Output Conductance, and  %%%%%
%%%%%  Capacitances as a Function of Drain Voltage  %%%%%
```

```
%%%%%%%%   Constant:   %%%%%%%%

q = 1.6 * 10^-19; % Electric charge [C]
k = 1.3807 * 10^-23; % Boltzmann's constant [J/K]
T = 300; % Temperature [K]
eps_o = 8.8542 * 10^-12; % Vacuum permitivity [F/m]
eps_rsi = 11.7; % Relative permitivity of silicon
eps_si = eps_o * eps_rsi; % Silicon permitivity
eps_rox = 4; % Relative permitivity of $SiO_2$
eps_ox = eps_o * eps_rox; %Permitivity of $SiO_2$
t_si = 20 * 10^-9; % Silicon thickness [m]
t_ox = 2  * 10^-9; % Oxide thickness [m]
ni = 1.45 * 10^16; % Intrinsic concentration [m^3]
mu = 300 * 10^-4; % Electrons mobility [m^2/Vs]
W = 1e-6; % Channel's width [$\mu m$]
L = 1e-6; % Channel's length [$\mu m$]

a = t_ox/eps_ox * sqrt(2*k*T*eps_si*ni);
b = sqrt(q*q*ni/(2*eps_si*k*T));

const = sqrt(8 * eps_si * ni * k * T);
Qg_constant = -2*mu * W*W;
Qd_constant = mu*mu * W*W*W/(L);
ct = mu * W/L;
Cox = eps_ox/t_ox; % Oxide capacitance per unit area

%%%%%%%%   Code:   %%%%%%%%

Vgs = 1; % Gate to source voltage [V]
Vds = 0:0.001:2; % Drain to source voltage [V]

for i = 1:length(Vds)
   if (i==1)
   % Calculation of psi_o for a Vds = 0 V and Riemann's sum for the
   % first iteration:

   V = 0;
   psi_omax_0 = V + (2*k*T/q)*log(pi/(b*t_si)); % Maximum value of
     % the silicon central electrostatic potential
   psi_ox = 0:0.0001:psi_omax_0;
   deltaVds = 0.001; % The rate for Riemann sum

   for j = 1:length(psi_ox)
      z = psi_ox(j);
```

```
   f1(j) = Vgs - z;
   g1(j) = a*exp(q*(z-V)/(2*k*T)).*abs(tan(b*exp(q*(z-V)/(2*k*T))
           *t_si/2))-2*k*T/q*log(abs(cos(b*exp(q*(z-V)/(2*k*T))
           *t_si/2)));
   h1(j) = f1(j) - g1(j);
   if abs(h1(j)) <= 0.1
      psi_ov = z; % Minimum electrostatic potential obtained for
                  % the first iteration
   end
end

% Drain current for the first iteration:
Id(i) = ct*deltaVds*exp(q*(psi_ov-V)/(2*k*T)).*abs(tan(b*exp(q
        *(psi_ov-V)/(2*k*T))*t_si/2))*const;

% Silicon surface electrostatic potential for the first iteration:
psi_s(i) = psi_ov-(2*k*T/q)*log(cos(b*exp(q*(psi_ov-V)/(2*k*T))
           *t_si/2));

funct(i) = exp(q*(psi_ov-V)/(2*k*T)).*abs(tan(b*exp(q*(psi_ov-V)
           /(2*k*T))*t_si/2));

% Inversion charge for the first iteration:
Qi(i) = const * funct(i);

% Gate charge for the first iteration:
Qg_num(i) = (Vgs - psi_s(i)) * Qi(i) * deltaVds;
Qg(i) = Cox * Qg_num(i)/Id(i);

% Drain charge for the first iteration:
F(i) = Qi(i) * deltaVds;
Qd_num(i) = F(i)*Qi(i)*Qi(i) * deltaVds;
Qd(i) = Qd_num(i)/(Id(i)*Id(i));

% Source charge for the first iteration:
Qs1_num(i) = Qi(i)*Qi(i) * deltaVds;
Qs1(i) = Qg_constant * Qs1_num(i)/(2*Id(i));
Qs(i) = Qs1(i) + Qd_constant * 2 * Qd(i);

else
   t = Vds(i);
   psi_omax = t + (2*k*T/q)*log(pi/(b*t_si));
   psi_o = 0:0.0001:psi_omax;
   for j = 1:length(psi_o)
      z = psi_o(j);
```

```
            f = Vgs - z;
            g = a*exp(q*(z-t)/(2*k*T))*abs(tan(b*exp(q*(z-t)
                /(2*k*T))*t_si/2))-2*k*T/q*log(cos(b*exp(q*(z-t)
                /(2*k*T))*t_si/2));
            h = f - g;
            if abs(h) <= 0.06
               psi_ovf(i) = z;
               V_ds(i)=t;

               % Silicon surface electrostatic potential:
               psi_s(i) = psi_ovf(i)-2*k*T/q*log(cos(b*exp(q
                         *(psi_ovf(i)-V_ds(i))/(2*k*T))*t_si/2));

               % Drain current:
               funct(i)=exp(q*(psi_ovf(i)-V_ds(i))/(2*k*T))*abs(tan(b
                        *exp(q*(psi_ovf(i)-V_ds(i))/(2*k*T))*t_si/2));
               Id(i) = Id(i-1) + funct(i)*deltaVds*const *ct;

               % Inversion charge:
               Qi(i)= const *funct(i);

               % Gate charge:
               Qg_num(i) = Qg_num(i-1)+(Vgs-psi_s(i))*Qi(i)*deltaVds;
               Qg(i) = Cox * Qg_num(i)/Id(i);

               % Drain charge:
               F(i) = F(i-1) + Qi(i) * deltaVds;
               Qd_num(i) = Qd_num(i-1) + F(i)*Qi(i)*Qi(i) * deltaVds;
               Qd(i) = Qd_num(i)/(Id(i)*Id(i));

               % Source charge:
               Qs1_num(i) = Qs1_num(i-1) + Qi(i)*Qi(i) * deltaVds;
               Qs1(i) =Qg_constant * Qs1_num(i)/(2*Id(i));
               Qs(i) = Qs1(i) + Qd_constant * Qd(i);
            end
         end
      end
   end
end

Q_g = Qg_constant * Qg;
Q_d = Qd_constant * Qd;

% Calculation of capacitances and output conductance:

for i=1:length(Q_g)
```

```
    if ( i==1 || i==2 )
        Cgd(i)=-(-Q_g(i+2)+4*Q_g(i+1)-3*Q_g(i))/(2*deltaVds);
        Cdd(i)=-(-Q_d(i+2)+4*Q_d(i+1)-3*Q_d(i))/(2*deltaVds);
        Csd(i)=-(-Qs(i+2)+4*Qs(i+1)-3*Qs(i))/(2*deltaVds);
        god(i)=(-Id(i+2)+4*Id(i+1)-3*Id(i))/(2*deltaVds);
    elseif( i>=3 & i<(length(Q_g)-1))
        Cgd(i)=-(-Q_g(i+2)+8*Q_g(i+1)-8*Q_g(i-1)+Q_g(i-2))
               /(12*deltaVds);
        Cdd(i)=-(-Q_d(i+2)+8*Q_d(i+1)-8*Q_d(i-1)+Q_d(i-2))
               /(12*deltaVds);
        Csd(i)=-(-Qs(i+2)+8*Qs(i+1)-8*Qs(i-1)+Qs(i-2))
               /(12*deltaVds);
        god(i)=(-Id(i+2)+8*Id(i+1)-8*Id(i-1)+Id(i-2))
               /(12*deltaVds);
    elseif (i>=length(Q_g)-1)
        Cgd(i)=-(3*Q_g(i)-4*Q_g(i-1)+Q_g(i-2))/(2*deltaVds);
        Cdd(i)=-(3*Q_d(i)-4*Q_d(i-1)+Q_d(i-2))/(2*deltaVds);
        Csd(i)=-(3*Qs(i)-4*Qs(i-1)+Qs(i-2))/(2*deltaVds);
        god(i)=(3*Id(i)-4*Id(i-1)+Id(i-2))/(2*deltaVds);
    end
end

%%%%%    Representation of figures:    %%%%%

figure
   plot(Vds, psi_ovf, '-ks', Vds, psi_s, '-ko',...
               'LineWidth',1.25,...
               'MarkerEdgeColor','k ',...
               'MarkerFaceColor','r',...
               'MarkerSize',5); grid on
   xlabel('Drain voltage: V_{ds}(V)');
   ylabel('Electrostatic silicon potentials (V)');
   legend('Central silicon potential: psi_{o}(V)', 'Surface
          silicon potential: psi_s(V)', 2);

figure
   plot(Vds, Id); legend('V_{GS} = 1V')
   xlabel('Drain voltage: V_{ds}(V)');
   ylabel('Electric drain current (A)');

figure
   plot(Vds, god);
   xlabel('Drain to Source Voltage V_{DS} [V]');
   ylabel('Output Conductance g_{out} [S]');
```

```
figure
   plot(Vds, -Q_g, Vds, Q_d, Vds, -Qs);
   legend('Q_g','-Q_d','-Q_s',0); grid on
   xlabel('Drain to Source Voltage V_{DS} [V]');
   ylabel('Terminal Charge Q [C]');

figure
   plot(Vds,-Cgd/(2*Cox*W*L),Vds,Cdd/(2*Cox*W*L),Vds,
        -Csd/(2*Cox*W*L));
   legend('Cgd','Cdd', '-Csd', 0); grid on
   xlabel('Drain to Source Voltage V_{DS} [V]');
   ylabel('Capacitance (Normalized to C_{ox}WL)');
```

Appendix C

Verilog A Description of The Static Electrical Characteristics of an Un-doped Symmetric DG SOI MOSFET Device

This Appendix reveals a code written in Verilog A which is capable to provide the electrical behaviour of our un-doped symmetric $DG\ SOI\ MOSFET$. The code offers the possibility to characterize the novel device starting from the calculation of the electrostatic potentials and continuing with the derivation of the charges, drain current, conductances and capacitances in a similar manner with the one used in Matlab. In comparison with Matlab code, the obtained code in Verilog A is a library that can be used in the background of Cadence for further design of the analog and/or digital circuits. In the structure of the Verilog A code, one can see the usage of an instruction called "module Analyses(G,S,D)". Its role is to show the number of terminals of the created symbol which is used in further simulations. Since it is about a symmetrical $DG\ SOI\ MOSFET$ device, only three terminals (gate, drain, source) are going to be utilized in the obtained symbol from Cadence in order to describe the electrical characteristics of it.

The notations used in Verilog A code are in terms of:
- minimum electrostatic potential in the central part of silicon film: $psi_{ovf} = f(V_{GS}, V_{DS})$;
- silicon surface electrostatic potential: $psi_s = f(V_{GS}, V_{DS})$;
- inversion charge: $Qi = f(V_{GS}, V_{DS})$;
- drain current: $Id = f(V_{GS}, V_{DS})$;
- trans-conductance: $g_m = f(V_{GS}, V_{DS})$;
- output conductance: $god = f(V_{GS}, V_{DS})$;
- terminal charges: $Q_g = f(V_{GS}, V_{DS})$, $Q_d = f(V_{GS}, V_{DS})$, $Q_s = f(V_{GS}, V_{DS})$;
- capacitances: $Cgg = f(V_{GS}, V_{DS})$, $Csg = f(V_{GS}, V_{DS})$, $Cdg = f(V_{GS}, V_{DS})$, $Cdd = f(V_{GS}, V_{DS})$, $Cgd = f(V_{GS}, V_{DS})$, $Csd = f(V_{GS}, V_{DS})$.

```
// VerilogA for DG_MOSFET, Analyses, veriloga
```

```
‘include "constants.h"
‘include "disciplines.h"

module Analyses(G,S,D,psio,psis,Qgd,Qdd,Qsd,CCgd,CCdd,CCsd,ggout);
inout G,S,D,psio,psis,Qgd,Qdd,Qsd,CCgd,CCdd,CCsd,ggout;
electrical G,S,D,psio,psis,Qgd,Qdd,Qsd,CCgd,CCdd,CCsd,ggout;

  // Physical Constants:
parameter real q = 1.6e-19;  // C
parameter real Eps0 = 8.854187878e-12;  // F/m
parameter real Epssi = 11.7 * Eps0;
parameter real Epsox = 4 * Eps0;
parameter real ni = 1.45e16; // m-3
parameter real k = 1.380658e-23;  // J/K
parameter real pi = 3.1416;

  // Geometry:
parameter real W = 1e-6;  // Gate Wifth [m]
parameter real L = 1e-6;  // Gate Length [m]
parameter real t_ox = 2e-9;  // Gate Oxide Thickness [m]
parameter real t_si = 20e-9;  // Silicon Film Thickness [m]
parameter real mu =  300e-4;  // Low Field Mobility [m^2/Vs]
parameter real Rds = 1e12; // Resistance between drain and source
                           // [Ohm] -- it is used to eliminate
                           // the homotopy error

  // Operating Conditions:
parameter real T = 300;
parameter real V_FB = 0;  // Flat-Band Voltage [V]
parameter real deltaVds = 0.001;
parameter real deltaVgs = 0.001;

 // Parameters:
real     vds , vgs, vd , vs , vg , psi_omax, psi_omaxm, psi_ov,
         psi_ovf, psi_ox, psi_s, psi_o, psi_s1;
real     f, f1, g, g1, h, h1, t, t1, z, z1, funct, funct1;
real     V_ds, V1, dv_ds, max_step;
real     Qi, Q_g, Qs, Q_d, Qg, Qd, Qg1, Qg2, Qd1, Qd2, Qs1, Qs2,
         Qs11, Qg_num, Qd_num, Qs1_num;
real     Cgd, Cdd, Csd, Cox, gout;
real     a, b, const, ct, Qg_constant, Qd_constant, ix;
real     Id, Id2, Id1, F1;

analog begin
```

```
  // Derived Parameters:
a = (t_ox/Epsox) * sqrt(2.0*k*T*Epssi*ni);
b = sqrt(q*q*ni/(2*Epssi*k*T));
Cox = Epsox/t_ox;  // Gate Oxide Capacitance
const = sqrt(8 * Epssi * ni * k * T); // without mobility and
                                 // geometry parameters L and W
ct = mu * W/L;
Qg_constant = -2.0 * mu * W * W;
Qd_constant = mu * mu * W*W*W/(L);
psi_omaxm = (2.0*k*T/q)*ln(pi/(b*t_si));

   vd  = V(D);  // Drain Potential
   vg = V(G);   // Gate Potential
   vs = V(S);   // Source Potential
   vds = vd-vs; // Drain to Source Voltage
   vgs = vg-vs; // Gate to Source Voltage

  // Thermodynamic Equilibrium:

V1=0;

for (psi_ox=0.0 ; psi_ox<=psi_omaxm ; psi_ox=psi_ox+0.0001) begin
   z1 = psi_ox;
   f1 = vgs - z1;
   g1= a*exp(q*(z1-V1)/(2.0*k*T))*abs(tan(b*exp(q*(z1-V1)
       /(2.0*k*T))*t_si/2.0))-2.0*k*T/q*ln(abs(cos(b*exp(q
       *(z1-V1)/(2.0*k*T))*t_si/2.0)));
   h1 = f1 - g1;

   if (abs(h1) <= 0.05) psi_ov = z1;
   end

   psi_s1 = psi_ov-(2.0*k*T/q)*ln(cos(b*exp(q*(psi_ov-V1)/(2.0*k*T))
            *t_si/2.0));
   Id = ct*const*deltaVds*exp(q*(psi_ov-V1)/(2.0*k*T))*abs(tan(b
        *exp(q*(psi_ov-V1)/(2.0*k*T))*t_si/2.0));
   funct1 = exp(q*(psi_ov-V1)/(2.0*k*T))*abs(tan(b*exp(q*(psi_ov
            -V1)/(2.0*k*T))*t_si/2.0));

   Qi = const * funct1;

   // Gate Charge Calculation:
   Qg_num = (vgs - psi_s1) * Qi * deltaVds;
   Qg = Cox * Qg_num/Id;
```

```
Q_g = Qg_constant * Qg;

// Drain Charge Calculation:
F1 = Qi * deltaVds;
Qd_num = F1 * Qi * Qi * deltaVds;
Qd = Qd_num/(Id*Id);
Q_d = Qd_constant * Qd;

// Source Charge Calculation:
Qs1_num = Qi * Qi * deltaVds;
Qs1 = Qg_constant * Qs1_num/(2.0*Id);
Qs = Qs1 + Qd_constant * 2.0 * Qd;

// Thermodynamic Non-Equilibrium:

for(dv_ds=0.001; dv_ds<= vds; dv_ds=dv_ds+deltaVds) begin
   t1 = dv_ds;
   psi_omax = t1 + psi_omaxm;
   for (psi_o=0 ; psi_o <=psi_omax ; psi_o = psi_o+0.0001)
      begin
       z = psi_o;
       f = vgs - z;
       g = a*exp(q*(z-t1)/(2.0*k*T))*abs(tan(b*exp(q*(z-t1)
           /(2.0*k*T))*t_si/2.0))-2.0*k*T/q*ln(abs(cos(b
           *exp(q*(z-t1)/(2.0*k*T))*t_si/2.0)));
       h = f - g;
       if (abs(h) <= 0.05)begin
          psi_ovf = z;
          V_ds=t1;
       end
       psi_s = psi_ovf-((2.0*k*T)/q)*ln(cos(b*exp(q
               *(psi_ovf-V_ds)/(2.0*k*T)) * t_si/2.0));
       funct = exp(q*(psi_ovf-V_ds)/(2.0*k*T))*abs(tan(b
               *exp(q*(psi_ovf-V_ds)/(2.0*k*T)) * t_si/2.0));
       Id = Id + funct*deltaVds*const*ct;

       Qi= const *funct;

       // Gate Charge Calculation:
       Qg_num = Qg_num + (vgs - psi_s) * Qi * deltaVds;
       Qg = Cox * Qg_num/Id;
       Q_g = Qg_constant * Qg;

       // Drain Charge Calculation:
       F1 = F1 + Qi * deltaVds;
```

```
            Qd_num = Qd_num + F1*Qi*Qi * deltaVds;
            Qd = Qd_num /(Id*Id);
            Q_d = Qd_constant * Qd;

            // Source Charge Calculation:
            Qs1 =Qg_constant * Qs1_num/(2.0*Id);
            Qs = Qs1 + Qd_constant * Qd;
         end

         max_step=floor(t1/deltaVgs);
         if(ix==(max_step-2)) begin
            Qg2=Q_g;
            Qd2=Q_d;
            Qs2=Qs;
            Id2=Id;
         end
         if(ix==(max_step-1)) begin
            Qg1=Q_g;
            Qd1=Q_d;
            Qs11=Qs;
            Id1=Id;
         end
      end

    // Calculation of capacitances and output conductance:

      Cdd = -(3.0*Q_d-4.0*Qd1+Qd2)/(2.0*deltaVds);
      Cgd = -(3.0*Q_g-4.0*Qg1+Qg2)/(2.0*deltaVds);
      Csd = -(3.0*Qs-4.0*Qs11+Qs2)/(2.0*deltaVds);
      gout  = (3.0*Id-4.0*Id1+Id2)/(2.0*deltaVds);

    // Representation of Figures:

      I(D,S) <+ -Id - vds/Rds;
      I(Qgd) <+ Q_g;
      I(Qdd) <+ -Q_d;
      I(Qsd) <+ Qs;
      I(CCgd)<+ -Cgd /(Cox*W*L);
      I(CCdd)<+ Cdd /(Cox*W*L);
      I(CCsd)<+ Csd /(Cox*W*L);
      I(ggout) <+ -gout-1/Rds;
      I(psio) <+ psi_ov;
      I(psis) <+ psi_s;
  end
  endmodule
```

Appendix D

Perturbation Method for The Analysis and Design of Transient and Steady-State Regimes in Electronic Oscillators

The appendix provides an asymptotic perturbation method for the analysis of the transient and steady state oscillations in the third order oscillators with shifting bias [12, 13]. In simple words, we deal with electronic oscillators, whose operation is determined by three dominant passive components able to store energy and where the initial dc bias voltage of the circuit is shifted by an additional stable dc voltage generated by the oscillator. In agreement with the theory of the third order systems, let us consider that they are described by the non-linear differential equation:

$$N(D)x = \epsilon M(D)f(x) \tag{D.1}$$

in which

$$N(D) = \frac{d^3}{dt^3} + \epsilon a\frac{d^2}{dt^2} + b\frac{d}{dt} + \epsilon c \tag{D.2}$$

$$M(D) = k_2\frac{d^2}{dt^2} + \epsilon k_1\frac{d}{dt} + k_0 \tag{D.3}$$

In the relation $(D.1)$, x is a controlling variable of the non-linear active device with its response, $f(x)$ ($f(0) = 0$), D represents the derivative operator with respect to time and ϵ denotes the non-dimensional perturbation parameter of the oscillator, expressing circuit losses and being given by the $1/Q$, with Q as quality factor of the loop. In the above equation, the parameters a and c are assumed to be constant while b has the following form:

$$b(\epsilon) = b_0 + b_1\epsilon + b_2\epsilon^2 + ... \tag{D.4}$$

$$b_0 = 1 \tag{D.5}$$

This perturbation method allows us to develop a behavioral time-domain analytical model that describes both the transient and the steady state regime of the circuit response, and thus to obtain a straightforward design methodology for deriving the start-up duration, the stabilized frequency and amplitude values. The advantage of the method consists in the fact that the oscillation solution can be built iteratively to the degree of accuracy required by the application, by increasing the order of approximation from the first order to higher orders of ϵ, and also considering not only the fundamentals but also superior harmonic components, when needed. Thus, in a generic form, the oscillator solution can be written as follows:

$$x(t,\epsilon) = B(t,\epsilon) + A(t,\epsilon)cos(\nu) + \epsilon h(\nu,\epsilon) \tag{D.6}$$

$$\frac{d\nu}{dt} = \omega \tag{D.7}$$

where B is the dc component, A is the amplitude of the fundamental harmonic, h is the content of superior harmonics, and ω is the angular frequency. The essence of the approach is that all these solution elements (B, A, ω) are written in the form of power series as a function of perturbation parameter, ϵ.

Within this perturbation approach, the method of complex amplitudes is used, where a time-domain oscillation solution written in the imaginary space is forced for the equation $(D.1)$ and finally the real solution is extracted as follows:

$$x(\nu,\epsilon) = Re[B + Ae^{j\nu} + \sum_m H_m e^{jm\nu}] \tag{D.8}$$

where

$$B = B_0 + B_1\epsilon + B_2\epsilon^2 + ... \tag{D.9}$$

$$A = A_0 + A_1\epsilon + A_2\epsilon^2 + ... \tag{D.10}$$

$$H_m = H_{m,1}\epsilon + H_{m,2}\epsilon^2 + ... \tag{D.11}$$

and

$$\nu = \int_0^t \omega dt \tag{D.12}$$

$$\tau = \epsilon t \tag{D.13}$$

$$\omega = \omega_0 + \omega_1\epsilon + \omega_2\epsilon^2 + ... \tag{D.14}$$

One can remark that the coefficients of the power series in ϵ for A, B, H_m and ω are considered to be functions of the slow variable $\tau = \epsilon t$. This means that the time derivative should be carefully performed for solving the equation $(D.1)$ with the proposed solution $(D.8)$. For example, $\frac{d\omega}{dt} = \frac{d\omega}{d\tau}\frac{d\tau}{dt} = \epsilon\frac{d\omega}{d\tau}$. Further, the appendix deals with the calculation of the complete solution of the equation $(D.1)$ in the form of $(D.8)$.

The complex function $f(x)$ can be also written as a power series expansion and it has the following form:

$$f(x) = f(x_0 + \epsilon x_1 + \epsilon^2 x_2 + ...) = f_0 + \epsilon f_1 + \epsilon^2 f_2 + ... \tag{D.15}$$

where the real coefficients f_n are 2π periodic in the variable ν and developed as Fourier series:

$$f_n = Re[F_{0,n}(\tau) + F_{1,n}(\tau)e^{j\nu} + \sum_{m\geqslant 2} F_{m,n}(\tau)e^{jm\nu}], n \geqslant 0 \tag{D.16}$$

$$F_{m,n} = \frac{1}{\pi}\int_0^{2\pi} f_n e^{-j\nu} d\nu \tag{D.17}$$

$$F_{0,n} = \frac{1}{2\pi}\int_0^{2\pi} f_n d\nu \tag{D.18}$$

The last above two relations are based on the supposition that the functions f_n and $f_n e^{-j\nu}$ do not significantly change in τ.Thus, $f(x)$ in the real domain becomes:

$$f(x) = Re[F_0 + F_1 e^{j\nu} + \sum_{m\geqslant 2} F_m e^{jm\nu}] \tag{D.19}$$

where

$$F_0 = F_{0,0} + F_{0,1}\epsilon + F_{0,2}\epsilon^2 + ... \tag{D.20}$$

$$F_1 = F_{1,0} + F_{1,1}\epsilon + F_{1,2}\epsilon^2 + ... \tag{D.21}$$

$$F_m = F_{m,0} + F_{m,1}\epsilon + F_{m,2}\epsilon^2 + ... \tag{D.22}$$

At the end of this entire analysis, one can see that the Equation $(D.1)$ can be rearranged as follows:

$$N(D)[B(\tau) + A(\tau)e^{j\nu} + \sum_{m\geqslant 2} H_m(\tau)e^{jm\nu}] = \epsilon M(D)[F_0(\tau) + F_1(\tau)e^{j\nu} + \sum_{m\geqslant 2} F_m(\tau)e^{jm\nu}] \tag{D.23}$$

After performing all the described calculations, within the perturbation method, the solution of the third order oscillators with shifting bias can be derived for any order of

approximation and harmonics as needed. Thus, the final form of equation $(D.1)$ can be obtained by equating the right members of the equations from below:

$$\begin{aligned}
N(D)[B(\tau)+A(\tau)e^{j\nu}+\sum_{m\geqslant 0}H_m(\tau)e^{jm\nu}] &= \epsilon^3[\frac{d^3B(\tau)}{d\tau^3}+a\frac{d^2B(\tau)}{d\tau^2}\\
&+e^{j\nu}(\frac{d^3A(\tau)}{d\tau^3}+a\frac{d^2A(\tau)}{d\tau^2})+\sum_{m\geqslant 2}e^{jm\nu}(\frac{d^3H_m(\tau)}{d\tau^3}+a\frac{d^2H_m(\tau)}{d\tau^2})]\\
&+\epsilon^2[e^{j\nu}(3j\omega\frac{d^2A(\tau)}{d\tau^2}+(2aj\omega+3j\frac{d\omega(\tau)}{d\tau})\frac{dA(\tau)}{d\tau}+j\frac{d^2\omega(\tau)}{d\tau^2}A(\tau))\\
&+\sum_{m\geqslant 2}e^{jm\nu}(3jm\omega\frac{d^2H_m(\tau)}{d\tau^2}+(2ajm\omega+3jm\frac{d\omega(\tau)}{d\tau})\frac{dH_m(\tau)}{d\tau}+jm\frac{d^2\omega(\tau)}{d\tau^2}H_m(\tau))]\\
&+\epsilon[b\frac{dB(\tau)}{d\tau}+cB(\tau)+e^{j\nu}((3j^2\omega^2+b)\frac{dA(\tau)}{d\tau}+(3j^2\omega\frac{d\omega(\tau)}{d\tau}+aj^2\omega^2)A(\tau)+cA(\tau))\\
&+\sum_{m\geqslant 2}e^{jm\nu}((3j^2m^2\omega^2+b)\frac{dH_m(\tau)}{d\tau}+(3j^2m^2\omega\frac{d\omega(\tau)}{d\tau}+aj^2m^2\omega^2)H_m(\tau)+cH_m(\tau))]\\
&+(j^3\omega^3A(\tau)+bj\omega A(\tau)+\sum_{m\geqslant 2}(j^3m^3\omega^3H_m(\tau)+bjm\omega H_m(\tau))) \quad \text{(D.24)}
\end{aligned}$$

$$\begin{aligned}
\epsilon M(D)\sum_{m\geqslant 0}(F_me^{jm\nu}) &= \sum_{m\geqslant 0}e^{jm\nu}[\epsilon^3(k_2\frac{d^2F_m(\tau)}{d\tau^2}+k_1\frac{dF_m(\tau)}{d\tau})+\epsilon^2(2k_2jm\omega\frac{dF_m(\tau)}{d\tau}\\
&+k_2jm\frac{d\omega(\tau)}{d\tau}+k_1jm\omega)+\epsilon(k_0-k_2m^2\omega^2)] \quad \text{(D.25)}
\end{aligned}$$

One can remark that the initial behavioral third-order differential equation written in the time domain, t, was translated to a time domain differential third order equation as a function of slow time, τ, where $\tau=\epsilon t$.

The above equation can take different forms as a function of desired values for ϵ and m, i.e, respectively, the order of approximation (power of ϵ terms) and the harmonics required. Further, the zero, first order and second approximations are going to be explained in detail.

D.1 Zero-order Approximation

According to the zero-order approximation, the perturbation parameter ϵ is zero and the coefficients used in the relation $(D.1)$ are the following:

$$B(\tau) = B_0(\tau) \tag{D.26}$$
$$A(\tau) = A_0(\tau) \tag{D.27}$$
$$H_m(\tau) = 0 \tag{D.28}$$
$$F_0(\tau) = F_{0,0}(\tau) \tag{D.29}$$
$$F_1(\tau) = F_{1,0}(\tau) \tag{D.30}$$
$$b = b_0 \tag{D.31}$$
$$\omega = \omega_0 \tag{D.32}$$

and the final equation $(D.1)$ becomes:

$$j\omega_0(b_0 - \omega_0^2)A_0 e^{j\nu} = 0 \tag{D.33}$$

From the above expression, we get:

$$b_0 = \omega_0^2 \tag{D.34}$$
$$\omega_0(\tau) = 1 \tag{D.35}$$

The last equation should be interpreted like this: In an ideal system (without losses, $\epsilon = 0$), the fundamental frequency is the only present component during the transient regime, and its value cannot be changed. Actually, for non-ideal, realistic system (with losses and where $\epsilon \neq 0$), the fundamental harmonic will be perturbed as shown by the results obtainedfor the higher order of approximations.

D.2 First-order Approximation

In order to analyze the first order approximation, only the terms with zero power of epsilon and those with first power of epsilon will be used. With this condition, the terms of the overall equation $(D.1)$ will take the following form:

$$B(\tau) = B_0(\tau) + B_1(\tau)\epsilon \tag{D.36}$$
$$A(\tau) = A_0(\tau) + A_1(\tau)\epsilon \tag{D.37}$$
$$H_m(\tau) = H_{m,1}(\tau)\epsilon \tag{D.38}$$
$$F_0(\tau) = F_{0,0}(\tau) + F_{0,1}(\tau)\epsilon \tag{D.39}$$
$$F_1(\tau) = F_{1,0}(\tau) + F_{1,1}(\tau)\epsilon \tag{D.40}$$
$$b = b_0 + b_1\epsilon \tag{D.41}$$
$$\omega = \omega_0 + \omega_1\epsilon \tag{D.42}$$

At this point, both dc component and fundamental harmonic can be calculated. So that, when $m = 0$, the time dependence of the dc component is given by the following differential equation:

$$b_0 \frac{dB_0}{d\tau} + cB_0 = k_0 F_{0,0} \tag{D.43}$$

while, for $m = 1$, the (slow) time dependence of the amplitude A_0 of the fundamental harmonic can be derived from the equation $(D.1)$, as follows:

$$e^{j\nu}(-3\omega^2 \frac{dA_0}{d\tau} - 3\omega \frac{d\omega}{d\tau} A_0 - j\omega^3 A_1 - a\omega^2 A_0 + b_0 \frac{dA_0}{d\tau} + j\omega b_0 A_1 + j\omega b_1 A_0 + cA_0) \\ + b_0 \frac{dB_0}{d\tau} + cB_0 = e^{j\nu}(k_0 - k_2\omega^2)F_{1,0} + k_0 F_{0,0} \tag{D.44}$$

and the differential equation of the fundamental harmonic differential equation is:

$$-2\omega_0^2 \frac{dA_0}{d\tau} + (c - a\omega_0^2)A_0 = (k_0 - k_2\omega_0^2)F_{1,0} \tag{D.45}$$

By arranging the relations $(D.43)$ and $(D.45)$, a system of non-linear first-order differential equations in τ are derived and, thus $B_0(\tau)$ and $A_0(\tau)$ can be determined:

$$\frac{dB_0}{d\tau} = -c(B_0 + k_{0c}F_{0,0}) \tag{D.46}$$

$$\frac{dA_0}{d\tau} = \frac{c}{2}[k_{0c}(1 - k_{20})F_{1,0} - pA_0] \tag{D.47}$$

where $b_0 = \omega_0^2 = 1$, $k_{0c} = -\frac{k_0}{c}$, $k_{20} = \frac{k_2}{k_0}$ and $p = \frac{a}{c} - 1$.

If $m > 1$, the higher harmonics amplitudes for the first order approximation are going to be obtained as follows:

$$H_{m,1} = j\frac{k_0 - k_2 m^2}{m(m^2 - 1)} F_{m,0} \tag{D.48}$$

One can remark the non-linearity property of the above first-order differential equations in B_0 and A_0, characterizing respectively the time evolution of the dc component and the fundamental harmonic of the oscillator within its first order approximation. The bottom line of the entire oscillator operation is the fact that, when powered ON (at $t = 0$), the system should be in unstable equilibrium state ($B_0 = A_0 = 0$). If it is well designed, it will evaluate toward an equilibrium stable state ($B_0^* \neq 0$, $A_0^* \neq 0$) established at the end of this so-called start-up time. Therefore, the design of the third order oscillator with shifting bias described by the first order approximation should arise from imposing to the above first-order differential equation system in A_0 and B_0 to be unstable in the time

origin and stable at the steady state, after the start up time (when the so-called limit cycle is reached). Fortunately, Lyapunov has developed the mathematical background of stability for the systems described by the non-linear first order differential equation system. Here, we have to understand that if the equation system is stable then the physical system (in our case the oscillator) described by those equations is stable. Actually, Lyapunov stated that if the linearized system derived from a non-linear system is stable, then the initial non-linear system is also stable. Similarly, if the linearized equation system derived from a non-linear equation system is unstable, then the initial non-linear equation system is unstable. Lyapunov's first method is also saying that a linearized differential equation system is stable if the eigenvalues of the Jacobian matrix associated to the linearized equation system are either negative or with negative real parts. This condition of negative eigenvalues should be applied for the deriving the stable values of the dc component and fundamental amplitude of the oscillator. Similarly, according to this first method of Lyapunov, if the eigenvalues of the Jacobian matrix of the linearized equation system are either positive or with real parts, then the equation system is unstable, and so it is the physical system (in our case the oscillator). This condition of positive eigenvalues of Jacobian matrix of the linearized equation system should be applied for forcing unstable condition for oscillator at t=0.

Therefore, as per Lyapunov first stabilization method, all we have to do for the derivation of the stability and instability conditions for our oscillator is:

1. The linearization of equations $(D.46)$ and $(D.47)$ around the steady state values of (A_0^*, B_0^*) and around the values $A_0 = 0$, $B_0 = 0$;
2. The extraction of Jacobian matrix from the linearized equations obtained in the previous step;
3. The extraction of the characteristic polynomial equation of the Jacobian matrix;
4. The implementation of the stability conditions (Lyapunov's first method);
5. The implementation of the instability conditions (Lyapunov's first method).

Linearization principle:

The above two non-linear differential equations can be easily linearized by expanding the two functions $F_{0,0}$ and $F_{1,0}$ as power series over the two values mentioned above ($B_0 = A_0 = 0$, specific to time origin and A_0^* and B_0^* specific to steady state) and eliminating higher order terms. Thus, the linearized expressions for $F_{0,0}$ and $F_{1,0}$ are as follows

$$F_{0,0} = F_{0,0}(A_0, B_0) + \frac{\partial F_{0,0}}{\partial B_0} B_0 + \frac{\partial F_{0,0}}{\partial A_0} A_0 \tag{D.49}$$

$$F_{1,0} = F_{1,0}(A_0, B_0) + \frac{\partial F_{1,0}}{\partial B_0} B_0 + \frac{\partial F_{1,0}}{\partial A_0} A_0 \tag{D.50}$$

By introducing the equations ($D.49$) and ($D.50$) in the equations ($D.43$) and ($D.44$) and by assuming that $F_{0,0} = F_{1,0} = 0$ (actually these neglected terms are not considered for the calculation of the Jacobian matrix), the system of equations ($D.43$) and ($D.44$) leads to:

$$\frac{dB_0}{d\tau} = (k_0 \frac{\partial F_{0,0}}{\partial B_0} - c)B_0 + k_0 \frac{\partial F_{0,0}}{\partial A_0} A_0 \tag{D.51}$$

$$\frac{dA_0}{d\tau} = \frac{1}{2}(k_2 - k_0)\frac{\partial F_{1,0}}{\partial B_0} B_0 + \frac{1}{2}[(k_2 - k_0)\frac{\partial F_{1,0}}{\partial A_0} + (c - a)]A_0 \tag{D.52}$$

The extraction of the Jacobian matrix:

Having the linearized equations, the Jacobian matrix ($\dot{x} = Jx$) results in the form of:

$J = \begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix}$

where $A_{11} = \frac{d\frac{dB_0}{d\tau}}{dB_0}$ performed in the above ($D.51$) equation and thus, $A_{11} = k_0 \frac{\partial F_{0,0}}{\partial B_0} - c$, $A_{12} = k_0 \frac{\partial F_{0,0}}{\partial A_0}$, $A_{21} = \frac{1}{2}(k_2 - k_0)\frac{\partial F_{1,0}}{\partial B_0}$ and $A_{22} = \frac{1}{2}(k_2 - k_0)\frac{\partial F_{1,0}}{\partial A_0}$.

In our case the Jacobian matrix is a 2x2 matrix.

The extraction of the characteristic polynomial equation of the Jacobian matrix

The characteristic polynomial P_j is obtained by calculating the determinant of the matrix $M = (J - \lambda I_2)$, i.e. $P_j = det(J - \lambda I_2)$, where J is the above Jacobian matrix and I_2 is the unity matrix of $2x1$ elements. By doing the calculations, the matrix M becomes $M = \begin{pmatrix} A_{11} - \lambda & A_{12} \\ A_{21} & A_{22} - \lambda \end{pmatrix}$.

Thus the characteristic polynomial is obtained as a second-order algebra equation from below:

$$P_j = \lambda^2 - \lambda(A_{11} + A_{22}) + (A_{11}A_{22} - A_{12}A_{21}) \tag{D.53}$$

By solving the equation $P_j = 0$ one can obtain the eigenvalue of the Jacobian matrix for the linearized first-order differential equation system, as shown below:

$$\lambda^2 - \lambda(A_{11} + A_{22}) + (A_{11}A_{22} - A_{12}A_{21}) = 0 \tag{D.54}$$

For this equation, the determinant and the solutions are calculated as follows:

$$\Delta = A_{11}^2 + A_{22}^2 - 2A_{11}A_{22} + 4A_{12}A_{21} \tag{D.55}$$

$$\lambda_{1,2} = \frac{A_{11} + A_{22} \pm \sqrt{\Delta}}{2} \tag{D.56}$$

The implementation of the stability condition (Lyapunov's first method)

As already presented up to now, the condition for the above system of the linear- first-order equation to be stable (which applies also for the non-linear first-order system as demonstrated by Lyapunov) is that the above eigenvalues to be real and negative. As the eigenvalues are the solutions of the simple algebra equation of the second order, this translates to the following conditions from below

$$\lambda_1 + \lambda_2 < 0 \tag{D.57}$$

$$\lambda_1 \cdot \lambda_2 > 0 \tag{D.58}$$

$$\Delta > 0 \tag{D.59}$$

If we take into considerations the expressions for the matrix elements A_{11}, A_{12}, A_{21}, A_{22}, then the above stability conditions (around A_0^* and B_0^* as defined above) become as follows:

$$k_0 \frac{\partial F_{0,0}}{\partial B_0} + \frac{k_2 - k_0}{2} \frac{\partial F_{1,0}}{\partial A_0} - \frac{c + a}{2} < 0 \tag{D.60}$$

$$(k_0 \frac{\partial F_{0,0}}{\partial B_0} - c)(\frac{k_2 - k_0}{2} \frac{\partial F_{1,0}}{\partial A_0} + \frac{c - a}{2}) > k_0 \frac{k_2 - k_0}{2} \frac{\partial F_{0,0}}{\partial A_0} \cdot \frac{\partial F_{1,0}}{\partial B_0} \tag{D.61}$$

Therefore the circuit elements of the third order oscillator with shifting bias should follow the above conditions to get the oscillation stability around A_0^* and B_0^*, becoming thus the steady state values of the oscillation.

For those circuit values (passive components as well as active device parameters) that obey the stability and instabilities conditions from above, the system of equations $(D.46)$ and $(D.47)$ can be solved (in most of the cases numerically) and thus provide the A_0 and B_0 dependencies as function of time, from the zero time till the steady state is reached. Finally the envelopes of the oscillation solution is obtained by representing $B_0(\tau) + A_0(\tau)$ and $B_0(\tau) - A_0(\tau)$ as functions of time. These envelopes are shown on a real case in the Chapter 5.

The implementation of the instability conditions (Lyapunov's first method)

As described above, a well designed oscillator should be unstable at the initial moment when the power supply is set ON. Therefore, an instability condition should be "forced" at $t = 0$ at the design level so, that the initial small (noise) oscillating signal to grow continuously till the steady state is reached. By opposition to the stability condition, if the eigenvalues are positive then the oscillation is unstable. This is the condition we need to push at t=0 for our oscillator. Starting from the characteristic polynomial, again, the instability condition becomes.

$$\lambda_1 + \lambda_2 > 0 \tag{D.62}$$

$$\Delta > 0 \tag{D.63}$$

By introducing the explicit values of the matrix M we get the following instability condition for our oscillator:

$$k_0 \frac{\partial F_{0,0}}{\partial B_0} + \frac{k_2 - k_0}{2} \frac{\partial F_{1,0}}{\partial A_0} - \frac{c + a}{2} > 0 \tag{D.64}$$

$$(k_0 \frac{\partial F_{0,0}}{\partial B_0} - c)(\frac{k_2 - k_0}{2} \frac{\partial F_{1,0}}{\partial A_0} + \frac{c - a}{2}) > k_0 \frac{k_2 - k_0}{2} \frac{\partial F_{0,0}}{\partial A_0} \cdot \frac{\partial F_{1,0}}{\partial V_0} \tag{D.65}$$

D.3 Second-order Approximation

The first order approximation is all you need for the practical design considerations in the case of third order oscillators. However, as in many practical cases, for the first order approximation, the term ω_1 expressing the deviation of the real resonant frequency from the resonant frequency of the ideal system ($\epsilon = 0$) is showing the value $b_1 = 0$, then for the study and for the analysis of the frequency shift in the real oscillating systems, the second order approximation is needed.

In order to analyze the second order approximation, only the terms up to the second order ϵ^2, inclusive, are going to be used for $B(\tau)$, $A(\tau)$, $H_m(\tau)$, $F_{0,n}(\tau)$, $F_{1,n}(\tau)$, b and ω. With this condition, the terms of the overall equation $(D.1)$ will take the following forms:

$$B(\tau) = B_0(\tau) + B_1(\tau)\epsilon + B_2(\tau)\epsilon^2 \tag{D.66}$$

$$A(\tau) = A_0(\tau) + A_1(\tau)\epsilon + A_2(\tau)\epsilon^2 \tag{D.67}$$

$$H_m(\tau) = H_{m,1}(\tau)\epsilon + H_{m,2}(\tau)\epsilon^2 \tag{D.68}$$

$$F_{0,n}(\tau) = F_{0,0}(\tau) + F_{0,1}(\tau)\epsilon + F_{0,2}(\tau)\epsilon^2 \tag{D.69}$$

$$F_{1,n}(\tau) = F_{1,0}(\tau) + F_{1,1}(\tau)\epsilon + F_{1,2}(\tau)\epsilon^2 \tag{D.70}$$

$$b = b_0 + b_1\epsilon + b_2\epsilon^2 \tag{D.71}$$

$$\omega = \omega_0 + \omega_1\epsilon + \omega_2\epsilon^2 \tag{D.72}$$

As shown in [12], for the second order approximation analysis the following form for the Fourier coefficients $F_{m,n}$ is used:

$$F_{m,n} = K_m^A A_n(\tau) + K_m^B A_n(\tau) + R_{m,n}(\tau) \tag{D.73}$$

where

$$\frac{C_k}{d\tau} = \frac{1}{2\pi}\int_0^{2\pi} \frac{df(x)}{dx}|_{x=B_0+A_0cos(\nu)} cos(k\nu)d\nu \tag{D.74}$$

$$K_m^A = \frac{C_{m-1}}{d\tau} + \frac{C_{m+1}}{d\tau} \tag{D.75}$$

$$K_m^B = 2\frac{C_m}{d\tau} \tag{D.76}$$

$$R_{m,n}(\tau) = R_{m,n}^H(\tau) + R_{m,n}^X(\tau) \tag{D.77}$$

$$R_{m,n}^H(\tau) = \sum_{s\geqslant 2}^{\infty}[(\frac{C_{m-s}}{d\tau} + \frac{C_{m+s}}{d\tau})ReH_{s,n} + j(\frac{C_{m-s}}{d\tau} - \frac{C_{m+s}}{d\tau})ImH_{s,n}] \tag{D.78}$$

$$R_{m,n}^X(\tau) = \frac{1}{\pi}\int_0^{2\pi}(\sum_{l_1...l_{n-1}} \frac{x_1^{l_1}x_1^{l_2}...x_{n-1}^{l_{n-1}}}{l_1!l_2!...l_{n-1}!}(x_0))e^{-jm\nu}d\nu \tag{D.79}$$

In this context, the solution for the second order approximation can be obtained for each m value, starting from $m = 0$ (dc component) till any higher order harmonics. So that, for $m = 0$ the obtained solution is:

$$\omega_0^2\frac{dB_1}{d\tau} + [c - k_0K_0^B]B_1 - k_0K_0^AA_1 = k_0R_{0,1}^H \tag{D.80}$$

When $m = 1$, we get a solution with two components because of the presence of the real and imaginary terms in the second approximation equation:

$$-2\omega_0^2\frac{dA_1}{d\tau} - [(k_0 - k_2\omega_0^2)K_1^B]B_1 + [c - a\omega_0^2 - ((k_0 - k_2\omega_0^2)K_1^A)]A_1 = (k_0 - k_2\omega_0^2)ReR_{1,1}^H \tag{D.81}$$

$$\begin{aligned}2A_0\omega_0^2\omega_2 = -(k_0 - k_2\omega_0^2)ImR_{1,1}^H - k_1\omega_0F_{1,0} - 2k_2\omega_0\frac{dF_{1,0}}{d\tau} + A_0b_2\omega_0 + 3\omega_0\frac{d^2A_0}{d\tau^2}\\ +2a\omega_0\frac{dA_0}{d\tau}\end{aligned} \tag{D.82}$$

For $m > 1$, we get a solution by considering the following equation:

$$\begin{aligned}m(m^2-1)\omega_0^3H_{m,2} = j(k_0 - k_2m^2\omega_0^2)F_{m,1} - k_1m\omega_0F_{m,0} - 2m\omega_0k_2\frac{dF_{m,0}}{d\tau}\\ +j(am^2\omega_0^2 - c)H_{m,1} + j(3m^2-1)\omega_0^2H_{m,1}\end{aligned} \tag{D.83}$$

It worths to notice, that the equation ($D.82$) contains a term ω_2 which represents the deviation of the resonance frequency from the natural resonance frequency of the system. One can see that it varies in time after the equation written below:

$$\omega_2 = \frac{1}{2A_0}[(k_2 - k_0)Im(R_{1,1}) - k_1 F_{1,0} + b_2 A_0 - 2k_2 \frac{dF_{1,0}}{d\tau} + 3\frac{d^2 A_0}{d\tau^2}] \tag{D.84}$$

Consequently, the current appendix has presented an accurate perturbation method for the analysis and the design of the non-linear third order oscillator with shifting bias. The quasi analytical methodology described here has the advantage of constructing an iterative oscillator solution where the transient time, the steady state regime and the harmonic content of the oscillating solution can be evinced. The oscillator solution is obtained very accurately from the first order approximation approach, where the Lyapunov's stability method is used for identifying and designing the conditions for oscillator instability at the time origin and, respectively, the conditions for stability at the steady state. From the system of equation characterizing the first order approximation, the time dependence of the envelopes of oscillation is deduced. The system resonance frequency is also obtained as a perturbation of the natural resonance frequency. The accurate deviation of the real resonance frequency from the ideal value (given by the natural resonance frequency of the feed-back loop circuit) can be derived by using the second order approximation calculations.

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