Zuverlässigkeitsstudien an Höchstfrequenzbauelementen mit gepulsten Techniken (TLP-Methode)

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Für Yanneck Elias

Vorwort

Die vorliegende Dissertation ist in meiner Zeit am Institut für Hochfrequenztechnik der TU Darmstadt entstanden. Dieser Zeitraum zeichnet sich durch vielfältigste Aufgaben und Herausforderungen in der Lehre, der Forschung und dem Projektmangement aus, die mich sowohl fachlich als auch menschlich reifen ließen. An erster Stelle möchte ich Prof. Dr. Eng. h.c. H. L. Hartnagel für sein Vertrauen, seine Unterstützung und seinen Rat danken, sowie für die Möglichkeit, im Rahmen der Forschungstätigkeiten mit Wissenschaftlern auf nationaler und internationaler Ebene arbeiten zu können. Außerdem danke ich Prof. Dr. rer. nat. Kostka für alle hilfreichen Hinweise. Die Unterstützung durch die Deutsche Forschungsgemeinschaft (DFG) möchte ich hervorheben, da durch ihre Mithilfe Forschung in manchen Fällen erst ermöglicht wird. Im Speziellen gilt mein Dank allen Partnern, mit deren Hilfe die durch die DFG, die ESA und die EU ermöglichten folgenden Projekte erfolgreich bearbeitet werden konnten, wobei ich an dieser Stelle Laurent Marchand, Sylvain Delage, David Raboso, Stephan Biber und Viktor Krozer besonders erwähnen möchte:

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Kurzfassung

Diese Arbeit beschreibt die gezielte Anregung zuverlässigkeitsrelevanter Degradations- und Defektmechanismen bei III/V Höchstfrequenzbauelementen (InGaP/GaAs Heterostruktur Bipolartransistor, Pt/GaAs THz-Schottkydiode) unter Verwendung elektrischer Pulse (bekannt als Transmission Line Pulse, TLP-Methode). Desweiteren wird die Einführung von Prozesskontrollschritten und eines erweiterten Prozesskontroll-Systems im Fabrikationsprozess von Terahertz (THz)-Schottkydioden sowie die Auswirkungen auf die Bauteilzuverlässigkeit erläutert. Anhand planarer Schottkydioden wird die Bedeutung der Verknüpfung von Technologie-Entwicklung, Hochfrequenz-Design und Zuverlässigkeits-Tests erörtert.

Als wichtigste Ergebnisse werden die Demonstration der Vergleichbarkeit der Ergebnisse der TLP-Methode mit Arrhenius-beschleunigten Zuverlässigkeitsmethoden sowie ihre Anwendbarkeit im Fabrikationsprozess planarer THz-Schottkydioden vorgestellt. Im Vergleich zu Arrhenius-beschleunigten Testmethoden verwendet die hier vorgestellte Methodik elektrische Rechteckpulse zur Beschleunigung der Ausfallmechanismen. Durch eine dem zu stressenden Bauteil mit individueller thermischer Zeitkonstante angepasste Wahl der Pulslänge, d.h. des Zeitraums der elektrischen Belastung, wird sichergestellt, daß die Bauteildegradation hauptsächlich durch elektrische Größen (U, I, P) und weniger thermisch angeregt wird.

Abstract

This work describes the well-directed excitation of reliability relevant degradation and defect mechanisms for highest-frequency components (InGaP/GaAs heterostructure bipolar transistor, Pt/GaAs Schottky diode for THz-frequencies) using electrical pulses (also known as the transmission line pulse, TLP-method). Further, it introduces an enhanced process control system for the fabrication of planar THz-Schottky diodes and the effect on reliability. With respect to planar Schottky diodes, the importance of linking technology development, RF design and reliability tests is pointed out.

The most important results are the demonstration of comparability between the results from the TLP-method and from Arrhenius-based reliability test methods. Additionally, the TLP-method proved the applicability for process optimization with planar THz-Schottky diodes. In comparison to Arrhenius test methods the proposed methodology applies electrical square pulses for acceleration of degradation mechanisms. Electrical stress is ensured by choosing the pulse length, i.e. the electrical stress time, adapted to the thermal time constant of the device. With this approach, mainly electrical parameters (U, I, P) and not thermal ones excite device degradation.

Contents

Chapter 1

Introduction

The basics of semiconductor technology and devices were established in the 50'ies by the work of WILLIAM SHOCKLEY, JOHN BARDAIN and WALTER BRATTAIN among others. 1947, after 10 years of research in the BELL laboratories, the first transistor was invented [1, 2] based on Germanium. The motivation for this effort was the substitution of electromagnetic switching relays in telephone systems with more reliable switches. The search for improved system reliability turned out to be the driving force for a technology which becomes the basis of today's modern communication technology [3].

The further rapid development was characterized by the emergence of new semiconductor materials and device principles. The introduction of Hetero Bipolar Transistors (HBT) by HERBERT KROEMER, theoretically described in 1957 and primarily proposed in 1951 by SCHOTTKY, and the HBT operation principle marks a new way of fabricating device for high-frequency and optical applications. In 2000, he is awarded with the NOBEL prize in physics for his lifework - the development of semiconductor hetero-structures for optoelectronic and microwave circuits [4–6]. In a sense, every electronic device implies a hetero-junction, namely the obligatory metal contact, which may be Ohmic or Schottky type. Based on these still valid theories, the semiconductor fabrication technology steadily improves and the device dimensions are decreasing down into the sub-micron and even nanometer-scale. The speed of active elements is accordingly increasing up to the point that in 2001 the first experimental Tera-Hertz (THz)-transistor was presented (INTEL) and verified by a French team in 2004. The leading edge in THz-research is currently the realization of Schottky devices for mixing and frequency multiplication as well as their system integration at the JET PROPULSION LABORATORY [7–9] and the University of Virginia [10], VDI[1] respectively. In this context, this work focuses on the study of reliability-relevant defect mechanisms for heterostructure- and sub-micron devices and the establishment of a new approach to their well-directed and accelerated excitation for process control and verification.

Although reliability analysis was not experiencing the same acceleration, compared to the development of device technology and integration density (MOORE'S law), dedicated reliability analysis techniques have nowadays become crucial. In particular for higher frequency and space applications, where newly introduced devices have to face stringent requirements for qualification. Higher operating frequency means small dimensions for the device structure, resulting in high current densities [11], and the introduction of new materials and complex fabrication techniques. Adapted tools for accelerated reliability analysis are necessary in order, through faster feedback, to shorten the path to technological maturity and device time to market. Within the scope of these requirements, the motivation for this work is given in the following section.

[1] VDI=Virginia Diodes Incorporated

1.1 Background of this work

The importance of reliability investigations has been always increasing from the beginning of semiconductor technology up to now. Reliability data are delivered for each semiconductor process or device and constitute a decision criterion for customers in the automotive, the aviation or space industry. Reliability data are usually extracted using accelerated methods with increased stress parameters since the lifetime of semiconductor devices can reach several years or even decades. The industrial quasi-standard for accelerated reliability testing is the measurement of device lifetime under increased ambient temperature and increased DC-current conditions [12]. The lifetime under "normal" operating conditions is extracted using the ARRHENIUS-law, which originally described thermally activated chemical processes. It is evident that the acceleration factor for reliability tests is the key parameter for a fast feedback to the fabrication process and the realization of shorter technological development cycles. The demand for a shorter time to market results in the research on alternative test methods, especially with regard to high frequency device technology. With decreasing lateral and horizontal device dimensions of high-frequency devices up to 10 THz, not only temperature induced defect mechanism, exemplarily described in [13], but also electrically induced defect mechanisms (e.g. by high current densities) contribute to device degradation, cf. chapter 2.

The Transmission Line Pulse (TLP)-method can provide an acceleration down to 24 hours testing time and therefore is suitable for an acceleration of technology optimization as it will be presented in this work, cf. chapter 3. This approach belongs to the family of electrical stress test methods like Electrostatic Discharge (ESD), Human Body Model (HBM), Charged Device Model (CDM) and Very Fast TLP (VTLP). These methods apply a finite electrical pulse of a certain shape to the device under test (DUT). The TLP-method for the accelerated excitation of electrically induced defect mechanisms is based on applying short electrical square pulses, with typically $t_p = 20 \ldots 100\ ns$, to the device as described in [14, 15]. The separation of thermally and electrically induced defect mechanisms is possible, if the electrical pulse length is kept short in comparison to the devices thermal time constant. A further advantage of this method is an additional acceleration of defect mechanisms to only few days [16, 17], which can result in an acceleration of the technology optimization process. This method can be applied to any device and degradation mechanisms are separated by appropriate adjustment of stress-parameters. The key point in this work is the testing methodology, which allows well-directed excitation of degradation mechanisms.

In this work, the devices under test are mainly Schottky diodes developed and fabricated at the IHF, TU DARMSTADT in the framework of several ESA/ESTEC[2]-projects and heterostructure bipolar transistors provided by several European semiconductor manufacturers in the framework of a European BRITE EURAM project, HERO'S for the establishment of an European HBT source,detailed in chapter 4. The advantage of the in-house fabricated diodes is the exact knowledge of device geometries, parameters and process technology and their impact on degradation and defect mechanisms. For the first time, the TLP-method is used for a very fast feedback to the in-house fabrication process for planar Schottky devices and accelerates the optimization process. The advantage in case of the HBT is the access to a state of the art industrial hetero-device technology. In this context, the TLP-method is firstly used as an alternative reliability test method, which helped to reveal potential process and device weaknesses in the development of an industrial process and is able to give a fast feedback to the fabrication process. This work describes an entire test methodology, cf. section 3.2 which allows for the first time a comparison to Arrhenius-based

[2] ESA=European Space Agency, ESTEC= ESA Technical Center

lifetime and reliability test methods.

Further on, this work answers basic questions such as for example, at which locations which current-induced or field-induced defect mechanisms occur in compound semiconductors for microwave applications and how they are excited using pulsed electrical stress. Reliability analysis requires a deep understanding of device physics for the measurement and the analysis of degradation mechanisms at interfaces and in layers. The respective review is presented in chapter 2. Usually, metal-semiconductor or semiconductor-semiconductor interfaces or both are used for microwave devices. At these interfaces, dislocations, atom diffusion and other irregularities lead to defects. The interfaces make the device, as already KROEMER recognized, but they are also the weak point concerning device stability. Pure semiconductor layers have only in their crystalline form the desired electrical properties and are destroyed by temperatures beyond their melting point due to the loss of their crystalline structure. A major topic of this work is the investigation of metal contact stability on semiconductors if high current densities are applied. Results for heterostructure devices are exemplarily shown with InGaP/GaAs-HBT and the respective Transmission Line Model (TLM)-structures, those for sub-micron devices with planar and whisker-contacted III/V-Platinum Schottky diodes for THz-frequencies, cf. chapter 6. Results for Hetero-barrier varactors (HBV) and power-sensor structures are presented in [18–20].

1.2 THz-spectroscopy and technology

THz-radiation is non-ionizing and sensitive to changes in the refractive index, which is optimal for medical and security-related applications. The high absorption of THz-signals by water or vapor is ideal for the detection of tumors, e.g. cancer, but limits the signal-transmission capabilities in atmosphere. The increasing interest in atmospheric research and in the effect of the world-wide industrialization on the atmospheric composition enforces research efforts in the THz-frequency region from 0.1 THz to 10 THz. Some of the more important greenhouse gases, e.g. OH^-, CLO, NO_x or O_3, can be detected in this frequency range, at which they emit electromagnetic waves with the transition between different rotational modes, cf. table 1.1. Further, the possibilities in medical and security applications awake the public opinion though there are still a lot of development steps to reach industrial maturity.

Rotation transition	frequency / GHz	$\frac{Eu}{k_b}$ / K	n_{crit} / cm^{-3}
CO(1-0)	110	5.5	$3 \cdot 10^3$
CO(2-1)	230	16.6	$2 \cdot 10^4$
CO(3-1)	345	33.2	$5 \cdot 10^4$

Table 1.1: *Frequencies for different material transitions.*

Bridging the gap between optics and the millimeter waves with wavelengths between 3 mm and 30 μm requires a reduction of device dimensions and an optimization of material systems for a reduction of noise temperatures, parasitic effects and the capability of cut-off frequencies up to $f = 10\,THz$. These THz-capable devices are key-elements in radioastronomy and medical applications and without them the respective instruments can not be manufactured. Table 1.2 shows the requirements from space industry for the realization of low-noise mixers for heterodyne receivers.

In this context, the low series resistance and the low noise temperature is mandatory to achieve sufficient signal to noise ratios for THz-signal detection. The reduction of the parasitic capacitance is mandatory for operation at highest frequencies, cf. section 4.2. Noise temperature and ideality factor are strongly dependent on the interface technology while the parasitic capacitance depends on the design of the periphery, e.g. air-bridge, pads or ohmic contact.

Electrical parameter	Symbol	Value	Requirement
Series resistance	R_s	$\leq 6\,\Omega$	Low noise, low conversion loss
Ideality factor	η	≤ 1.2	Low conversion loss
Junction capacitance	C_j	$1 \ldots 2\,fF$	Matching on junction
Parasitic capacitance	C_p	$\leq 10\,fF$	Bandwidth
Noise temperature	T_{noise}	minimal	Radiometer sensitivity

Table 1.2: *Requirements from space industry.*

The following paragraph explains the impact of this work on Schottky device development in connection with former research efforts at the IHF[3] and with respect to requirements from space industry. Former research considered either the technology development (e.g. for noise reduction) or high-frequency design. With this work, both disciplines are combined as detailed in the following.

Figure 1.1: Example of a planar IHF Schottky diode.

Compound semiconductors, e.g. GaAs or InP, turned out to be material systems of choice for this frequency region. In comparison to silicon, their advantage is the higher electron mobility

[3]Institut für Hochfrequenztechnik, TU Darmstadt

resulting in higher cut-off frequencies and a higher bandgap resulting in a better immunity against ionizing radiation and the possibility of operation at higher temperatures. For frequencies beyond 1 THz the Schottky-diode, cf. figure 1.1, or the heterostructure barrier varactor (HBV) are suitable elements for mixing or frequency multiplication [21–23]. The basic electrical properties of realized planar Schottky mixer diodes are shown in chapter 4. The application in satellites requires a close look at device reliability to guarantee operation under space conditions. The optimization of the technological process in view of repeatability, reliability and RF- and DC-characteristics is one major topic of this work, cf. chapter 5. The introduction of process monitoring, standard reliability tests and the application of the TLP-method for a fast feedback to technology is a first step to space qualification of these devices. The noise properties as well as the reliability are mainly influenced by the metal-semiconductor interface, which is more closely discussed.

At this stage, one recognizes that only perfect devices will fulfill all these requirements and can comply with ESA quality standards and that a high financial effort is necessary for an industrial infrastructure and technology. In contrary, the Schottky-diodes of this institute, the IHF TU DARMSTADT originate from an experimental process at a research laboratory, which is steadily developed since 1990. Taking this into account, the technological process is permanently optimized to reach this ambitious goal. The last optimization steps included the introduction of a process control system based on Process identification documents (PID) and Lot travelers (LT) for the Schottky diode process. On the basis of this process documentation, further optimization includes the design of a new mask set with additional process control structures for the analysis of single process steps described in chapter 5. With these efforts, the fabrication of high-quality Schottky diodes with excellent noise properties is possible with sufficient fabrication yield. This was a necessary condition for the realization of future steps like the integration with filter structures and micro-machined waveguides for THz-systems, which are currently under investigation.

Chapter 2

Reliability, Theory and Mechanisms

Reliability gains more and more importance in semiconductor industry due to the growing demand for devices operating in security relevant systems in automotive and space application (airbag, near-distance radar, spacecraft-control). Semiconductor manufacturers established Arrhenius-based reliability evaluation procedures, which usually do not allow a fast feedback to the technological process. Some of these procedures follow the MIL-217 standard [24] others are manufacturer and application specific. Reliability is defined as the probability of a device to operate with defined properties under certain conditions for a certain time. Following the ISO 9000 standard, it is defined as "the probability that a product will perform its intended function for as specified period of time under stated conditions" [25]. Device reliability depends on many different influencing variables, e.g. application conditions, design, production tolerances, which are not always distinguishable and must be separately determined and evaluated with respect to their relevance.

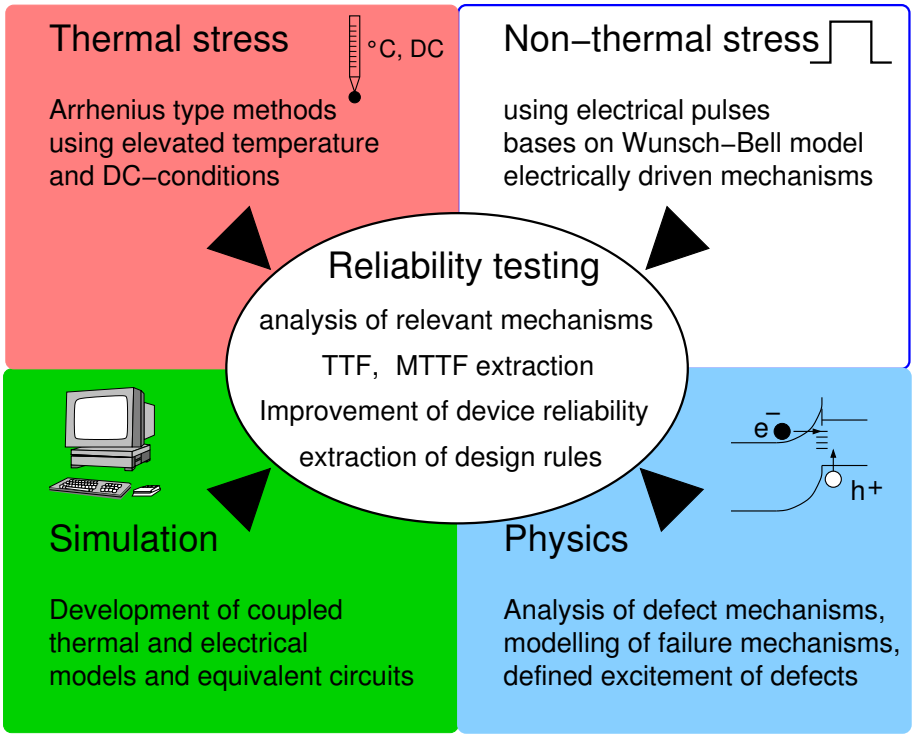


Figure 2.1: Reliability analysis.

Reliability analysis is in its nature interdisciplinary and requires knowledge in various areas as device physics, device and defect mechanism analysis, device simulation and accelerated stress techniques as indicated in figure 2.1. The before mentioned analytic instruments allow, in combination with a statistical approach, the formulation of reliability for each specific device. The following sections give an overview on the different parts of reliability analysis starting with a system theory approach, cf. section 2.1, continuing with the available degradation models and ending with the relevant defect and degradation mechanisms in section 2.2. At the end of this chapter, a survey of defect mechanisms is given for HBT and Schottky diodes, cf. section 2.2.3 and 2.2.4. These sections are the basis for the interpretation of the measurement results in chapter 6. In the case of Schottky devices, reliability limiting effects influence the design of the process control system, which is detailed in chapter 5. As lifetime of semiconductor devices may be up to several decades, accelerated testing procedures are mandatory for the excitation of defect mechanisms, as it will be detailed in chapter 3.

Defect mechanisms are generally separated into failure mechanisms, such as those leading to catastrophic device malfunction, and degradation mechanisms. Degradation is a slow change in device properties up to the point, where it exceeds a specified tolerance and therefore leads to device failure. The mathematical description of reliability is based on stochastic processes with random variables, i.e the theory of probability. For modern devices, especially for those with dimensions in the sub-micron range, different failure and degradation mechanisms are likely to occur (e.g. thermally or electrically activated). The separation of these mechanisms and their correct modeling is the main task for proper reliability analysis.

2.1 System theory approach

The following sections describe the general system theory approach and the basics of kinetics-based modeling for failure and degradation mechanisms. The majority of available degradation models is either based on temperature enhanced diffusion, cf. section 2.1.2, or on mass transport processes, cf. section 2.1.5 like the electron wind effect or field enhanced material transport mechanisms, cf. section 2.2. The analysis of material modifications is important because the structure of an electronic element determines its function. Every structural change, especially in very thin active layers (e.g. the HBT base layer with a thickness of 100Å), either by diffusion or by mass transport, can drastically change the device performance or even destroy the device.

The lifetime of electronic components usually consists of different phases with respect to the dominating failure mechanism. The failure rate function is a superposition of these phases. It is used for the analysis of component failure and is visualized by the bath-tube curve, cf. figure 2.2, which is briefly explained in the next paragraph.

The probability that a component functions at the time t_0 will fail at $t_0 + \Delta t$ is given by the product of failure rate $h(t)$ and the time interval Δt, which is shown in equation 2.1.

$$P(t < TTF \leq t + \Delta t|_{TTF \geq t}) = h(t) \cdot \Delta t \tag{2.1}$$

In the first phase, components fail due to mistakes in the fabrication process or due to material problems. This is followed by the second phase with stochastic component failure. This area is characterized by a constant failure rate, which equation 2.2 expresses. This constant failure rate is a result from the dominating defect mechanism or from a superposition of different independent failure mechanisms. These are caused by physical or chemical reactions which are modeled by

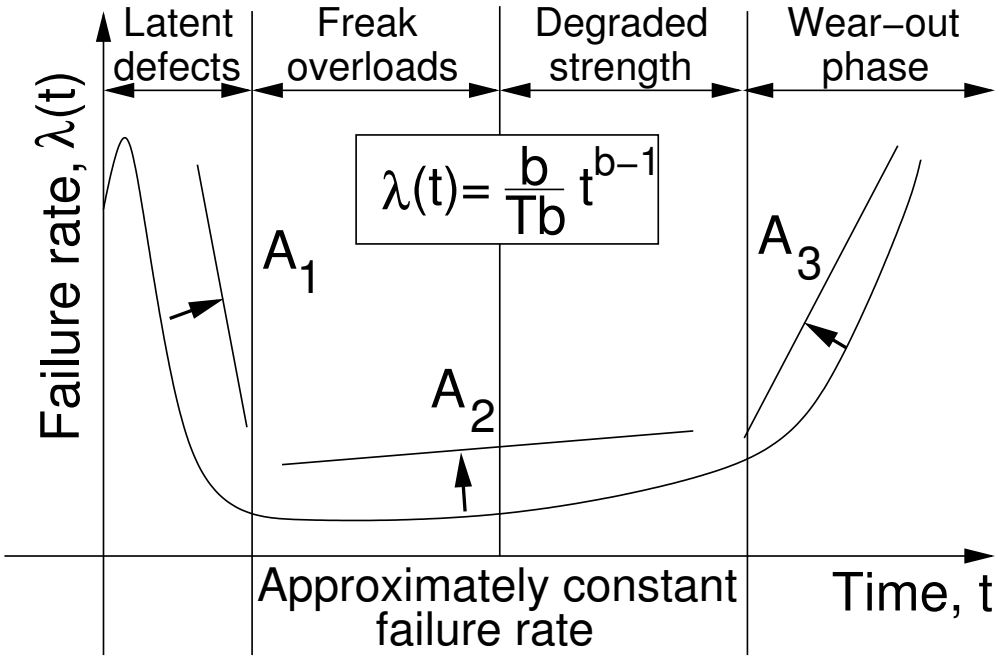


Figure 2.2: Bathtub curve describing the component failure rate as a function of time.

different approaches, e.g. the Arrhenius law for diffusion processes. The last two phases, also called the wear-out phase, are dominated by failure due to ageing effects. The degradation mechanisms in each phase can be accelerated using dedicated stress tests. This results in the acceleration factors A_1, A_2 and A_3 for the different phases.

$$\lambda = \frac{\partial N}{\partial t} = const. \tag{2.2}$$

The nature of degradation and failure mechanisms is not deterministic so that a statistic approach is required for its modeling. The problem formulation is as follows. By the application of a stressing unit X_i, there is no failure for the following condition $X_{S,min} < X_i < X_{S,max}$. In the contrary there is a failure for $X_i \leq X_{S,min} \cup X_{S,max} \leq X_i$. The respective probability of survival and failure are defined by equation 2.3 and equation 2.4, and finally satisfying equation 2.5.

$$R = p_R = P(X_{S,min} < X_i < X_{S,max}) \tag{2.3}$$

$$P = p_F = P(X_i \leq X_{S,min} \cup X_{S,max} \leq X_i) \tag{2.4}$$

$$p_F + p_R = 1 \tag{2.5}$$

The problem is the definition of the limits and the determination of the values for the stressing unit. The solution is found using the interference analysis principle as it is described in section 2.1.1.

2.1.1 Interference analysis principle

In general, the definition of limits and the stressing unit is made using probability density functions (PDF) for the limits and the stressing unit. This interference analysis principle is schematically shown in figure 2.3.

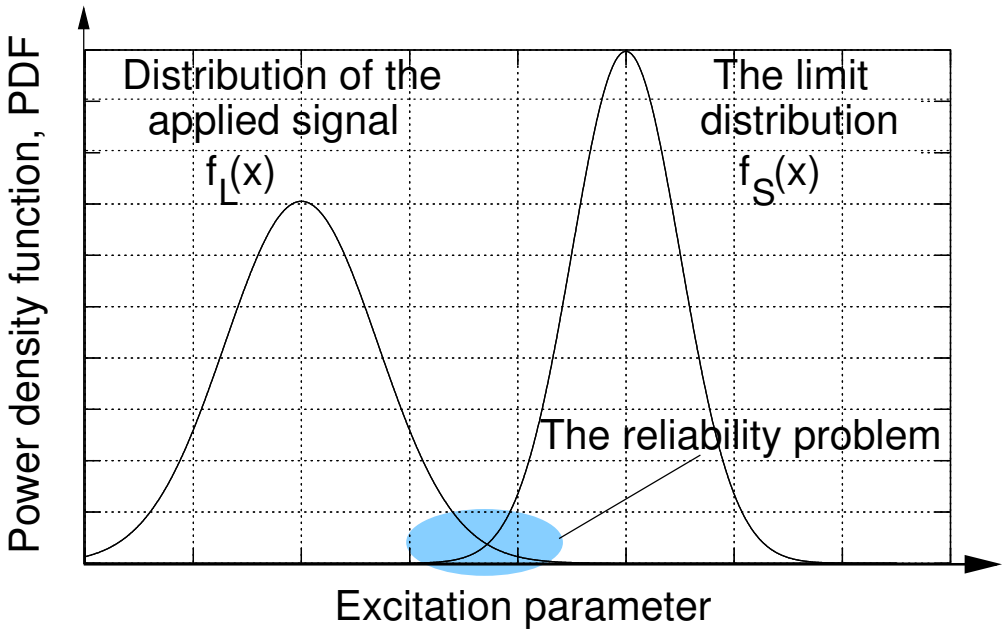


Figure 2.3: Schematic visualization of power density distributions and their intersection at which the reliability problem occurs.

In general, the probability of survival is defined by equation 2.6 where $f_L(x)$ is the PDF for the excitation parameter and $f_S(x)$ is the PDF for the limit, respectively. The reliability problem exists in this example at the intersection of the two normally distributed PDF for the applied signal and the limit distribution, as shown in figure 2.3. In other words, there are signals, which are larger than the minimal threshold for device degradation, resulting in equation 2.6.

$$p_R = \int_{-\infty}^{\infty} \left[f_S(x_S) \int_{-\infty}^{x_s} f_L(x)dx \right] dx_s = \int_{-\infty}^{\infty} \left[f_L(x_L) \int_{x_L}^{\infty} f_S(x)dx \right] dx_L \tag{2.6}$$

The application of k consecutive signals leads to equation 2.7

$$p_R = \int_{-\infty}^{\infty} \left[f_S(x_s) \left(\int_{-\infty}^{x_s} f_L(x)dx \right)^k \right] dx_s \tag{2.7}$$

The solution of this equation is possible for normally distributed excitation signals and if the excitation occurs at a constant rate, as it is with the TLP-method (see section 3.3.3). This way, it can be modeled as a homogenous POISSON process and therefore using the POISSON distribution. The difference of the normal distribution for X_L and the normal-distribution for X_S again is a $N(\mu_S - \mu_L, \sqrt{\sigma_S^2 + \sigma_L^2})$ distribution. Equation 2.8 describes the normalized random variable *SM*

for the respective tabulated standardized normal distribution. This parameter is in this context the safety margin and reliability improves if SM improves. This is relevant for the exclusion of coarse degradation as it is detected using the pulsed-step stress test approach shown in section 3.3.2.

$$SM = \frac{\mu_S - \mu_L}{\sqrt{\sigma_S^2 + \sigma_L^2}} \tag{2.8}$$

The homogenous POISSON process and the exponential distribution are linked together by the relation between the rate of occurrence for the Poisson process and the failure rate of the exponential probability distribution given in equation 2.9.

$$\lambda = p_f \cdot \rho \tag{2.9}$$

For simplicity, the power density distribution of the limit is replaced by a limit value $C_{A,i}$ and the failure probability of a device is modeled using equation 2.10.

$$P_F(C_{A,i}, X_i) = K \cdot \lambda(C_{A,i}, X_i) = \int_{C_{A_i}}^{\infty} f_b(C_{acc,i}) dC_{acc,i} \tag{2.10}$$

with

$C_{A,i} =$ failure threshold
$X_i =$ stressing unit
$C_{acc,i} =$ activation unit
$f_B(C_{acc,i}) =$ density function of the activation unit

2.1.2 The Arrhenius law

Originally, the ARRHENIUS law [26] was used for the description of the reaction rate for diffusion controlled chemical processes in aqueous solutions. The original experiment describes the reaction behavior of one single activated chemical process in a narrow temperature range. The ARRHENIUS law is derived using the MAXWELL-BOLTZMANN distribution as the density function following equation 2.11.

$$f_B(C_{acc}) = f_B(E,T) = F_{MB}(E,T) = K \cdot e^{\frac{-E-E_F}{kT}} \tag{2.11}$$

Using equation 2.10 one gets the ARRHENIUS law 2.12. The activation energy E_A represents the threshold energy for the initiation of a chemical reaction. The corresponding ARRHENIUS-plot directly matches to equation 2.12 by adequate choice of the axis-units. The activation energy is then equal to the slope of the line connecting different (TTF,temperature)-points plotted with logarithmic time scale on the y-axis and the inverse temperature on the x-scale.

$$\lambda = \lambda_0 \cdot e^{-\frac{E_A}{k_B \cdot T}} \tag{2.12}$$

with

$\lambda =$ reaction rate
$\lambda_0 =$ temperature independent coefficient
$E_A =$ activation energy
$T =$ absolute temperature

The ARRHENIUS law turned out to describe a broad range of other diffusion processes in gases, fluids and interfaces [26]. For the application with semiconductors, the MAXWELL-BOLTZMANN approach has some limitations. The electron energy distribution in semiconductors is modeled using the FERMI-DIRAC distribution shown in equation 2.13.

$$f_B(C_{acc}) = f_B(E,T) = F_{FD}(E,T) = \frac{1}{1+e^{\frac{E-E_F}{kT}}} \tag{2.13}$$

The approximation of the FERMI-DIRAC distribution by the MAXWELL-BOLTZMANN distribution is only valid because highest reaction energies are necessary for diffusion in solids, for which the MAXWELL-BOLTZMANN distribution approximates the FERMI-DIRAC distribution. In semiconductors, it is the same situation with electrons having an energy $E \gg E_f$, justifying the application of the ARRHENIUS-law [27].

Under these circumstances, the activation energy for the diffusion of dopants in GaAs has been determined to be in the range of $E_A = 1.4 \ldots 1.6\ eV$ at room temperature and therefore lower compared to the activation energies for the diffusion of dopants in silicon ($E_A = 3 \ldots 3.5\ eV$).

2.1.3 The Einstein diffusion equation

In contrary to the Arrhenius-based degradation models there is the EINSTEIN diffusion equation, which describes the diffusion of charged particles in an electrostatic field in the direction opposite to the electron flow (relevant in [28]), following equation 2.14.

$$J(x) = Z^* \cdot C(x) m E(x) + \frac{k_B \cdot T}{q} \cdot m \cdot \frac{\partial C(x)}{\partial x} \tag{2.14}$$

with

$J =$ particle flux
$E =$ electrostatic field
$Z^* =$ effective particle charge
$m =$ particle mass
$C =$ concentration of particles

2.1.4 The Fick diffusion laws

Another set of degradation models is based on the physical diffusion of materials as it is known from filaments in lamps. These kind of processes are usually modeled using the first FICK's law [29] following equation 2.15.

$$J_m = -D(T) \cdot \frac{\partial C}{\partial x} \tag{2.15}$$

with

$J_m =$ material flux
$C =$ concentration
$D =$ diffusion coefficient
$T =$ absolute temperature

The case of a time-dependent concentration gradient diffusion is described by equation 2.16.

$$\frac{\partial C}{\partial t} = -D \cdot \frac{\partial^2 C}{\partial x^2} \tag{2.16}$$

2.1.5 The Black equation

The BLACK equation empirically models mass transport mechanisms in solid structures caused by electrical current, e.g. the electro-migration effect, and constitutes the theoretical background for the TLP-method (section 3.2). In this case, electrons transfer their kinetic energy to metal atoms, which in consequence are moved in the direction of the electron flow, cf. section 2.2.2. This effect occurs with the TLM-structures, HBT and Schottky devices under test, see chapter 6. The main parameter for the excitation of electro-migration effect is the electrical current density J. Typically, this effect is observed at current densities above several kA/cm^2. This equation can be used to fit various electro-migration processes of different origin by determining the proper exponent n for the current acceleration and the activation energy E_A for thermal acceleration.

$$t_{50} = \frac{A}{d^m \cdot j^n} \cdot e^{\frac{E_a}{k_B \cdot T}} \tag{2.17}$$

with

$t_{50} =$ median time to failure
$j =$ current density
$d = \frac{t_{on}}{T}$ duty cycle
$m =$ duty factor exponent
$n =$ current density exponent
$A =$ arbitrary constant

(2.18)

This is also understood as the Arrhenius law with an extension for the influence of the current density dependent degradation mechanisms. A further extension concerns the integration of the duty cycle d, which is proposed for pulsed excitation in [30,31]. For $m = 0$, equation 2.17 reduces to the original black-equation, for $m = 1$, it expresses an "on-time" dependence and for $m = n$,

this is known as the "average current density" model taking an effective DC current density into account. The respective acceleration factor for identical duty cycles is expressed by equation 2.19.

$$A_F = A_{FJ} \cdot A_{FT} = \underbrace{\left(\frac{j_2}{j_1}\right)^n}_{A_{FJ}} \cdot \underbrace{e^{-\frac{E_A}{k_B}\cdot\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}}_{A_{FT}} \tag{2.19}$$

with

$$\begin{aligned} A_F &= \text{acceleration factor} \\ j_1, j_2 &= \text{current densities} \\ n &= \text{current density exponent} \\ T_1, T_2 &= \text{absolute temperatures} \end{aligned}$$

The model parameters n and E_A are extracted following the equation 2.20.

$$n = -\left[\frac{\partial lnt}{\partial lnJ}\right]_T \text{ and } E_A = k_B \cdot \left[\frac{lnt}{ln\left(\frac{1}{T}\right)}\right]_J \tag{2.20}$$

For the experimental extraction of these parameters, one can define a test stress matrix with different current densities J_1, J_2, J_3 for current acceleration and different temperatures T_1, T_2, T_3 for temperature acceleration following equation 2.21. In the best case, one requires three measurements using the TLP-method as detailed in chapter 3. The current density is adjusted modifying the pulse amplitude, while the temperature is modified with the pulse length. Worst case, 5 measurements are necessary for the extraction of characteristic parameters.

$$TM_{Stress} = \begin{matrix} \\ J_1 \\ J_2 \\ J_3 \end{matrix} \begin{matrix} \begin{matrix} T_1 & T_2 & T_3 \end{matrix} \\ \begin{bmatrix} - & - & X \\ - & - & X \\ X & X & X \end{bmatrix} \end{matrix} \tag{2.21}$$

2.2 Relevant defects and degradation mechanisms

This section concentrates on electrically and thermally excited degradation mechanisms knowing, for example, that the mechanical robustness of todays MEMS[1] type devices is a big reliability issue. A precise description of the device structure is essential for a classification of relevant degradation and failure mechanisms (an overview is found in [32]) and a respective process control system (cf. chapter 5). Device reliability depends, in particular for semiconductor components, on the reliability of its single layers and behavior of the weakest part is relevant for proper device operation and lifetime. In this view, subsequent material layers can be separated into layers and interfaces. The layer is the part for which the material parameters are supposed to be constant (electrically, physically). The interface is the inhomogeneous part with varying material parameters (e.g space charge region interdiffusion). Every electronic semiconductor device consists at least of a semiconducting layer and the contact metalization, which can be Ohmic or Schottky-type and consequently a metal-semiconductor interface. More complicated devices have different semiconductor layers with meta- or pseudomorph, homo- or hetero-interfaces and the required contact metalization. Using this separation scheme, even a simple pn-diode, as exemplary shown in figure 2.4, is separated into 7 different parts.

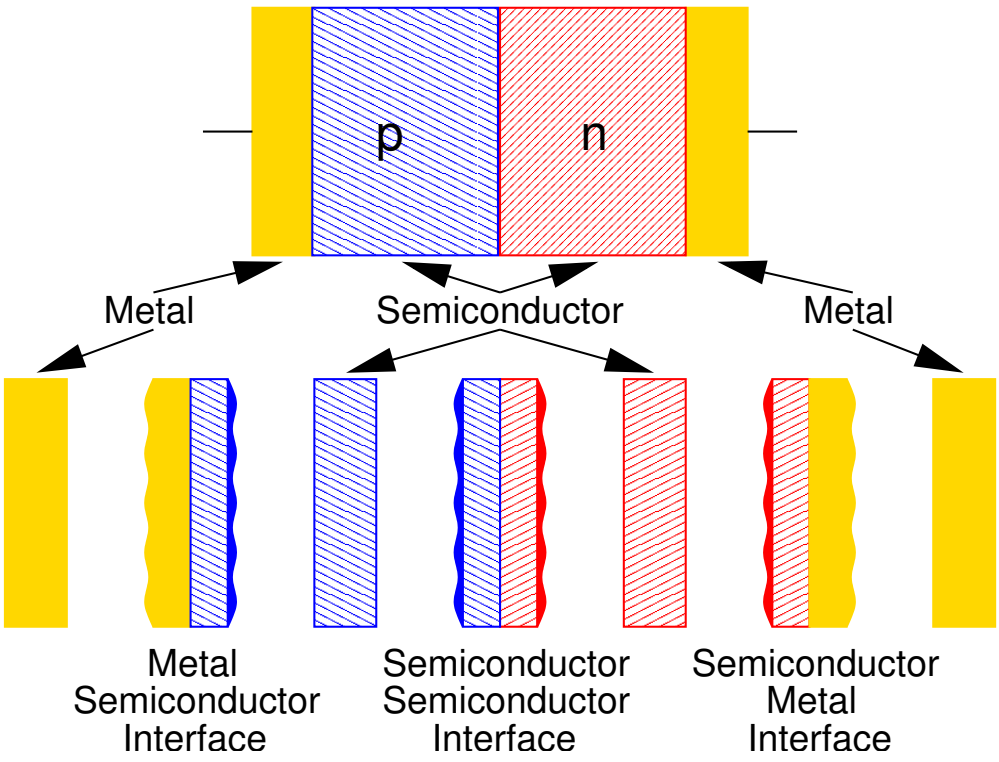


Figure 2.4: Separation of a device in homogeneous and inhomogeneous parts.

This model is still not complete. The interfaces usually are not perfect as a consequence of the fabrication process, during which e.g. the semiconductor is exposed to atmosphere and may react before or during metalization as detailed in section 2.2.4. It is evident that each imperfection of the device either in a layer or in an interface influences the electrical characteristic and is a possible

[1] MEMS=Micro Electro Mechanical Systems

device weakness regarding reliability. The operation principle of the device determines the importance of defects in layers or interfaces (e.g. in a Schottky-diode the Schottky-metal semiconductor interface is important, in a HBT the hetero-interface is important). The following sections give an overview of relevant defect and degradation mechanisms. The correct identification and separation of device specific failure mechanisms is mandatory for the evaluation of the results achieved with the TLP-method.

2.2.1 Defects and degradation mechanisms in layers

Most of the defects in layers are introduced into the lattice during material growth. These lattice imperfections influence the electrical properties of the device. Figure 2.5 shows possible defects as they are detailed in the following.

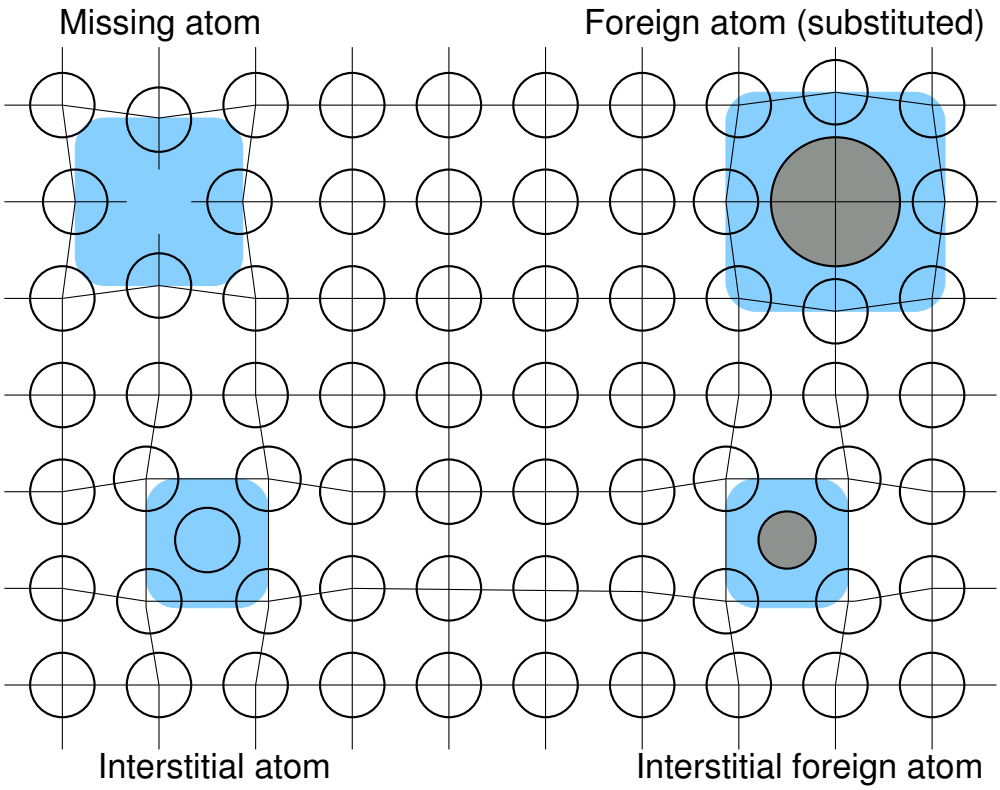


Figure 2.5: Lattice defects in crystalline structures.

On the one side, there are zero-dimensional crystal defects, which separate into lattice vacancies with open bonds, the substitution of a atom by a foreign atom and interstitial atoms (from the crystal or from another material). The lattice vacancies form low energy states and are the most common zero-dimensional defects. Additionally, the missing atom sites are necessary for diffusion processes. The appearance of interstitial atoms is seldom. The activation energy for the generation of inter-lattice atoms is at least one order of magnitude above the one for the generation of lattice vacancies. Usually, foreign atoms are incorporated in the lattice on a lattice node. More often, very small atoms (e.g. H, C, N) are also placed on a lattice interstitial. Due to the atom insertion, strain is induced into the lattice around each impurity. From the electrical point of view, the incorporation of H and C is problematic for device operation. C is often used for the p-doping of the

base layer and therefore intentionally introduced. With the "hydrogen"-effect these C-atoms form also molecules with unintentionally introduced H atoms and therefore reduce the effective dopant concentration [33]. This effect is intensively investigated in further work by CEZARY SYDLO. The diffusion mechanisms in crystalline structures are mainly separated in the diffusion via lattice sites (substitutional diffusion) and the diffusion via inter-lattice sites (interstitial diffusion). Interdiffusion is categorized by the path of the movement into lattice diffusion, grain-boundary diffusion, dislocation pipe diffusion and surface diffusion. A detailed survey on diffusion and interdiffusion mechanisms with semiconductor devices is given in [34] and [35].

Diffusion via lattice places, substitutional diffusion

- Lattice exchange mechanisms:

  The diffusive atom is initially situated on a lattice site. Only a direct exchange with neighboring atoms or a ring exchange is energetically possible in an ideal crystal lattice. The required elastic deformation of the lattice is only possible for high energies. For this reason, this mechanism occurs usually only at temperatures near the melting point of the crystal.

- Diffusion via lattice vacancies:

  In contrary, diffusion processes are easier, if empty places exist in the lattice. The diffusive atom is capable to exchange its place with the lattice vacancy. The elastic deformation is much less than in the first case and thus, requires lower activation energy for the exchange. This is the dominating mechanism for the Cr/GaAs, or Pt/Au interaction

Diffusion via inter-lattice places, interstitial diffusion

- One-step interstitial mechanism:

  This mechanism occurs if foreign atoms are located on lattice interstitials. The activation energy for the movement to the next lattice interstitial depends on the size of the foreign atom. The activation energy is relatively low if the foreign atom is small compared to the lattice atoms because the elastic deformation of the lattice is small. Additionally, this mechanism does not depend on the availability of empty places in the lattice. This can result in high diffusion coefficients, even comparable to those in liquids, e.g. Cu is very diffusive in GaAs due to this mechanism taking place.

- Two-step interstitial mechanism:

  The two-step interstitial mechanism occurs if the impurity atom is to big for a movement between the lattice. In this case, it is energetically better if the foreign atom exchanges its interstitial lattice place with a lattice atom in a first step. In a second step, the foreign atom moves to the next interstitial lattice place releasing the lattice place again enabling a return of the lattice atom to its initial place.

Bulk semiconductor crystal defects

Bulk semiconductor crystal defects are usually incorporated during material growth. One distinguishes between one- and two-dimensional crystal defects in the bulk semiconductor. One-dimensional crystal defects include step shifts (described by the Burgers vector) or screw-type shifts or a mixture of both of it.

Additional there are two-dimensional crystal defects as there are corn-, twin- or packaging defects. Grain boundaries arise if the growth of the metal of the semiconductor was poly-crystalline. The crystals from different seed crystals form a continuous transition from one crystal orientation to the other. The bulk semiconductor crystal defects enhance the diffusivity of other atoms in the crystal lattice as described in the following paragraphs.

Diffusion along defects

The metal contact realized on semiconductor devices is rarely mono-crystalline. The evaporated or sputtered metal layers are polycrystalline because several crystals with different orientation grow starting at seed crystals. Finally they touch at their borders and form a homogeneous metal layer consisting of several crystals. This results in a huge amount of missing atoms and lattice interstitials at the boundaries which support the diffusion via these vacancies. The respective diffusion process is fast because the density of such vacancies is high. This diffusion is also called short-diffusion because it is exponentially faster than the volume diffusion process. Step-shifts also provide a high density of vacancies, which also results in high diffusion velocities. The grain boundary diffusion is the dominating diffusion mechanism for a poly-crystalline metal-layer or metal-semiconductor interface under normal conditions, i.e. operation temperature$\ll$ melting-temperature.

2.2.2 Defects and degradation mechanisms at interfaces

There are three relevant interfaces for semiconductor devices, the atmosphere-semiconductor, the metal-semiconductor and the semiconductor-semiconductor interface. All of them influence the electrical properties of the respective device and are correspondingly optimized for the application of interest. Figure 2.6 illustrates possible device degrading mechanisms in the case of a metal-semiconductor interface in atmosphere.

Atmosphere-semiconductor and metal interface

The atoms at the atmosphere-semiconductor interface have, in contrary to the bulk-atoms, open bounds. This is an energetically weaker state and the reactive surface atoms provide free electrons responsible for surface leakage currents. Additionally, this surface tends to absorb gas- and water molecules from the atmosphere and therefore also changes the electrical properties. In contrary to Si, this mechanism is typical for GaAs and other compounds because it does not form a stable protecting high-quality native oxide at its surface. For this reason an additional passivation layer, e.g. SiO or SiON, cf. section 4.2, is used to protect the semiconductor surface from contamination with atmospheric molecules or the surface is passivated with another semiconductor layer like the base-passivating AlGaAs-ledge in case of HBT, cf. section 4.1.3. In the case of the IHF THz Schottky-diodes this passivation layer was optimized by LIN [23] with the aim to match the thermal expansion coefficients of the SiOx-layer and the GaAs-layer to avoid mechanical stress or even cracking.

Metal-semiconductor interface

The metal-semiconductor interface is the most critical part of a compound semiconductor device. There have been already extensive investigations on the realization of stable contact systems on GaAs for high-temperature applications [13]. An overview of possible degradation mechanisms

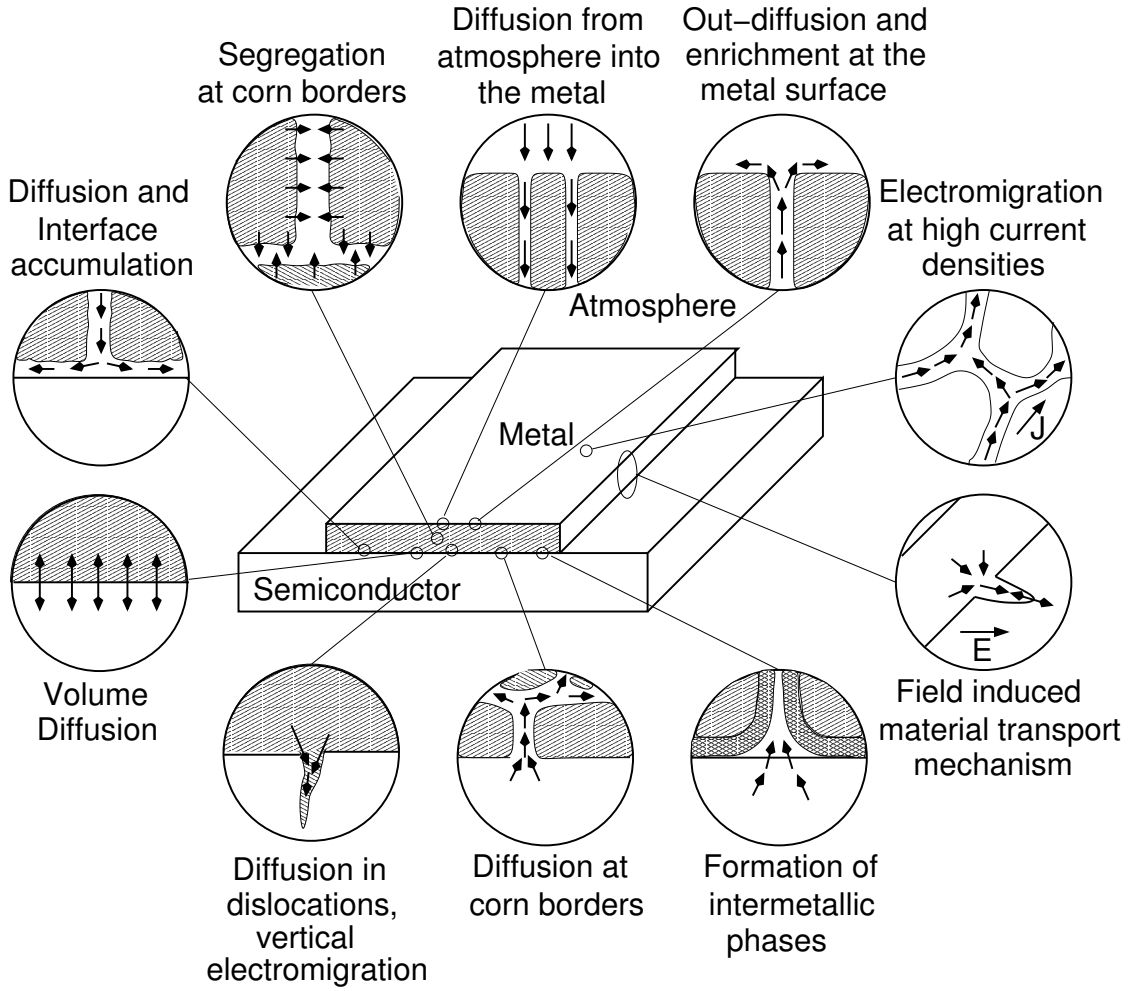


Figure 2.6: Schematic description of metal semiconductor interface defects and degradation mechanisms.

for metal-semiconductor interfaces is given in figure 2.6. These are excited either by electrical or by thermal stress. The electrically activated defect mechanisms are the field and the current-density induced mechanisms (e.g. electro-migration, electron wind effect, metal spiking) [36]. The temperature induced mechanism, which are mainly diffusion processes, are also listed in the following paragraphs.

- Current induced electro-migration, ”Electron wind effect”:

  Electro-migration is defined as the transport of lattice atoms/elements of a conductor in the direction of the electric current flow and mathematically described in section 2.1.5. This effect occurs at very high current densities in metal contacts or wires. The material transport is a result of an impulse transfer from electrons in the conduction band to lattice atoms of the conductor (electron wind effect) [11]. Basic theories state that electro-migration is supported by missing atoms at moderate temperatures. With these missing atoms and the impulses from the electron, the probability is increased that atoms move into the free place in the direction of the current. The vacancies move in the opposite direction. Electro-migration is enhanced at grain boundaries due to the availability of many empty places, which re-

sults in a lower activation energy than for the inner crystal. Electro-migration leads to depleted regions and those with material accumulation. Finally, this may lead to an interruption of the conductor. The threshold current density for electro-migration is in the range of $J_{crit} = 10^4 ... 10^6\, A/cm^2$. These high current densities are reached in very thin conducting layers. The IHF Schottky-diode metalization, for example, is able to withstand current densities up to $J_{crit} = 8 \cdot 10^5\, A/cm^2$, refer to chapter 6.

- Vertical electro-migration, "Spiking":

  Vertical electro-migration, which is also called metal spiking, is the migration of metal into the semiconductor material. This migration mechanism starts very non-uniformly with the formation of metal spikes. The formation of these spikes usually starts along shifts in the crystal and penetrates the semiconductor. The starting point for this process may be hot spots caused by non-uniform current distribution in the metal. At these sites, the metal may even melt and the so formed liquid metal phase easily penetrates the semiconductor, as shown with TLM-structures and Schottky devices in chapter 6.

- Vertical field induced electro-migration:

  Another possibility for the excitation of vertical electro-migration are high electric fields over the metal-semiconductor interface, which is mathematically described in section 2.1.3. In this case, charged particles or empty places are moving following the electric field gradient or vice versa depending on their charge.

- Formation of intermetallic phases:

  Intermetallic phases are formed at the interface between different metals or metal and semiconductor. There is an exchange of atoms from different metals according to the diffusivity of the used materials following section 2.1.4. One can observe this effect also a metal-semiconductor interfaces after out-diffusion, cf. section 2.2.4.

- Out-diffusion and enrichment at the metal surface:

  Forming contacts on compound semiconductors, atoms from the semiconductor surface diffuse out through the metal and enrich at the metal surface. This effect exemplary takes place Forming Pt-contacts on GaAs. Ga diffuses out and enriches on the metal surface. Excess Arsenic remains at the interface and provides deep traps [37].

A two-dimensional defect is the phase boundary between two different materials (phases), which is subject to volume diffusion. This volume diffusion process is intentionally used for the ohmic contact formation, e.g in the Ni/AuGe/Ni-contact system. A thermal post-treatment (annealing) after evaporation provides the diffusion of Ge into the GaAs bulk material and increases the effective doping which results in an ohmic contact.

Semiconductor-semiconductor interface

- Volume diffusion:

  The volume diffusion is the primary degradation mechanism at semiconductor-semiconductor interfaces. In the case of homo-junctions, the dopants from the differently doped regions diffuse and change device characteristics. This effect may be even more pronounced with hetero-junctions.

2.2.3 HBT relevant mechanisms

This section gives details on degradation mechanisms observed for III/V-HBT with respect to the former sections. The primary degradation mechanics for HBT are recombination-enhanced defect mechanisms, bulk lattice defect generation, ohmic contact instability (e.g. base contact migration with AlGaAs-HBT) [38], hot-carrier effects [39] and electro-migration forming e.g. a parasitic B-E[2] diode [40] or B-C[3] diode degradation [41, 42]. The InGaP/GaAs HBT show impressive reliability figures compared to AlGaAs/GaAs, which is mainly due to the surface passivation of the extrinsic base layer (ledge) [43, 44]. With beryllium-doped AlGaAs/GaAs and carbon-doped InGaP/GaAs HBT, an early increase of the gain is observed due to a reduction of the surface recombination at the extrinsic base, which is known as the "*burn-in effect*" [33, 45, 46]. Further degradation is observed resulting in an increase of the base-leakage current [47]. These effects are reported to be as well thermally as also electrically activated [48]. The typical shift of the turn-on voltage U_{be} is designated to the current-induced interstitial Be movement from the highly-doped base to the wide-band emitter, which results in a modification of the B-E junction [49]. The degradation mechanisms, relevant for AlGaAs/GaAs-HBT and InGaP/GaAs-HBT, are detailed in table 2.1.

Failure mode dependence	Failure mechanism	Activation energy, E_A	Current
B-E leakage	Tunneling recombination current due to mid-gap transformation	0.3-0.7	Directly through non-radiative electron-hole recombination
$U_{BE} - Shift$	Hydrogen de-passivation of acceptors in base	0.6	Likely through non-radiative electron-hole recombination
DLD	Dislocation propagation	0.1	Directly through non-radiative electron-hole recombination
Collector resistance increase	AuGe/Ni/Au contact degradation	0.8-1.1	Device self-heating
B-C leakage	Base-metal spiking into collector	1.2-1.8	Device self-heating
B-C short (catastrophic failure; Burn-out)	Base- and/or collector contact degradation followed by localized $R \cdot I^2$-heating, metal and semiconductor melting	0.8-1.8	Device self-heating for initial contact degradation
B-E short (catastrophic failure)	Contact degradation followed by metal and GaAs melting due to localized $R \cdot I^2$-heating	0.8-1.8	Cf. B-C short

Table 2.1: *Summary of degradation mechanisms and the estimated failure mode dependence for HBT as proposed by* HENDERSON.

[2] B-E=Base-Emitter
[3] B-C=Base-Collector

An excellent overview is given by CHRISTIANSON [50]. The first row shows the influence of the failure mechanism on the HBT-characteristics, which is detailed in 6. The degradation of the base-contact due to metal migration or spiking can result in a short of either the B-E diode or the B-C diode, because the base layer is very thin (in the range of 100 nm). This effect is schematically shown in figure 2.7.

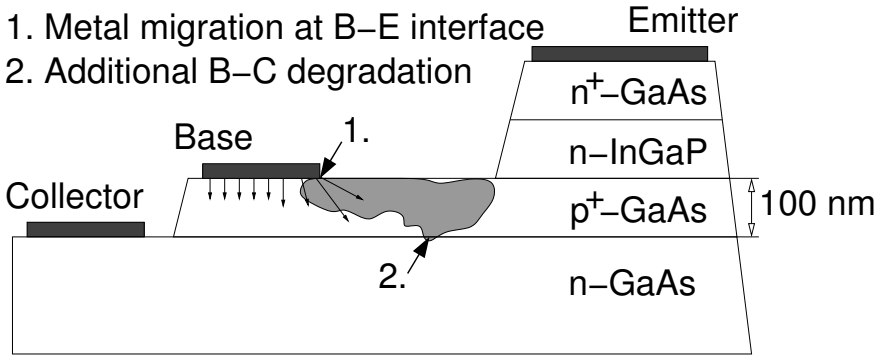


Figure 2.7: Schematic visualization of base-metal migration resulting in a BE-short or in a BC-short.

The dominant failure mechanism for InP-HBT, which is identical to that for AlGaAs/GaAs HBT, is the base-collector leakage current. In the case of AlGaAs/GaAs HBT this leakage current results from implant isolation damages, in the case of InP-HBT it results from the narrowness of the energy gap in the InGaAs collector. Figure 2.8 shows an overview on possible degradation mechanisms with HBT and clarifies the importance of their separation.

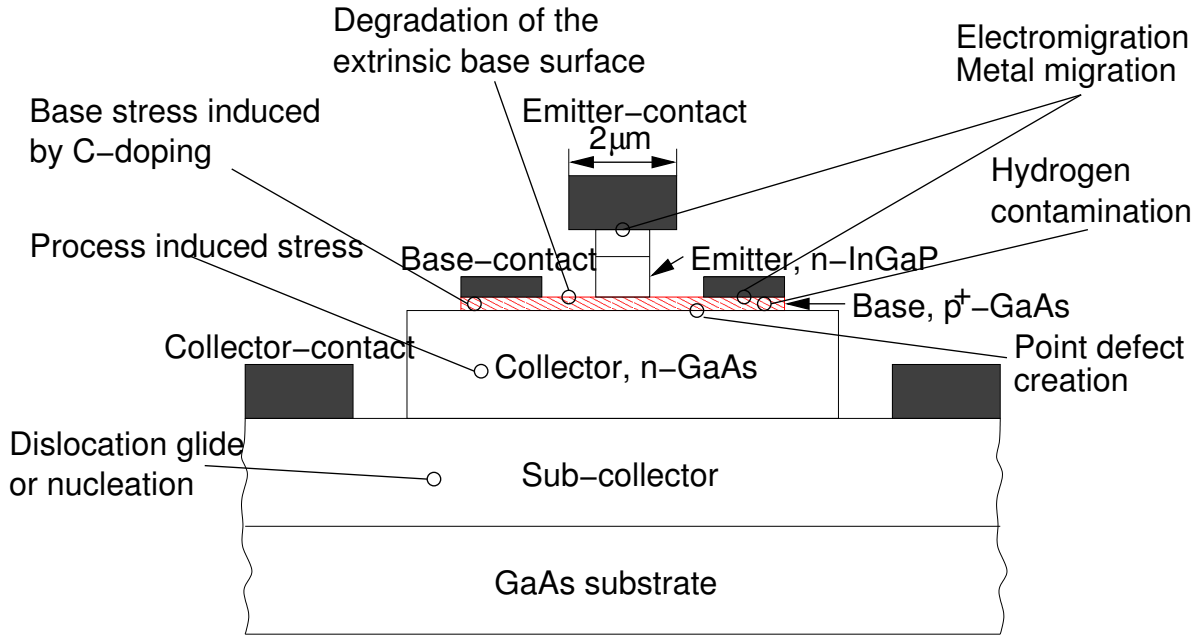


Figure 2.8: Schematic visualization of different degradation mechanisms, which are observed with HBT.

2.2.4 Schottky-diode relevant degradation mechanisms

The investigated THz-Schottky diodes are representative for highest-frequency devices, which are based on a Schottky contact (i.e. III/V-FET type, MESFET[4], HEMT[5]). In case of MESFET and HEMT, gate metal sinking is reported in [42, 51, 52], which results in a reduction of the distance between gate metal and device channel and a change of the gate potential to a more negative value, respectively. Electro-migration effects are reported in [53], being failure mechanisms comparable to the Schottky contact degradation in this work.

In the case of Pt-GaAs Schottky diodes, table 2.2 shows the predominating interdiffusion effects at different stress temperatures and for different stress duration [54]. In this context, BRANDT shows the evolution of Schottky diode parameters with different temperature stress levels using the TLP-approach. There are three temperature regions with distinguishable degradation behavior:

1. for $0\ ^{\circ}C < T < 150\ ^{\circ}C$ an improvement of the ideality factor η ("burn-in"),
2. for $160\ ^{\circ}C < T < 400\ ^{\circ}C$ an increase of ideality factor η and saturation current, I_{sat},
3. for temperatures $T > 400\ ^{\circ}C$, device failure.

Temperature, T / $^{\circ}C$	Stress time, t / min	Result from X-Ray diffractometry
200	5000	Pt and GaAs, no intermetallic phase
	6000	initial $PtAs_2$ formation
250	60	significant $PtAs_2$ formation, no change in Pt-seed cell
300	15	significant $GaPt_3$ formation, additionally GaPt and $PtAs_2$ detectable, modification of Pt microstructure
	30	strong GaPt- and $PtAs_2$ formation, no $GaPt_3$ except (111)
	60-150	only week $GaPt_3$ formation
	240	$PtAs_2$ and GaPt formation predominates, slight $GaPt_3$ super-lattice
	300	only $PtAs_2$ and GaPt formation

Table 2.2: *Thermally activated interdiffusion effects observed with Schottky contacts as proposed by* MURARKA.

This is supported by GRÜB in [55] who reports a "*burn-in effect*", in this case a slight reduction of the ideality factor and series resistance, for Schottky diodes under electrical stress due to modifications of the platinum morphology at the Schottky interface. The work of RODRIGUEZ shows the formation of a variety of intermetallic phases and complex reactions at the metal semiconductor interface during electrolytic Schottky contact formation [56]. This effect is comparable to the Ga oxidization and out-diffusion, even trough SiO_2, and the generation of excess As as it is reported

[4]MESFET=Metal Semiconductor Field Effect Transistor
[5]HEMT=High Electron Mobility Transistor

for electrical and thermal stress in [57–61]. Degradation by field- and current-induced metal migration and contact melting at local hot-spots using electrical overstress is reported in [58, 62–64].

In addition to the interdiffusion effect, this work analyzes electrically excited degradation mechanisms using the TLP-method with respect to the fabrication technology. According to the schematic cross-section of a IHF-Schottky diode, TEM[6] analysis after FIB[7] preparation, cf. section 6.5.6, reveals the following reliability relevant features and effects (which are partly exaggerated in figure 2.9). These effects are listed in the following and result either from technological imperfection or from thermal/electrical stress.

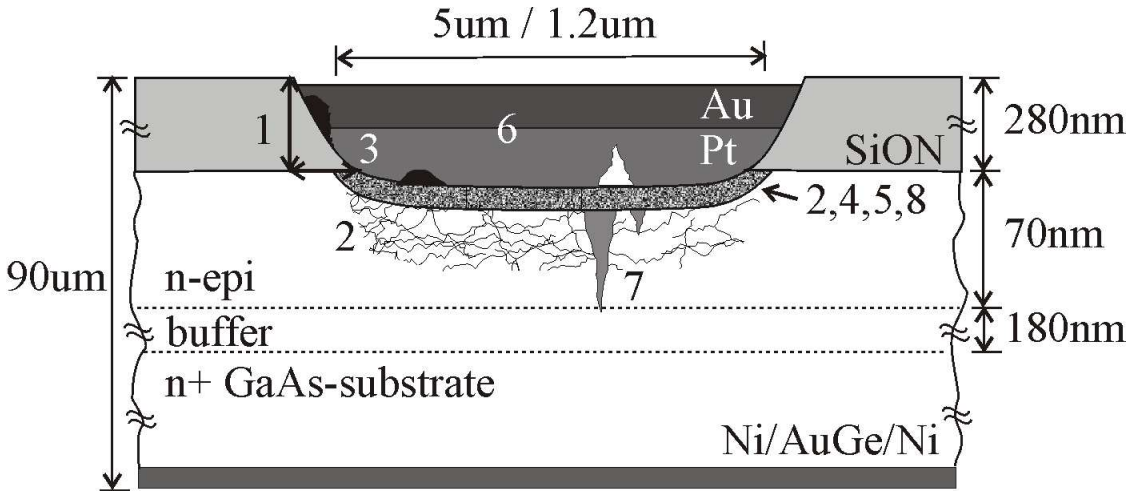


Figure 2.9: Imperfections of the Schottky contact after formation due to fabrication technology.

1. Aspect ratio of the anode opening in comparison of SF_6-plasma etching and CHF_3-RIE[8],
2. Contamination (residuals and redeposition products due to etching processes),
3. Radiation surface damages due to ion bombardment as a result of etching processes (e.g. defects, dislocations),
4. Oxidation / amorphous semiconductor surface,
5. Modification of the chemical composition (stoichiometry) of the semiconductor surface due to the fabrication process (Contamination, reaction / interdiffusion of metal/GaAs, outdiffusion / formation of excess arsenic),
6. Pt/Au crystallization, cluster formation,
7. Degradation effects, e.g. interdiffusion at the metal/semiconductor interface (spiking,
8. Hydrogen desorption, elevated Si concentration at the junction.

[6]TEM=Transmission Electron Microscopy
[7]FIB=Focused Ion Beam
[8]RIE=Reactive Ion Etching

Chapter 3

Accelerated Reliability Analysis

The purpose of reliability analysis is the determination of lifetime reducing defect- and degradation mechanisms and a precise estimation of device lifetime. In the development phase of new devices, technologists require a fast feedback from reliability investigations. In this sense, accelerated reliability tests are obligatory because semiconductor device lifetime can be in the range of several years. It is evident that fast accelerated test methods abbreviate the time required for reaching product maturity and allow shorter innovation cycles. The problem is the trade-off between test acceleration and the seriousness of extracted lifetime data. Comparability must be ensured between degradation/defect mechanisms under normal operating conditions and those excited by accelerated tests [65].

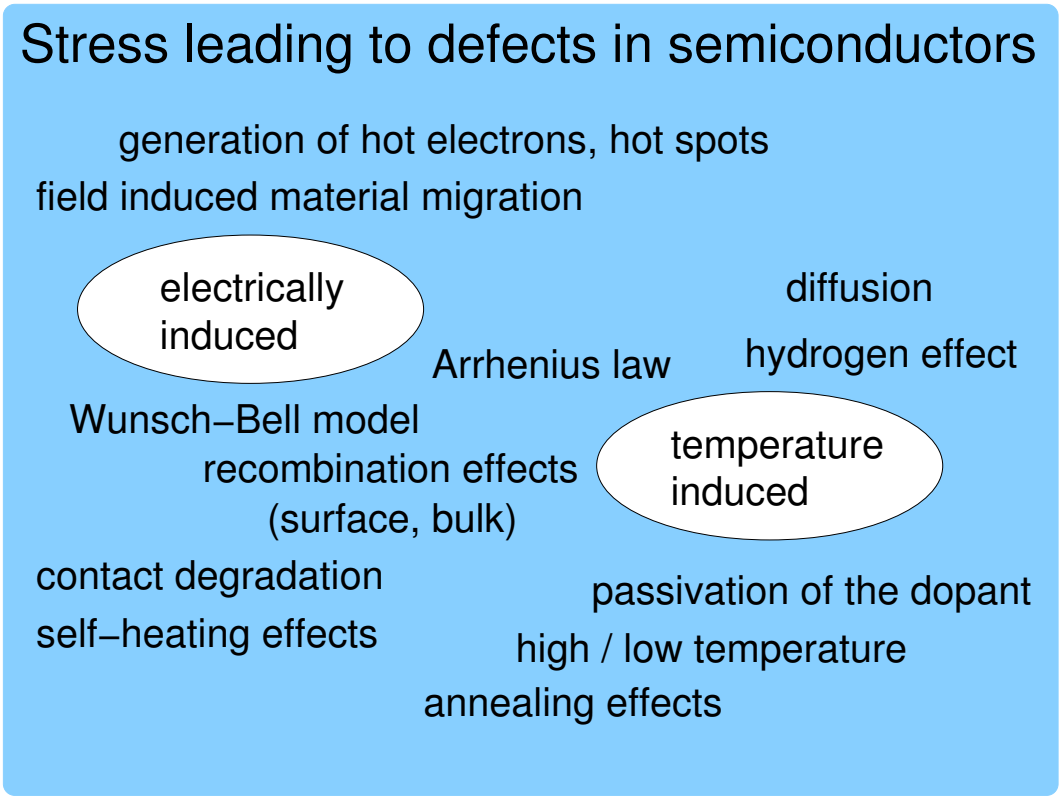


Figure 3.1: Defects and degradation mechanisms with semiconductor devices.

Figure 3.1 schematically shows the dependence of possible degradation mechanisms from thermal or electrical excitation. Generally, there is a sliding transition from pure electrical stress, electro-thermal to thermal stress, which does not allow a strict separation. It must be mentioned, that the industrial standard is set by the Arrhenius-based stress tests which use an elevated temperature and DC-level as stress parameters for acceleration. Section 3.1 will discuss the limit of this method, the advantages and the disadvantages. In comparison, section 3.2 describes the Transmission Line Pulse (TLP)-method which is based on elevated current density as acceleration parameter without increased thermal stress.

The acceleration is usually based on a stress increase, which can be thermal, electrical, mechanical or radiation stress depending on the application of the device. Section 3.1 and 3.2 concern the accelerated electrical stress and compare the industrial standard method with an alternative test methodology, the Transmission Line Pulse (TLP) method, for very fast acceleration. The required electrical diagnostic tools are comparable for all accelerated stress methods and described in section 3.4. The diagnostic section is essential for degradation monitoring and determination of the defects occurring in the device. Section 3.3 shows the TLP-test approach as it is used for stress tests with HBT and Schottky devices. Further, section 3.3.1 denotes the relevance of devices thermal time constants and sections 3.3.2 and 3.3.3 explain the approaches for the excitement and separation of different degradation mechanisms and the limits of its application.

3.1 Conventional Arrhenius-based accelerated method

Standard reliability tests are based on the Arrhenius law [26] and use temperature and DC as acceleration parameters. An industrial standard specification for the reliability of semiconductors is exemplary set with time to failure, $t = 6000\ h$, at an increased temperature of $T = 180\ ^{\circ}C$ and increased current density $J = 80\ \frac{kA}{cm^2}$. The Arrhenius approach allows the approximation of lifetime by determining activation energies for different degradation mechanisms, cf. section 2.1.2 and 2.1.5. Semiconductor manufacturers usually give reliability data and failure probability for their components in the respective data-sheet. These data are based on the test of several identical samples with increased electrical and thermal stress and the extraction of the mean lifetime under the different stress conditions. These results are extrapolated to the specified operating temperature T_0 using a modified form of the Arrhenius law, cf. equation 3.1.

$$T_M(T_0) = T_M(T_1) \cdot e^{\frac{E_A}{kT_1}\left(\frac{T_1}{T_0}-1\right)} \tag{3.1}$$

This method has two main disadvantages. The first is the long duration of the experiment (e.g. a test time of 1000 hours, which is still shorter than lifetime under normal operating conditions) for a conservative extrapolation. The second is the excitation of several degradation mechanisms without the possibility to determine the dominating one. In other words, the effect with higher activation energy screens effects occurring at lower temperatures. Using this approach, dedicated stress of device interfaces is not possible because power dissipation is high in the parasitic elements, e.g. device periphery or substrate, due to its high thermal mass. With increased temperatures, there is the risk of shifting the failure mechanism occurring under normal operating conditions to a new one with higher activation energy, which was previously not effective. Another problem is the change of material properties with temperature, which may result in strain-, diffusion- or dislocation increase [65].

The Arrhenius-based degradation models are always based on the parameters temperature and time and do not consider temperature independent mechanisms, e.g. electrically induced mechanisms. Though the Arrhenius-based degradation modeling is widely accepted for lifetime prediction there are many questions, which can not be answered for present-day complex electronic components: How can different simultaneously occurring degradation mechanisms be separated? How can one be sure that identical degradation mechanisms are excited with different temperatures? How are the degradation mechanisms at higher temperatures related to those under operating conditions? The well-directed stress of device elements is the motivation for the application of the TLP-method as detailed in the following sections.

3.2 Transmission line pulse method

The transmission-line pulse method (TLP) originates from ESD-testing approaches [66] using cable-pulse generators for the generation of very short electrical pulses (historically, first tests with electrical pulses were based on Hg-switches). Actually, there are several competing electrical stress approaches like the human-body model (HBM), the machine model (MM) the charged device model (CDM) and the very fast transmission line pulse method (VFTLP). The TLP-method is based on transient electrical stress of devices beyond their specified operation conditions. First approaches to this method were done by Dwyer and Franklin [51, 52, 63] in 1990 and Brandt [14] in 2000. Franklin was limited by a minimum available pulse length $t_{p,min} = 500\ ns$ and therefore was not capable to apply electrical stress significantly shorter than the devices thermal time constant. Brandt proposed and introduced the application of the TLP-method in it's current form and firstly tested it for a directed excitation of degradation mechanisms, in this case, field- and current induced material transport mechanisms. With the latest developments, even a draft standard is available from *http://www.esda.org* since 2004 [67].

This work describes the methodology of the TLP-method for the excitation of degradation and ageing mechanisms comparable to those with Arrhenius-based methods and shows for the first time comparative measurement results. The advantage of the TLP-method is the very high acceleration factor and the test flexibility without the requirement of a climate chamber as it will be detailed in section 3.3. The design of an automated measurement set-up, cf. section 3.4.1, allows automated stress and analysis cycles on-wafer without re-contacting. The measurement set-up is designed to allow on the one side high current/voltage state for the stress cycles with proper matching for the electrical pulses, and, on the other side to perform high-precision measurements in the pA-range. The employed pulse generator is a HP 8114A, which offers a minimum rise- and fall-time of $t_{rise} = t_{fall} = 4\ ns$ and a minimum pulse length $t_{p,min} = 8\ ns$.

The pulse voltage and current is limited by a maximum open source pulse voltage, $U_{p,max} = 100\ V$ and a maximum pulse current $I_{p,max} = 2\ A$, respectively. Pulsed stress allows to adjust various stress test parameters for flexible testing and well directed excitation of defect mechanisms, cf figure 3.2, which are:

- the pulse length, t_p / ns,
- the pulse amplitude, U_p / V
- the duty cycle, $\frac{t_p}{T_0}$,
- pulses per test cycle, N.

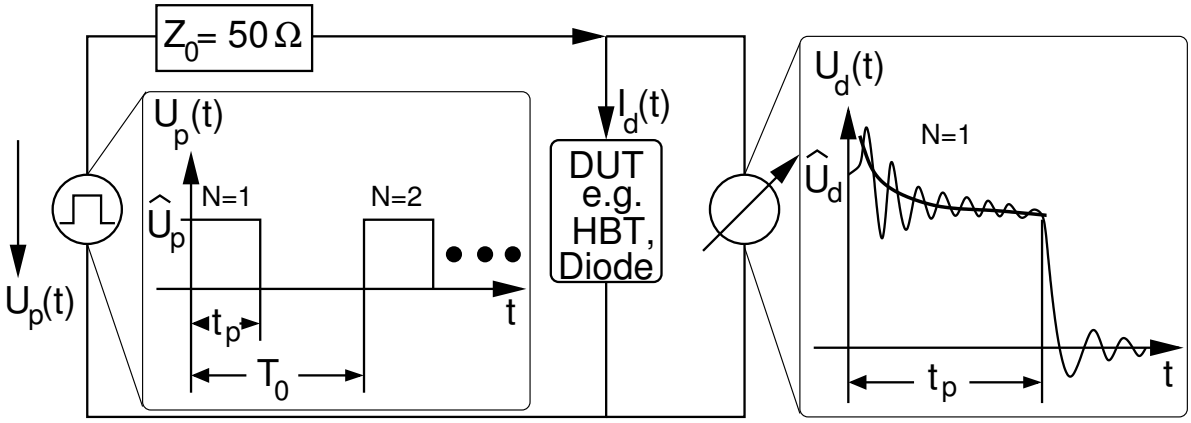


Figure 3.2: Basic approach for applying pulses to DUT.

This pulsed method is based on non-thermal acceleration of defect mechanisms. Therefore, the pulse length is chosen significantly shorter than any thermal time constant of the device [68]. Figure 3.3 schematically shows the applicable power as a function of the pulse length according to the WUNSCH-BELL-approach as detailed in the following.

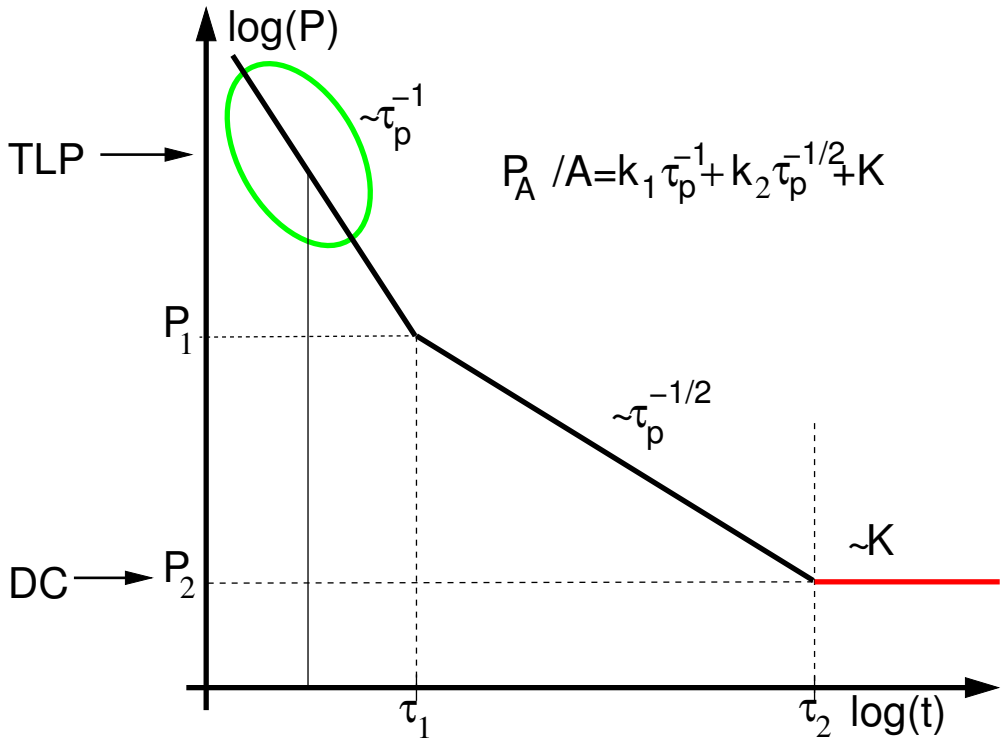


Figure 3.3: Applicable electrical power P as a function of the pulse length t_p following the WUNSCH-BELL*-approach.*

The diagram is divided into three parts, which are identified by

- the devices intrinsic time-constant τ_j^{th} (e.g. the junction)

- the peripheral time-constant τ_p^{th} (e.g. air-bridge, contact metalization, substrate).

In fact, with this method, using electrical pulses with a pulse length $t_{pulse} < \tau_p^{th}$, the thermal power is completely dissipated in the junction as the periphery is unable to act as a heat sink. The device is operated under adiabatic conditions. In this range the applicable power follows a $t_p^{-\frac{1}{2}}$-relation. Choosing a pulse-length smaller than the intrinsic time-constant, theoretically, any thermal stress is excluded and only electrical degradation mechanisms are excited. The corresponding range is characterized by a t_p^{-1} applicable power to pulse-length ratio. It is evident that this method is also applicable for Arrhenius-based tests, if the pulse-length is chosen significantly larger than the devices outer thermal time constant and therefore device heating is possible and can be calculated, cf. section 4.2.5. The excitement of different degradation mechanisms is explained in the sections 3.3.2 and 3.3.3.

A long pause between two pulses ensures that consecutive pulses do not lead to an increase in mean temperature. Corresponding experiments with Schottky devices are shown in 6.5.5. The acceleration level depends on the current densities applied to the device during stress. The maximum acceleration factor is limited by coarse degradation, which shows a very sharp threshold for its excitement for the tested devices, as shown in chapter 6.

In the framework of the Brite-Euram-project HERO'S, this limitation with HBT is found to be the contact stability and the emitter ledge quality [14]. Deficiencies are revealed for these parts of the device by determining the threshold for this kind of degradation and resulted in an optimization of the metalization and the emitter ledge, cf. section 2.2.3. These degradation mechanisms are not directly relevant for lifetime but negatively influence device performance. During experiments it turned out that bad-performing devices also have a low lifetime. Measurement parameters are varied for excitement of lifetime relevant mechanisms [48, 69] and to avoid coarse degradation. The separation of degradation mechanisms is possible by adequate choice of stress parameters as detailed above. The excitation parameters for degradation mechanisms using the TLP-method are the following:

- the electrical power density, P_D,
- the electric field, E,
- the current density, J,
- for longer pulse length the temperature, T.

A further advantage of the TLP method is the additional information provided by the pulse response which reveals device degradation or breakdown in real-time. Section 3.4 explains the details of the respective measurement set-up and the required analysis instruments. The main disadvantage of the TLP method is the lack of reputation in industry because there is no experimental TLP data available. In this sense, the TLP method has to compete with long established reliability prediction methods. Section 3.3 explains the basic TLP test approach required for the excitation of degradation mechanisms which are comparable to those from Arrhenius-based stress tests.

3.3 TLP test approach

The TLP test approach consists of different parts as indicated by figure 3.4. Initially, a device dependent stress type is defined for each kind of device (e.g. base-emitter-stress in the case of a HBT in forward direction). This stress type is chosen adequate for the potential weak points of the device (e.g. the hetero-interface). In case of the Schottky-diode, a stress of the junction in forward direction allows an evaluation of the Schottky interface stability.

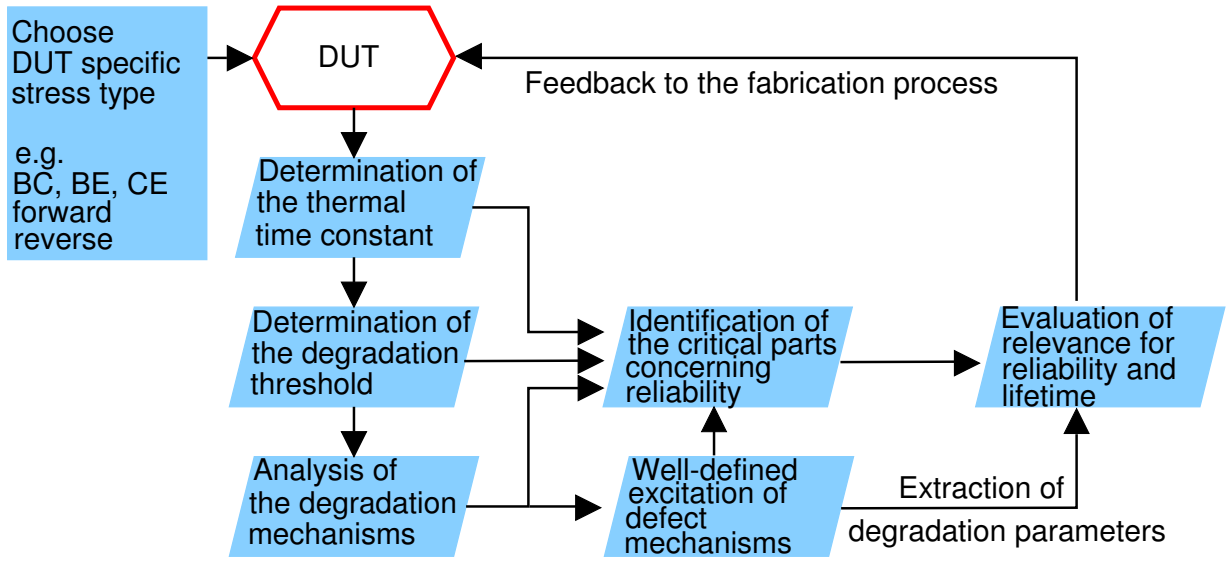


Figure 3.4: TLP test approach for one- and two-port devices.

The next step is the extraction of the thermal time constant which allows the adjustment of the pulse length, c.f. section 3.3.1. The further test approach is based on the knowledge of the well-directed excitation of different degradation mechanisms by adjustment of the test parameters. The target of the TLP test is the excitation of degradation mechanisms which also occur under normal operation conditions and are comparable to those excited with Arrhenius-based stress tests. In contrary to the Arrhenius-based stress, the TLP-method is based on electrical stress and thermal stress is avoided as far as this is possible. This is ensured determining the thermal time constant of the DUT as it is described in the following for one-port devices, e.g. Schottky diodes and two-port devices, e.g. HBT, cf. section 3.3.1.

Secondly, the limit for the application of the TLP-method is set by the stress level for which coarse degradation by current- or field induced failure mechanisms occurs. Using the pulsed step stress approach, c.f. section 3.3.2, a sharp threshold can be found at which devices fail. At this stage, the stability of metal contacts is evaluated for high current densities and/or electric fields and the responsible degradation or failure mechanisms are determined. With this knowledge, the accelerated test starts keeping the stress level significantly below the stress level, for which coarse degradation is observed. This allows electrical ageing of the device with degradation comparable to Arrhenius-based stress tests. Finally, after device degradation, the degradation mechanisms are analyzed and their impact on device reliability and lifetime under normal operating conditions is evaluated. Section 6.5.1 shows the TLP test approach for IHF THz-Schottky diodes and section 6.2 the one for HBT.

3.3.1 Determination of thermal time constants

The thermal time constant characterizes the thermal properties of a device. The thermal conductances and capacitances depend on device geometry and the location of heat sinks. A thermal equivalent circuit consists of thermal resistances R^{th} and thermal capacitances C^{th}, comparable to an electrical equivalent circuit. Usually, these are separated into the intrinsic resistance R_i^{th} and capacitance C_i^{th} and the peripheral resistance R_p^{th} and capacitance C_p^{th} [70]. The thermal time constant forms to equation 3.2 and is a measure for the devices thermal time response after thermal excitation. The devices intrinsic time constant $\tau_{th,i}$ is usually orders of magnitude smaller than their peripheral time constant $\tau_{th,p}$, as explained in section 3.2.

$$\tau_{th} = R^{th} \cdot C^{th} \tag{3.2}$$

The TLP test starts with the determination of the devices thermal time constants. This ensures that the electrical pulse length t_{pulse} is significantly smaller than the devices intrinsic thermal time constant $\tau_{th,i}$ for the following stress tests and the device is operated under adiabatic conditions. Additionally, an analysis of the devices thermal characteristics is possible with the following approach.

The thermal time constant is extracted measuring the pulse-response $U_p(t)$ of pulses with a pulse width $t_p = 500\,ns \ldots 10\,ms$. The exponential decay or increase of $U_p(t)$ determines the thermal time constant of the specific device, shown in chapter 6. Stationary operating conditions are reached at the end of the pulse (for example $U_p(10\,ms)$, i.e. $U_p(t \to \infty)$), which determines the maximal temperature T_{max}. The thermal resistance R_{th} is determined in combination with the electrical power at the end of a pulse with sufficient pulse length (e.g. $P_{el}(t = 10\,ms)$) to $R_{th} = \frac{\Delta T}{P_{el}}$.

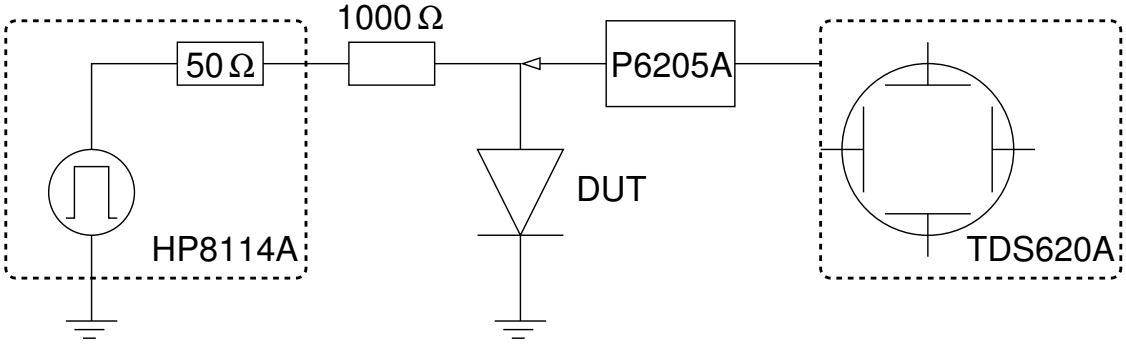


Figure 3.5: Principal measurement set-up for the determination of the thermal time constant for unipolar devices.

In the case of unipolar devices like TLM-structures and diodes the set-up for the extraction of thermal time constants is as follows. A sequence of pulses with sufficiently high amplitude, sufficient pulse length and adequate duty cycle (e.g. $U_p = 80\,V$, $t_p = 20\,\mu s$, $d = 1:1000$) is applied to the DUT in series with a resistance $R \gg R_{DUT}$ (e.g. $R = 1000\,\Omega$), which emulates a current source. The voltage response is monitored using a digital oscilloscope (e.g. TEKTRONIX TDS620A, bandwidth=500 Mhz) with active probe (TEKTRONIX P6205A, bandwidth=600 MHz) and can be used for the extraction of the thermal time constant by fitting it to analytic functions. Figure 3.5 schematically shows this approach.

In the case of two-port devices, e.g. a HBT, the thermal time constant is determined using the principal measurement set-up detailed in figure 3.6.

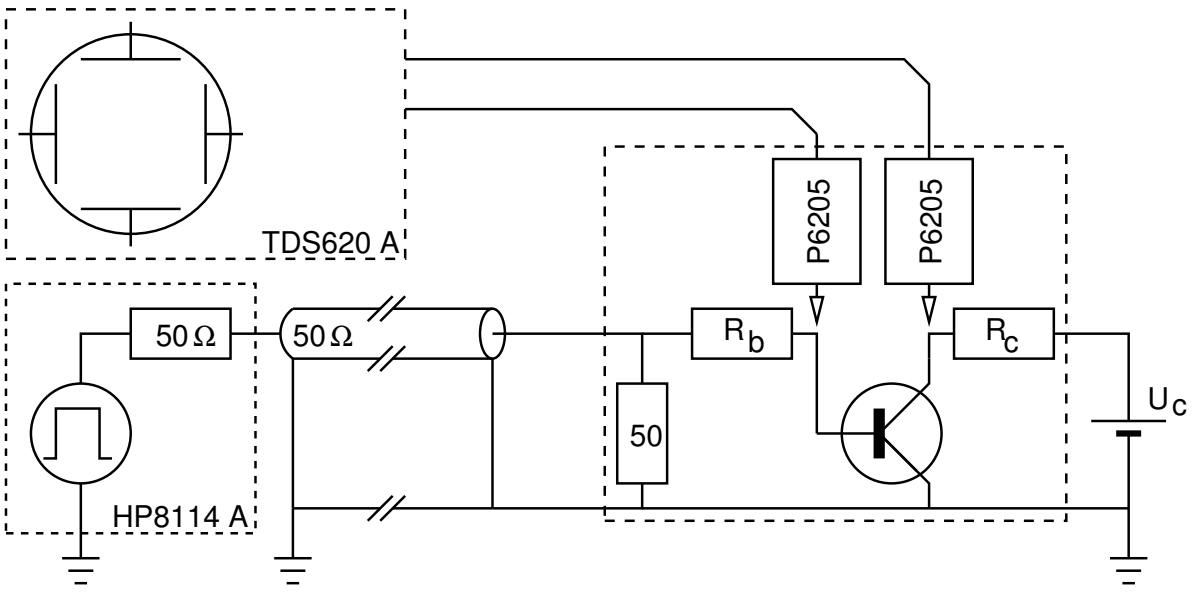


Figure 3.6: Principal measurement set-up for the determination of HBT thermal time constants.

The thermal time constant of a diode- or transistor junction can be used to roughly estimate the temperature in this region during the pulsed stress. Additionally the thermo-electrical coupling factor has to be determined.

Figure 3.6 shows the measurement set-up which is modified device dependent for the extraction of this constant: A collector voltage is applied to ensure that the bigger portion of the heating current results from the collector current. This is necessary to avoid heating of the base series resistance, which leads to a second thermal time constant. The external base resistor has to be higher than the dynamic resistance of the base emitter diode in the chosen bias point to measure the change in the base-emitter voltage more sensitively. Besides, the higher external base resistor can be used to adjust the base current more precisely. A thermal time constant of the junction has be determined for the RF-HBT to be about $1\,\mu s$, as detailed in chapter 6.

3.3.2 Excitation of field and current induced degradation mechanisms

The approach for the excitation of field and current induced degradation mechanisms using electrical overstress, cf. section 2.2.2, is called in the following "pulsed-step stress test". This name already indicates the basic procedure as it is introduced in [14]. The electric field and the current density are a function of the pulse voltage amplitude. A step-wise increase of the pulse voltage with subsequent analysis of characteristic parameters, cf. section 4.2.3 and 4.1.2, allows a precise determination of the threshold for these degradation mechanisms, which is schematically shown in figure 3.7. The real-time pulse-response additionally allows the extraction of the voltage at the DUT and the current for the extraction of dissipated power and the calculation of the current density. The extraction of the acceleration factor is done using the approach described in section 2.1.5 using the measured current-densities and extracted junction temperatures. BRANDT already showed respective results and compared them to Arrhenius-based stress tests [54, 55, 61]. The disadvantage of this approach is the lack of information about the device degradation history.

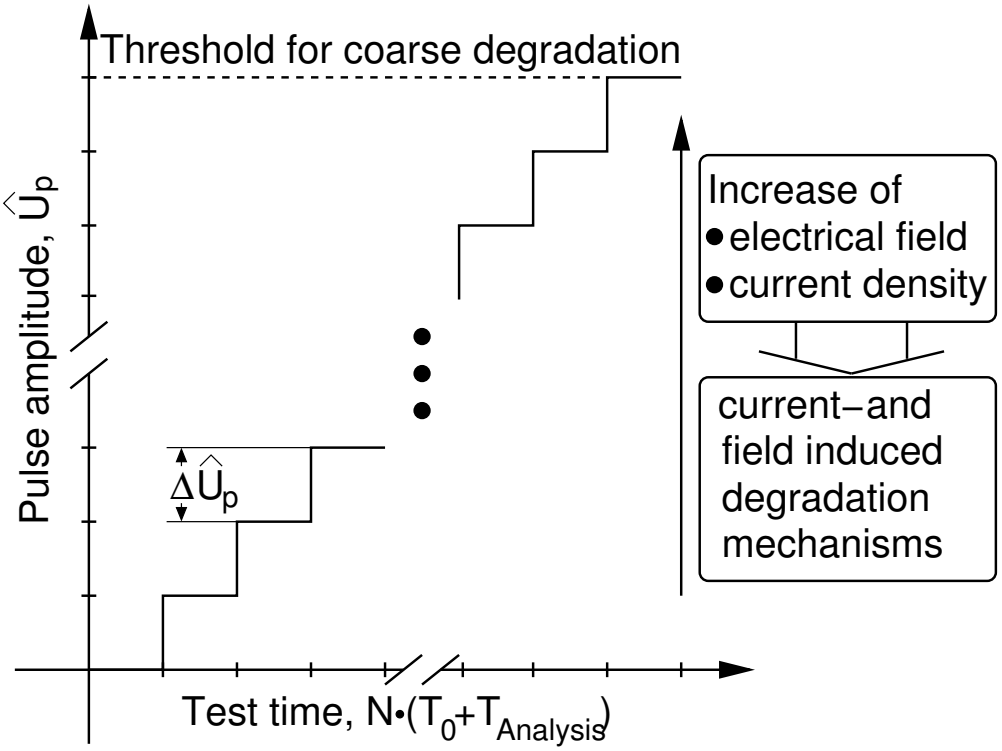


Figure 3.7: Pulsed step-stress test approach.

3.3.3 Excitation of diffusion and ageing processes

Up to now, there was no methodology available for the excitation of diffusion or ageing processes, cf. section 2.2.1, using pulsed electrical stress. Thus, this work concentrates on the development and the verification of such a procedure. The solution to this problem is the application of a set of pulses N with linerarily or logarithmically spaced analysis cycles. The logarithmic increase of the pulse number emerged to be the optimal approach for the excitement of device degradation without loosing information about the degradation history. Mathematically, this approach is justified in

section 2.1.1, which allows the definition of a safety margin for coarse degradation. The main parameter for the excitation of diffusion or material ageing processes is the number of pulses N in combination with the duty cycle $\frac{t_{pulse}}{T}$. A modification of these parameters allows a sliding transition between pure electrical and coupled thermo-electrical excitation of diffusion and ageing processes, cf. results for Schottky devices in section 6.5.5. The pulse-voltage amplitude is set to a value significantly below the extracted threshold for coarse degradation by field- and current-induced degradation as described in section 3.3.2. The main advantage of this approach is the monitoring of the device degradation history as a function of the number of applied pulses.

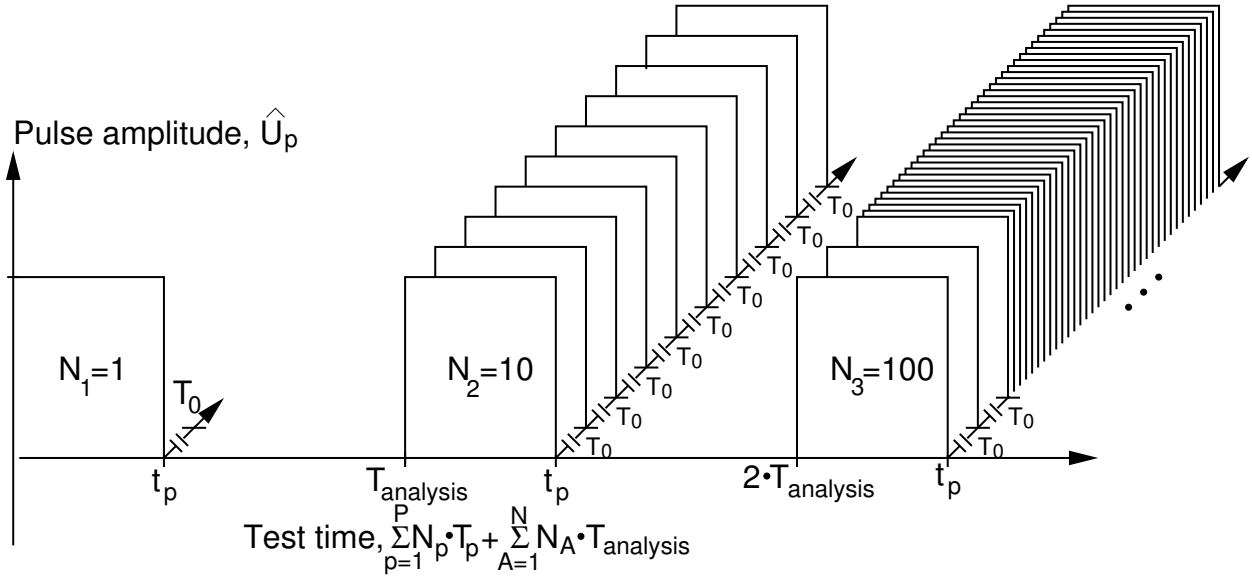


Figure 3.8: Application of pulse sequences for the excitation of electrical ageing and degradation.

3.4 Diagnostics

The main task of the diagnostic section is the description of the realized measurement set-up, cf. section 3.4.1, which allows TLP-stress and analysis cycles without manually re-contacting the device for a constant, reproducible test environment with respect to contact resistance. Devices are characterized by measurements of electrical parameters which are either extracted from IV-, CV- or noise measurements and may slightly change by re-contacting. This is not acceptable because device degradation is monitored as the change of these characteristic parameters as a function of time or the number of pulses. Usually, the change of device parameters is in the range of only few percent in the case of degradation and should not be influenced by other factors. In the case of whisker-contacted Schottky diodes, re-contacting is even not possible because it is un-probable to contact the same diode in a honeycomb array twice due to their small anode diameter ($d_a = 0.8\,\mu m$). The relevant parameters and their extraction from measurements is shown in the subsections 3.4.4, 3.4.5 and 3.4.6. In the case of the Arrhenius-based accelerated tests, these measurements are performed only once a day even manually and do not necessarily require any automation. For the TLP-method, the stress- and analysis cycles are much shorter with increasing acceleration of the

ageing tests. In consequence, automation of the set-up is necessary for detailed analysis of the degradation behavior as shown in section 3.4.1.

3.4.1 Automated measurement setup

The automated measurement setup is realized based on the concept presented in [14,71]. The main feature is the capability of automated stress and analysis cycles on-wafer level. The respective work is separated into the development of the software section based on Labview of NATIONAL INSTRUMENTS and the hardware design and realization part. The challenge for the automation consists in the connection of sensitive measurement instruments with diverse requirements (e.g. IV-,CV-measurements) on the one side and current or voltage pulse sources with high output levels and real-time pulse-response monitoring on the other side. The solution is the development of a switching matrix and a probe head providing a proper connection of a device to each instrument for the respective task (e.g. pulsed stress, IV-analysis), resulting in a measurement setup shown in figure 3.9.

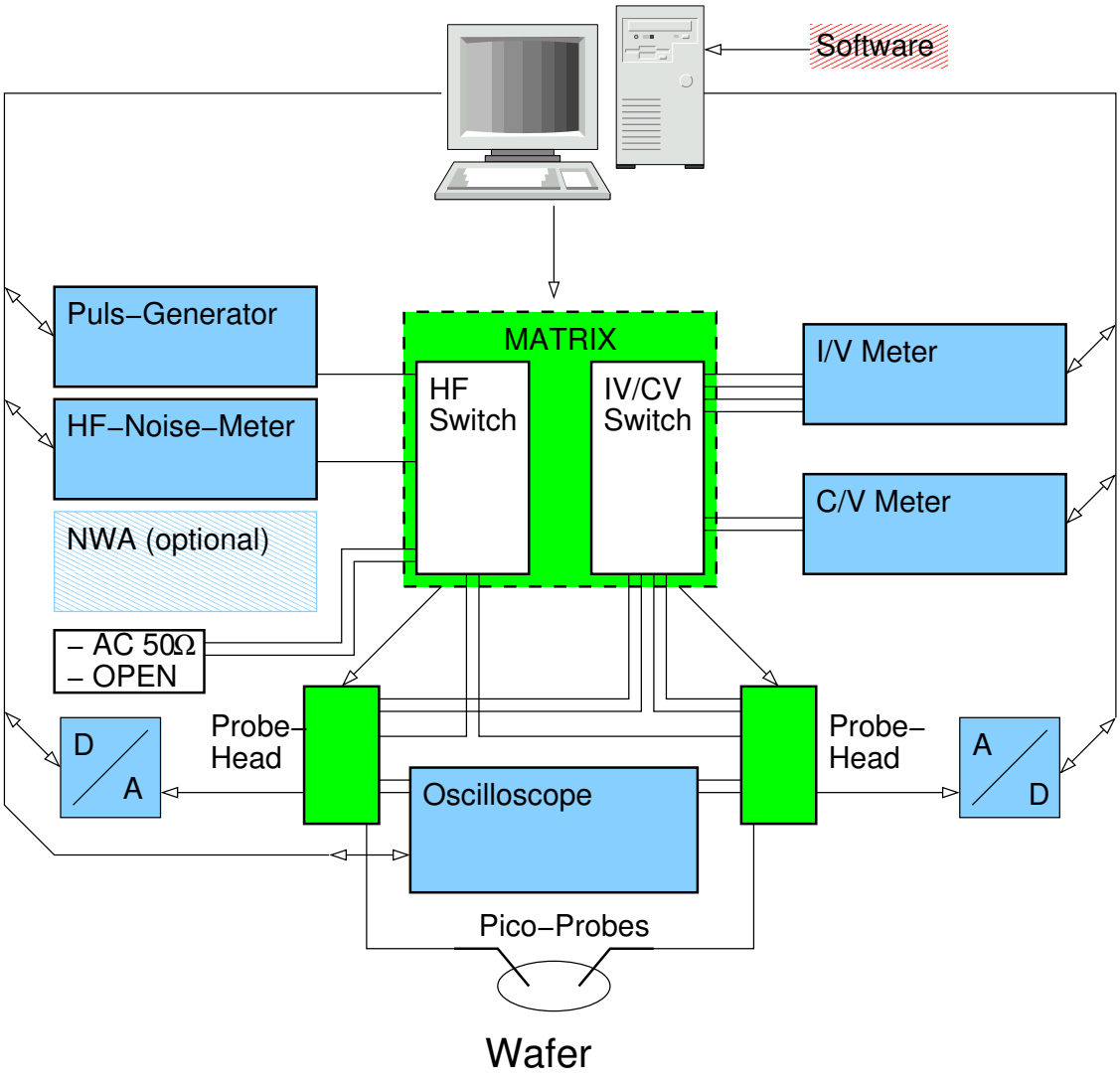


Figure 3.9: Principal measurement setup.

The software development is based on the graphical programming interface of LABVIEW 5.0. The programming is performed in a modular way as far as this is possible using LABVIEW. The interface to the instruments is the HP-IB bus, the matrix-switch and the probe-heads are controlled by a NATIONAL INSTRUMENTS PCI-card, which also allows AD-conversion. Originally, this feature was foreseen for the analysis of the 1/f-noise in combination with ultra-low-noise amplifiers (ULNA) in the probe-heads developed at the TECHNISCHE UNIVERSITÄT CHEMNITZ. Unfortunately, there are some limitations for this application. Firstly, the ULNA's require a settling time of at least 3 minutes and secondly, the dynamic range of the AD-conversion section is not sufficient. Due to these limitations mainly the switching capabilities of the probe-heads are used.

3.4.2 TUC ULNA

The probe-head design attacks a number of issues in one box. Firstly, a voltage divider for voltage measurements and a 1 Ω resistor for current measurement are located directly next to the microstrip line (semi-rigid cable RG-58). By this, the series inductance responsible for system oscillation is efficiently reduced. The connection lines for the I/V and C/V measurement, as well as those for the ULNA are shielded. This improves the dynamic range of the I/V measurement and reduces leakage currents, due to the instrument's canceling facility. In the case of C/V measurements, the effect is even more pronounced, such that only by introducing these lines it is possible to measure capacitance values down to several fF with an accuracy of approximately 0.1 fF. The simplified schematic diagram of the circuit with this functionality is sketched in 3.10

3.4.3 Switching matrix

The switching matrix is specially developed for the application of the TLP-method in combination with the required measurement instruments for device analysis. It performs on the one side adequate coupling of the pulse generator to the device and features the capability of real-time pulse-response measurements isolating the very sensitive measurement instruments at the same time. The switching matrix is realized with three printed circuit boards for the control of the different switching sections by a NATIONAL INSTRUMENTS DA/AD[1] PC controller card. The first board controls the IV/CV switching section with the integrated switches[2]. The second one is the coaxial switch driver board for the control of the SR-2 Min-H coaxial switches[3]. The third board controls the single pole 5 throw, 5 times coaxial switch[4].

The complete RF section employs asymmetrically grounded SMA-compatible interconnections and is designed for a frequency range up to 18 GHz for network analyzer measurements. The probe interface is formed by two PICOPROBE Model 40A coplanar probes which are connected to the TUC probe head. The two outputs of the probe head can be switched to the different measurement channels by two SP5T1 coaxial relays. The pulse generator can be connected either to the left or to the right coplanar probe for a flexible selection of stressing procedures. In the case of transistors, switching between B-E stress and C-E stress during the reliability tests requires this feature. Especially the entire coaxial interconnections are of great importance for the pulse response measurement and for the avoidance of device/system oscillation. The IV/CV section of the switching matrix is demonstrated in figure 3.11. For the IV measurement, a ground-free configuration of the

[1] DA/AD=Digital Analog/Analog Digital
[2] OMRON
[3] RLC ELECTRONICS (MT Kisko New York)
[4] HP 8768 K, SP5T

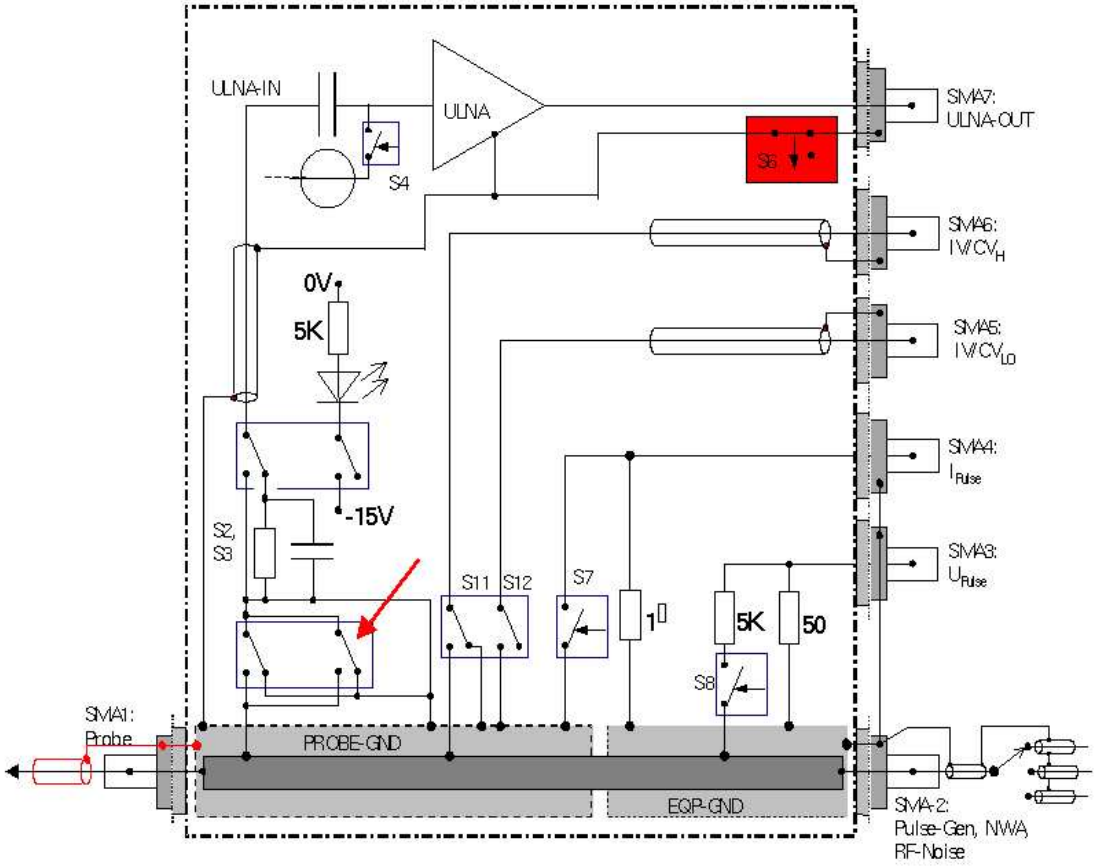


Figure 3.10: Schematic representation TUC probe-head.

probes has to be provided. The potential grounding conflict of the coplanar probes was avoided by the adequate design of the integrated TUC probe head.

An additional relay circuitry is included into the switching matrix (right part of Figure 3.11) in order to avoid potential grounding conflicts between IV- and CV measurement. The outer conductors of the IV-parameter analyzer have to be kept ground-free, whereas the CV measurement requires asymmetrically grounded terminals. Nevertheless, the measurement cables require shielding in order to avoid device oscillation and electromagnetic interference. Therefore coaxial relays are used to switch between IV- and CV measurement programs and the ground connection is only established during CV measurements. In case of transistors, B-E diode, B-C diode and C-E characteristics can be independently measured without any re-contacting. For the IV measurement, this flexibility is achieved by programming the semiconductor parameter analyzer via the control software.

By employing this new hardware, fully automated HBT testing procedures with automatic measurement data acquisition are possible. Gummel-plot, output characteristics and both diode characteristics of the transistor are measured without any re-contacting during HBT stressing.

A very accurate real-time pulse response measurement is achieved for pulse current and for pulse voltage. pulsed stressing and monitoring is applicable down to a pulse width of $t_p = 30\,ns$. The voltage monitor shows a rise time of $t_r = 8\,ns$, which is in the range of the rise time of the HP 8114A pulse generator $t_r = 4\,ns$, whereas the current monitor exhibits a greater value of $t_r = 10\,ns$

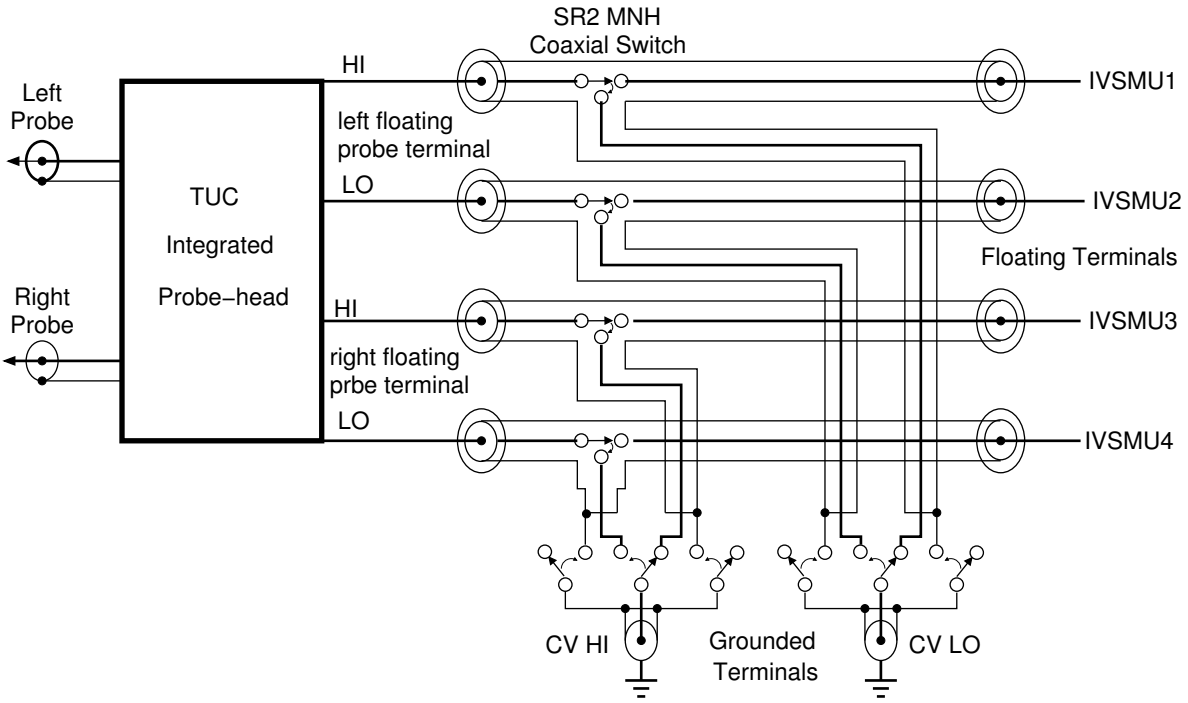


Figure 3.11: Schematic representation of the IV/CV-switch.

because of the influence of a parasitic inductances. A measured pulse response ($t_p = 100\ ns$) for a collector TLM structure from TH-LCR (RMS 1146) process is presented in figure 3.12.

The sample resistance is approximately $R = 20\ \Omega$ which can also be calculated from the steady state pulse voltage and pulse current. It has to be notified, that the pulse response was not measured for 50 Ω termination, but on-wafer during an experiment with a collector TLM ($R = 20\ \Omega$) including all test equipment, sample impedance mismatch and transmission lines of approximately $l = 15\ cm$ length with respective inductance. Nevertheless, the measurement result is very accurate and reproducible. An even improved pulse response measurement is achieved if the sample impedance is close to 50 Ω as reflection problems will be avoided. The cable reflections are identified in the range of $t = 0 \ldots 40\ ns$ of pulse duration.

The pulse current monitor is a very important improvement in the test bench: Beforehand only a direct extraction of the pulse voltage was possible and the current had to be calculated from the internal resistance of the pulse generator which induces significant measurement errors caused by any series impedance. From the pulse current and pulse voltage, the electrical power transmitted to the DUT, the large signal device characteristics and the thermal properties of the device can be extracted with good accuracy. The characteristic patterns of the pulse response enable a direct analysis of the device stability and reliability. Even a non-destructive prediction of the degradation threshold is possible.

Acquisition and processing of the pulse response during the stressing cycle has been automated in order to obtain data series for reliability and thermal characterization. The control software under LABVIEW 5.0 is further improved and offers duration test facilities and a flexible adjustment of measurement procedures. Measurement data can be extracted to a spreadsheet ASCII file format which is directly applicable for any data post processing, especially in co-operation with other partners. The improved set-up is tested, characterized and calibrated for all measurement channels,

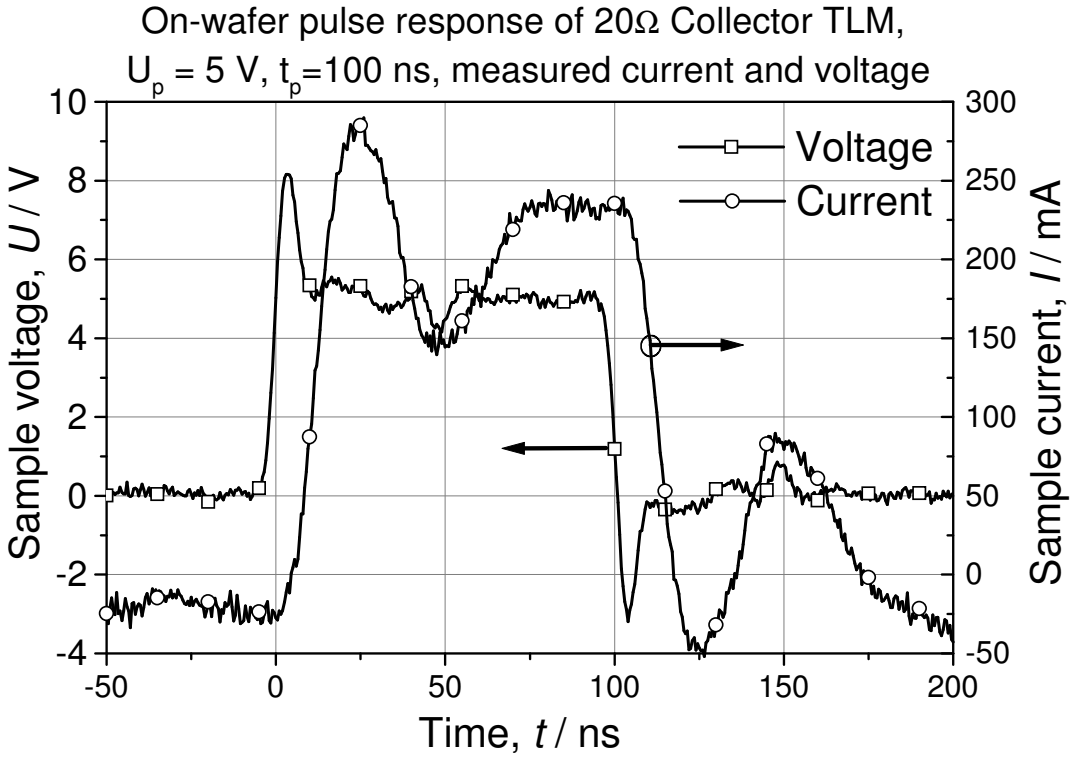


Figure 3.12: Example of the pulse response of a collector TLM.

including 1/f noise measurement. The 1/f noise amplifier delivered by TUC exhibits a significantly improved noise performance in comparison with the formerly used amplifier but the settling time is to long for application with accelerated stress tests.

3.4.4 IV-measurements

The analysis of the current-voltage relation turned out to be a very effective tool for the detection of device degradation. The IV-measurements are used for the extraction of device characterizing parameters, which sensitively indicate any degradation. In the case of TLM-structures, this parameter is the resistance R, for HBT the current gain β, cf. section 4.1.2 and for Schottky diodes the ideality factor η, cf. section 4.2.3. A HP 4145B parameter analyzer allows the measurement of currents down to the pico-Ampere range.

3.4.5 CV-measurements

CV-measurements provide information about the doping profile in diode-like interfaces and are used for the detection of dopant diffusion.

3.4.6 1/f-noise measurements

One possibility for the investigation of crystal quality is the measurement of 1/f-noise [72]. 1/f-noise is a very sensitive parameter for the degradation of a device by electro-migration.

Chapter 4

Compound Semiconductors

The basic advantage of compound semiconductors compared to silicon is the ability to form a wide variety of interfaces between material systems with similar lattice constants but different energy gaps (bandgap engineering) [73]. This additional degree of freedom resulted in heterostructure devices, e.g. high electron mobility transistor (HEMT), hetero-barrier varactor (HBV), or hetero bipolar transistor (HBT). A further advantage is the high electron mobility (and therefore short electron transit time), which leads to higher maximum operation frequencies. Some of those compound semiconductors are suitable for operation at higher temperatures in high-voltage applications due to the higher bandgap and high-current applications because of higher thermal resistance. This is especially valid for the wide bandgap semiconductors e.g. GaN, which are supposed to be the basis for future high power applications. From the technological point of view, parasitic effects are reduced and integration with other elements is facilitated using semi-insulating substrate materials. The disadvantage is the lack of a high-quality native oxide on the surface of the III/V-system, which necessitates an additional process step, the passivation of a surface e.g. with silicon oxide. Further, the silicon technology is more simple and mature than the III/V-technology making silicon the first choice for digital circuits.

Nevertheless, compound semiconductors are still the only option for real analog high frequency applications [74, 75]. In contrary to digital circuitry, the integration density for RF-circuits is mainly determined by their peripheral passive circuitry (e.g for matching) and does not follow MOORE'S law. The electric properties of III/V devices result either from metal-semiconductor interfaces (Schottky-diode, MESFET) and their lateral dimensions, compare section 4.2, or from semiconductor-semiconductor interfaces (HBT), cf. section 4.1. Latest research efforts for the generation of THz signals concern the low-temperature growth of GaAs, which acts as a photo-sensor in combination with mixed optical laser signals with a mixing frequency in the THz range. The following sections describe the technological and mathematical background of the IHF-Schottky diode and the investigated HBT, which are representatives for state of the art European device and technology research. This background is obligatory for the extraction of degradation indicators from measurements and for the reliability analysis of these devices as shown in chapter 6.

4.1 The Heterostructure-Bipolar-Transistor

The theoretical operation principle of heterostructure bipolar transistors (HBT) has already been postulated by SCHOTTKY and then by HERBERT KROEMER in 1957. Nevertheless, it took over 20 years up to the technological realization of the first III/V-materials based HBT. The basic advantages of III/V-HBT are their high cutoff frequency, the low phase noise, the very linear behavior

and the good power efficiency. This recommends HBT for RF applications like oscillators or linear amplifiers. Despite their good RF-characteristics, there was a lack of reliability because several reliability and power dissipation problems were not satisfactorily solved. One limiting factor for lifetime evaluation with InGaP-HBT was the long time required to promote failures in the device [12]. In the framework of the HERO'S-project, the first reliable European HBT process is established. A combination of several technological optimization steps increased reliability and efficiency (e.g. carbon as dopant, an additional ledge-passivation, heat sink optimization, contact optimization, cf. section 2.2.3) but always are a compromise between the different requirements. From the technological point of view, the most important innovative step was the replacement of the formerly AlGaAs/GaAs HBT by carbon-doped InGaP/GaAs-HBT [33, 44, 46]. From the reliability point of view, the HBT is a suitable candidate for the application of the TLP-method, as these devices are reported to be prone to electrical field- and current induced degradation mechanisms [48–50].

4.1.1 Application Areas

Devices with a hetero-interface usually are characterized by better RF-capabilities(f_T and f_{max}) and low noise figures. HEMT, for example, are used for low-noise amplifiers in MMIC for automotive and radar applications. GaAs HBT have a high amplification, a high power density, a high power added efficiency (PAE) and the same good matching properties as bipolar transistors. Concerning RF-properties and breakdown-voltage III/V-HBT are superior to the mature SiGe-HBT technology.

InGaP/GaAs HBT already have a strong impact on telecommunication applications development as linear amplifiers of oscillators (e.g. high-efficiency amplifiers in mobile telephone systems, as millimeter- and microwave power amplifier for satellite systems, x-band radar or as laser drivers in light-wave communication, e.g. OC-162).

The InGaP/GaAs HBT RF-properties are enhanced in comparison to the GaAs HBT due to better material properties. The lower conduction band discontinuity and higher valence band discontinuity results in high electron injection ratio and allows low-current operation. Besides, they offer lower 1/f-noise and better temperature stability of the current gain [12, 50, 76].

4.1.2 Basics

This section gives an introduction in HBT theory. This is relevant for proper understanding of the challenges with the investigated devices and the definition of the degradation indication parameters used in chapter 6. Additional fundamentals on HBT including DHBT[1] and graded heterojuntions are detailed by LIU in [39]. The following paragraphs describe SHBT[2], which are HBT with an abrupt hetero-junction for the base-emitter interface while the base-collector interface is homojunction.

The Hetero-interface

With the B-E hetero-interface, the reduction of the base-layer width is facilitated to allow, under normal operating conditions, the injected electrons from the emitter to diffuse quickly through the base without being recombined. This results in a reduction of the base-transit time and an

[1] DHBT=Double HBT
[2] SHBT=Single HBT

increase of device speed. At the reverse-biased base-collector junction, the high electric field drives the electrons across the collector. HBT have one additional degree of freedom for transistor design in comparison to BJT requiring $N_E > N_B$ for $I_C > I_B$ for reduction of B-E backward hole injection. A high base-doping reduces the base resistance and therefore increases the power gain. At the same time, low emitter doping reduces the base-emitter junction capacitance. With HBT, the backward-injection of holes from the base into the emitter is reduced, because the holes experience a larger energy barrier (ΔE_V) than the electrons (ΔE_C). Consequently, the base doping can exceed the emitter doping without affecting transistor performance. The hetero-interface is realized at the Base-Emitter interface using AlGaAs/GaAs, InGaP/GaAs or InGaP/InP material transitions. The material with higher bandgap, i.e. for example $Al_{0.35}Ga_{0.65}As$ ($E_g = 1.8\ eV$) or $In_{0.5}Ga_{0.5}P$ ($E_g = eV$), is on the emitter-side while the material with smaller bandgap, GaAs ($E_g = 1.424\ eV$) or InP ($E_g = 1.34\ eV$), is on the base-side. A detailed review on material properties band parameters of III-V semiconductors is given in [77]. Figure 4.1 shows a band diagram of an abrupt HBT with an AlGaAs/GaAs base-emitter hetero-interface.

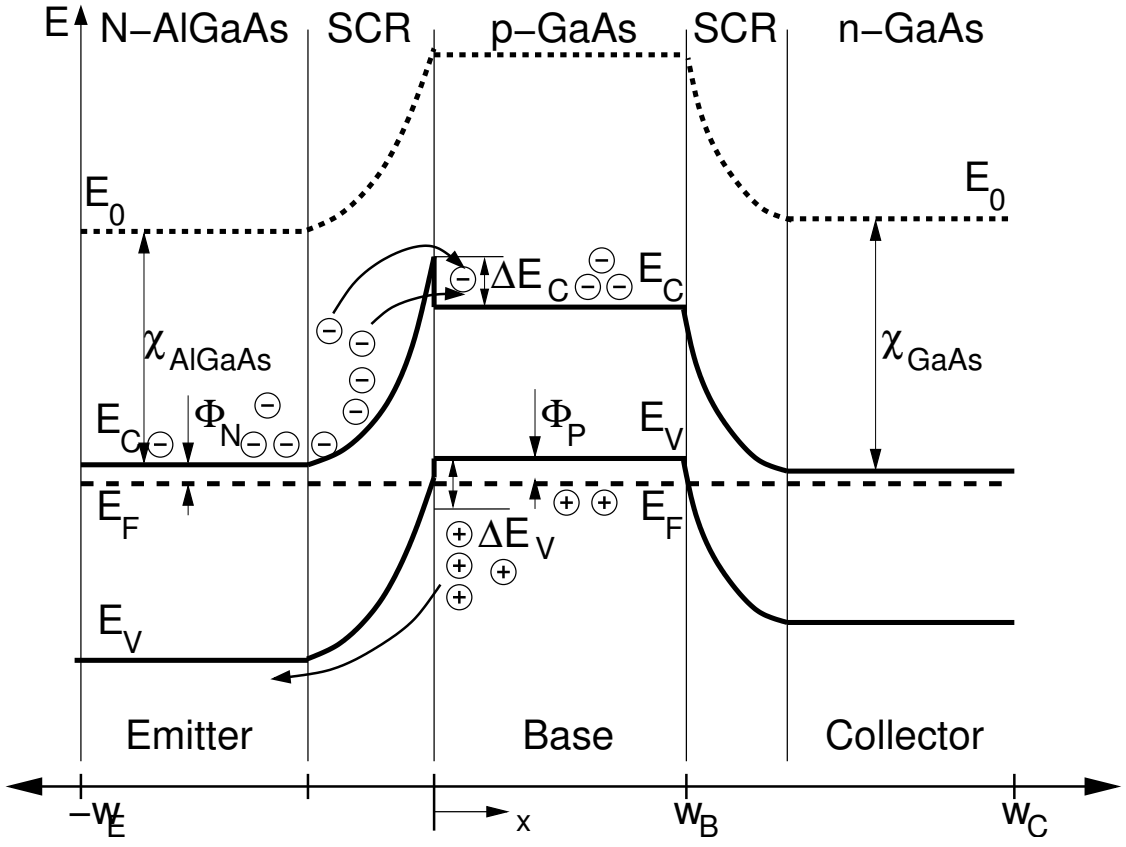


Figure 4.1: Band diagram of an abrupt HBT with an AlGaAs/GaAs base-emitter hetero-interface.

The development of the hetero-interface is the technological challenge for HBT, directly followed by the realization of reliable contacts on the base, emitter and collector-layers. In the case of the hetero-interface reliability relevant parameters are the base-doping and the surface properties of the different layers. The contact stability is important because the contacts are exposed to high temperatures, current densities and electric fields.

HBT currents

Measurements of HBT DC-currents give insight into many transistor properties. One can exemplary detect base-dopant irregularities (e.g. growth problems) or the removal of the base surface passivation ledge by measuring the DC gain, β. A correct understanding of β requires knowledge on the different components contributing to the base- and the collector current. Under forward bias, electrons are forward-injected from the emitter into the base and a comparably low number of base holes is back-injected from the base into the emitter region, resulting in the current I_{Bp}. Without electric field at the base, these electrons diffuse through the base to the collector. Every electron, which is not collected on the collector side contributing to I_C but therefore recombines in the base, requires a hole from the base contact for the recombination event. These holes are the main contribution to the base current I_B, which is separated into four parts depending on the location for recombination, which are:

1. Surface recombination current in the exposed extrinsic base, $I_{B,surf}$,
2. Interface recombination current at the base contact, $I_{B,cont}$,
3. Bulk recombination current in the base region, $I_{B,bulk}$,
4. Space-charge recombination in the B-E space-charge region, $I_{B,SCR}$.

The surface recombination current, $I_{B,surf}$, results from the high surface recombination velocity of GaAs ($\approx 1 \cdot 10^6 cm/s$). Without passivation measures, minority carriers injected from the emitter recombine with base majority carriers at the surfaces. This current is proportional to the emitter periphery and is a major contribution to the recombination current for small devices with large perimeter-to-area ratio [39]. The InGaAs surface recombination velocity ($\approx 1 \cdot 10^3 cm/s$) is relatively small resulting in negligible contribution to the base recombination current for InGaP/GaAs devices. The interface recombination current at the base contact, $I_{B,cont}$, results from the surface recombination velocity of a metal-semiconductor interface ($\approx 2 \cdot 10^7\ cm/s$). The contribution to the recombination current is smaller compared to $I_{B,surf}$ because the excess carrier concentration decreases with increasing distance of the contact from the intrinsic base. For a large base-emitter contact separation, this contribution is $I_{B,cont} = 0$.

DC Current gain

The current gain β is the relation between the collector current and the base current defined by equation 4.1.

$$\beta = \frac{I_C}{I_B} \tag{4.1}$$

The emitter current is the addition of the base and the collector current, cf. equation 4.2.

$$I_E = I_C + I_B \tag{4.2}$$

The relation between the collector current and the emitter current is defined by equation 4.3.

$$\alpha = \frac{I_C}{I_E} \tag{4.3}$$

With this the current amplification factor is defined as 4.4.

$$\alpha = \frac{\beta}{\beta + 1} \tag{4.4}$$

For modern HBT, β is in the range between $40 \ldots 120$, which results in $\alpha \approx 1$. This results in equation 4.5. This assumption does not hold for degraded devices, if the emitter current increases and becomes even higher than the collector current due to an increased base current. For this reason, the current amplification factors are a sensitive measure for the detection of device degradation with HBT as shown in chapter 6. Any degradation results in a decrease of $\alpha(t) < \alpha(t_0)$. The base currents before and after ageing for the same collector current are expressed following equation 4.6

$$I_C \approx I_E \tag{4.5}$$

$$\frac{I_B(t)}{I_B(t_0)} = \frac{\alpha(t_0)}{\alpha(t)} \tag{4.6}$$

The currents are measured either separately for the B-E or B-C diode or using the Gummel-plot[3]. A measured Gummel-plot is shown in figure 4.2, the current gain β can be directly extracted from this measurement.

The current voltage dependence for HBT is described using the Ebers-Moll model [78] following equation 4.7. The fit of measurements of the B-E or BC diode allows the extraction of characteristic parameters and degradation monitoring for device parts.

$$I_B = I_S \cdot e^{\frac{U_{BE}}{\eta \cdot k_e T}} \tag{4.7}$$

with

I_S = saturation current
k = Boltzmann constant
T = absolute temperature
η = ideality factor
U_{BE} = base-emitter voltage

Figure 4.3 shows the output characteristics of an EPI 3302 HBT, which is measured with the automated measurement set-up after integration of proper matching termination.

[3]The Gummel-plot visualizes base current, I_B, and collector current, I_C, vs. collector-emitter voltage, U_{CE}, for $U_{BC} = 0$

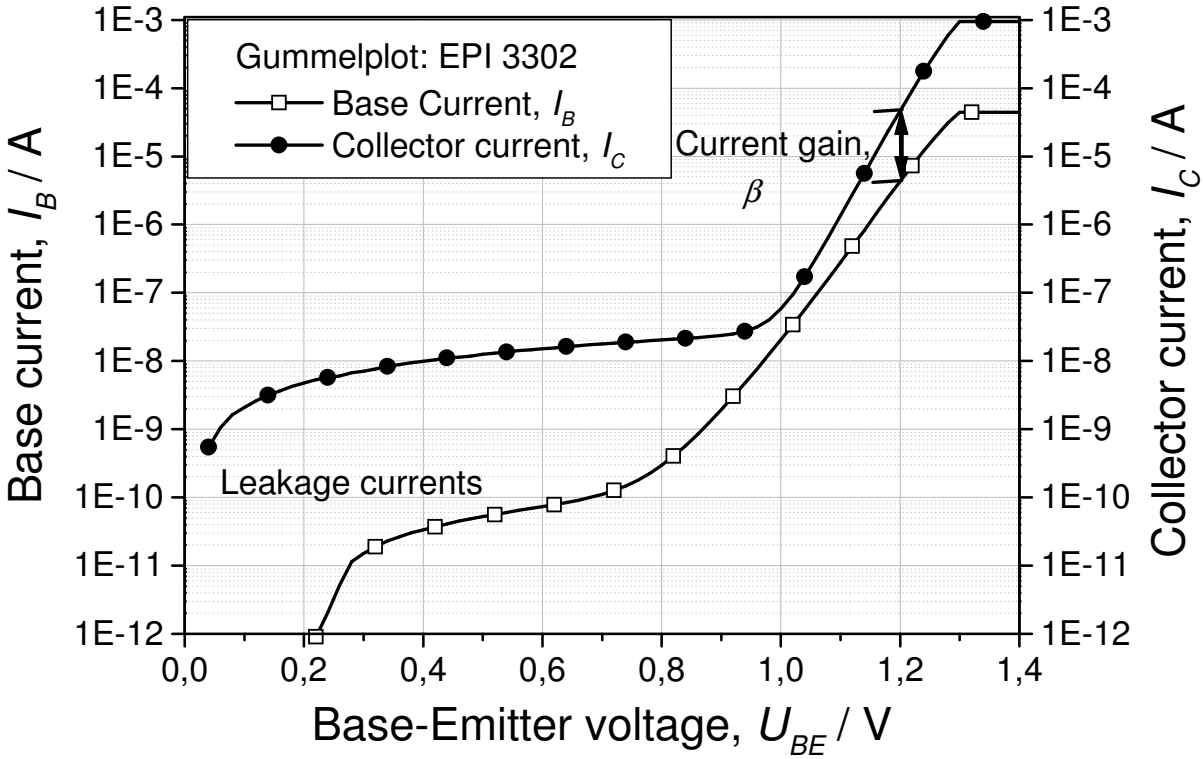


Figure 4.2: Measured Gummel-plot of a EPI 3302 Censa 10 HBT.

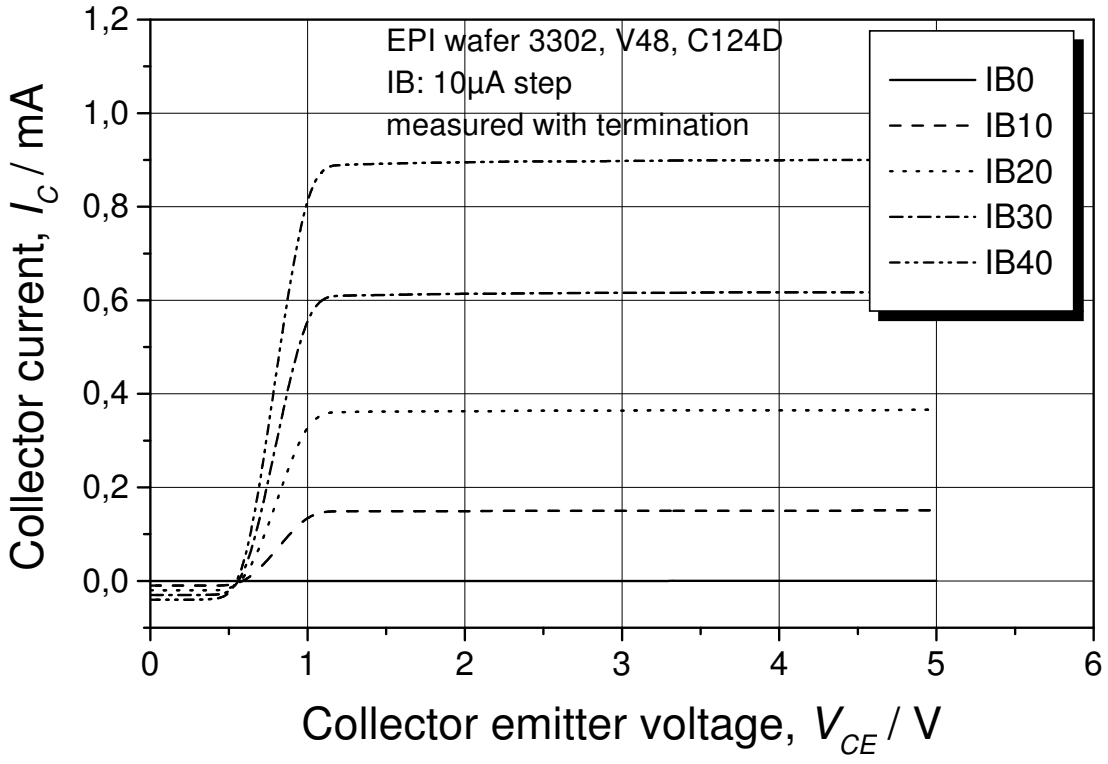


Figure 4.3: Output characteristics of a EPI 3302 C124D HBT measured with the automated measurement system.

4.1.3 Device geometry and technology

The investigated hetero bipolar transistors are based on a MOVPE[4]-grown InGaP/GaAs hetero-interface. They are fabricated by THALES[5] and IQE[6] in the framework of the HERO'S-project. In addition to the advantages of the AlGaAs/GaAs hetero-interface, this material system offers high etching selectivity of InGaP versus GaAs, a high valence band offset, $\Delta E_V = 0.24 \ldots 0.35\ eV$ in combination with relatively small conduction band offset, $\Delta E_C = 0.03 \ldots 0.22\ eV$. The base-dopant is Carbon, which is known for its low diffusivity and responsible for lattice shrinkage, in combination with In-codoping for lattice strain relaxation. The base surface is covered by a passivating InGaP-layer (ledge-passivation) for suppression of leakage currents across the 2µm ledge. The contact systems are non-alloyed Ti/Pt/Au for the base contact and alloyed AuGe/Ni/Au for the collector- and emitter contact optimized in view of reliability. The emitter fingers are 2µm x 40µm[7]

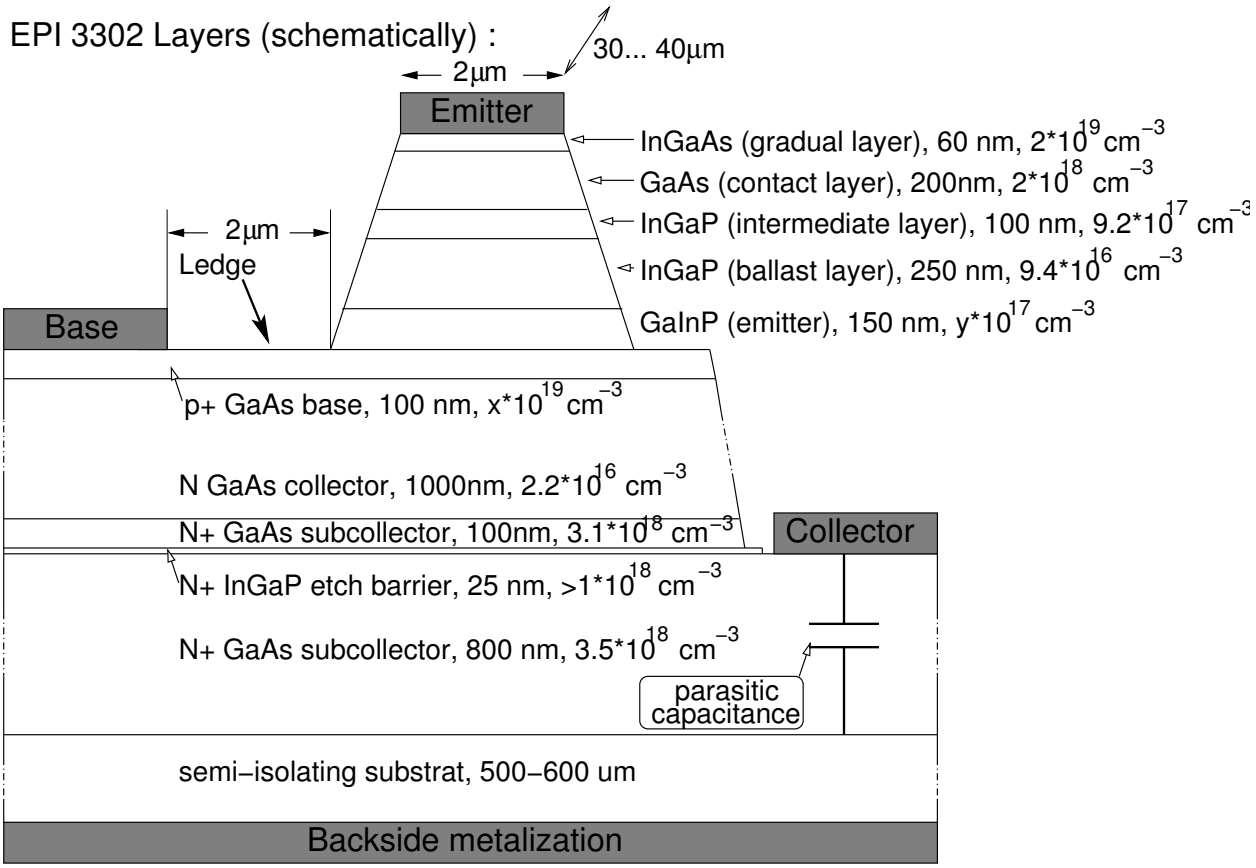


Figure 4.4: Principal structure of a InGaP/GaAs HBT.

[4]MOVPE=Metal-Organic Vapor Phase Epitaxy
[5]formerly: THOMSON LCR
[6]formerly: EPI
[7]Details on wafer structure on request

4.2 The IHF THz-Schottky diode

The Schottky diode is reported as the device of choice for uncooled mixer systems operating at THz-frequencies. There are research efforts on this topic in several international research institutes (Virginia, JET PROPULSION LABORATORIES, CHALMERS, NMRC, IHF TUD, Lille) now for more than ten years, starting with the development of whisker-contacted Schottky diodes, which were integrated in the first radiometers. This research resulted in a stable fabrication process of planar diodes and respective integrated circuits in one case (VDI Virginia Diodes Incorporated). The next step, the integration with filter structures and the development of mixer arrays is only possible if the fabrication process of single devices is stable and the fabrication yield is high.

This work contributes to the research efforts pursued at the TECHNISCHE UNIVERISTÄT DARMSTADT and resulted last year in "European state of the art Schottky devices" [79]. In the last two years, there was a breakthrough in the production of planar Schottky diodes, schematically shown in figure 4.5, with respect to the quality of fabricated Schottky interfaces, the diodes RF-properties and the fabrication yield. This development is the consequence of a variety research topics investigated at the IHF in the last decade [13, 21, 36, 56, 80], which mainly concerned the stability of metal/semiconductor interfaces and the optimization of the SiON-passivation layer.

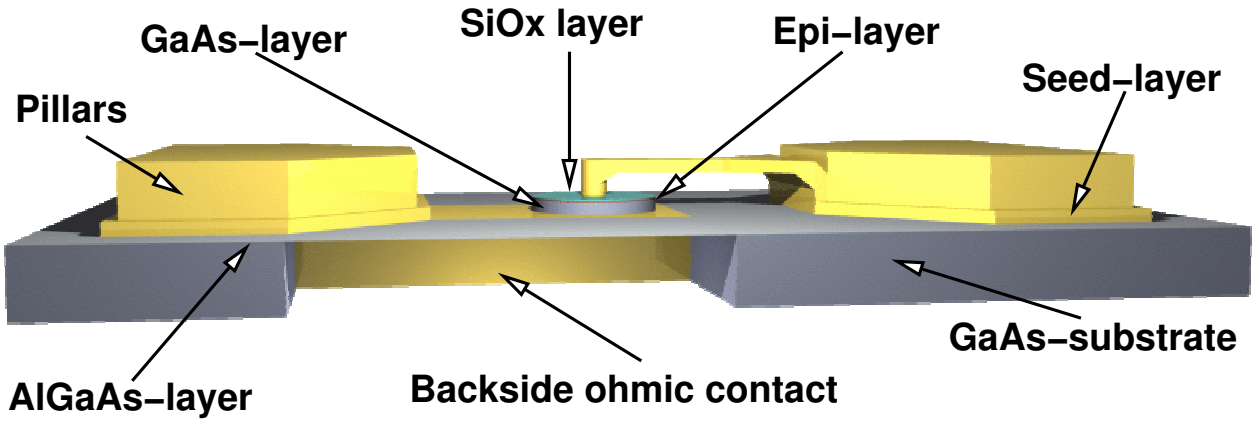


Figure 4.5: Basic structure of a quasi-vertical planar Schottky diode.

Figure 4.5 shows a schematic visualization of the actual diode. One can separate the challenges into technological challenges with respect to the mesa (i.e. epi-layer, Schottky-contact, passivation) and RF design challenges. A proper understanding of device physics, cf. section 4.2.3, a systematic investigation of the potential process weaknesses, the introduction of a process control system, cf. chapter 5 and the optimization of the critical process steps are the basis for this result [80–82]. Finally, the contribution of COJOCARI to the technology optimization with respect to noise properties and DC-characteristics is a prerequisite for this development [83–86]. Besides these technological challenges, the improvement of the high-frequency capabilities is a result of this work enabling these devices to operate at frequencies up to 1 THz.

In comparison to the KASIMIR-design of SIMON and LIN [22,23], the new IHF Schottky diode design presented in this work, cf. figure 4.6, is optimized in view of the parasitic capacitance C_p improving RF capabilities. The respective mask set includes additional process control structures for the identification of potential process weaknesses, as described in chapter 5. With this new diode design, the parasitic capacitance is reduced and therefore comparable to VDI-diodes. The reduction of the parasitic capacitance is mainly achieved by following measures:

- a decrease of the pad size,
- an increase of the distance between anode pad and ohmic backside contact,
- a reduction of ohmic backside contact dimensions.

The actual diodes are suitable for the integration with waveguide mixer blocks e.g. for heterodyne receivers. They are characterized by the electrical parameters detailed in table 4.1. These devices comply with industrial requirements shown in table 1.2. At this stage, the most critical parameter is the parasitic capacitance which requires further reduction.

Electrical parameter	Symbol	Value
Series resistance	R_s	$5 \ldots 9\ \Omega$
Ideality factor	η	$1.18 \ldots 1.2$
Junction capacitance	C_j	$1\ fF$
Parasitic capacitance	C_p	$8 \ldots 9\ fF$
Noise temperature	T_{noise}	$280 \ldots 320\ K$

Table 4.1: *Electrical parameters of the actual* IHF *THz-Schottky diode.*

The specialty of the IHF THz-Schottky diode is the quasi-vertical design approach in combination with the electrolytic deposition of the Pt-contact. The advantage of this approach is the vertical current flow through the junction, the excellent noise properties and the good heat sink capabilities of the ohmic backside contact. Further on, this design allows the technology transfer from the whisker-contacted device technology (including the electrolytic deposition of the Schottky contact) to the planar device technology using "dummy"-anode arrays, cf. section 5.1. This allows the optimization of process steps using cheap and easy to fabricate whisker-contacted diodes and a subsequent transfer to the planar device technology, since the junction properties with respect to formation and reliability are similar. The disadvantage of this approach is a complex air-bridge technology with additional technological challenges and the requirement of an additional backside process in comparison to lateral diodes.

The following sections give a short overview on device composition and dimensions and provide the mathematical background of device physics, which is necessary for the correct modeling (refer to section 4.2.4) and analysis of the device and the extraction of device parameters, e.g. ideality factor, junction capacitance, parasitic capacitance or junction temperature.

4.2.1 Application areas for THz-Schottky diodes

The THz frequency region gains increasing interest in the public opinion as a growing number of applications arises in the following fields [87]:

- environmental engineering (e.g. atmospheric observation),
- bio- and medical engineering (e.g. detection of skin cancer),
- security applications (e.g. as a replacement for x-rays).

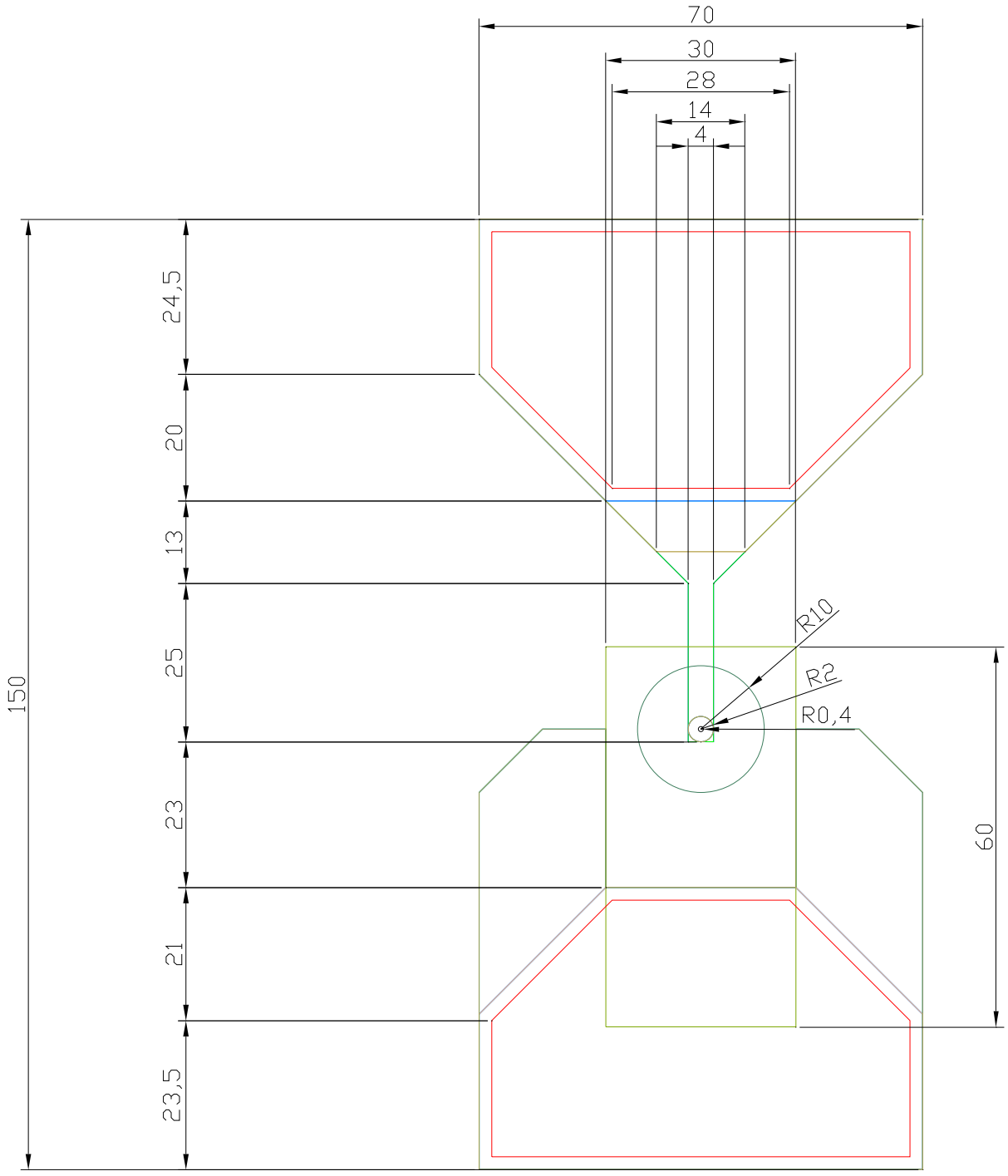


Figure 4.6: Basic layout of the planar IHF *THz-Schottky diode, all dimensions are in µm.*

The Schottky diode is nowadays the only non-cryogenic device which is able to operate at highest frequencies. The Schottky-diode is used as the non-linear element in mixer- and multiplier systems. The tested IHF planar Schottky diodes are developed in the framework of several ESA-projects for atmosphere observation.

4.2.2 Structure and equivalent circuit of the realized planar Schottky diodes

A Schottky contact can be described as a resistive hetero-junction of metal and semiconductor with rectifying non-linear characteristics similar to an one-sided abrupt pn-diode [88]. The Schottky interface mainly determines device quality in the case of the IHF THz-Schottky-diodes. The current transport is governed by carrier majorities resulting in high drift velocities and short recombination times in comparison to carrier minorities. This enables these devices to operate at highest frequencies. Usually, only n-type semiconductors are used for the realization of high-frequency Schottky devices because electron mobility is significantly higher than the mobility of holes. Figure 4.7a) shows the principle structure of a whisker-contacted diode and the intrinsic part of a quasi-vertical planar Schottky diode.

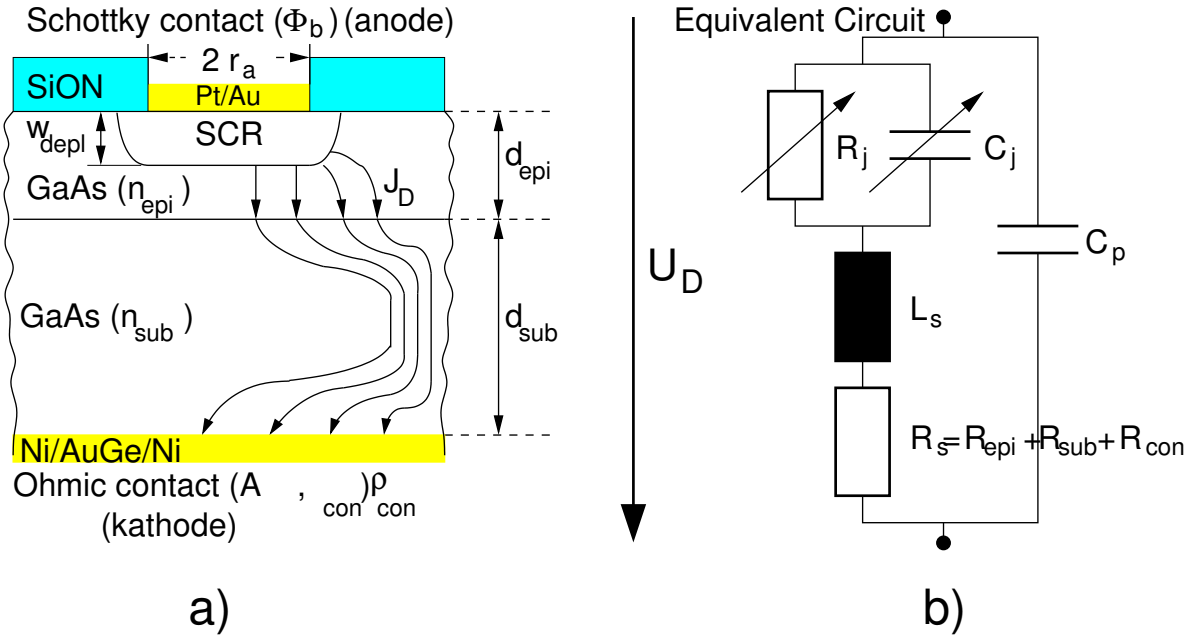


Figure 4.7: a) Principle structure of a Schottkydiode, b) Equivalent circuit of a Schottkydiode.

The planar diode is separated into its intrinsic part, the metal-semiconductor junction, which is described in section 4.2.3, and the peripheral equivalent circuit, modeling substrate and contact resistances as well as parasitic capacitances and inductances. The intrinsic part mainly determines the IV-characteristic while the periphery influences the high-frequency behavior. In this context, a reduction of peripheral parasitics is mandatory to allow operation at THz-frequencies. The large-signal model of the planar diode is shown in section 4.2.4 according to the analytic equations, shown in section 4.2.3. The model is validated using RF-measurements up to 110 GHz at different bias currents. The current crowding at the walls, as shown in figure 4.7a), determines the substrate resistance for high-frequency operation (see section 4.2.3).

The whisker-contacted and planar THz-Schottky diodes, realized at the IHF, consist of a circular platinum-anode with radius r_a, an epitaxially grown GaAs-layer with doping concentration n_{epi} and epi-layer thickness d_{epi}, the GaAs-substrate with doping concentration n_{sub} and substrate thickness d_{sub} and, finally, the ohmic backside contact, which is characterized by its area $A_{contact}$ and its specific contact resistance $\rho_{contact}$. Figure 4.7b) shows the basic equivalent circuit as it

is used for simulations with whisker-contacted and planar diodes. The non-linear depletion-layer resistance R_j and the corresponding junction capacitance C_j are a function of the depletion layer width. The series inductance L_S and the series resistance R_S are a function of diode geometry and technological realization of the diode periphery. The parasitic capacitance C_p depends on the one side on the technological realization of the diode and on the other side on the contact dimensions and packaging. The junction capacity ranges from $C_j = 1\ fF$ for whisker-contacted mixer diodes to $C_j = 10 \ldots 15\ fF$ in the case of varactor diodes. The parasitic capacitance is extracted to $C_p = 8 \ldots 10\ fF$ in the case of discrete planar mixer or varactor diodes on GaAs substrate, as schematically shown in figure 4.5. Basic investigations for these devices and their technology development have been performed by SIMON and LIN [21–23, 55]. The modeling of device parameters, which is mandatory for the large-signal model, is detailed in section 4.2.3.

4.2.3 Physical model for the equivalent circuit

At a metal-semiconductor interface, there is an exchange of free charge carriers due to the difference between the metal work-function Φ_M and the semiconductor electron affinity χ_H. Charge carriers are relocated from the semiconductor to the metal face by tunneling processes or thermic excitation until a thermodynamic equilibrium is attained and Fermi levels are equalized. This results in the formation of a depletion layer in the semiconductor and a negative surface charge on the metal. The stationary fixed charges result in an electrostatic field and the Schottky barrier Φ_B is formed following the thermionic emission model, equation 4.8, if an ideal interface between both components is assumed. Following the Schottky-Mott-model [89], the band diagram of a metal semiconductor interface is described by figure 4.8.

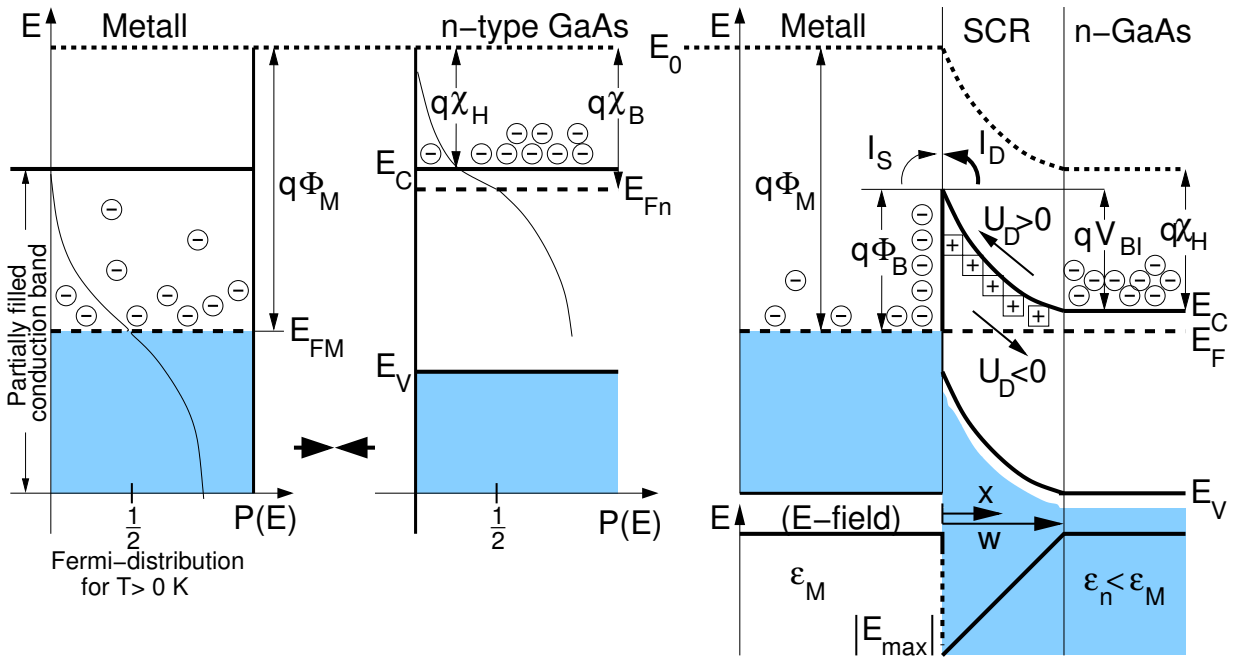


Figure 4.8: Band diagram of a metal/ n-semiconductor Schottky contact before and after contact between the metal and the semiconductor (SCHOTTKY-MOTT-model).

$$\Phi_B = \Phi_M - \chi_H \tag{4.8}$$

Technological constraints result in a imperfect metal-semiconductor interface and therefore invalidate the SCHOTTKY-MOTT theory. For realized devices, the Schottky barrier is almost insensitive to the metal work-function and mainly depends on surface energy states in the forbidden band. These surface states are due to interruptions of the perfect crystal periodicity (e.g. due to interdiffusion) resulting in broken covalent bonds (dangling bonds), cf. section 2.2.2, which are almost saturated below E_F.

The BARDEEN model, in contrary, takes the Fermi-level pinning into account and models the barrier height following equation 4.9 [23, 90]. Additionally, the Schottky-effect is taken into account, if an electric field is applied. This effect describes a lowering $\Delta\Phi$ of the effective barrier Φ' due to electrons in the space charge region and an equivalent positive image charges at the metal. The respective band diagram is shown in figure 4.9. This effect is well-known for III/V based Schottky devices and is also observed for the IHF-Schottky devices under investigation (chapter 6 shows a TEM image of such a non-perfect Schottky interface and illustrates the requirement for the application of this model).

$$\Phi'_B = \frac{E_G}{e} - \Phi_0 \tag{4.9}$$

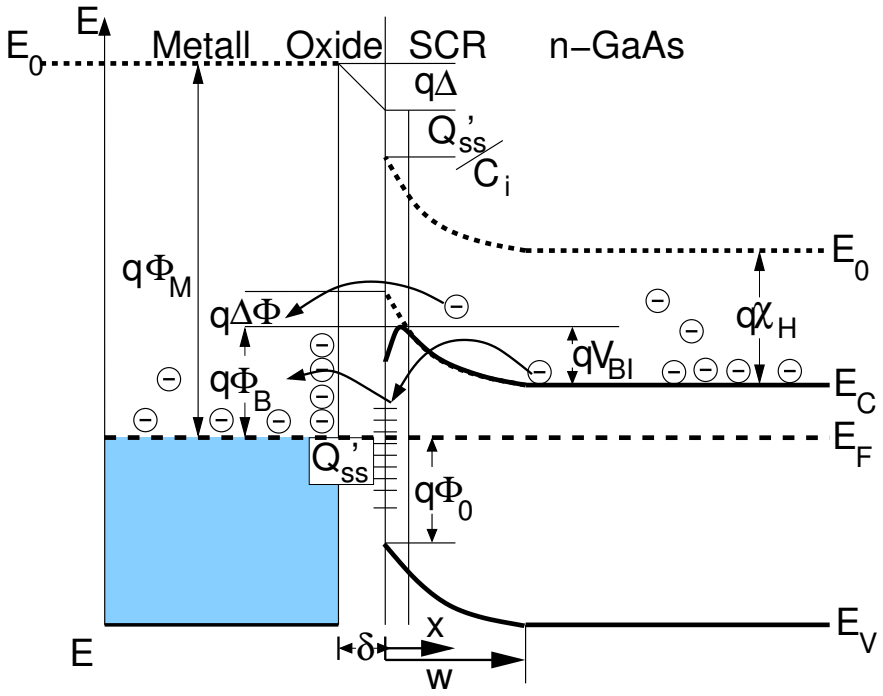


*Figure 4.9: Band diagram of a metal/ n-semiconductor Schottky contact with Fermi-level pinning and Schottky barrier lowering, $\Delta\Phi$ (*BARDEEN-*model).*

This finally results in a current-voltage dependence (IV-characteristics), which is exemplarily shown for a planar IHF Schottky diode in figure 4.10. This figure shows the IV-characteristic in

semi-logarithmic scale and several deviations from the ideal behavior are evident. These deviations affect the ideality factor $\eta > 1$ due to technological imperfections, the leakage currents, the series resistance R_S and a shift in the saturation current I_s.

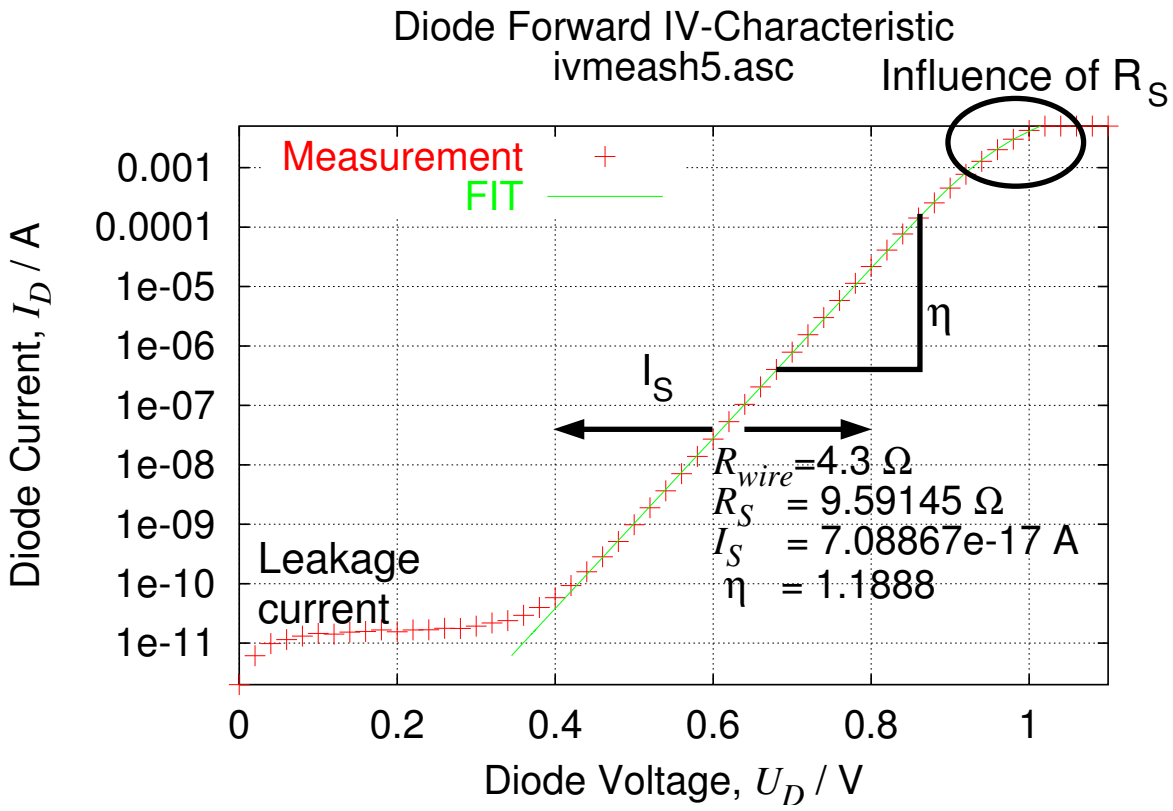


Figure 4.10: IV-characteristics of a planar IHF-*Schottky mixer diode and extraction of characteristic parameters.*

The experimental extraction of non-ideal diode parameters is performed following the approach proposed in [91]. R_s is extracted from DC.measurements fitting current-voltage (I/V) measurements in forward-bias conditions to the diode's current equation:

$$I_D = I_{Sat}\left(\exp\left(\frac{U_D - R_s I_D}{\eta\, U_T}\right) - 1\right) \tag{4.10}$$

The three parameters to be fitted are the diode's reverse saturation current, the series resistance and the ideality factor η.

The diode current I_D

MAXWELL's equations correlate the displacement $\vec{D}$ to the charge density ρ following equation 4.11. This results in the POISSON equation, cf. equation 4.12, by replacing the electric field with the potential gradient.

$$div\vec{D} = div\left(\varepsilon\vec{E}\right) = \rho \tag{4.11}$$

$$div\vec{E} = -div\,(gradV) = \frac{\rho}{\varepsilon} \tag{4.12}$$

In thermodynamic equilibrium, the so-called built-in potential results from a continuous current in either one direction without external voltage. A forward bias of the anode (metal electrode) with a positive voltage $V > 0V$ lowers the potential barrier to $\Phi_{bi} - V$, which then is surmounted by an excess electron drift current. Reverse bias of the anode ($V < 0V$) increases the built-in potential and extends the space charge region, w_{depl}. In this case, there is still a comparatively small saturation current I_{sat} due to thermionic emission. The diode current I_D is described as a function of the thermo-voltage U_T, the saturation current I_{sat} and the diode voltage U_D following SHOCKLEY's diode equation. This equation may be extended following the approach of JELENSKI [92] for flat-band operation, i.e. $U_D = U_{bi}$

$$I_D = I_{sat} \cdot \left(e^{\frac{U_D}{\eta U_T}} - 1\right) \text{ with } U_T = \frac{k_B T}{q} \tag{4.13}$$

$$I_{sat} = \pi r_a^2 \cdot A^* \cdot T^2 \cdot e^{\frac{-\Phi_{bi}}{U_T}} \text{ with } A^* = \frac{m_n}{m_0} \cdot A \tag{4.14}$$

The non-linear junction resistance R_j

From equation 4.13 one can derive the non-linear junction resistance R_j, cf. equation 4.15, ($A^* = 8.6 \cdot 10^4 \frac{A}{m^2 K}$ for n-(100)GaAs) if the saturation current is assumed to be constant [89].

$$\frac{1}{R_J} = \frac{I_D}{U_D}|_{U_D=0} = \frac{1}{\eta U_T} \cdot (I_{D_0} + I_{Sat}) \tag{4.15}$$

Ideality factor $\eta(I)$

The current dependent ideality factor is physically understood as the sum of all barrier reducing effects. The ideality factor is described by equation 4.16. Details can be found in [55] In the case of nearly ideal diodes with relatively large areas (diameters $d \geq 3\,\mu m$) the ideality factor is more or less constant over a wide current range. The ideality factor is experimentally extracted from IV-measurements using equation 4.16.

$$\eta(I) = \frac{1}{U_T} \cdot \frac{\partial U_D}{\ln \partial I_D} \tag{4.16}$$

For small anode diameters, the ideality factor is described with additional contributions for thermionic field emission, η_{tf}, and for the image force effect, η_{if}. This way, the ideality factor is only a function of the epi-layer doping. The resulting ideality factor is given by equation 4.16.

Diodes with diameter $d < 3\,\mu m$ show a strong increase of the ideality factor with increasing current density, which cannot be described by equation 4.16. The strong increase in η at high bias voltages is caused by the increasing series resistance under forward bias condition. The ideality factor is minimal at a certain bias condition, from which on equation 4.19 is valid as proposed in [55]. An additional current is added modeling edge effects for lower bias conditions resulting in equation 4.20.

$$\eta_{if} = \frac{1}{1 - \frac{\Delta\Phi_b}{4\Phi_{bi}} \cdot \left(1 - \frac{U_D}{\Phi_{bi}}\right)^{-\frac{3}{4}}} \quad \text{with } \Delta\Phi_b = \left[\frac{q^3 N_{epi} \Phi_{bi}}{8\pi^2 \varepsilon_s' 2\varepsilon_s \varepsilon_0^3}\right]^{\frac{1}{4}} \tag{4.17}$$

$$\eta_{tf} = \left[\frac{E_T}{E_0} - \frac{U_T}{2\left(\Phi_{bi} - U_D\right)}\right]^{-1} \quad \text{with } E_0 = E_{00} \coth\left(\frac{E_{00}}{U_T}\right) \; ; E_{00} = \frac{h}{4\pi}\left[\frac{N_{epi}}{m \cdot \varepsilon_0 \varepsilon_s}\right]^{\frac{1}{2}} \tag{4.18}$$

$$\eta = 1 + (\eta_{if} - 1) + (\eta_{tf} - 1) \tag{4.19}$$

$$I = I_{id} + \Delta I \quad \text{with} \quad \Delta I = I_{sm} \cdot e^{\frac{V}{mV_T}} \tag{4.20}$$

In this case I_{sm} is the crossing of ΔI and the y-axis and $m \sim 2 \ldots 5$ is the slope of ΔI. This additional contribution ΔI to the current I is assumed to be caused by interface effects at the metal semiconductor interface [55].

The series resistance R_s

The contributions to the series resistance are the contact resistance $R_{contact}$, the un-depleted part of the epi-layer R_{epi} and the highly doped GaAs-substrate in the order $R_{epi} > R_{sub} > R_{contact}$. The epi-layer resistance R_{epi} is calculated in equation 4.21 with the correction factor, γ_R, for fringing field effects at the edges as proposed in [93]. The correction factor is approximated in the large-signal model by equation 4.23 as proposed in [94].

$$R_{epi} = \frac{\rho_{epi} d_{epi}}{\pi r_a^2} \cdot \gamma_R \tag{4.21}$$

$$\gamma_R = \frac{1}{d_{epi}} \int_0^\infty \frac{tanh\left(z d_{epi} sin\left(z r_a\right)\right) J_1\left(z r_a\right)}{z^2}\, dz \tag{4.22}$$

$$\gamma_R = \left[1 + \frac{4 d_{epi}}{\pi r_a}\right]^{-1} \approx 1 \text{ for } r_a \gg d_{epi} \tag{4.23}$$

The skin-effect strongly influences the substrate resistance (spreading resistance) and can not be neglected anymore for devices operating at THz-frequencies. Equation 4.24 gives an approximation as proposed by DICKENS in [95].

$$R_{Sub} = \frac{1}{2\pi\sigma_{sub}} \left(\frac{1}{\delta_{skin}} \cdot ln\left(\frac{r_{mesa}}{r_a}\right) + \frac{1}{r_a} tan^{-1}\left(\frac{r_{mesa}}{r_a}\right) \right) \text{ with } \delta_{skin} = \sqrt{\frac{1}{\pi f_s \mu \sigma_{sub}}} \quad (4.24)$$

RODRIGUEZ shows basic investigations using a finite element solver (CST MICROWAVE STUDIO) on the substrate resistance in his PHD thesis which are based on the model by CALVIELLO et. al. and consistent with the results by HUBER [56, 96–98]. The substrate resistance for whisker-contacted and quasi-vertical planar Schottky diodes is separated into 5 parts as shown in equation 4.25.

$$R_{sub} = R_1 + R_2 + R_3 + R_4 + R_5 \quad (4.25)$$

with

$$R_1 = \frac{\delta_{skin}}{2\pi \cdot r_a^2 \cdot \sigma_{sub}}$$
$$R_2 = \frac{1}{4\pi \cdot \delta_{skin} \cdot \sigma_{sub}}$$
$$R_3 = \frac{1}{2\pi \cdot \delta_{skin} \cdot \sigma_{sub}} \cdot ln\left(\frac{r_{mesa}}{r_a}\right)$$
$$R_4 = \frac{d_{sub}}{2\pi \cdot r_{mesa} \cdot \delta_{skin} \cdot \sigma_{sub}}$$
$$R_5 = \frac{j\beta \cdot \rho_{ohm} \cdot J_0(j\beta \cdot r_{mesa})}{2\pi \cdot r_{mesa} \cdot J_1(j\beta \cdot r_{mesa})}$$
$$\beta^2 = \frac{1}{\sigma_{sub} \cdot \rho_{ohm} \cdot \delta_{skin}}$$

An additional effect at highest frequencies (>1 THz) is the plasma resonance effect, which describes the coupling of the displacement current with the carrier inertia [99]. In this case, the conductivity becomes complex and is described by equation 4.26.

$$\underline{\sigma_s} = \sigma_s + j\omega\varepsilon = \sigma_s \cdot \left(\frac{1}{1 + j\left(\frac{\omega}{\omega_s}\right)} + j \cdot \frac{\omega}{\omega_s} \right) \quad (4.26)$$

ω_s is the scattering frequency and ω_s is the relaxation frequency. The conductivity is minimal for $Im\{\underline{\sigma_s}\} = 0$, which is the case for the plasma frequency $\omega_P = \sqrt{\omega_s \omega_s}$.

The junction capacitance C_j

Figure 4.11 shows a comparison of the measured and the approximated CV-characteristics for a whisker-contacted mixer diode with anode diameter $d_a = 5\ \mu m$ used for process control.

There are two possibilities for the mathematical description of the junction capacitance C_j. The first derives the junction capacitance from the POISSON equation with the assumption of a one-dimensional abrupt diode model and a constant carrier distribution in the space charge region $\rho(x) = q \cdot N_{epi}$.

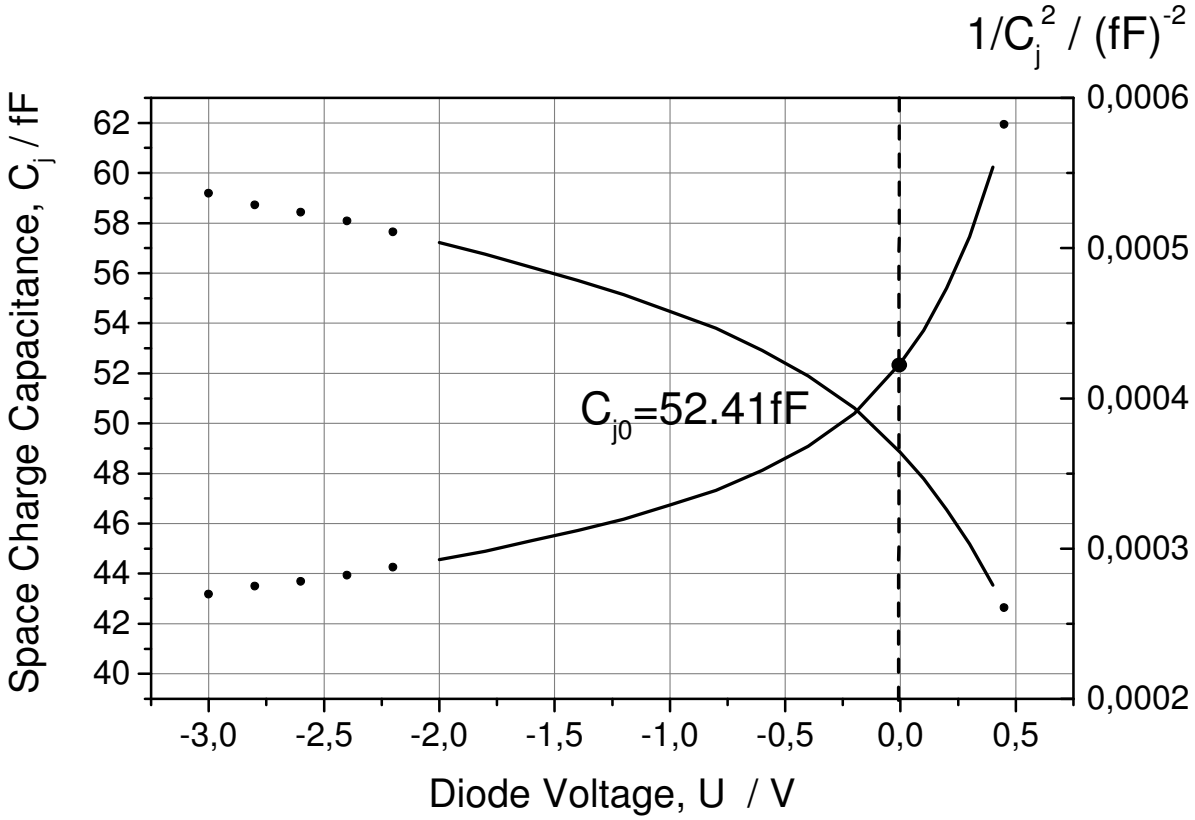


Figure 4.11: CV-characteristics of a whisker-contacted IHF *Schottky mixer diode with anode diameter $d_{anode} = 5\ \mu m$ and extraction of capacitance.*

$$E(x) = \int_0^x \frac{\rho(x)}{\varepsilon_{GaAs}} dx \rightarrow |E_{max}| = \frac{q \cdot N_{epi} \cdot w_{depl}}{\varepsilon_{GaAs}} \tag{4.27}$$

External bias modulates the potential barrier and changes the depletion layer width according to the following equations. An extension to the well-known equations for Schottky diodes was formulated in 1993 by JELENSKI [92], cf. equation 4.31.

$$U_{bi} - U_D = \int_0^w E(x) dx = \frac{q \cdot N_{epi} \cdot w_{depl}^2}{2 \cdot \varepsilon_{GaAs}} \tag{4.28}$$

$$w_{depl} = \sqrt{\frac{2\varepsilon_{GaAs} \cdot (U_{bi} - U_D - U_T)}{q \cdot N_{epi}}} \tag{4.29}$$

$$Q_j = A \cdot q \cdot N_{epi} \cdot w_{depl} = A \cdot \sqrt{2\varepsilon_{GaAs} \cdot N_{epi} \cdot q \cdot (U_{bi} - U_D - U_T)} \tag{4.30}$$

$$C_j(V_D) = \frac{\partial Q_j}{\partial V_D} = \frac{A \cdot \varepsilon_{GaAs}}{w_{depl}(V_D)} = A \cdot \sqrt{\frac{q \cdot \varepsilon_{GaAs} \cdot N_{epi}}{2 \cdot (U_{bi} - U_D - U_T)}} = \frac{C_{j0}}{\sqrt{\left(1 - \frac{U_D}{U_{bi}} - \frac{U_T}{U_{bi}}\right)}} \tag{4.31}$$

with

$$A_{exp} = \left[1 - e^{\left(-\frac{U_{bi}-U_D}{U_T}\right)}\right] \tag{4.32}$$

In the second case, the junction capacitance C_j is a function of the applied voltage and is approximately (below flat band operation) modeled by a parallel plate capacitance following 4.33 [94, 100].

$$C_j(U_D) = \frac{A \cdot \varepsilon_{GaAs}}{w_{depl}(U_D)} \cdot \left(1 + b_1 \frac{w_{depl}}{r_a} + b_2 \cdot \frac{w_{depl}^2}{r_a^2}\right) = \frac{\pi r_a^2 \cdot \varepsilon_{GaAs}}{w_{depl}(U_D)} \cdot \gamma_c \tag{4.33}$$

The influence of fringing effects is taken into account using the correction factors $b_1 = 1.5$ and $b_2 = 0.3$ proposed in [101]. These effects can not be neglected for small anode diameters and an entirely depleted epi-layer, $w_{depl} = d_{epi}$, [22, 102].

Cutoff frequency

The RF-capabilities of varistor diodes are determined using the cutoff frequency. The cutoff frequency is a function of the series resistance R_S and the device capacitance C following equation 4.34 and in the case of varactor diodes following 4.35 [99]. M is defined as the capacity modulation ratio following equation 4.36. With respect to equation 4.34, the requirement of parasitics reduction is evident.

$$f_c = \frac{1}{2\pi \cdot R_s \cdot C_{j0}} \tag{4.34}$$

$$f_{cV} = \frac{1}{2\pi \cdot R_s} \cdot \left(\frac{1}{C_{jmin}} - \frac{1}{C_{j0}}\right) = \frac{1}{2\pi \cdot R_s} \cdot (M-1) \tag{4.35}$$

$$M = \frac{C_{j0}}{C_{jmin}} \tag{4.36}$$

4.2.4 THz-Schottky diode model and RF-measurements

This section refers to the proposed Schottky diode model for AGILENT ADS and evaluates the model capabilities with respect to S-parameter measurements ranging from 7-110 GHz, which are performed at MILLILAB. These measurements, in combination with additionally extracted characteristic parameters, have been requested by ESA/ESTEC as an external reference for diode quality. The S-parameter measurements are performed using a coplanar waveguide (CPW) test mount (3 μm thick gold metalization) on a 500 μm thick quartz wafer and suitable calibration structures.

THz-Schottky diode model

The simulation of the electric properties is based on the BARDEEN model as described in 4.2.3. The substrate layer resistance is calculated including the bulk spreading resistance following [99]. Further the skin-effect is included, which strongly influences the series resistance for THz-frequencies. The substrate layer resistance is calculated following [97] [56].

The model for the THz-Schottky mixer diode is implemented in an industrial RF- and digital circuit simulator, AGILENT ADS 2003C. The model is separated into:

- an intrinsic diode model using analytic expressions following section 4.2.3,
- an extrinsic diode model with lumped elements taking the diode periphery into account.

While the intrinsic model is only applicable for mixer operation, the extrinsic model holds for mixer and varactor Schottky diodes with similar peripheral dimensions.

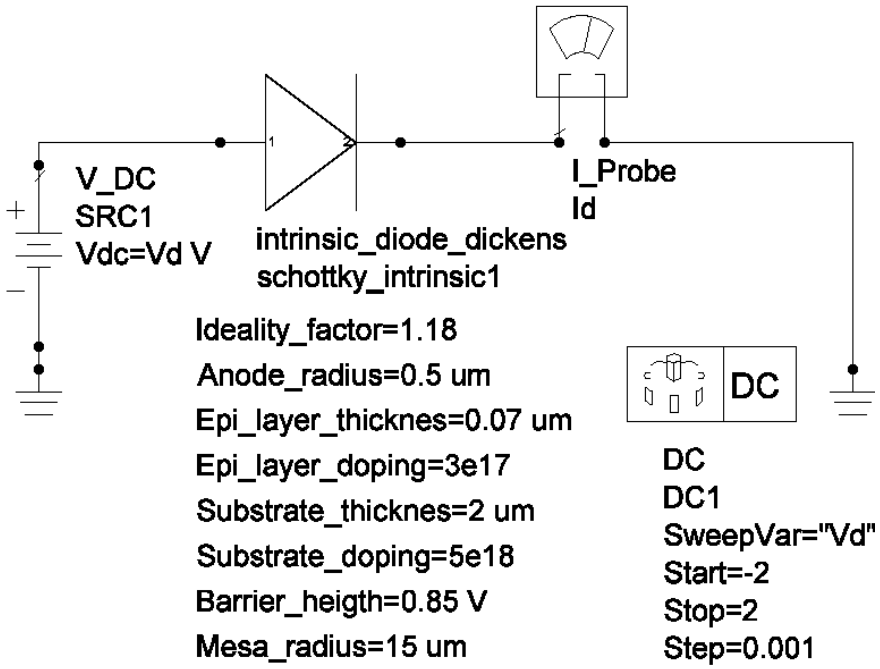


Figure 4.12: ADS2003C-*Model ESB representation of the* IHF *THz-Schottky diode.*

Figure 4.12 shows the intrinsic diode model equivalent circuit representation. The physical input parameters are the epi-layer doping and thickness, the substrate doping and thickness, the anode and mesa-diameter. The ideality factor and the barrier height are extracted from DC-measurements for good agreement with diode measurements. Figure 4.13 and 4.14 show a comparison of the measured and the simulated DC-characteristics. The simulated DC-characteristics is dominated by the intrinsic device properties and the employed interface model.

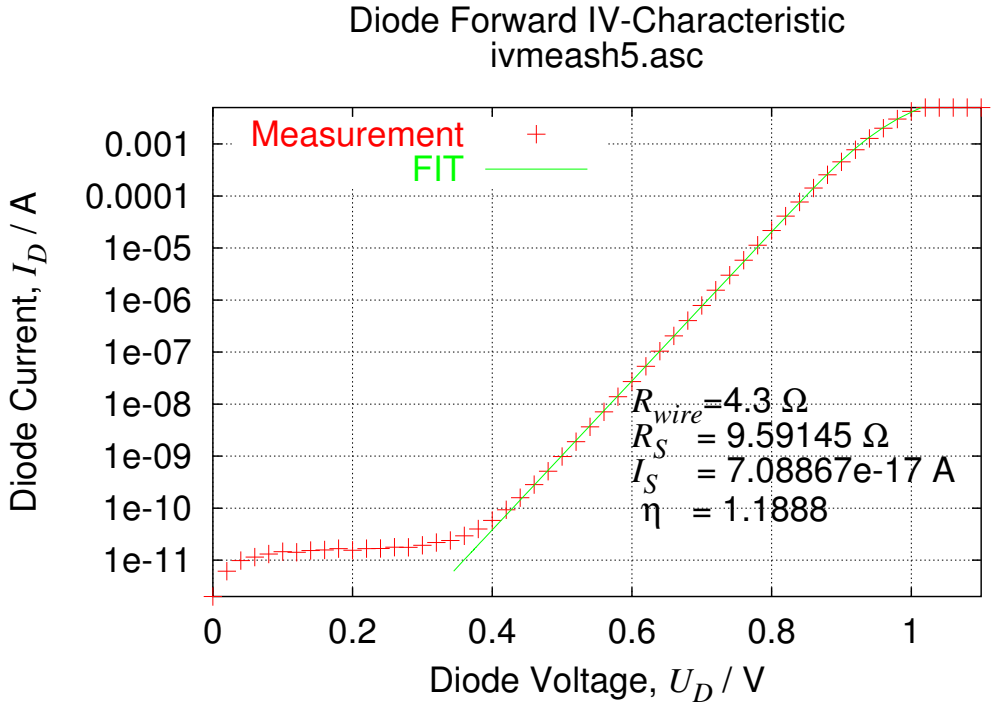


Figure 4.13: Measured IV-characteristics of a planar mixer diode, $r_a = 0.5\ \mu m$.

The extrinsic model consists of a capacitance for the parasitics in parallel to the diode junction, an inductance for the air-bridge, an additional capacitance for the periphery and two pad capacitances. The model is suitable for DC-simulations, S-parameter simulations, harmonic balance analysis and time domain analysis.

S-Parameter measurements 7-110 GHz

This section shows S-parameter measurements in the range $f = 7 \ldots 110\ GHz$ performed at the HELSINKI UNIVERSITY OF TECHNOLOGY and the MILLILAB, Helsinki for IHF THz-Schottky diodes, fabricated with the new design. The measurements are performed with flip-chip mounted diodes on coplanar test mounts on quartz substrate, thickness 500 μm. In combination with additional CV-measurements at 1 MHz, the parasitic capacitance of the actual design for planar mixer and varactor diodes is extracted to $C_p = 8.9 \ldots 10\ fF$.

Figure 4.16 shows a comparison of the measured reflection coefficient S_{11} and the simulated S11 for $I_{bias} = 0\ A$. Figure 4.17 shows the deviation of the simulated reflection coefficient from the measured one. and $I_{bias} = 1\ mA$. The simulation results fit well to the measurement. The maximum error in magnitude is 0.001 and the maximum error in phase is 1.75°. Figure 4.18

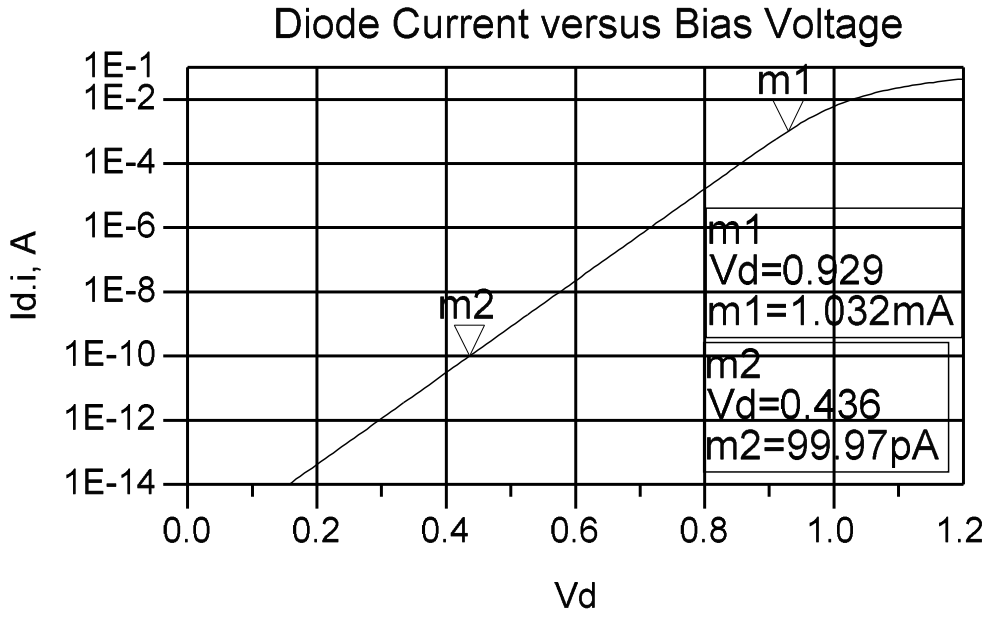


Figure 4.14: ADS2003C *DC simulation results for a planar mixer diode,* $r_a = 0.5\ \mu m$.

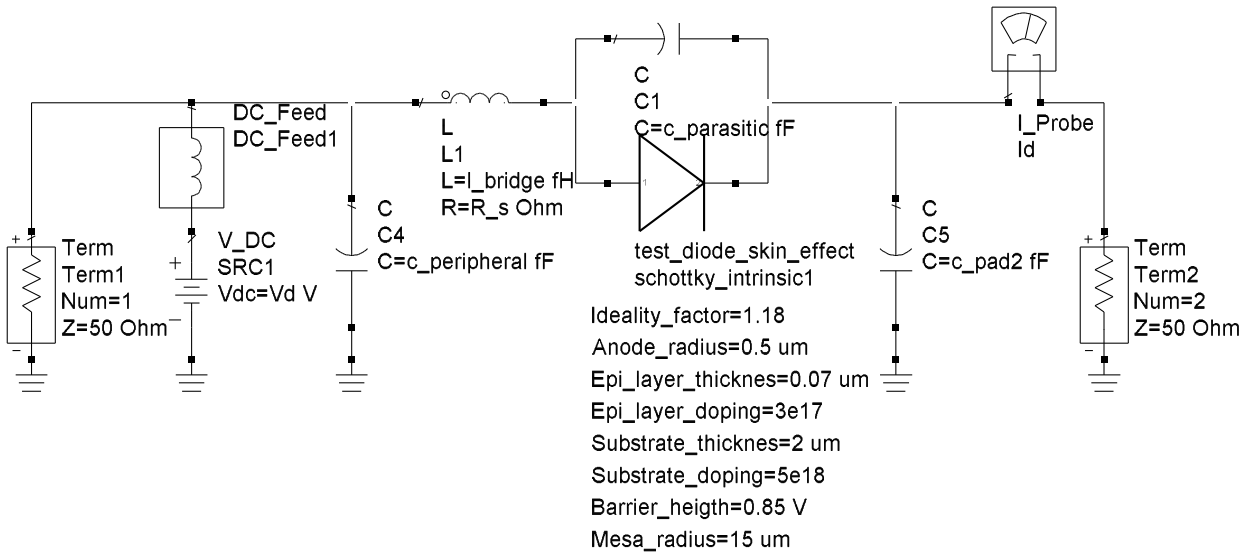


Figure 4.15: ADS2003C *extrinsic model of the IHF THz-Schottky diode.*

shows a comparison of measured and simulated S11 in the high-current region for $I_{bias} = 5\ mA$. The simulation results fit well to the measurement. The maximum error in magnitude is 0.025 and the maximum error in phase is 6°. For higher frequencies up to 110 GHz, the relative error is slightly increasing. With these results, the Schottky-diode model can be used for the simulation of entire mixer systems.

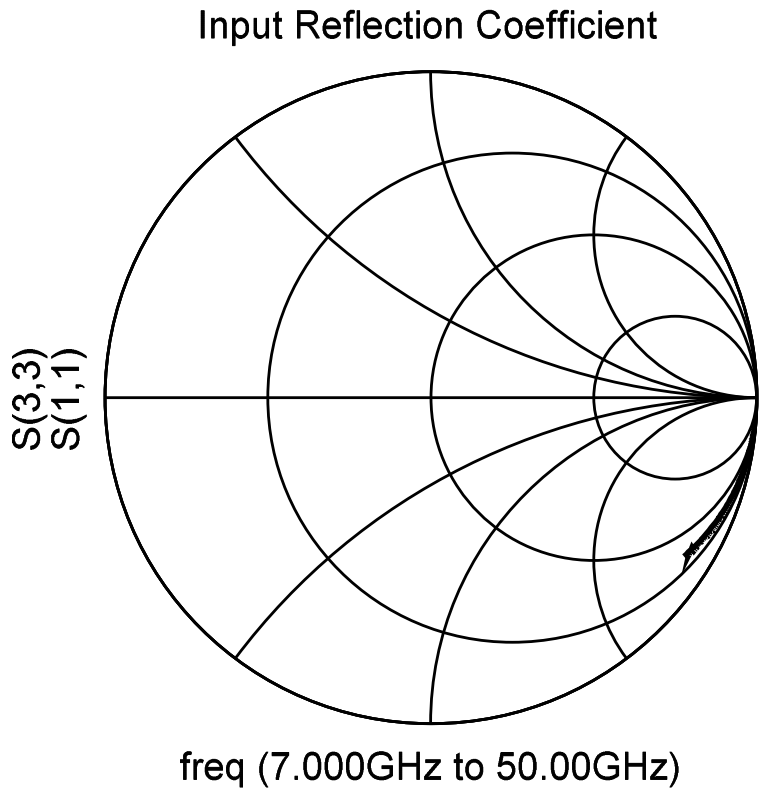


Figure 4.16: Reflection coefficient of a planar THz-Schottky diode, $U_D = 0\,V$.

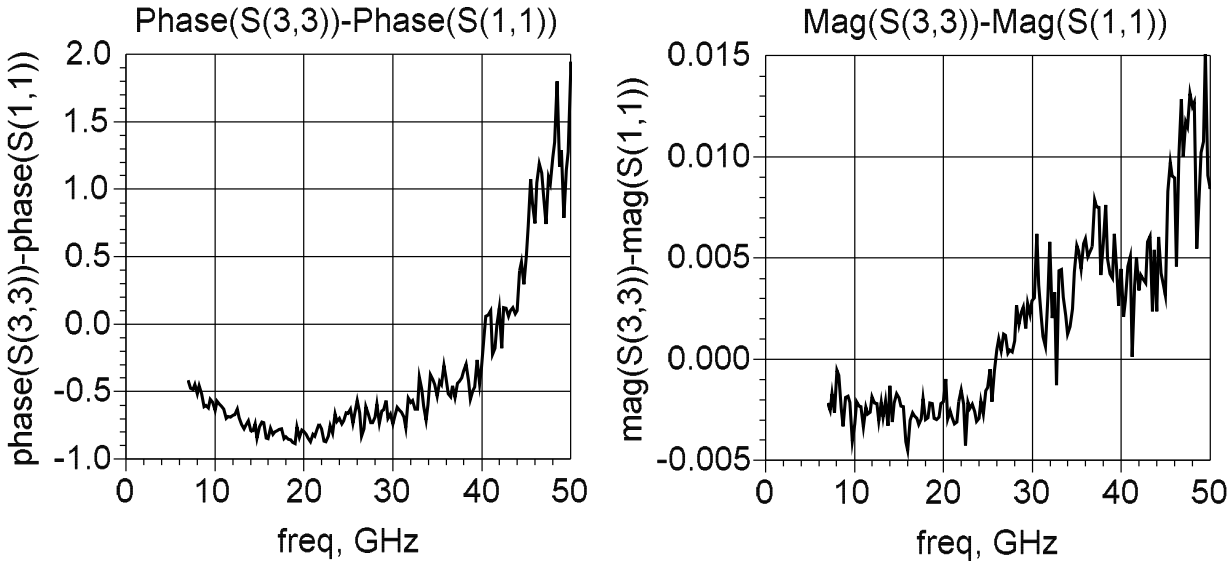


Figure 4.17: Error in phase and magnitude, $U_D = 0\,V$.

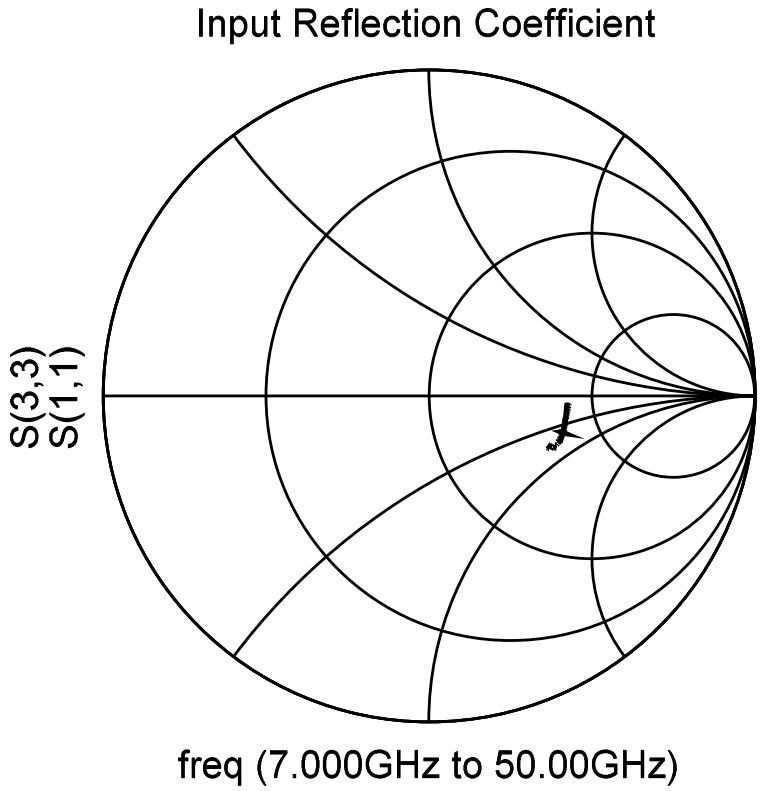


Figure 4.18: Reflection coefficient of a planar THz-Schottky diode, $U_D = 0.98\,V$, $I_D = 5\,mA$.

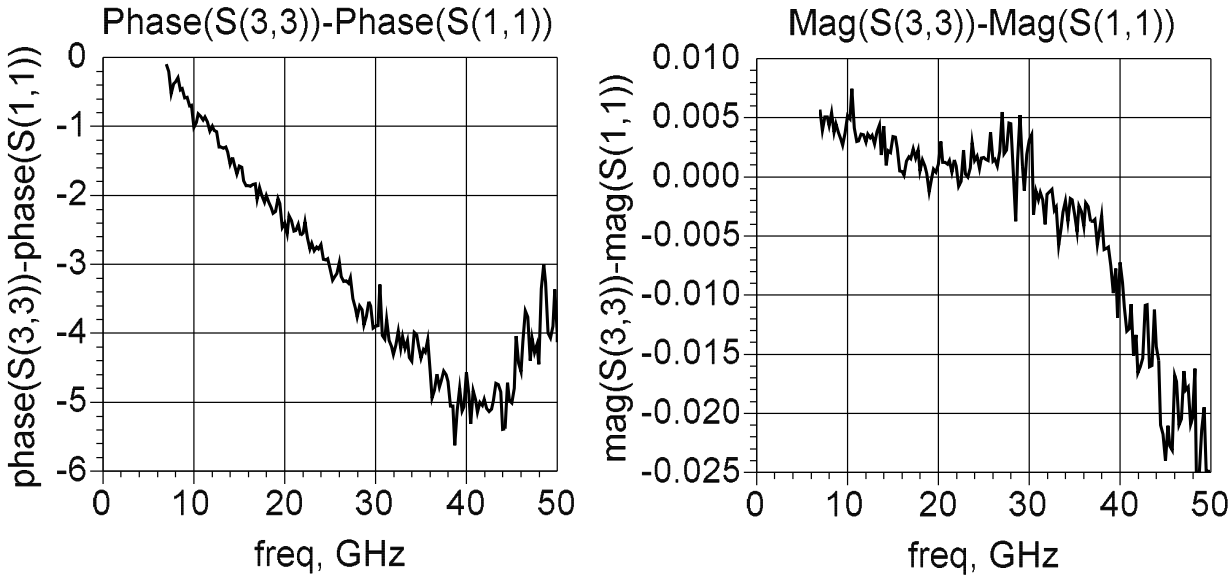


Figure 4.19: Error in phase and magnitude, $U_D = 0.98\,V$, $I_D = 5\,mA$.

4.2.5 Extraction of the junction temperature

The junction temperature of a diode is a figure of interest for reliability tests. The junction temperature is extracted either by the application and the monitoring of electrical pulses of sufficient length or by the increase of the ambient temperature. In the case of the electrical pulses, the shift ΔU in the voltage response is a measure for the temperature increase ΔT. In the case of the temperature method, this shift is detected, if the junction temperature is exceeded. These methods only give an estimation of the junction temperature and do not allow the extraction of temperature distribution in the device. Additionally, numerical electro-thermal simulations are performed for the localization of hot-spots. Using equation 4.13 the diode voltage is described by equation 4.37.

$$U_d = \eta \cdot U_t \cdot \ln\left(\frac{I_d}{A \cdot J_{sat}} + 1\right) \tag{4.37}$$

The temperature dependence of the diode voltage α_{SD} is then determined to equation 4.38.

$$\alpha_{SD} = \frac{\partial U_d}{\partial T} = \frac{K}{q} \cdot \ln\left(\frac{I_D}{A \cdot J_{sat}}\right) - \frac{k \cdot T}{q} \cdot \frac{1}{J_{sat}} \cdot \frac{\partial J_{sat}}{\partial T} = -0.5\,\frac{mV}{K} \tag{4.38}$$

The temperature dependence of the saturation current is determined using equation 4.39

$$\begin{aligned}
\frac{\partial J_{sat}}{\partial T} &= 2 \cdot R^* \cdot T \cdot e^{-\frac{q \cdot \Phi_B(T)}{k \cdot T}} - R^* \cdot T^2 \cdot e^{-\frac{q \cdot \Phi_B(T)}{k \cdot T}} \cdot \frac{\partial}{\partial T}\left(\frac{q \cdot \Phi_B(T)}{k \cdot T}\right) \\
\frac{\partial J_{sat}}{\partial T} &= 2 \cdot R^* \cdot T \cdot e^{-\frac{q \cdot \Phi_B(T)}{k \cdot T}} - R^* \cdot T^2 \cdot e^{-\frac{q \cdot \Phi_B(T)}{k \cdot T}} \cdot \left(-\frac{q \cdot \Phi_B(T)}{k \cdot T^2} + \frac{q}{k \cdot T} \cdot \frac{\partial \Phi_B(T)}{\partial T}\right)
\end{aligned} \tag{4.39}$$

System theory for temperature extraction

The measured pulse response $u_m(t)$ of a diode characterizes the thermal and the electrical properties of the device. Figure 4.20 shows the system theory approach for the extraction of thermal properties.

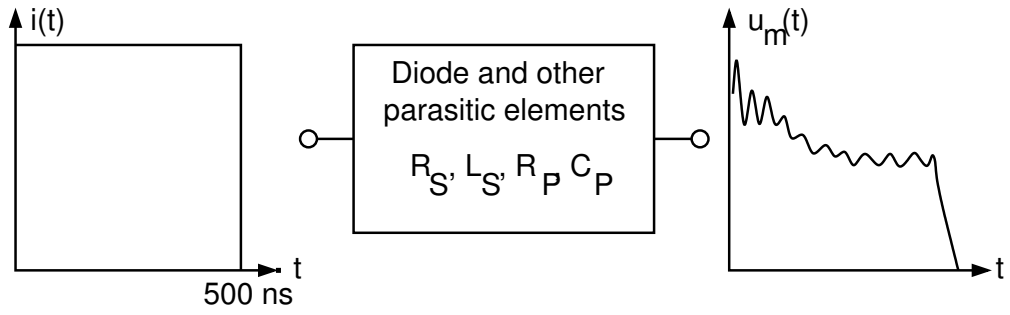


Figure 4.20: Voltage response of a Schottky diode and extraction of the junction temperature.

Explanation of the voltage pulse response

The attenuated sinus-oscillation is caused by the parallel resonance circuit formed from the parasitic elements L_S, C_P, R_S and R_P. The average voltage pulse response $U_m^*(t)$ describes the temperature dependent voltage drop at the diode and the series resistance R_S.

$$\Rightarrow U_m^*(t) = \underbrace{U_D(T)}_{\text{thermal}} + i(t) \cdot R_S \tag{4.40}$$

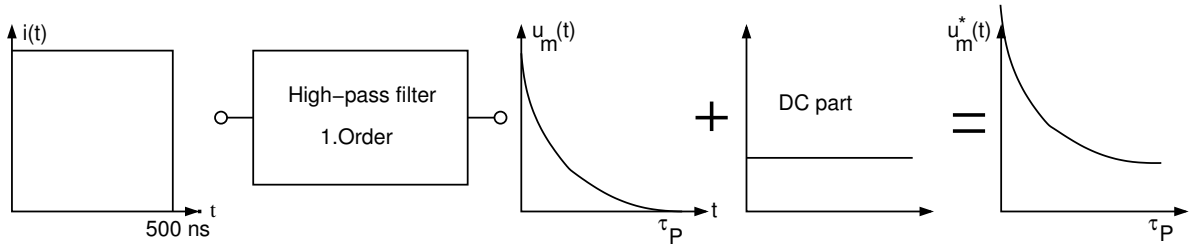


Figure 4.21: Contribution of different parts to the voltage pulse response.

Explanation of the DC part of the voltage pulse response

The DC-part of the voltage response constitutes from the voltage drop over the diode $U_D^* = U_D(T)$ for the maximal junction temperature $T_{max} = T(500\,ns) \approx T_2$ and from the contribution of the series resistance $i(t) \cdot R_S = I_0 \cdot R_S$. The DC part is determined from the stationary state.

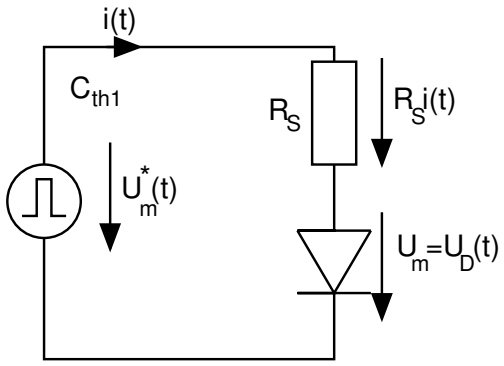


Figure 4.22: Thermal equivalent circuit of the diode.

Simplification for calculation of junction temperature

Equation 4.41 is the linear approximation for the description of the GaAs n-type Schottky diode voltage temperature dependence [103]. The assumptions are in the following given as: $(R_s = 5\,\Omega,\ L_s, C_s \to 0,\ R_p \to \infty,\ I_d = 200\,mA,\ T_0 = 300\,K)$.

$$U_D(T) = 0.98\,V + \alpha_{SD} \cdot (T - T_0) = 0.98\,V - 0.5\,\frac{mV}{K} \cdot (T - T_0) \tag{4.41}$$

The junction temperature of a diode is extracted from the voltage impulse response, cf. figure 4.23 comparing the voltage at $t_1 = 50\,ns$ and $t_2 = 450\,ns$.

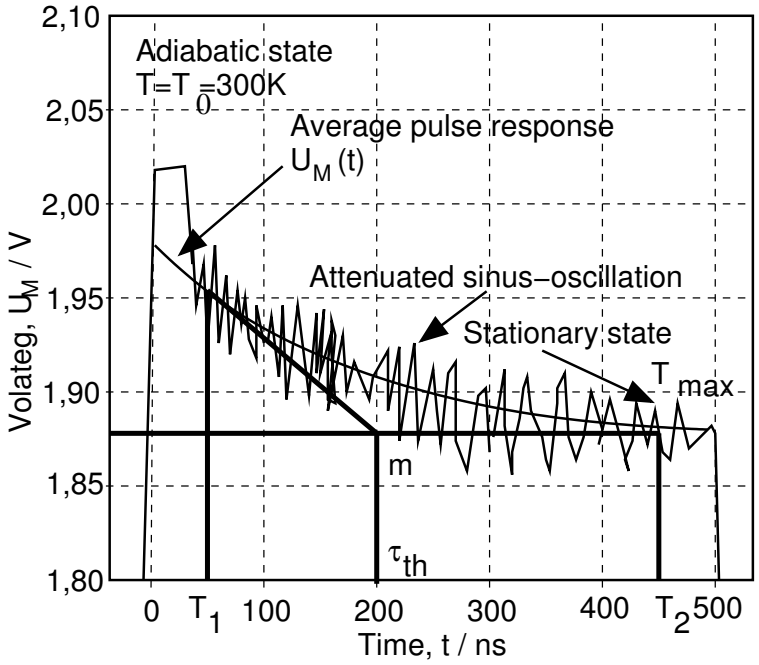


Figure 4.23: Voltage response of a Schottky diode and extraction of the junction temperature.

At $t_2 = 450\,ns$ the diode reached a stationary temperature $(T = const)$. R_s is necessary for the modeling of the power dissipation in the substrate and the peripheral circuitry.

Junction temperature of the diode

This leads in consequence to the extraction of the junction temperature:

$$U_m^*(T) \stackrel{!}{=} R_S \cdot I_d + 0.98\,V - \frac{0.5\,mV}{K} \cdot (T - T_0) \Rightarrow T = T_0 + \frac{1K}{0.5\,mV} \cdot (1.98\,V - U_m^*(T))$$

$$T_1 = T(t_1) = T(U_m^* = 1.95\,V, 50\,ns) \approx 360\,K,\ T_2 = T(t_2) = T(U_m^* = 1.88\,V, 450\,ns) \approx 500\,K$$

Thermal resistance and specific heat capacity of the diode

$$t = t_1 = 450\,ns \quad \Delta T_2 = 500\,K - 300\,K = 200\,K \stackrel{!}{=} P_{el} \cdot R_{th}$$

$$R_{th} = \frac{\Delta T_2}{P_{el}} = \frac{\Delta T_2}{R_S \cdot I_0^2 + U_D(500\,K) \cdot I_0} = \frac{200\,K}{0.2\,W + 0.376\,W} = 347\,\frac{K}{W}$$

$$\tau_{th} = R_{th} \cdot C_{th} \Rightarrow C_{th} = \frac{\tau_{th}}{R_{th}} = \frac{200\,ns}{347\,\frac{K}{W}} = 5.76 \cdot 10^{-10}\,\frac{Ws}{K}$$

Chapter 5

Process Control System

The fabrication process for Schottky-diodes at the IHF TU DARMSTADT is based on a hand-operated technology. A reproducible device quality is only assured by using a process control system for the entire process, which relies on PID's (Process Identification Document), LT's (Lot Travelers) and process control structures for single process steps as initially introduced by ICHIZLI [104–106]. The main technological process steps are the photolithographic definition of structures (including exposure and development of the photo-resist), etching (including dry- and wet-etching) and the deposition of other materials (including SiON and contact metalization). Prior to the introduction of the process control system there existed major problems, not only with electrical device characteristics and a very low fabrication yield but also with mechanical robustness (e.g. the adhesion of the air-bridge) [107].

Figure 5.1 shows this mechanical problem by the way of an planar example diode with torn air-bridge. Mechanical stability enhances changing the airbridge deposition method from magnetron sputtering to e-beam and thermal evaporation with an additional Ni/Ag seed-layer for airbridge adhesion.

In the case of the photolithographic steps, alignment precision and proper choice of exposure & development times are important and can only be controlled by additional control structures. The etching process is controlled by measuring the etch depth and verifying the etching rate. The thickness of other deposited materials are also measured but in case of the metals, the electrical and mechanical properties have to be determined using additional test-structures. The process control parameters are described in section 5.2. The corresponding control structures are integral part of the latest mask set for the fabrication process and are shown in section 5.3. These process control structures for each technological step enable a repeatable fabrication of planar structures and a yield increase from 6 % to over 60 % [83].

Figure 5.2 and 5.3 give a survey of the process (boxes) and the process control parameters (triangles), separated into backside and front-side processing, which corresponds to the fabrication process. The single fabrication steps are divided on the one hand in critical and uncritical steps, on the other hand in reversible and irreversible steps. Therefore, there are 4 groups of process steps:

- critical-reversible process steps
- critical-irreversible process steps
- uncritical-reversible process steps
- uncritical-irreversible process steps.

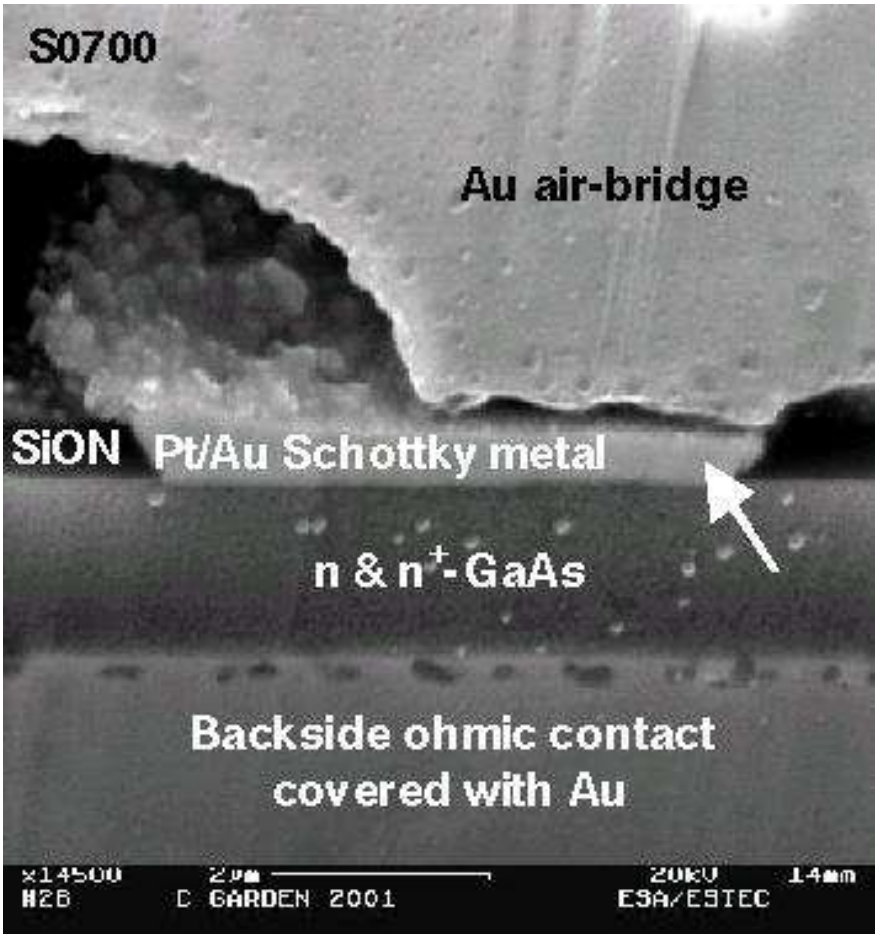


Figure 5.1: REM image showing adhesion problems of the air-bridge with magnetron sputtering as deposition technique.

There are process steps, which are critical in view of their controllability or strongly affect device performance. Small variations in critical process steps have a strong influence on device characteristics (e.g. an increased anode diameter strongly affects the electrical behavior of the device) or even prevent proper operation of the device (e.g. misalignment of the air-bridge to the anode, over-etching). The uncritical steps are either easy to control from the technological point of view (e.g. metal evaporation) or variations only have a negligible influence on the electrical characteristic of the final device (e.g. the thickness of the pillars). The reversible process steps are mainly the lithography steps (except the lithography for the air-bridge formation). These steps are repeatable, if misalignment, over- or under-exposure is determined. The irreversible process steps modify the sample permanently (e.g. etching, metal evaporation) [83, 85].

Considering figure 5.2 and 5.3, one can determine three process steps, which are critical and irreversible with respect to DC characteristics. On the one hand, these process steps are connected to the anode formation, on the other hand to the air-bridge formation.

The following paragraph shortly explains critical, irreversible process steps. Anodes are defined on the SiON-layer using photo-resist (reversible). In the next step, anodes are opened using reactive ion etching (irreversible) or SF_6-plasma etching. Directly afterwards, anode contacts are formed by electro-chemical plating of platinum (irreversible). These steps are of major impor-

tance for device quality and small variations can change the final device characteristics. Therefore, there is only a small tolerance range for these steps. A breakthrough for the Schottky contact formation is the introduction of "dummy"-anodes, refer to section 5.1, which provide plating conditions similar to those for whisker diodes and are removed after electrochemical deposition of the Schottky-contact [84]. In the case of the airbridge formation, the lithography step is not repeatable. The airbridge is defined by photo-resist and then plated on a seed-layer that itself partly is also on the top of a photo-resist layer. Removing the photo-resist for the airbridge definition (e.g. because of misalignment) before plating endangers the seed-layer (e.g. by unintentional lift-off).

With respect to RF properties, the formation of the ohmic backside contact is critical, too. The dimensions of the backside contact and the distance to other conductive material is a key factor for the reduction of the parasitic capacitance, C_p, as indicated in section 4.2. With the actual wafer design, a further reduction of C_p is not possible because of technological constraints (see step 3 and 4 in figure 5.2). As a consequence a new wafer design must be developed with an additional AlGaAs etch-stop layer. Beyond, a new mask-set with reduced contact dimensions is mandatory for further improvement of RF capabilities.

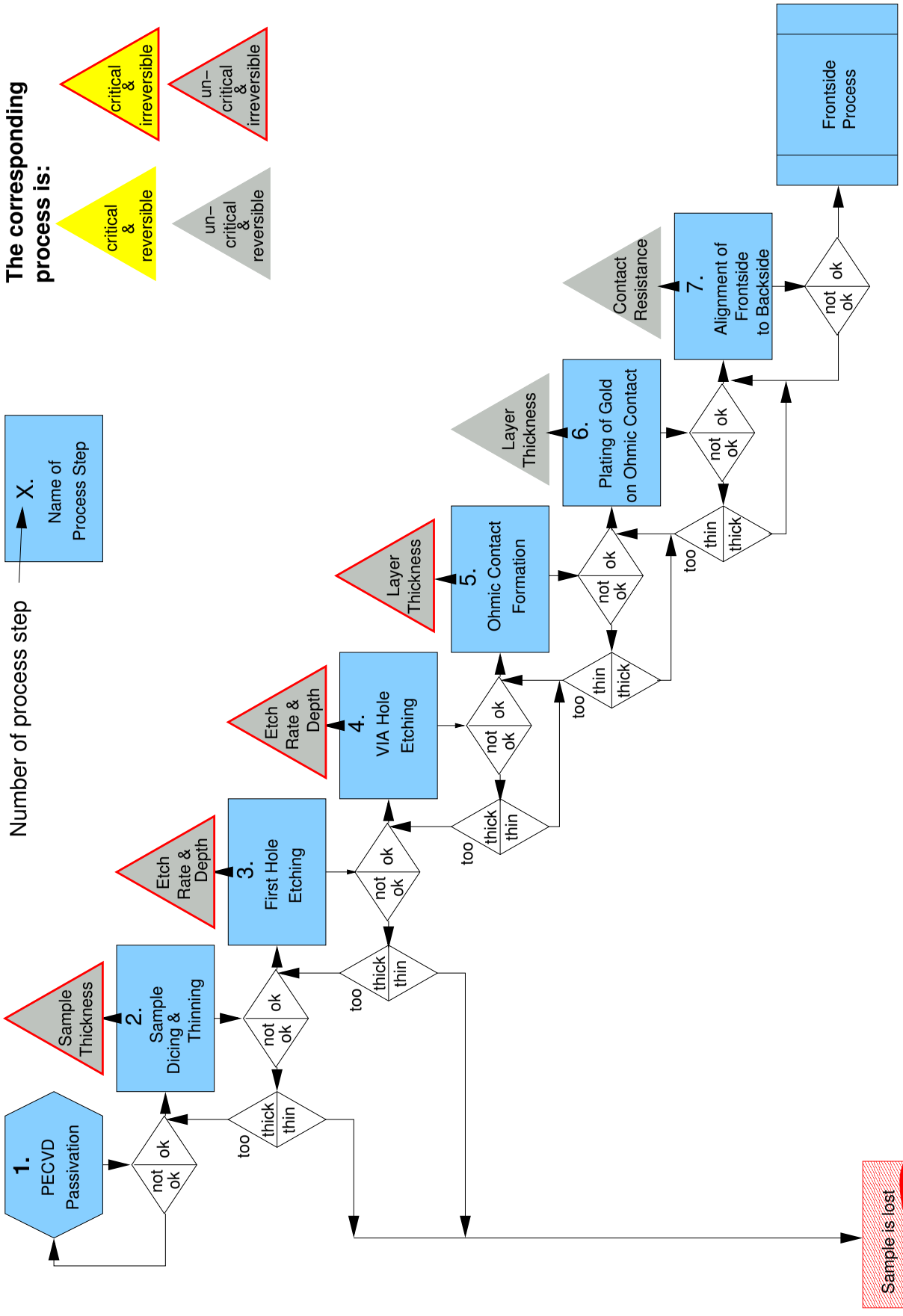


Figure 5.2: Process control for the backside ohmic contact of planar Schottky diodes.

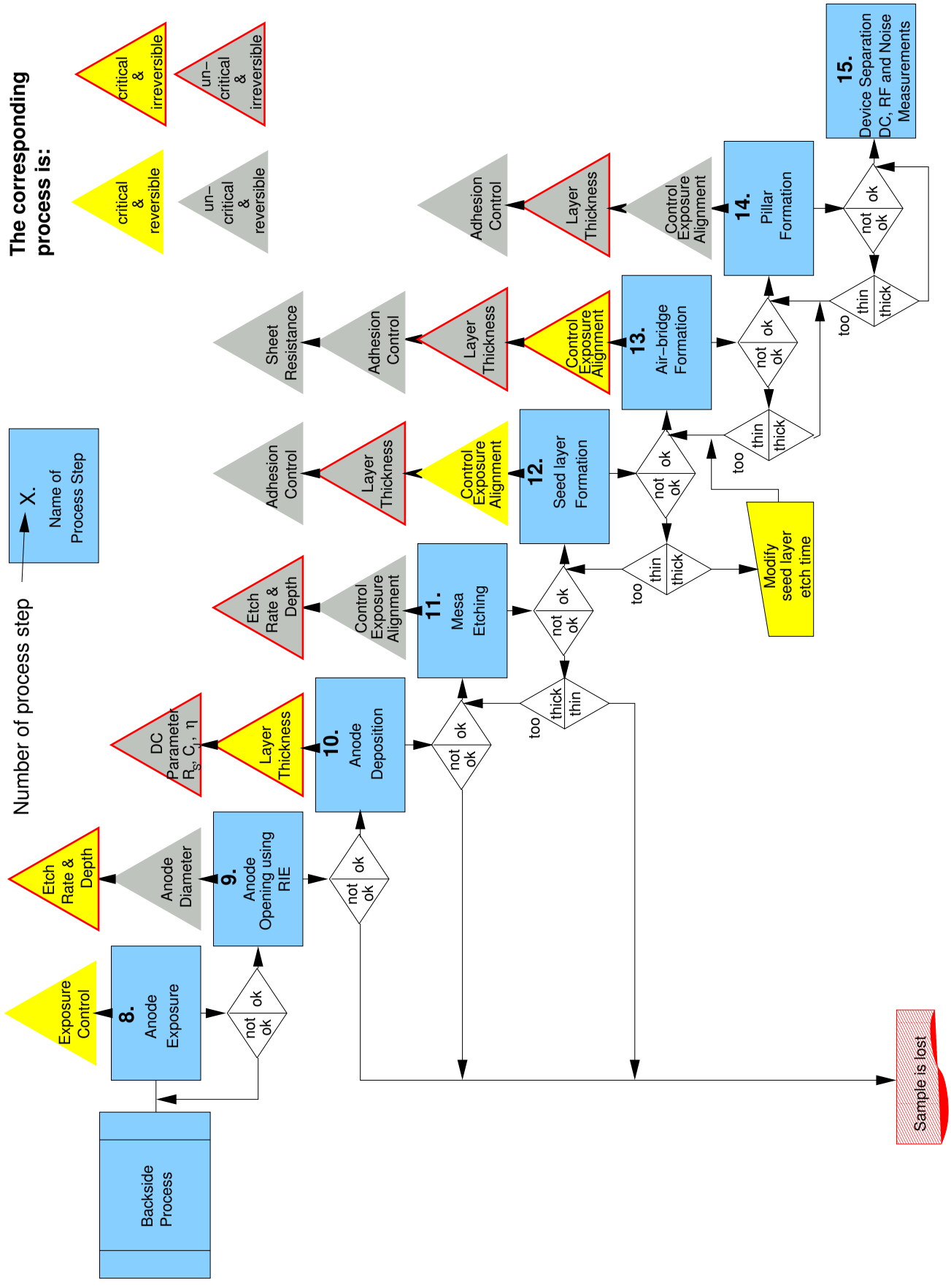


Figure 5.3: Process control for the front-side process of planar Schottky diodes.

5.1 Introduction of honeycomb "Dummy"-anode arrays

The electrolytic Schottky metal deposition step is most critical in view of planar diode performance. Figure 5.4 shows a FIB prepared TEM-image of a planar Schottky diode with non-uniform Platinum deposition. A detailed analysis of the electrolytic Pt-deposition on GaAs is performed in 2001 [37] under supervision of RODRIGUEZ. This work describes the occurrence of complex reaction processes at the metal-semiconductor interface during electrolytic deposition (e.g. Ga-outdiffusion through the Pt-layer during formation) as it is shortly explained in 2.2.4. An additional challenge is the Schottky contact formation with planar mixer diodes ($r_a < 1\ \mu m$). Figure 5.4 shows a TEM-image of a FIB-prepared planar mixer diode before optimization of the deposition process. Platinum is only deposited in the left side of the anode area. The rest of the anode area is covered with a Ni/Ag seed-layer, which results in poor diode and reliability characteristics due to enhanced diffusion and localized high current densities. In this case, optimization steps are mandatory because reliability analysis makes only sense with good devices.

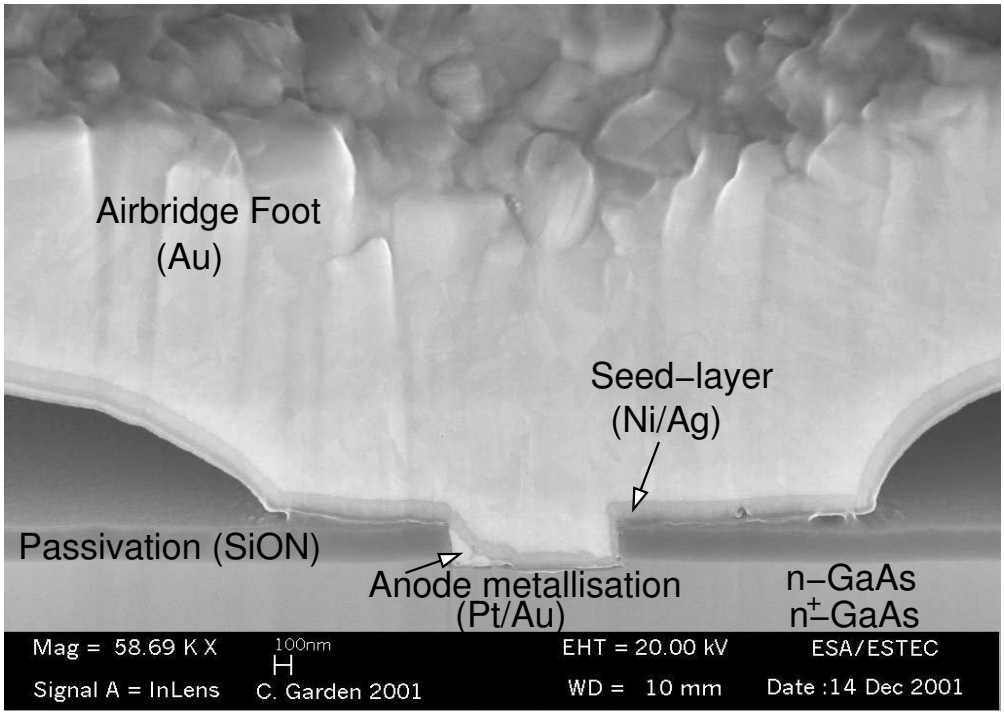


Figure 5.4: SEM image of FIB prepared planar diode showing Non-uniform electrolytic Pt deposition with planar Schottky diodes.

The contact formation optimization is based on the introduction of honeycomb "dummy"-anode arrays additional to the real anodes before deposition of the metal. The advantages of these measures with regard to process control and subsequent optimization are detailed as follows. A comparison of CHF_3 RIE- and SF_6-Plasma etching shows a reduction of RIE-induced defects, which are microscopic seed-cells for degradation, due to the high selectivity of SF_6 plasma-etching. Different approaches for the electrochemical deposition of the Schottky metal are currently under investigation, e.g. a quasi-in-situ approach or very complex pre-processing prior to deposition are investigated.

In this context, a new measurement set-up allows the online-monitoring of electrical pulses

during electrochemical deposition, cf. appendix C. This systematic analysis resulted in excellent noise- and DC-characteristics [86]. The introduction of the "dummy"-anodes is based on the knowledge of electrochemical deposition characteristics for whisker-contacted diodes which demonstrate excellent RF- and noise performance. The "dummy"-anodes allow a transfer of the deposition parameters as well as a transfer of the pre- and post-processing from whisker-technology to the planar diode fabrication [84]. On the other hand, this transferability allows process control and reliability studies on whisker-diodes, which is cheaper and less time-consuming than on planar diodes.

5.2 Process control parameters

The process control system relies on the control of process-relevant parameters as early as possible after the processing of the corresponding fabrication step. The extracted parameters are the basis for the decision to continue or to stop the batch (i.e. the samples under process). The process control mechanisms can be classified into three groups.

1. Process-step control
2. Material properties control
3. Final device characterization

The first group consists of control mechanisms that help to evaluate the quality of single process steps and if appropriate, determine whether correction actions should be taken. The second group of parameters provides information on the electrical and mechanical behavior of the processed structures. The third group of parameters characterizes the quality of the final device.

5.2.1 Process-step control parameters

The technological related process parameters to be controlled are:

- alignment
- exposure & development times
- etching depth and uniformity
- thickness, adhesion and roughness of deposited materials.

The etching depth and the thickness of deposited materials are controlled using an ALPHA-STEP measurement instrument providing a resolution down to 50 nm. Furthermore, quick control can be performed with the optical microscope or a micrometer screw MITUTOYO ABSOLUTE, Code 215-150) down to an accuracy of 1 µm. The etching and metal deposition steps are not reversible and the measured values are recorded for process evaluation. Usually, these process steps are either well controllable or have no influence on the electrical parameters because a deviation from the desired value does not affect the performance of the final device up to a certain degree. If one of these parameters is out of the tolerance range, the sample is lost, and a completely new process must be started. In contrary, the alignment precision and the exposure time are directly controlled after processing and the process can be repeated if either the alignment or the exposure

parameter is out of the tolerance range. The tolerance for alignment is ± 4 %, the tolerance for the exposure is ± 0.1 µm. In case of the anode formation, exposure control is of special interest for the fabrication of anodes with a certain diameter. The alignment control is important for the symmetry of the entire structure. In the worst case, the anodes are not in the center of the mesa and the air-bridge has no contact to the anode prohibiting proper device operation.

5.2.2 Electrical and mechanical process parameters

The electrical and mechanical process parameters are necessary for the in-line process control. They mainly concern the quality of the metal that is deposited either on the backside as the cathode, or on the front-side as anode, seed-layer or air-bridge metalization. The parameter for the determination of the ohmic contact quality is the contact resistance, which is extracted from measurements with TLM structures (see section 5.3.2). The parameters for the quality of the anode Schottky-contact are the series resistance R_S and the ideality factor η that are determined directly after the formation of the Schottky-contact using whisker-contacted diodes, which are described in 5.3.2. The adhesion of the different metal layers to the underlying surface is the parameter for the determination of the mechanical robustness.

5.2.3 Parameters for the characterization of the final device

The performance of the final device is determined considering the electrical properties which are detailed in section 4.2.3. The corresponding parameters are extracted firstly from DC-measurements in terms of the series resistance R_S, the ideality factor η, the reverse breakdown voltage U_{br} and the junction capacitance C_j, secondly from noise measurements and last from RF S-Parameter measurements [86]. The cut-off frequency of the device is estimated by R_S and C_j. These parameters are extracted using different calibration structures that have the calibration reference level on the one hand at the pads, on the other hand at the mesa. Using these parameters, an equivalent circuit for the planar diode is designed e.g. for AGILENT ADS (section 4.2.4) or with OCTAVE. The interface quality and the microwave noise properties are characterized by noise measurements at 2...5 GHz in collaboration with the LHFT UNI ERLANGEN.

Up to now there is no knowledge about the influence of the presented parameters in this section on the performance of the final device. Therefore, the first steps to an evaluation programme are presented in section 5.4 and section 5.5. Latest results show a correlation between IF-noise measurement and high-frequency noise measurements at 150 GHz.

5.3 Control structures

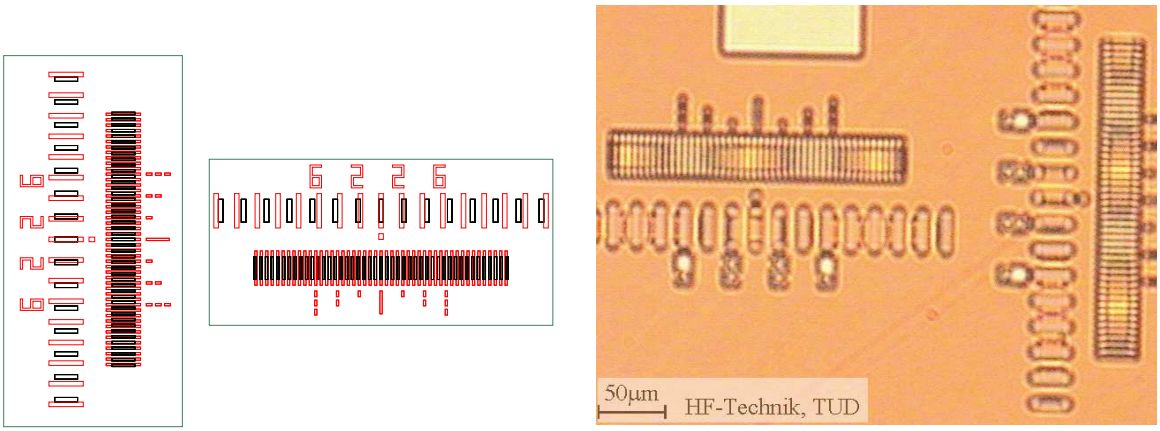
The control structures are divided into three groups equivalent to the process control parameters. The first group contains control structures for the technological process, which are alignment- and exposure control structures. The second group is necessary for the control of the typical electrical parameters during the fabrication process (in-line process-control) and for adhesion control. The third group consists of calibration structures for network analyzer measurements and the extraction of equivalent circuit parameters. Additionally, noise measurements are an indicator of the interface quality and device performance. In the following description, these three groups of control structures are referred to as:

1. Technology control structures:
   - Alignment control structure,
   - Exposure control structure.
2. Device control structures:
   - TLM-structures for control of the ohmic contact quality,
   - Whisker-contacted diodes for control of the Schottky-contact quality,
   - Meander structure for control of the metal layer quality,
   - Pads for adhesion control.
3. Calibration structures:
   - Open, short and 50 Ω resistance with pads as the reference plane,
   - Open and short with anode and mesa as reference plane.

5.3.1 Technology control structures

Alignment control structure

The alignment is performed using high-precision alignment marks based on a double VERNIER structure with $\frac{9}{10}$-division (bar width 5 µm) and $\frac{19}{20}$-division (bar width 2 µm). The one part of this marks is formed in the anode formation step. The counterparts are on the masks of the following process steps. With these structures the alignment control is precise down to 0.5 µm, which is sufficient for the alignment in all process steps. The alignment control structures can be used for the alignment itself and the result can be verified after exposure and development. The rectangles around the alignment control structure are 325 µm × 156 µm.

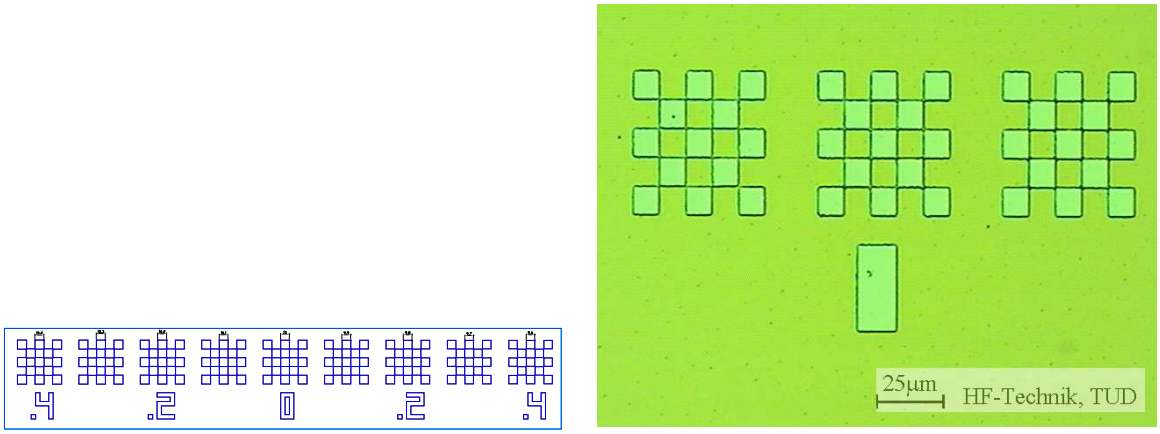


(a) *Alignment control structure.* (b) *Realized alignment control structure.*

Figure 5.5: Comparison of designed and realized alignment control structure.

Exposure control structure

The exposure control structures give information on over/under-exposure of the sample, or over/ under-developing. This control structure consists of squares with dimensions varying from 9.6 to 10.4 µm with 0.1 µm steps. Depending on which square corners have contact, the exposure is controlled. There are two exposure control structures at different height levels (one on the top of the SiON-layer and one on top of the AlGaAs-layer). Therefore, there is additional information on the exposure corresponding to the sample topology.



(a) *Exposure control structure.* (b) *Realized exposure control structure.*

Figure 5.6: Comparison of designed and realized exposure control structure.

5.3.2 Device control structures

TLM-structures for control of the ohmic contact quality

(2 TLM Structures per sample)

The quality of the Ohmic contact is controlled using the TLM-method. The TLM-structures, cf. figure 5.7 are fabricated using GaAs-channels of 20 µm width with linearly increasing length (200 µm, 400 µm, 800 µm and 1600 µm) and consecutively resistance. The contact area is 20 $\times$ 20 µm^2. The ohmic contacts are realized as backside contacts and processed in the same way as the ohmic contacts for the planar Schottky-diodes. The accuracy of this technique depends on the contact dimensions. With this design, these dimensions are influenced by the back-to-front alignment step, the via-hole opening and the contact formation. The contact resistivity can be determined after the front-to-back alignment. The backside contacts are opened with this process step and are contacted from the front-side with whiskers determining the contact resistance with DC-measurements.

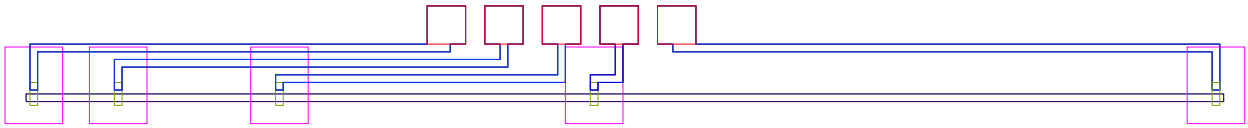


Figure 5.7: TLM structure for the determination of the ohmic contact resistance.

Whisker-contacted diodes for control of the Schottky-contact quality

(4 whisker-contacted diodes per sample)

The control structures, cf. figure 5.8 for the Schottky contacts are similar to the whisker-contacted Schottky-diodes and the diameter is the same as that of the planar diodes.

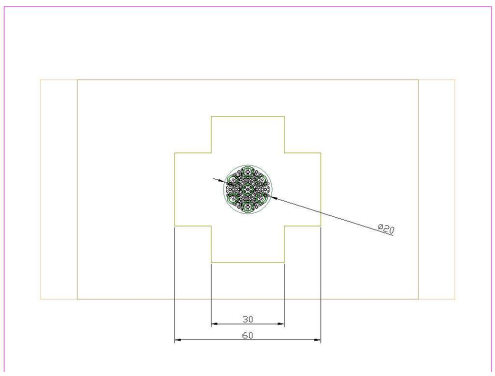


Figure 5.8: Whisker contacted Schottky diodes.

The mesas have the same size and the backside ohmic contact corresponds to the superposition of two of the planar-structure backside contacts rotated 90°. They provide the possibility to measure the Schottky contact directly after the electrochemical deposition and allow a prediction of

the finally reached electrical DC parameters. The via-hole on the backside of these control structures consists of two crossed rectangles, which have the same dimensions as the via-hole for the Schottky-diodes.

Meander structure for control of the metal layer quality

(1 Meander structure per sample)

The resistivity of gold strongly depends on the purity and concentration of the electrolyte as well as on the plating rate. The following structure gives information on the quality of the plated gold-layer, which is used for the air-bridge formation. The meander structure in figure 5.9 provides a calculated resistance of approximately $R_M \approx 2 - 5\ \Omega$ and is therefore high enough for DC-measurements. The vertical distance of two lines is 100 µm, the horizontal distance of two lines is 250 µm. The width of the line is 5 µm. The distance between the two axes of the meander is 145 µm.

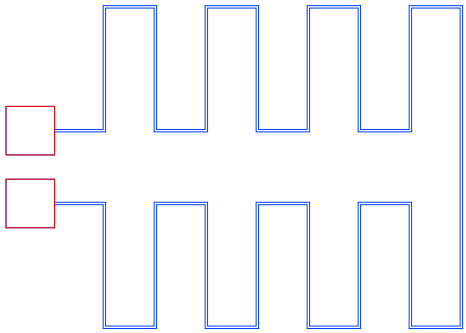


Figure 5.9: Meander structure.

Pads for adhesion control

In figure 5.10, there are four pads for adhesion control, which are squares of 100 µm $\times$ 100 µm^2. One is for the adhesion test of the anode metal, one for the seed-layer adhesion test, one for seed-layer and air-bridge adhesion test and one for the seed-layer, bridge and pillar adhesion test.

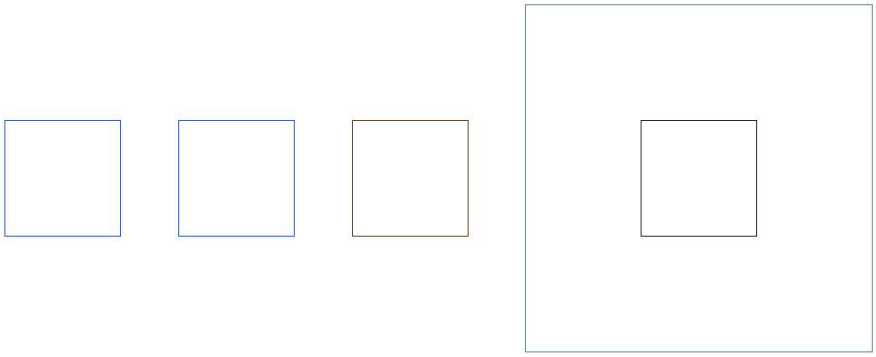


Figure 5.10: Pads for adhesion control

5.3.3 Calibration structures

Open, short and 50 Ω resistor with pads as reference plane

The calibration structures, refer to figure 5.11, 5.12 and 5.13 are designed with the pads as the reference plane. In the case of the open, there is no backside-processing and the pads are designed like the ones of the Schottky-diodes. The short is realized contacting the backside ohmic contact with the seed-layer and the bridge. The 50 Ω resistor is realized using a thin-film NiCr-layer, which has been developed for the IHF fabrication facilities. There are three structures with thin-film-metalization which differ by ± 7 % , which is the expected production tolerance for the thin-film technology.

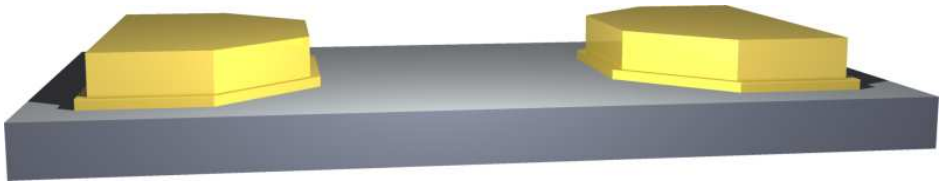


Figure 5.11: Open for calibration for S-Parameter measurements.

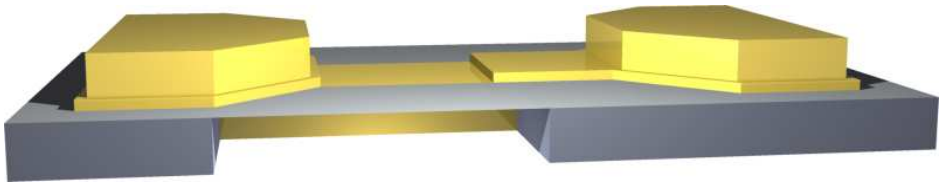


Figure 5.12: Short for calibration for S-Parameter measurements.

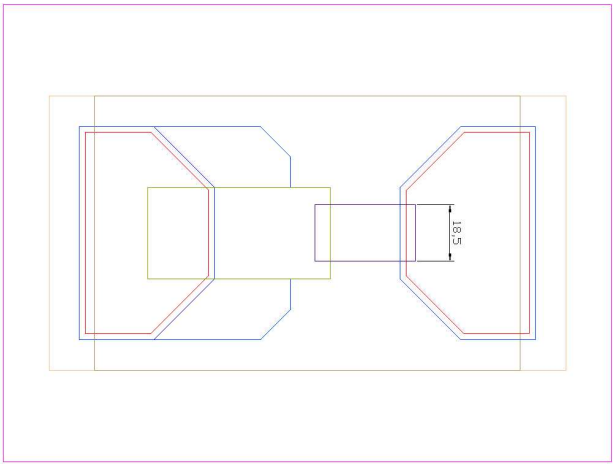


Figure 5.13: Thin film resistor with 50 Ω.

Open and short with anode and mesa as reference level

Additional to the common calibration structures an open and a short are designed, which have the mesa as reference level. These structures are identical to the Schottky-diodes, but have in the case of the open no anode and in the case of the short no mesa and thus a direct contact of the bridge on the backside ohmic contact. In the case of the short, the seed-layer opening on the mesa is increased to provide a secure opening of the photo-resist layer (which is in this case lower than for the Schottky-diodes).

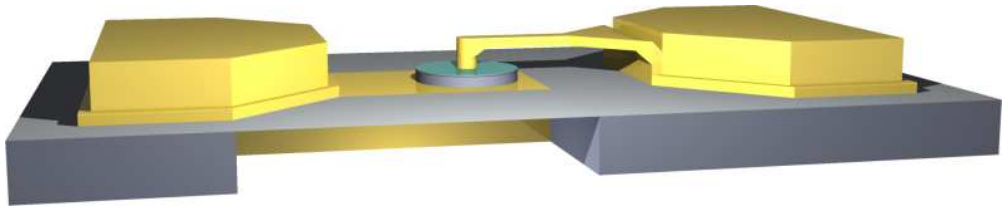


Figure 5.14: Open for the extraction of parameters for the design of an equivalent circuit

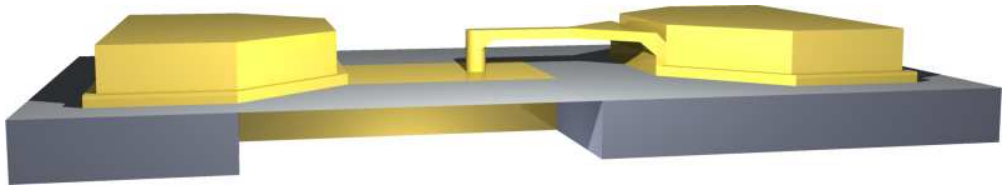


Figure 5.15: Short for the extraction of parameters for the design of an equivalent circuit

5.4 Quality criteria

The standard quality criteria for mixer and varactor Schottky diodes are the respective cut-off frequencies, the ideality factor, the reverse-bias breakdown properties, and the noise temperature as they are introduced in section 4.2.3. All these factors have direct influence on the performance of mixer and multiplier circuits. The calculation of the cutoff frequency of Schottky diodes, as defined in equations 4.34 and 4.35, requires the extraction of the values of R_s, C_{j0} and M. The different figures of merit can be derived from different measurements as outlined in this section. Section 5.5 briefly sketches the procedures followed for DC-, S-parameter and microwave noise measurements. C_{j0} and M may be obtained directly from capacitance-voltage measurements. The reverse-bias breakdown properties of the diode can be examined also through I-V measurements. The equivalent noise temperature of mixer diodes can be obtained from microwave noise measurements. Furthermore, the values of R_s, C_{j0} and M can be extracted from S-parameter measurements of the diodes and of calibration structures, which are available in the diode sample (see Section 5.3).

5.5 Diode characterization methods

The different measurements required for the characterization of the diodes are presented in detail in section 4.2.3. This section briefly describes the instruments foreseen for these measurements and the structures included in the diode mask for this purpose. DC measurements are performed using a HP 4145A Semiconductor Analyzer. The 2-point measurements are carried out contacting the diode pads with gold-plated AuNi wire whiskers or coplanar pico-probes. The whiskers add an additional 10Ω to 14Ω series resistance to the measurement which must be taken into account in the extraction of the diode parameter R_s. C-V measurements are performed using an HP 4279A C-V Meter operating at 1 MHz. Furthermore, the measurement set-up at IHF TUD enables subsequent I-V and C-V measurements of the same diode without re-contacting. The measurements can be performed on-wafer before and after device separation.

A problem encountered in the determination of C_{j0} of mixer diode arises from the inability of C-V measurements of planar diodes to discriminate between junction capacitance and parasitic capacitance, which can be viewed as connected in parallel. Since the parasitic capacitance of the planar structure has a value near 8 fF, the precision of mixer diode C_{j0} ($\simeq$1 fF) is seriously affected. However, whisker-contacted structures with nominally identical anode diameters as that of the planar structures are present on the mask and can be used to determine the value of $C_{j0} \approx 1\ fF$.

S-parameter measurements of the diodes and the corresponding calibrating structure kit can be performed at IHF-TUD using a HP 8510C Vector analyzer up to 26.5 GHz. One-port measurements are performed using a two-point probe. The distance between diode pads was designed considering the size of the probe. The use of the calibration structures and proper bias tees should allow the extraction of accurate equivalent circuits of the diodes. Microwave noise measurements at 2 GHz can be performed at the UNIVERSITY OF ERLANGEN. The details of the measurement procedure are found in [85, 86].

5.6 Diode characterization programme

Table 5.1 presents the characterization methods which will be applied to the different categories of diodes. These can be classified as fabricated, functioning and deliverable devices, where each

group represents a subset of the precedent one. All fabricated devices are characterized with I-V measurements and optical-microscope pictures. Also, selected non-functioning devices are SEM-characterized, if they show fabrication defects that might ease failure identification.

	Varactors			Varistors		
	Fab'd	Funct'g	Deliv.	Fab'd	Funct'g	Deliv.
Opt. Microscopy	√	√	√	√	√	√
SEM Microscopy	×	×	√	×	×	√
I-V measurements	√	√	√	√	√	√
C-V measurements	—	√	√	—	—	—
Measurements of C_{j0}	—	√	√	—	√	√
S-Parameter @ 26 GHz	—	×	√	—	×	√
Noise meas. @ 2 GHz	—	—	—	—	×	√
— : no structures characterized × : selected structures characterized √ : all structures characterized						

Table 5.1: *Diode Characterization Programme*

Full characterization is only applied to delivered diodes and some other functioning, non-delivered devices. Full characterization of all electrically functioning devices is not possible, due to the high cost of time-consuming characterization methods like SEM microscopy and S-parameter and noise characterization. Furthermore, no microwave noise measurements will be performed on varactor diodes, since microwave noise is not an important issue in frequency multiplication. Similarly, no C-V measurements will be performed on varistor diodes, for which the capacitance modulation properties are intrinsically limited due to the structure of the epitaxial layer.

Chapter 6

Results

This chapter illustrates the results for the investigated components. The TLP-approach is used for a very fast feedback to technology and as a reliability analysis tool in a process control system. The following sections show the measurement results and their interpretation for:

- HBT transmission line model (TLM)-structures,
- PCM-HBT,
- RF-HBT from different technologies,
- THz-Schottky diodes.

These results are obtained using the TLP-approach presented section 3.2. The presentation of the results is organized for each device following this test approach in three sections:

1. determination of the thermal time constant,
2. determination of the threshold for coarse degradation and,
3. electrical ageing tests using pulse sequences.

The characteristic parameters for degradation monitoring are selected following section 4.2.3 and section 4.1.2. The interpretation of the measurement results is based on the available theories for degradation and failure mechanisms as reviewed in chapter 2. In the case of the HBT, section 6.3 shows for the first time a comparison of an Arrhenius-based stress test at elevated temperature and DC level with the TLP-method. Relevant defect mechanisms and the influence of leakage currents on reliability issues in connection with HBT are discussed in [50, 76, 108]. In the case of THz-Schottky diodes, the application of the TLP-method for process control and optimization , cf. chapter 5, is demonstrated [106]. In this case, the TLP-method shows its advantage in contrary to Arrhenius-based stress tests, which are still performed by NMRC as a first step to space qualification of these components. Finally, the identification of degradation and failure mechanisms with different stress tests is supported by TEM-investigations on FIB-prepared samples.

6.1 Results for TLM structures

Transmission Line Model (TLM)-structures are control structures for the verification of the quality of different layers and contact systems. Basically, they consist of channels in the layer of interest with ohmic contacts with different spacing in between. Resistance measurements for different spacings provide information on the sheet resistance and the contact resistance. In the case of HBT, TLM-structures are available for the intrinsic and extrinsic base-, the collector- and the emitter-layer of the respective devices. The contact spacing varies in the range $w = 6$ ...60 μm. Additionally, these structures give information on the electrical stability of the respective layer when objected to the pulsed-step stress approach.

6.1.1 TLM thermal time constants

This section shows thermal time constants for TLM-structures for the collector and the base layer as representatives for other TLM-structures. The thermal time constant is extracted from the measured pulse response by fitting the measurement data to equation 6.1.

$$U = U_0 + A_1 \cdot \left(1 - e^{-\frac{(t-t_0)}{\tau^{th}}}\right) \tag{6.1}$$

The thermal time constant is extracted in the case of the collector-TLM to $\tau_{thermal} = 1.8\,\mu s$ and in the case of the base-TLM to $\tau_{thermal} = 2.7\,\mu s$ as shown in figures 6.1 and 6.2. The scattering in the measured impulse response is due to cable reflections in the system.

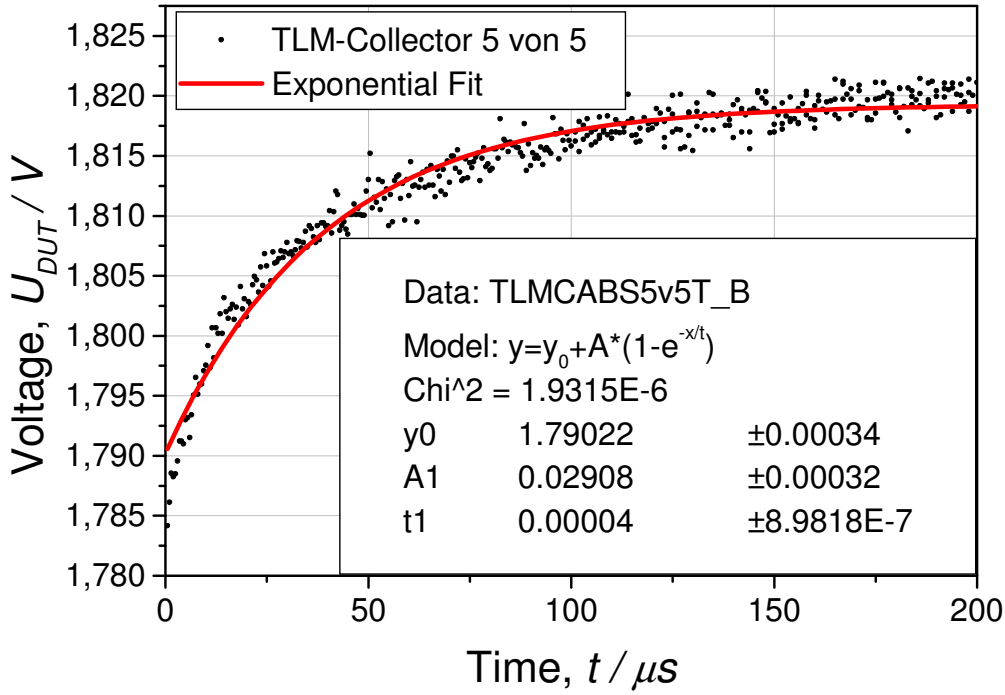


Figure 6.1: Measured on-wafer pulse voltage response of a TLM-collector structure with $w = 6$ μm spacing for the extraction of the thermal time constant $\tau_{thermal} = 1.8\mu s$.

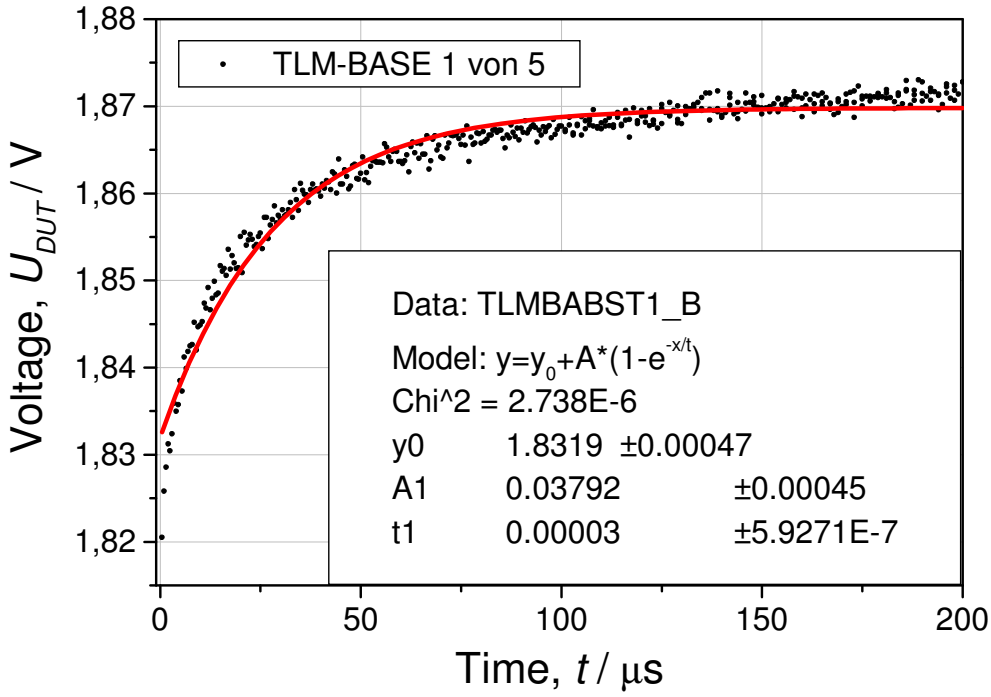


Figure 6.2: Measured on-wafer pulse voltage response of a TLM-base structure with $w = 60\,\mu m$ spacing for the extraction of the thermal time constant $\tau_{thermal} = 2.7\,\mu s$.

6.1.2 TLM pulsed step-stress test

At first, TLM-structures are investigated representing the base-, the collector- and the emitter-layer of HBT. The pulse response of a TLM-structure is shown in figure 6.3. A strong drift in the voltage response is measured for an open circuit pulse amplitude of $U_p = 38\ V$, which reflects a beginning instability in large-signal sample characteristics. When the pulse amplitude is increased to $U_p = 40\ V$, reversible sample breakdown can be extracted either from the voltage or from the current response. The voltage response in Figure 6.3 shows a sudden transient increase during the square pulse for this level because of current saturation.

Therefore, the sample current decreases at the same time point. For a further increase of the pulse amplitude to $U_p = 46\ V$, a higher instability is found, which leads to a non-reversible degradation of the sample. Only a slight increase in the sample resistance (+10%) is found for the maximum pulse amplitude of $U_p = 51\ V$ as is shown in figure 6.4. For an amplitude of $U_p = 46\ V$ (which already causes the strong distortion in pulse response visible in Figure 6.3), the variation is still within the measurement-error tolerance range. For a pulse amplitude of $U_p = 40\ V$ on the other hand, no visible degradation is found in the IV-characteristics although the voltage response measurement already reflects a clear instability for this voltage level. Similar response measurements have been conducted for TLM with a contact spacing of $w = 6 \ldots 60\ \mu m$ for base, emitter and collector layers.

Concluding, the pulse response already indicates initial degradation, which is not detectable using IV-measurements. With this approach, additional information on degradation behavior is extracted for TLM-structures. In the case of TLM-structures, no electrical ageing experiments using consecutive pulses are performed, as the threshold current density was already extracted.

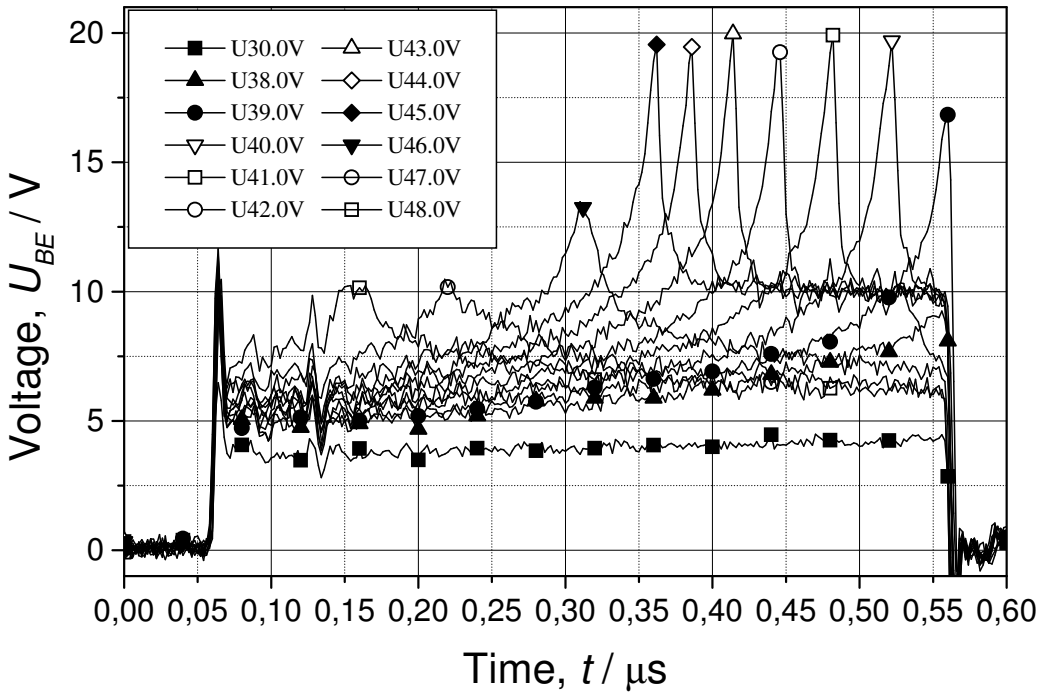


Figure 6.3: On-wafer pulse voltage response measurement for a collector TLM structure with $w = 6\,mm$ for different open circuit pulse voltages.

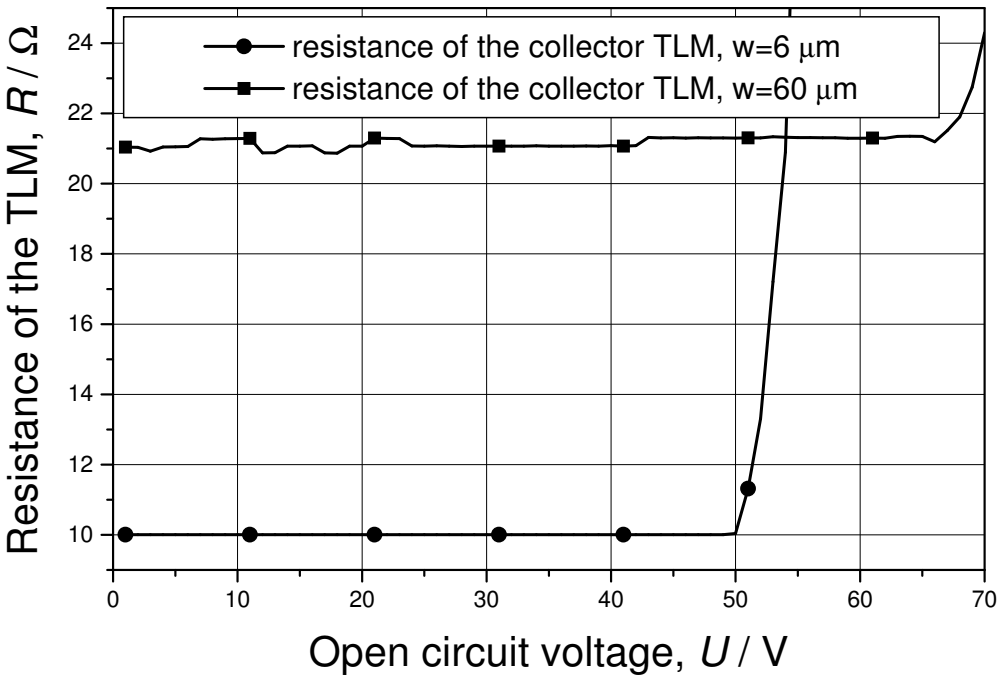


Figure 6.4: Resistance degradation of collector TLM structures with $w = 6\mu m$ and $w = 60\ \mu m$ over the applied pulse voltage.

6.1.3 TLM defect mechanisms

The relevant defect mechanisms for TLM-structures are field-related mechanisms including electro-migration and lateral material transport mechanisms [109],cf section 2.2. Such a material transport is shown in figure 6.5 for a collector TLM structure, which was stressed by a sequence of electrical pulses until the first degradation was detected in the IV-measurements. One can clearly identify metal spikes, which penetrate the semiconductor material. The corresponding electrical measurements are shown in section 6.1.2.

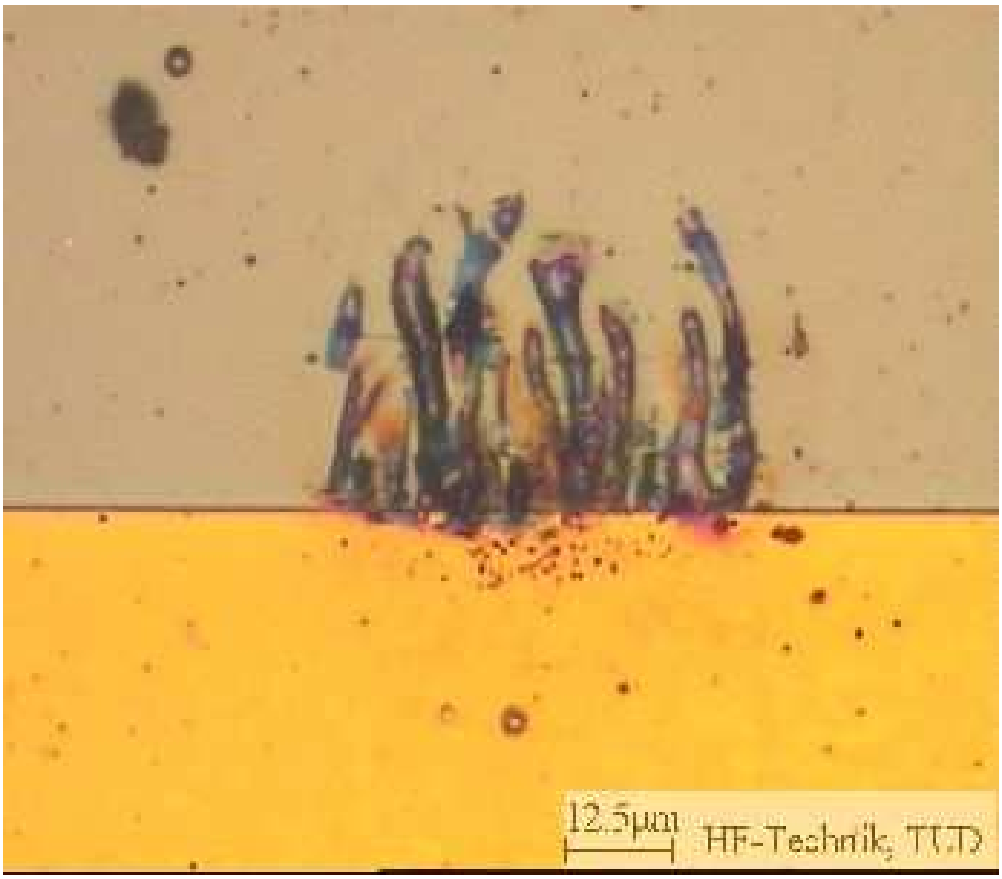


Figure 6.5: Optical photography of a degraded collector TLM structure ($w = 60\ \mu m$) stressed by pulses with increasing pulse amplitude due to electro-migration.

6.2 HBT TLP test approach

The base-emitter interface is the most critical part of the HBT in view of its reliability [39,76,110], refer to section 2.2.3. Additionally, the extrinsic base strongly influences HBT performance and reliability [43,111]. That is why the technology for processing of hetero-junctions is more complex than of the well established homo-junction. For this reason TLP stress is applied to the base-emitter diode of the device (in the following B-E stress). With B-E stress, BRANDT verified difficulties in separating the degradation of the hetero-interface from extrinsic base degradation when using the pulsed-step stress approach [14].

This work shows for the first time, that the separation of degradation mechanisms is possible with the TLP stress approach using consecutive pulses (see section 3.3.3), as it will be shown in the following sections. Figure 6.6 schematically shows the flow of electrons and possible degradation mechanisms using B-E stress. The metal migration leads to a degradation of the B-E interface and, depending on contact system and dominating degradation mechanism, to a degradation of the B-C interface, as well. Metal interdiffusion, dopant diffusion may lead to a modification of the intrinsic base and the B-E interface, while metal spiking or electro-migration can penetrate into the collector.

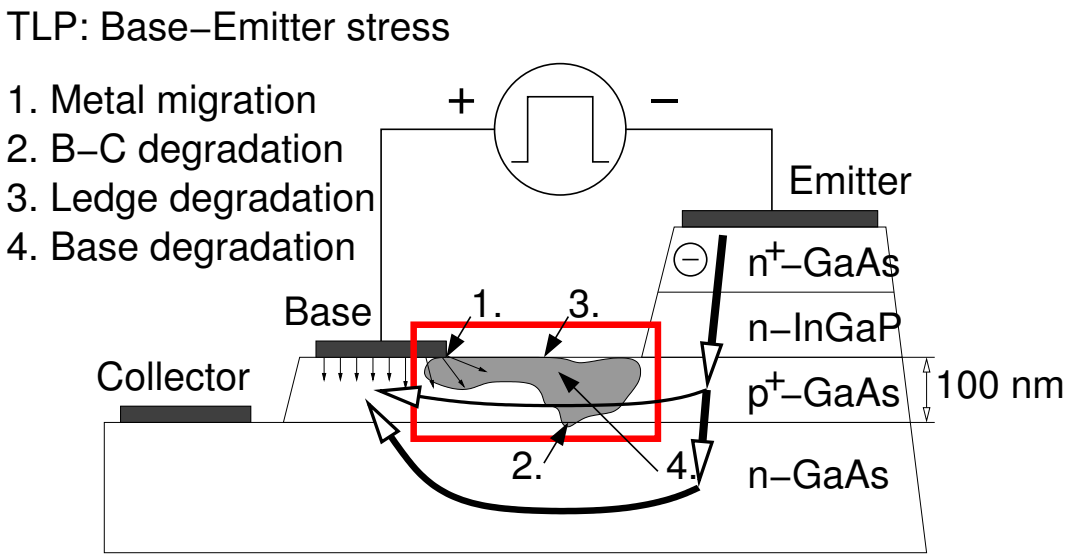


Figure 6.6: TLP-approach for excitation of degradation at the B-E interface, B-E stress.

Apart from that, the diffusion length of electrons is much longer than the base width that is about 100 nm. The value of the diffusion length of the minority carriers in the base layer is determined by equation 6.2.

$$L_N = \sqrt{D_N \cdot \tau_N} \approx 1.7\,\mu m \tag{6.2}$$

with

L_N = Diffusion length
τ_n = Electron lifetime
D_n = Diffusivity

The diffusion length is approximately 1.7 µm for a p-type GaAs with a doping density of $N_D = 10^{19}\ 1/cm3$, an electron lifetime of $\tau_n = 10-9\ s$ and a diffusivity of $D_n = 30\ cm^2/s$ [112]. According to this approach most of the electrons drift from the emitter through the base into the collector. Electrons are not extracted in the collector as it remains floating. The flow of electrons through the HBT under base-emitter stress is schematically shown in Figure 6.6.

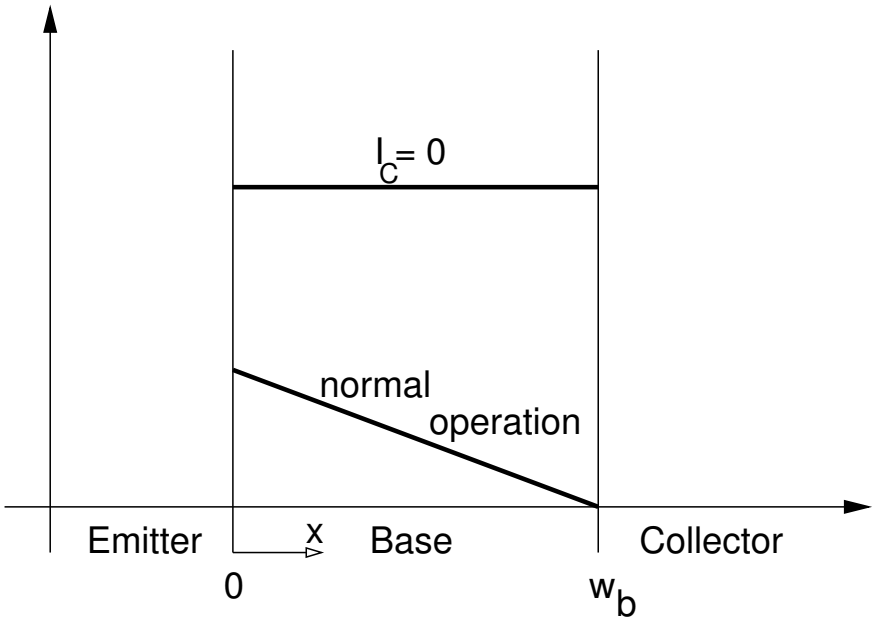


Figure 6.7: Minority charge carrier concentration in the base in conditions of normal operation and open collector.

Therefore, the number of charge carriers in the base rises above the level of normal operation as shown in figure 6.7. Thus the recombination in the base and the corresponding REDR effect is enforced. Electrons have only high energies while drifting from the emitter through the base into the collector during their movement through the device. So the electrons have these high energies while passing the most sensible parts of a HBT: the junctions, especially the hetero-junction. This stress is equivalent to the stress under normal operating conditions.

For reliability characterization, the electric field, the related current density and the resulting temperature are measured/calculated with respect to the device structure. The characteristics of the device are measured after each stress cycle and, thus, the history of degradation can be monitored as a function of the open source voltage or the number of pulses with a fixed stress level, cf. section 3.3. With pulsed-step stress test, the threshold stress level for a specific device is determined, when the first change in the device characteristic is observed. This procedure continues automatically until the device has been fully destroyed. The degradation level is extracted during the measurement using the diode-characteristics of the base emitter and the base collector diode [113],

as well as the Gummel- or output characteristics. Typical characteristics of a degraded HBT are shown in the following sections and in section 6.3.

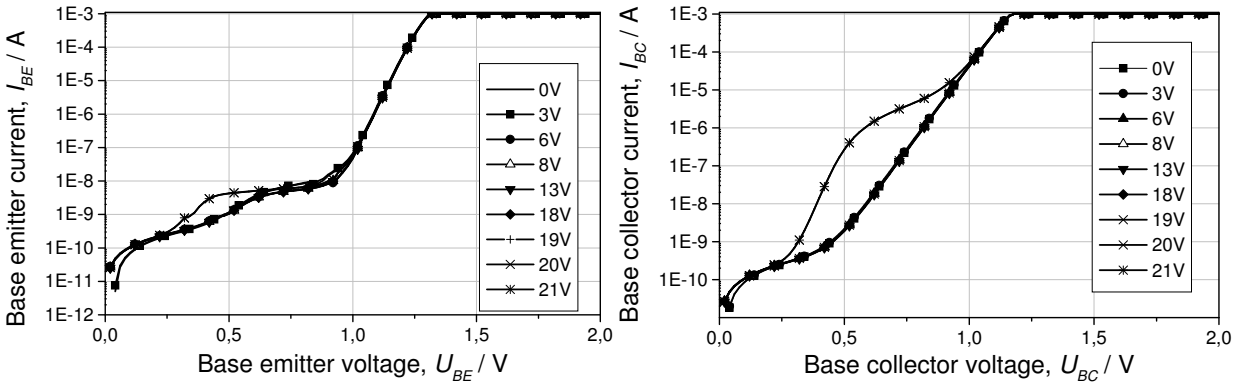
The main parameters for the analysis of semiconductor devices with this method are the pulse amplitude, duty cycle, the pulse length and the number of pulses as introduced in chapter 3. First, the degradation threshold for a device has to be determined. For this reason only one pulse for every voltage step and a stepwise increased amplitude is applied to the device. The pulse length $t_p = 50\ ns$ is chosen for non-thermal stress [68]..

The investigated test samples were obtained from THOMSON-LCR in February 2000. These include RF-HBT designs EPI 3302 (devices with thermal drain based on EPI-wafer material) and RMS 1146 (devices with thermal drain based on THOMSON-wafer material). Another set of RF-HBT was obtained from THOMSON in June 2000 (EPI 3301, wafer identical to EPI 3302). Firstly, the focus is set on the thermal characterization of the devices and the extraction of the devices critical current densities, which are the first important steps in characterizing a device with the TLP-method. In the following, the main focus is on the characterization of the B-E interface as it is reported to be the more critical interface.

Initial comparative tests with these devices resulted in the choice of B-E stress for accelerated degradation. The influence of B-E stress on the B-E interface as well as on the B-C interface is analyzed and described in the following sections. As far as available, transistors with the RF-design from the EPI 3302 wafer and from the RMS 1146 wafer are compared in the following sections. The observed degradation behavior of the compared devices differed as it is described below.

6.2.1 Stress of the B-E interface

Comparable investigations of RMS 1146 and EPI 3302 devices using the pulsed-step stress approach give the following results. The critical current density of the EPI 3302 for B-E stress with $t_p = 50\ ns$ is $I_{crit} \approx 0.23A$ ($\sim J_{crit} = 290\ kA/cm^2$).



(a) *B-E diode characteristics*

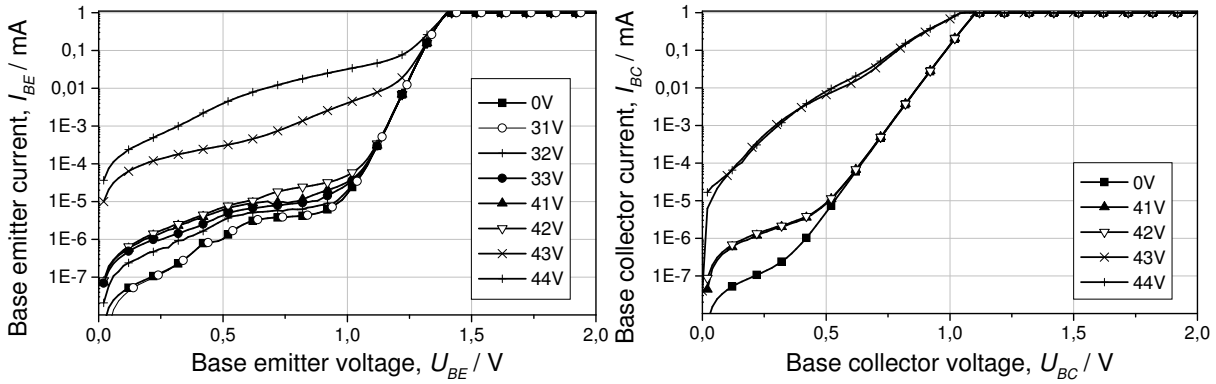
(b) *B-C diode characteristics.*

Figure 6.8: Degradation of the B-E and the B-C interface (forward) of a EPI 3302, B-E-stress ($t_p = 50\ ns$) for different current densities.

Figure 6.8 a) shows the modification of the B-E characteristics. Though the B-E-interface is stressed, the B-C interface in figure 6.8 b) shows a more significant degradation than the B-E interface. One can describe the characteristic of the degraded B-C interface as the formation of a

parasitic diode formed after migration of the base contact metal at the edge of the emitter mesa into the collector as it is described later on. The characteristic of the degraded B-E interface shows only a slight increase of the leakage current, which leads to the assumption that the hetero-interface is sufficiently stable for the EPI 3302.

On the other side, the critical current density of the Thomson RMS 1146 for B-E stress with $t_p = 50\ ns$ is $I_{crit} \approx 0.45\ A\ (\sim 560\ kA/cm^2)$. This critical current density is higher compared to the one of the EPI 3302 and indicates a higher contact stability. A direct comparison of degradation mechanisms is not possible because the B-C junction, cf. figure 6.9 b) does not degrade before the B-E junction as it was the case for the EPI 3302. In figure 6.9 a), the degradation characteristic of the B-E interface shows an overall increase of the leakage current. One can explain this behavior by an increase of the recombination current and a therefore increased defect rate in the hetero-interface.



(a) *B-E diode characteristics*

(b) *B-C diode characteristics.*

Figure 6.9: Degradation of the B-C interface (forward) of a RMS 1146, B-E-stress ($t_p = 50\ ns$) for different current densities.

The differences between the investigated devices are the different wafer material and base metal contact systems. In the case of the LCR 1146 HBT a non-alloyed Ti/Pt/Au system is used while the Ti/Pt/Au system on the EPI 3302 is alloyed. The device processing is identical. Concluding, this approach allows evaluation of the contact stability though the excited degradation mechanisms are not representative for normal operating conditions. One can see from these tests, that a separation of degradation mechanisms is not possible with the pulsed-step stress approach. With this knowledge, further devices are tested with consecutive pulses at a stress level well below the one, for which coarse degradation is detected.

The experimental results for the EPI 3301 leads to an empirical degradation description. The stressed hetero-interface is described by two diodes, which is the existing diode and a "parasitic diode" with high series resistance and low built-in potential in parallel as it is shown in Figure 6.10. This parasitic diode is formed by migration of the base metal contact into the collector and therefore changing the characteristic of the B-C interface. This metal migration effect mainly is based on the high electric fields applied to the device. It is concluded that this effect is not very relevant for HBT under normal operating conditions but gives information on the quality of the base contact and the influence of the ledge structure (extrinsic base) which is relevant for reliability improvement. As a result, the critical current densities should not be exceeded which have been extracted for the different transistors because otherwise relevant defect mechanisms are masqueraded.

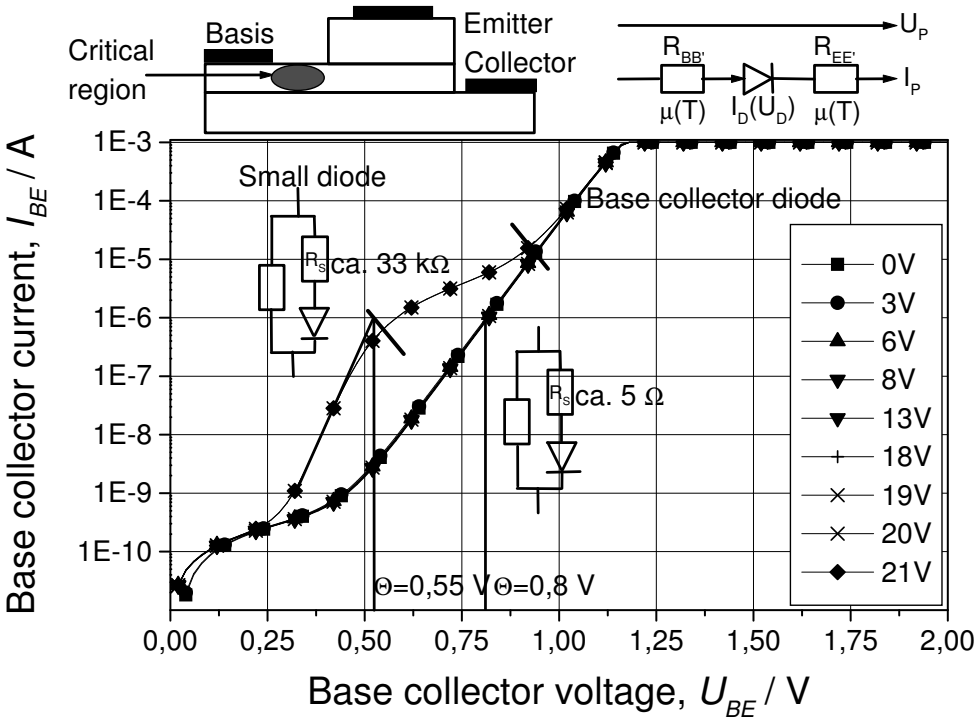


Figure 6.10: Formation of a parasitic Schottky diode.

Another defect mechanism is indicated by the overall increase of the leakage currents in the case of the RMS 1146. This increase is caused by the generation of recombination centers at the interfaces, especially at the B-E interface The device degrades due to recombination center generation in the base as a result of the high current densities in combination with an increased recombination ratio. Some of the recombination at these centers releases energy directly to the defect. Such localized energy is most likely to cause additional defects. This effect is reported to be "Recombination Enhanced Defect Reaction" (REDR) and is shown schematically in figure 6.11.

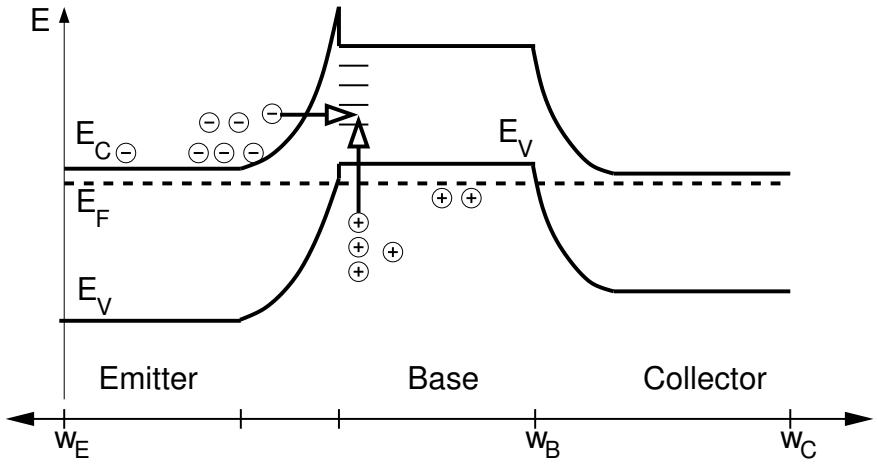
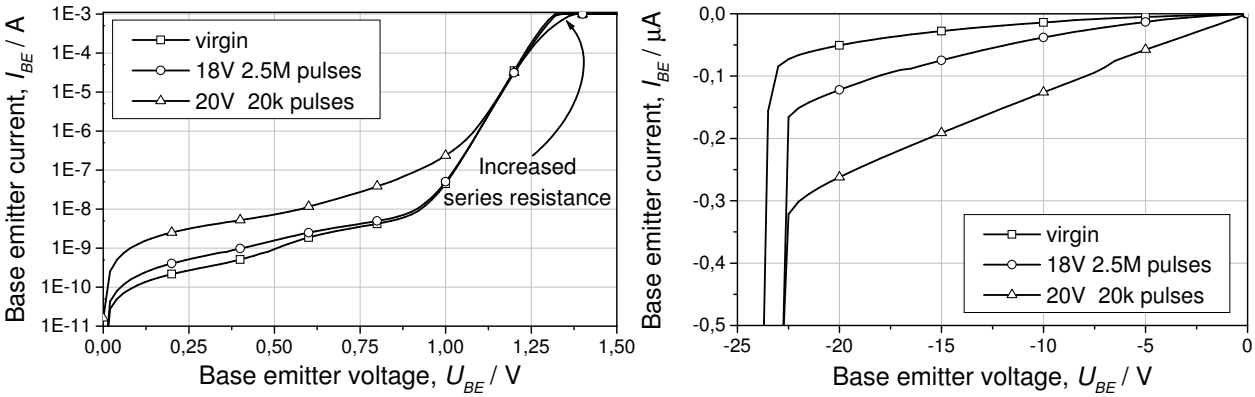


Figure 6.11: Recombination enhance defect reaction (REDR).

Further on the ”burn-in” effect is observed in several measurements. This initial increase in current gain is observed due to hydrogen compensation as it has been reported in conventional lifetime test for carbon-doped HBT. The third effect that was observed in some measurements was an annealing effect. A slight increase of the current gain is observed if the transistor was heated in connection with the I/V output measurements.

6.2.2 B-E stress with consecutive pulses

In the section before, different degradation mechanisms are excited using the pulsed-step stress approach. This section deals with the test approach using consecutive pulses for the separation of degradation mechanisms. The base metal migration should be avoided as this is not a relevant mechanism for the determination of device lifetime. In consequence, the open source voltage is chosen in a way, that the applied current density is smaller than the respective critical current density of the device and thus, other defect mechanisms can be detected. After the determination of the degradation threshold, the pulse amplitude is set to a value below this threshold to generate a certain current density. At the same time the pulse number for each run is increased in the range $N_p = [10^2..10^9]$. Characteristic values are extracted, such as the current gain of the HBT or the ideality factors of the diodes, and can be plotted versus the pulse number as degradation indicators.

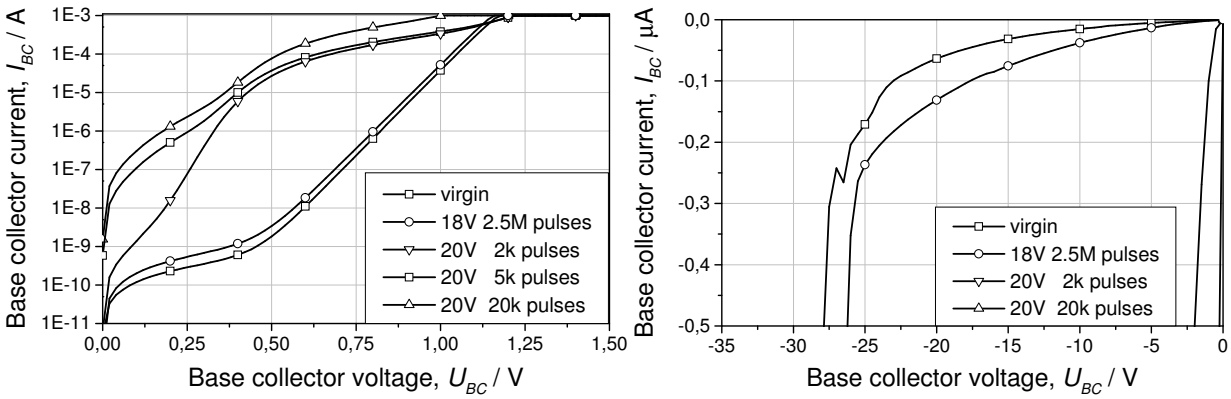


(a) *B-E diode forward characteristics.*

(b) *B-E diode reverse characteristics.*

Figure 6.12: Degradation of the B-E diode (EPI 3302) in dependence of the number of the applied pulses (B-E stress, $t_P = 50$ ns) and different open source voltages.

In figure 6.12, the I/V characteristic of the B-E interface is shown after $N_p = 2.5\,M$ pulses at U_p=18 V with B-E stress (t_p=50 ns). A slight overall increase of the leakage current and a decrease of the breakdown voltage of the device is observed after stress. The excitement of the degradation mechanisms is accelerated by increasing the current density to $J = 310\ kA/cm^2$. After $N_p = 20\,k$ pulses at $U_p = 20\,V$ with B-E stress a stronger overall increase of the B-E leakage current is detected. The respective characteristics for the B-C interface is described in figure 6.13. After 2.5M pulses at $U_p = 18\,V$ with B-E stress ($t_p = 50\ ns$) a slight increase in the leakage current and a decrease of the breakdown voltage is observed, which is similar to the behavior of the B-E interface. The increase of the open source voltage to $U_p = 20\,V$ leads to a significant change in the B-C characteristics. A first degradation is observed after $N_p = 2\,k$ pulses with $U_p = 20\,V$.

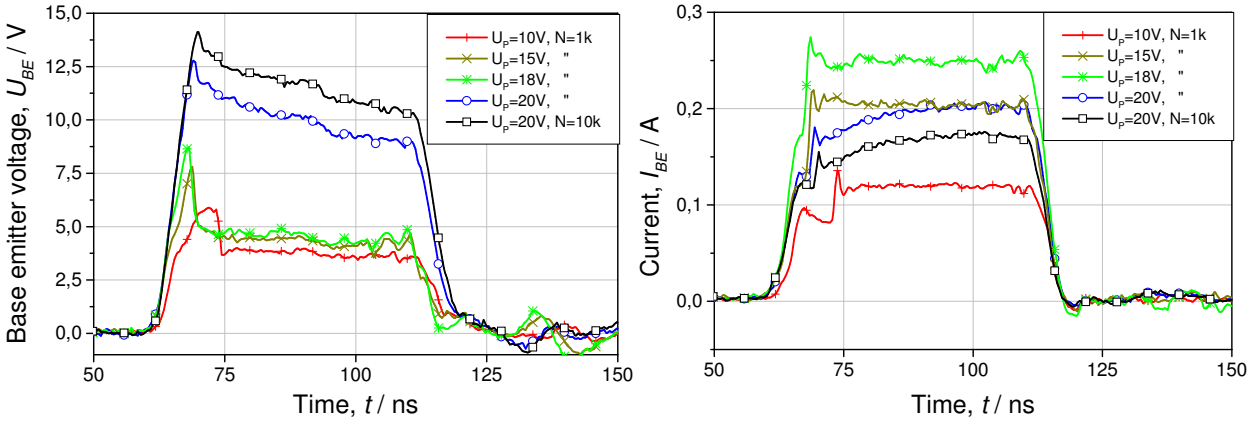


(a) *B-C diode forward characteristics.*

(b) *B-C diode reverse characteristics.*

Figure 6.13: Degradation of the B-C diode (EPI 3302) in dependence of the number of the applied pulses and different open source voltages (B-E stress, $t_P = 50$ ns) and different open source voltages.

The formation of a parasitic diode is observed after this stress, which is supposed to be caused by metal migration as mentioned before. A coarse B-C degradation is then observed after $N_p = 20\,k$ pulses at $U_p = 20\,V$ with B-E stress. This means that the maximum acceleration of certain degradation mechanisms is limited if the defect mechanisms under investigation are masqueraded by other non-relevant effects, as this is in this case the metal migration effect. With this result, the amplitude for the continuous test is optimized to generate more precise data. The duty cycle for the continuous test is lowered to 1/10000 to ensure that consecutive impulses cannot lead to a mean current that is increasing the device temperature. The impulse response is being analyzed in real time by measuring the voltage and current across the sample as shown in figure 6.14.



(a) *Voltage response*

(b) *Current response*

Figure 6.14: Comparison of the voltage and the current response of a $t_p = 50$ ns pulse applied to the BE-diode of a EPI3301 HBT before and after degradation (>105 Pulses).

6.3 Results for PCM- and RF HBT

The Process Control Monitor (PCM)-HBT are used as control devices for the verification of the material growth process. They have no air-bridge or thermal drain and are not suitable for RF application but provide identical DC characteristics compared to RF devices. This way, these devices are cheaper and suitable for reliability analysis, as they allow a direct observation of their surface after degradation.

The RF-HBT under investigation come from leading European industrial compound semiconductor manufacturers, such as Thomson and EPI. The advantage of these devices are their good RF properties compared to the PCM HBT and the good thermal capabilities using the air-bridge as a thermal drain. The disadvantage is that the air-bridge obscures the device surface, which does not allow visual inspection after degradation but requires more sophisticated and expensive analysis methods like TEM after FIB.

6.3.1 PCM HBT thermal time constants

The HBT thermal time constant is measured using the set-up described in section 3.3.1. From the voltage response in figure 6.15, the time constant is extracted to $\tau_{th} = 1.82\,\mu s$ following equation 6.3. The scattering in the measured pulse response originates from reflections and variations of the measurement setup (e.g. fluctuations of the used voltage source).

$$U = U_0 + A_1 \cdot e^{-\frac{(t-t_0)}{\tau^{th}}} \tag{6.3}$$

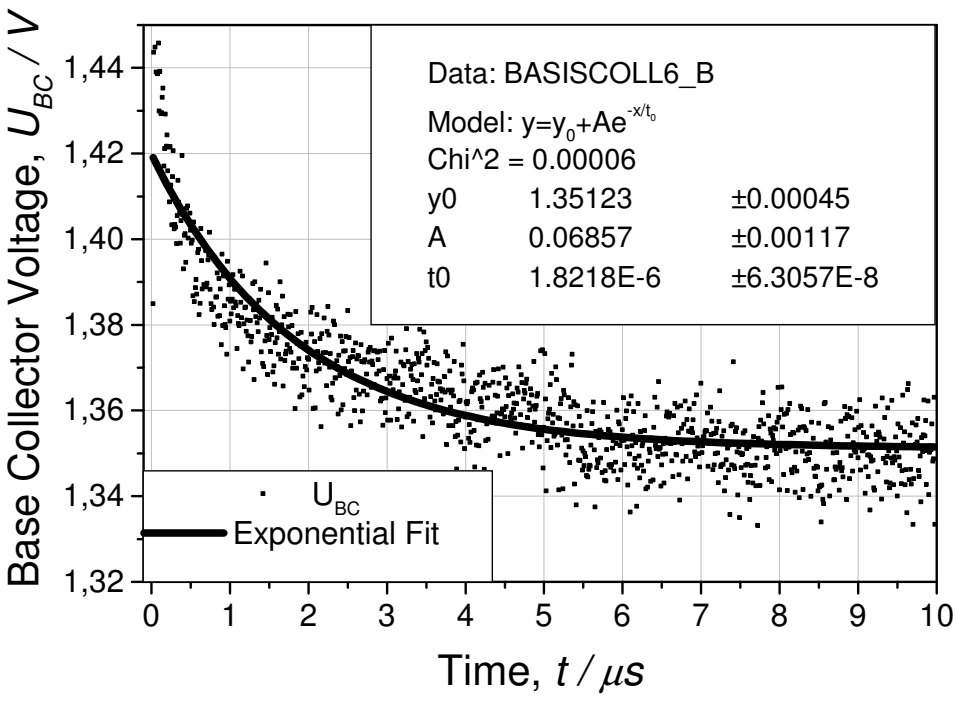


Figure 6.15: Measured B-C voltage response, U_{BC}, of a PCM-HBT under normal operation conditions.

6.3.2 RF HBT thermal time constants

First, the thermal time constant of a device is determined. In the following, the length of the applied pulses is chosen smaller than the determined time constant to avoid excitation of thermal effects, cf. chapter 3. With this approach, it is assured that the devices are exposed to non-thermal stress though very high current densities are used ($J_E \gg 100 kA/cm^2$). The thermal time constant of the investigated devices is determined to $\tau_{thermal} \approx 800 ns$. The minimum possible pulse length of $t_{p,min} = 10 ns$ allows to stay far below this time constant. This time constant is extracted by an analysis of the devices impulse response. Figure 6.16 shows the B-E voltage pulse response, U_{BE} of a HBT with the influence of electro-thermal coupling.

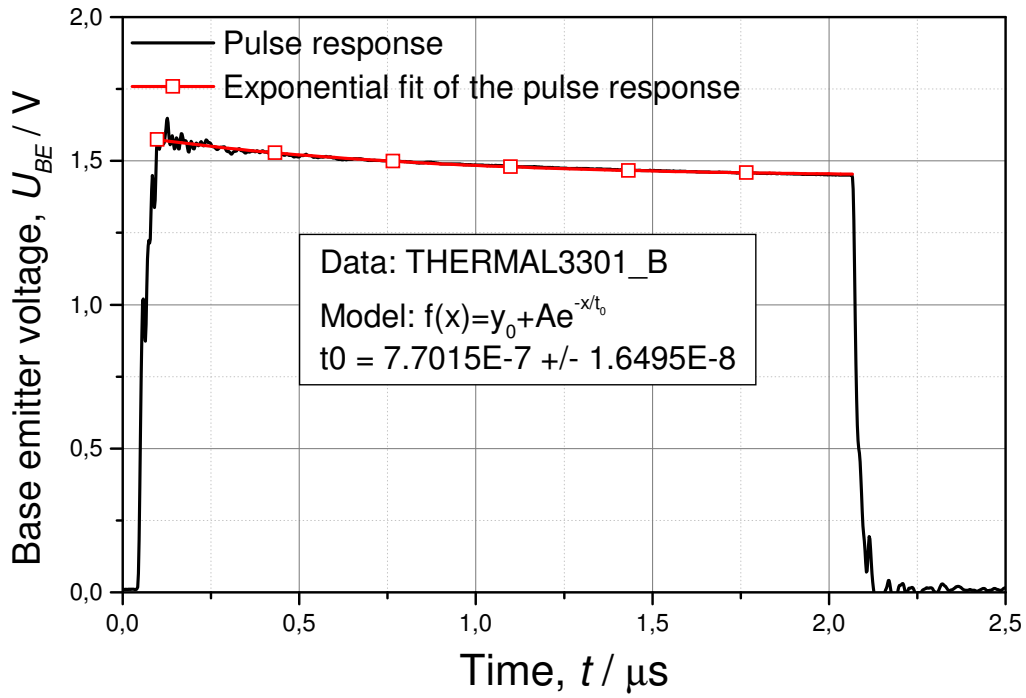


Figure 6.16: Measured voltage pulse response of a HBT under normal operating conditions.

6.3.3 RF-HBT pulsed step-stress test

Figure 6.17 shows the currents of the single diodes as a function of the stress voltage for extraction of degradation threshold. With increasing the base-emitter stress, a first degradation effect can be observed in figure 6.17 for a device-specific voltage. By further increase of the stress the degradation gradually increases total degradation of the device. As the current is fed into the base-emitter diode of the HBT, one would expect only this junction to degrade by the stress. Measurements show that some devices change even the base-collector diode characteristic first as seen comparing figure 6.18 a) and figure 6.18 b).

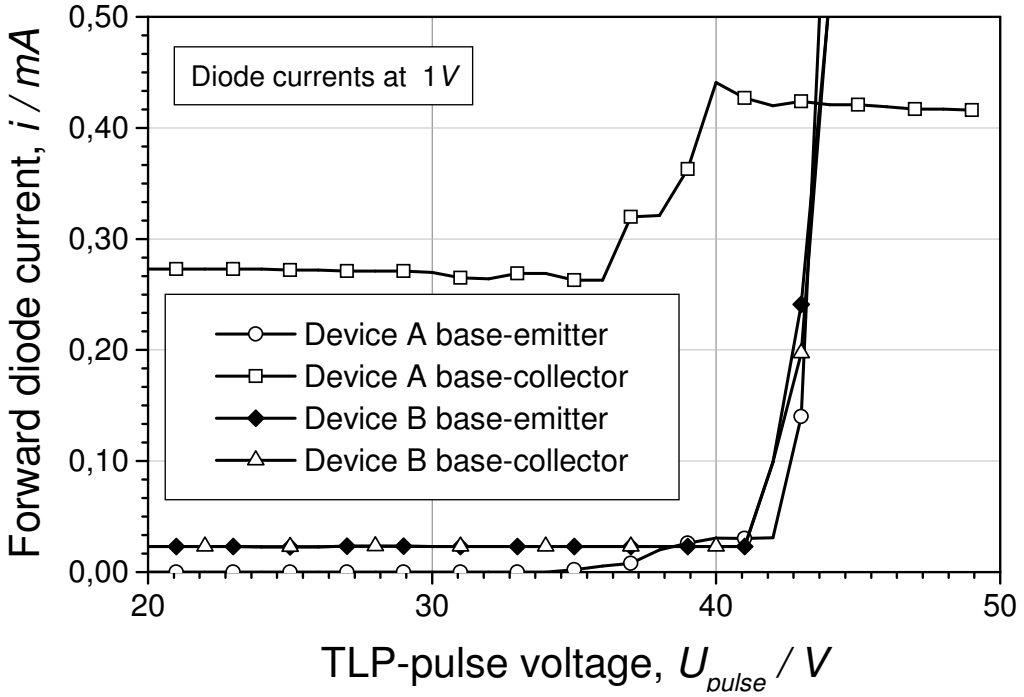
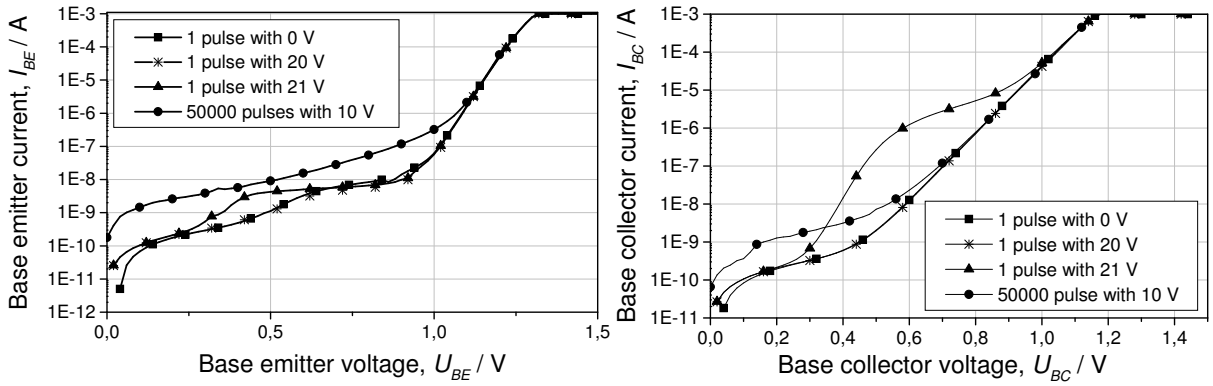


Figure 6.17: Base-emitter and base-collector current evolution under pulsed-step stress test for different HBT.



(a) *B-E diode characteristics*

(b) *B-C diode characteristics.*

Figure 6.18: Degradation of the B-E and B-C interface (forward) of a EPI3302, B-E-stress ($t_p = 50\,ns$) for different current densities and pulse numbers.

6.3.4 Separation of defect mechanisms using the TLP-method

After the determination of the degradation threshold, the pulse amplitude is set to a value below this threshold to generate a certain current density ($J = 100\,kA/cm^2 \ldots 400\,kA/cm^2$). The pulse number for each run is increased to $N_p = [10^2 \ldots 10^{10}]$ at the same time. Characteristic values are extracted, such as the current gain of the HBT or the ideality factors of the diodes and are plotted versus the pulse number. In the following, different single-finger HBT are investigated with an

emitter area of $A_{Emitter} = 50\,\mu m^2 \ldots 90\,\mu m^2$. Figure 6.19 shows the normalized current gain of two different devices with different stress current densities.

For device "B", two degradation effects take effect: The first effect occurs early during the measurement and decreases the gain rapidly but can only be seen at low base currents ($I_{BE} < 10\,mA$) because the B-E diode exhibits a high leakage current in this range as it is shown in Figure 6.18 ($N_p = 50000$ pulses with $U_p = 10\,V$). This effect is not representative for normal operation conditions, but it is a sensible diagnostic tool for the detection of defects in the interfaces. The decrease of current gain indicates leakage currents caused by recombination centers in the base-emitter junction. After this first breakdown of the gain, the device is stable over a high number of pulses and shows even an increase in gain as known for the burn-in effect due to hydrogen compensation. After a number of pulses - characteristic for a device - a slow degradation of the gain can be observed that leads finally to a total failure.

Device "A" withstands the stress without any indication of leakage currents. The only effect observable is a strong increase in current gain due to hydrogen compensation [39] as it has been reported in conventional lifetime test for carbon-doped HBT [48]. Comparing the curves for the different devices in Figure 6.17, it is evident that device "A" is less sensitive to current induced degradation mechanisms than device "B".

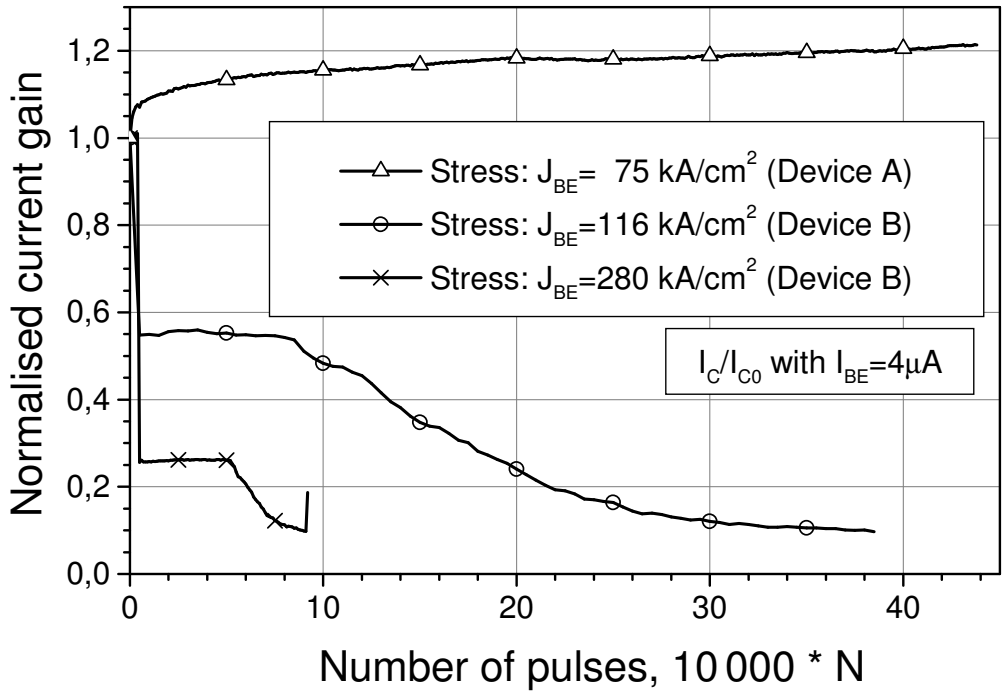


Figure 6.19: Normalized current gain over the number of applied pulses for different HBT.

It is assumed that for both diodes only one defect mechanism is responsible. This is the so called Recombination Enhanced Defect Reaction (REDR) mechanism which is explained in [39]. The device degrades due to recombination center generation in the base as a result of the high current densities. Some of the recombination at these centers releases energy directly to the defect. Such localized energy is most likely to cause additional defects. The base collector junction may also change its behavior when reached by such a defect domain. Relevant defect mechanisms and the influence of leakage currents on reliability issues are also discussed in [50, 76, 108].

6.3.5 Comparison of conventional lifetime tests and TLP-method

In the following, results for THALES-LCR single-finger InGaP HBT with an emitter area $A_{emitter} = 2 \cdot 30\,\mu m^2$ on IQE PLC Wafer materials are presented:

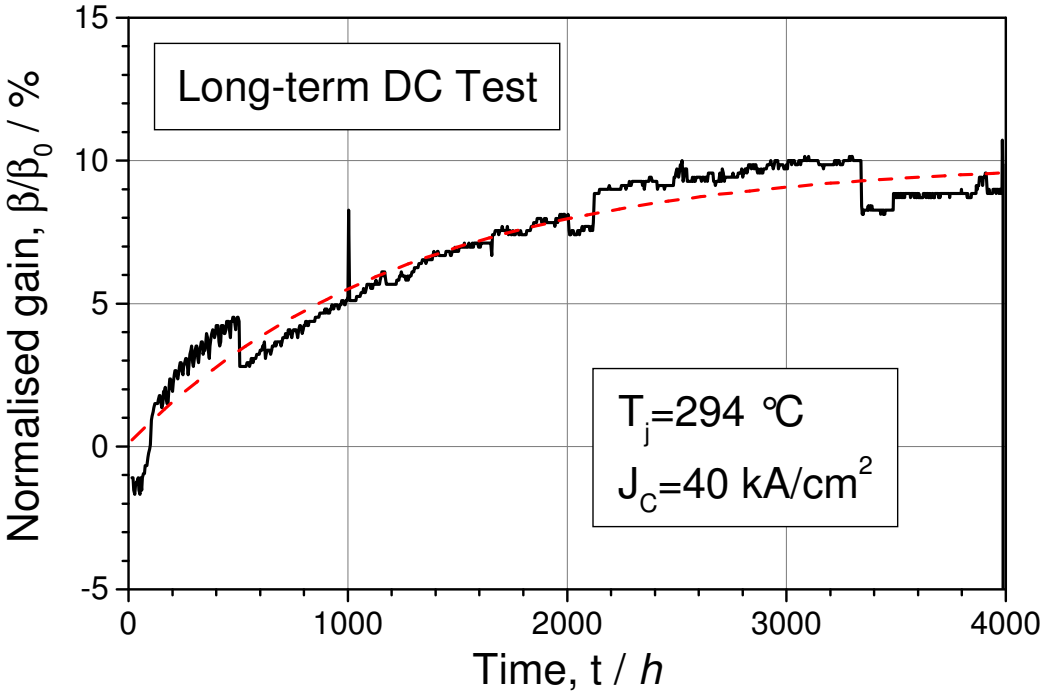


Figure 6.20: Development of the normalised gain using temperature stress ($T = 294\,°C$) and an elevated DC-level ($J_C = 40\,kA/cm^2$) and exponential fit.

Figure 6.20 shows the evolution of the current gain of a HBT under elevated temperature conditions and additional DC-stress. A 10%-increase can be observed, which is caused by the so called hydrogen effect [46]. The hydrogen effect is reported to be responsible for a reduction of recombination centers in the base and consequently leads to a fast increase of the current gain when bias is applied (burn-in effect). The rise of the current gain during this phase can be approximated by an exponential function. Under further bias stress the carbon acceptor de-passivation leads to a higher effective base doping and consequently to a decrease of the current gain. Comparable results with HBT and DC Base-Emitter stress are shown in [33]. Results from conventional reliability tests and from the TLP-method are presented in the following for InGaP/GaAs HBT. These devices have been tested for more than 6000 hours under a junction temperature $T_j = 296\,°C$ at a current density $J_E = 40\,kA/cm^2$ without failure applying conventional Arrhenius like methods.

Figure 6.21 shows the development of the current gain of a HBT from the same technology under pulsed stress. Under these conditions an increase of the current gain by 4% is observed. A correlation between both measurement-results is shown comparing 6.20 and 6.21. Therefore, a relation between the number of pulses and conventional testing time is assumed as the observed effect is reported to be caused by the current driven hydrogen diffusion mechanisms [33]. Differences between both measurement results can be explained by technological variations during the fabrication process as the investigated devices are not originated from the same wafer.

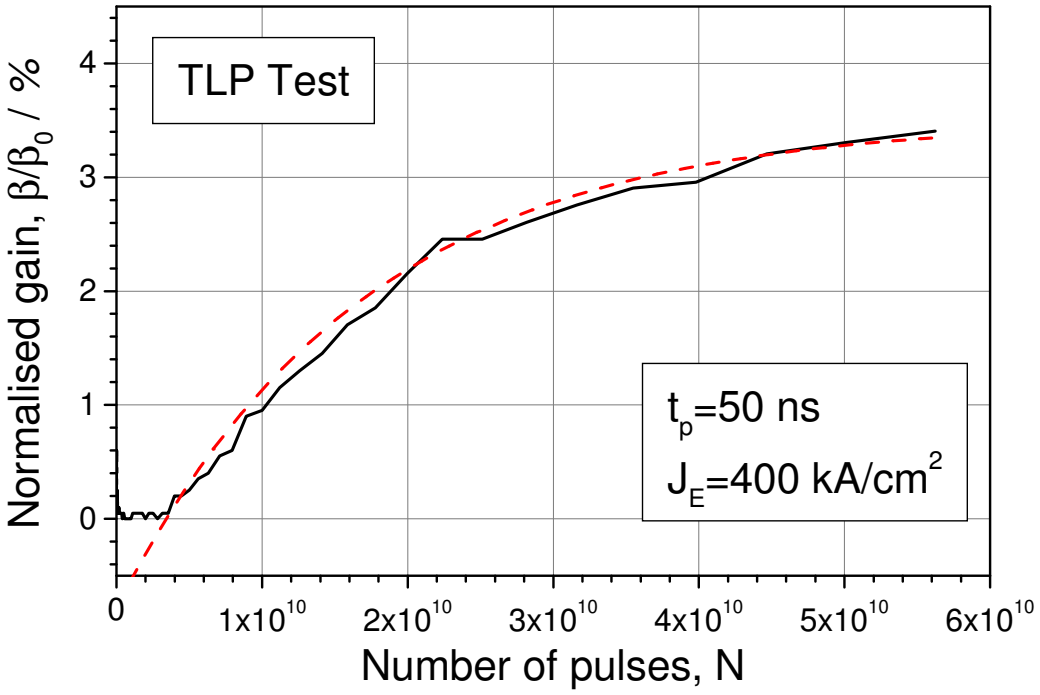


Figure 6.21: Development of the normalised gain using pulsed stress ($t_p = 50\,ns$, $J \gg 400\,kA/cm^2$) and exponential fit.

6.3.6 PCM- and RF HBT degradation and failure mechanisms

The B-E-interface was found to be the most critical part [39] because a degradation is observed for smaller voltages. A first degradation effect can be observed for a device-specific voltage at the B-E-interface increasing the base-emitter stress. An additional degradation is detected at the B-C-interface by further increase of the stress. The degradation of the interfaces is gradually increased with increasing stress until the breakdown of the device is detected. As the current is fed into the base-emitter diode of the HBT, one would expect only this junction to degrade by the stress. Measurements show instead that the B-C diode characteristic of the devices changed, too. It is assumed that only one defect mechanism is responsible for the degradation of both diodes. This is called Recombination Enhanced Defect Reaction (REDR) mechanism, which is explained in [39]. The base leakage current is caused by recombination centers in the base. Some of the recombination at these centers releases energy directly to the lattice defect and most likely additional defects are generated. The base current increases as the number of charge carriers in the base rises above the level of normal operation. Thus, the recombination in the base and the corresponding REDR effect is enforced. It is proposed here that the defect mechanisms observed at interfaces are dependent on the material quality.

Figure 6.22 shows the degradation of a PCM HBT ($A_{Emitter} = 2\,\mu m X 30\,\mu m$) after B-E stress. One can determine initial metal migration and diffusion of the base metalization into the semiconductor material providing a B-E short. Further electrical stress would lead to catastrophic failure due to heat generation, as it is demonstrated in the following for a RF HBT ($A_{Emitter} = 2\,\mu m X 30\,\mu m$). Figure 6.23 shows a RF HBT of which the air-bridge is removed after B-E pulsed step stress test, which was not stopped after the first degradation is observed. After catastrophic failure due to a B-E short, the emitter finger is entirely molten, as one can recognize in the center

of this REM. On the top and bottom of the REM the contact area of the air-bridge is visible.

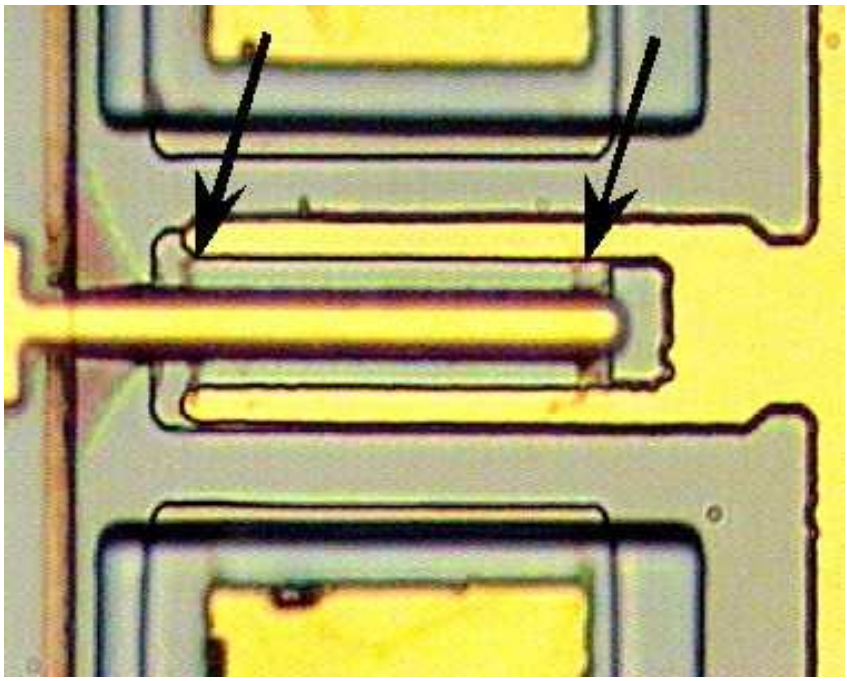


Figure 6.22: Optical image of a degraded PCM test HBT after B-E forward stress, pulse length $tp = 100$ ns, $I = 0.45$ A.

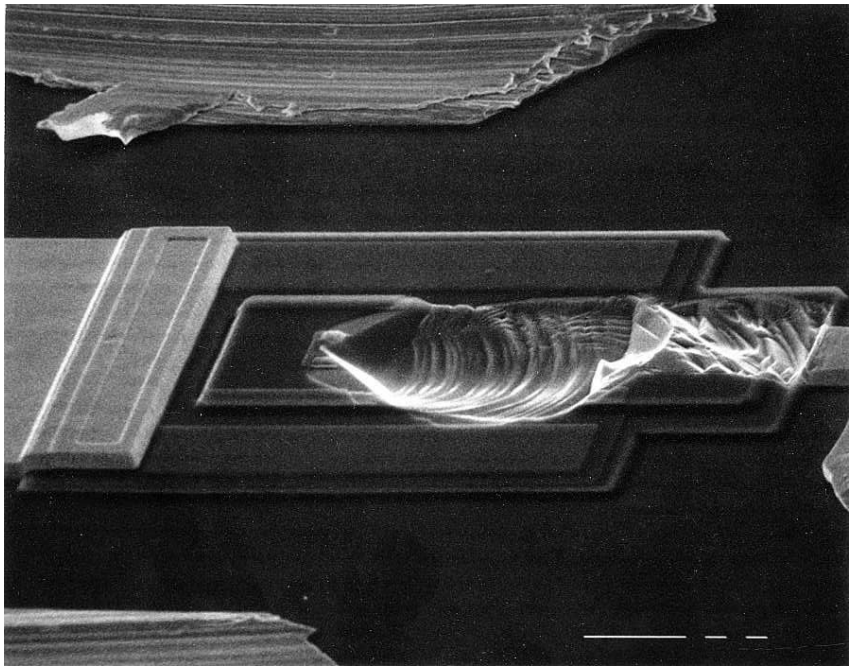


Figure 6.23: REM image of a degraded RF HBT after B-E forward pulsed step stress test, pulse length $tp = 50$ ns.

6.4 Simulation results for HBT

A numerical solver has been developed for the simulation of HBT devices at the UNIVERSITY OF TECHNOLOGY CHEMNITZ by KROZER and GANIS. The solver is based on the principles following [114] with additional modifications. This is a 2D-code with an appropriate interface condition for hetero-junctions and transient analysis capabilities.

6.4.1 Gummel-Plot

A comparison between simulated and measured Gummel plots is presented in figure 6.24. For voltages higher than $U_{BE} = 1\ V$ it shows a good agreement between measurement and simulation. The deviation in the lower voltage range is due to leakage currents with ohmic characteristic which are not taken into account in the simulation. Contact resistance is also not considered in the simulation, which leads to a small deviation under high current densities.

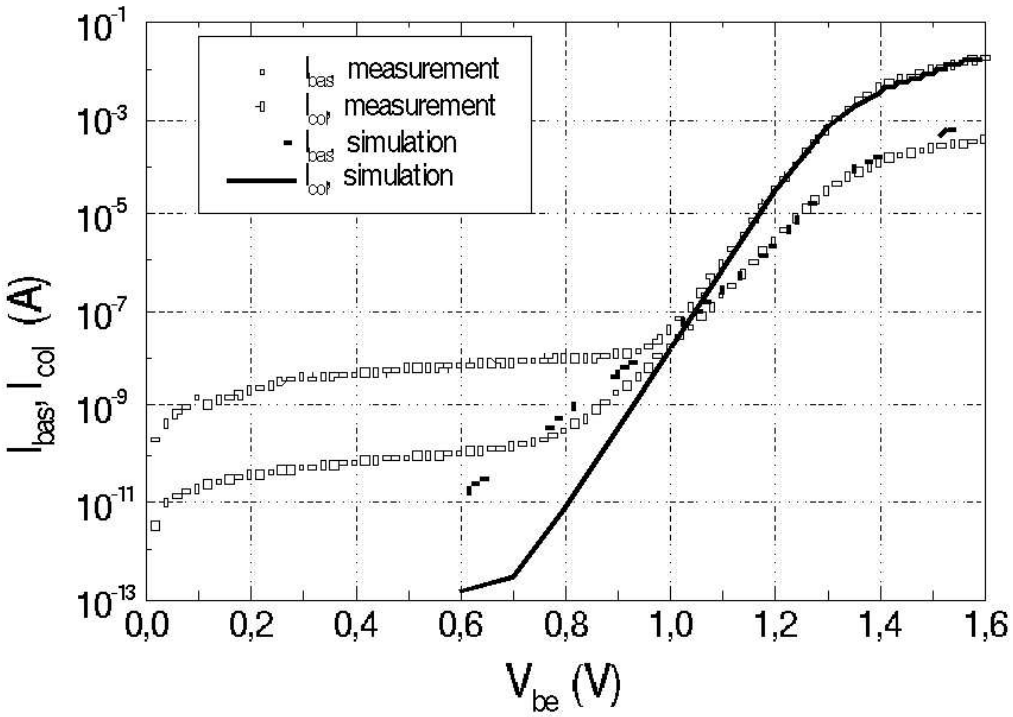


Figure 6.24: Simulated Gummel plots: For the simulation, the following carrier lifetimes are chosen: $\tau_{n,EMI} = \tau_{p,EMI} = 8.0 \cdot 10^{-13}\ s$ *and* $t_{n,BAS} = t_{p,BAS} = 1.0 \cdot 10^{-10}\ s$.

6.4.2 Variation of Carrier-Lifetime in Base and Collector

The contributions to the base current are:

- the current from recombination in the quasi neutral emitter ($I_{Rec,E}$) and base ($I_{Rec,B}$)
- the recombination current in the space-charge region ($I_{SCR,E}$), mainly in the emitter-side, since the very high base doping results in very thin space charge region in the base-side.
- the current from recombination at the surface of emitter side walls ($I_{Sfc,E}$) and at the surface of extrinsic base ($I_{Sfc,B}$)

The surface recombination is not taken into account in these simulations to ease the physical understanding. For lower base-emitter voltages U_{BE}, the space charge recombination in the emitter-side is the dominant contributor of base current, because of the large extent of the space charge region as shown in figure 6.25. Current stemming from space charge recombination has typically an ideality-factor of 2 [115].

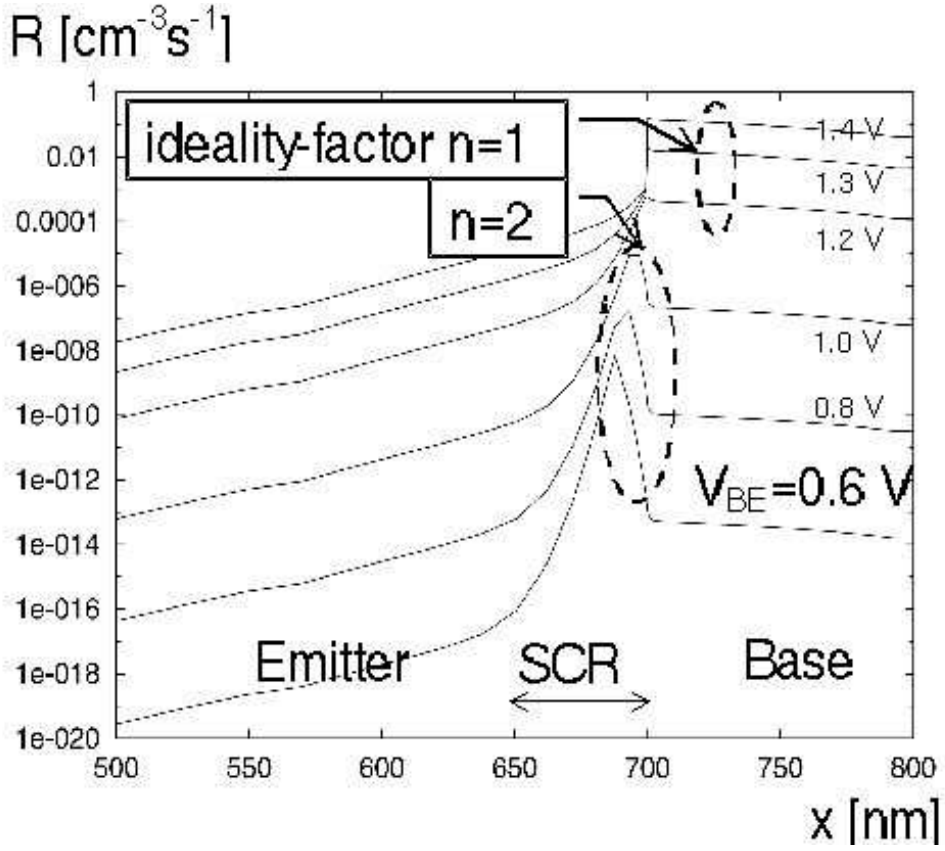


Figure 6.25: Recombination-rate in emitter and base at various base-emitter voltages U_{BE}

With the increase of the base-emitter voltage U_{BE}, the space charge region becomes narrower and the number of injected electrons into the base becomes larger. This leads to the increase of recombination in quasi-neutral base which is then the dominant part of base current. Recombination rate in the quasi-neutral base is proportional to collector current, hence the typical ideality-factor is 1.

The creation of defects can be expressed by a reduction of the carrier lifetime. Hence, the variation of the carrier lifetime indicates the amount of stress induced during the test. Figures 6.26

and 6.27 show simulation results for the impact of the variation of lifetime in emitter and base region.

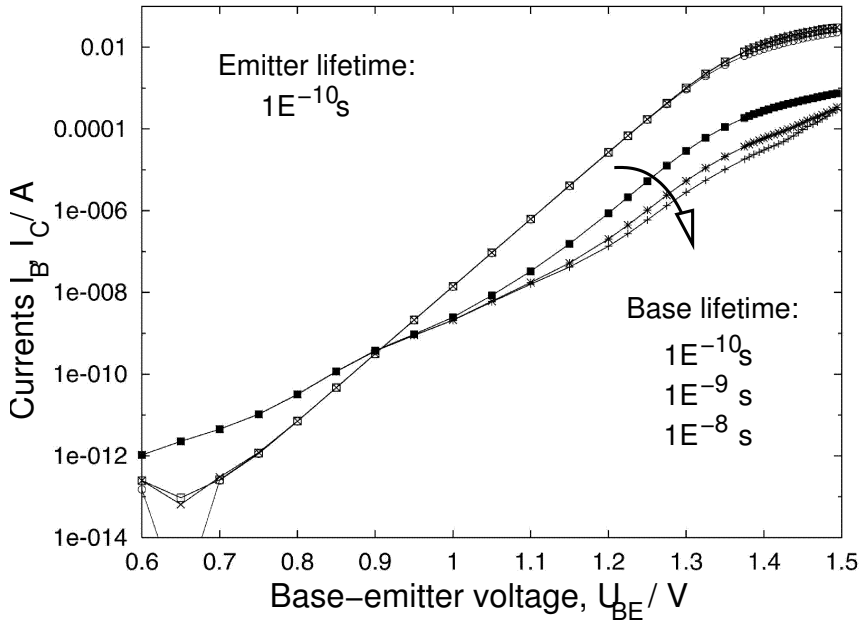


Figure 6.26: Base-lifetime variation on Gummel plot.

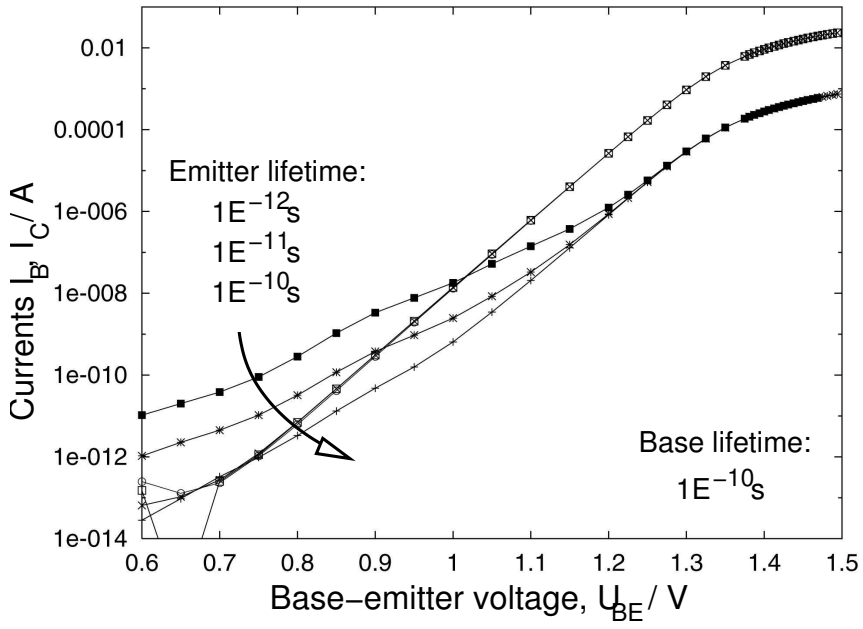


Figure 6.27: Emitter-lifetime variation on Gummel plot.

With these results, one can distinguish whether the stress has an impact on the base or emitter. It can be observed in figure 6.27 that the variation of the carrier lifetime in the emitter is responsible

for the increase of base current at low voltages. In this voltage range, the ideality factor is closer to 2. On the other hand, variation of the minority carrier lifetime in the base has a direct impact on the DC-current-gain at large base-emitter voltages. Here, the ideality factor is near to 1.

6.4.3 Current density distribution

Applying short pulses ($t_{pulse} \ll \tau_{thermal}$) to the device is equivalent to a current and voltage stress at the junction and at the volume of the device. Knowing the distribution of current density will enable to determine which region is more susceptible to electrical stress. The current density distribution from simulation shows a region with high current density peak around base-emitter-corner as it is shown in figure 6.28. A current density peak is observed at the base-emitter corner resulting from the device geometry and electrical conditions. Hence, the area near the base-emitter corner (especially the hetero-interface and emitter side-wall) is more endangered through current stress than other regions of the HBT device.

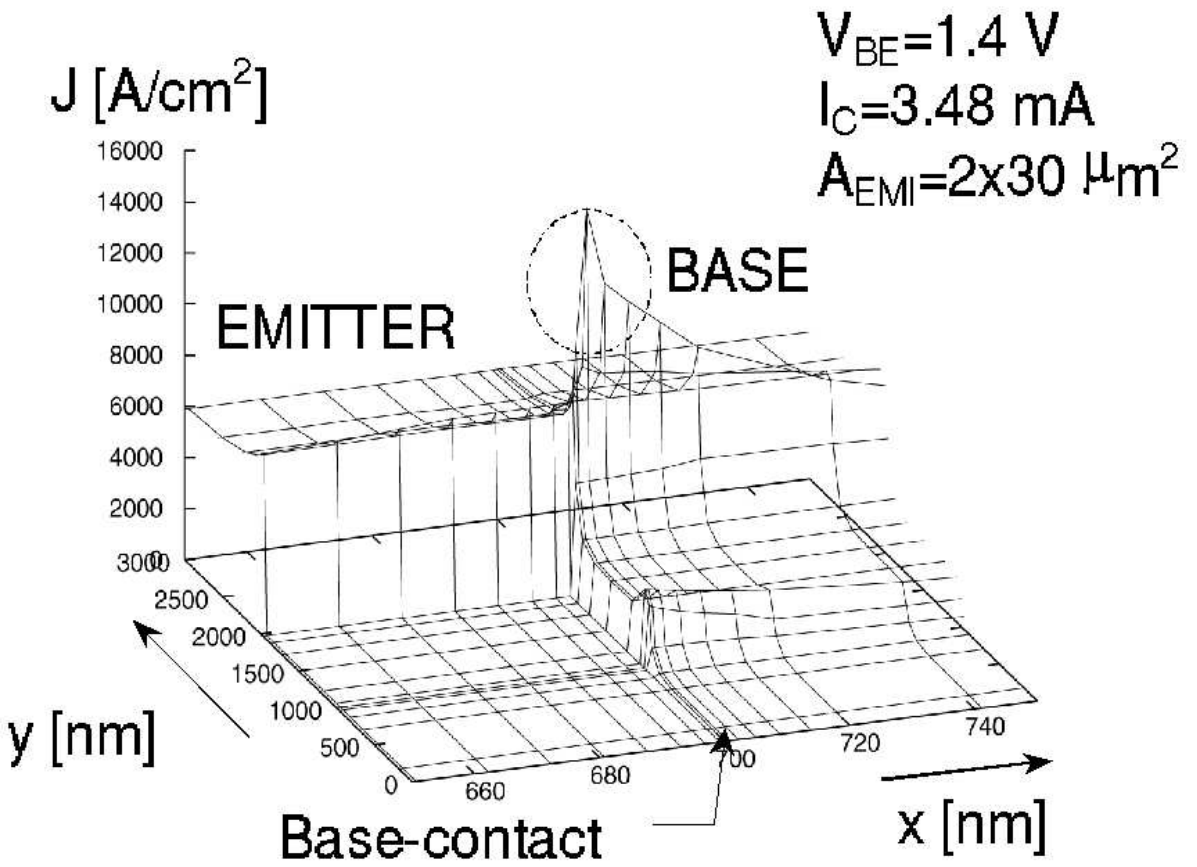


Figure 6.28: Simulated current density distribution

6.5 Results for Schottky diodes

Whisker-contacted and planar GaAs-based Schottky devices are key elements for signal detection, mixing and generation in the Terahertz (THz)-frequency range. The devices under test are the in-house fabricated planar and whisker-contacted mixer diodes as introduced in section 4.2. The first reliability tests and results for whisker-contacted diodes are shown in [55] considering ideality factor and noise temperature as a degradation indicator after accelerated stress tests with high current densities. BRANDT contributed the first TLP-investigations on whisker-contacted diodes [14, 116–118] using the pulsed-step stress test approach.

The introduction of a process optimization programme, cf. chapter 5 contributes to the detection of potential process weaknesses in and reliability improvement of the planar diode fabrication process. This leads to an understanding of the impact of basic technological process steps on device quality [55, 83] from the technological point of view with emphasis on the Schottky contact definition and formation [84, 85]. For the first time, statistically significant data is obtained for fabricated devices in the framework of a DFG[1]-project in collaboration with the LHFT, UNIVERSITÄT ERLANGEN. The automated extraction of IV-characteristics and noise temperature enables the characterization of hundreds of whisker-contacted diodes for the evaluation of impact of technological modifications and finally results in high-quality whisker-contacted and, after technology transfer, planar Schottky-devices shown in section 4.2.

The following sections show results from accelerated stress tests using the TLP-method,cf section 3.3, which already was shown to be a very fast feedback to the fabrication process of e.g. TLM-structures or HBT [16, 119], cf. section 6.1 and 6.3. Firstly, thermal time constants of whisker-contacted and planar mixer diodes are extracted, cf. section 6.5.2. The following sections will detail the importance of the thermal time constant for the TLP-testing of Schottky devices as indicated in section 3.2. Section 6.5.3 shows the degradation threshold for coarse degradation. Section 6.5.4 shows results from electrical ageing using repeated pulse, while section 6.5.5 identifies the influence of TLP-parameters and technology on device ageing characteristics. For the IHF Schottky diodes, the occurring degradation mechanisms are identified by IV-measurements and TEM after Focused Ion Beam (FIB) preparation, cf. section 6.5.6 [106].

6.5.1 Schottky diode TLP test approach

First approaches to TLP-testing of Schottky diodes are performed by Brandt [117, 118] comparable to the pulsed-step stress test. He did not use the advantage of the TLP-method, its flexibility. This work proposes for the first time the modification of different parameters - namely the pulse-duration, amplitude and number as well as the duty cycle - for the excitement of different degradation mechanisms, which are e.g. spontaneous ESD[2] damage, migration and diffusion induced defects or degradation mechanisms comparable to those under normal operating conditions. The test time to device failure can be reduced to 24 hours while exciting degradation characteristics comparable to the ones of conventional stress tests [119]. Using the TLP-methodology, technology optimization is accelerated, cf. chapter 5.

The following paragraph details the initiation of degradation mechanisms by applying the TLP-method and explains the required conditions for the proper use of this accelerated stress test. In general, devices are tested in forward mode. At first, the thermal time constant is determined to be $\tau_{th} = 1.4\,\mu s$ for anode diameters $d_a = 5\,\mu m$. For subsequent accelerated tests, the pulse duration

[1] DFG=Deutsche Forschungsgemeinschaft

[2] ESD=Electrostatic Discharge

$t_p = 50...500\,ns$ is kept significantly below τ_{th} for adiabatic operation, i.e. only heating of the interface, which is confirmed by electro-thermally coupled numerical simulation. The pulse amplitude is set to a level significantly lower than the one, for which coarse degradation of the device by field induced mechanisms is observed applying a pulsed-step stress test of single voltage pulses with increasing amplitude. This test approach shows a sharp threshold for the degradation by field induced mechanisms at a current density $J = 8.15 \cdot 10^5 \frac{A}{cm^2}$. The current density is set to $J = 4 \cdot 10^5 \frac{A}{cm^2}$ for further experiments. The ideality factor is observed to be the most sensitive parameter to device degradation.

6.5.2 Thermal time constants

The thermal time constant of Schottky diodes is extracted using the approach described in section 3.3.1. For Schottky diodes, one must distinguish between two operation modes:

- diode operation below flat-band voltage ($U_D < \Phi_{Bi}$),
- diode operation above flat-band voltage ($U_D > \Phi_{Bi}$).

Below flat-band voltage ($U_D < \Phi_{Bi}$), the diodes junction temperature increases during the pulse as the dominating thermal effects occur in the space charge region with high electrical resistance, R_j. This affects the diode saturation current, cf. equation 4.14, and results in a decrease of the diode voltage. In this case, the substrate is nearly unaffected due to the spreading resistance effect, cf. section 4.2.3. With increasing forward bias, $U_D > \Phi_{Bi}$, the depletion width is negligible (i.e. there is no depletion layer) and thermal heat is generated due to the epi-layer resistance, R_{epi} and the substrate resistance, R_{sub}, reducing majority carrier mobility.

In both cases, the resulting exponential decay of the voltage response, $U_D(t)$, fits to equation 6.4. The identification of diode parts contributing to the decay of the voltage response is unambiguous. Following figure 6.29, the thermal time constant of $d_a = 5\,\mu m$ whisker-contacted mixer diodes is extracted to $\tau_{th} = 1.4\,\mu s$.

The peripheral thermal time constant of a planar Schottky-mixer diode, $d = 1\,\mu m$, is extracted to $\tau_{th,p} = 7.8\,\mu s$. From the comparison with the thermal time constant of the whisker-contacted mixer diode, it is evident, that this is not the junction thermal time constant. Actually, the pulse response in figure 6.30 shows two distinguishable exponential slopes following equation 6.5. The intrinsic thermal time constant of $d_a = 5\,\mu m$ mixer diode is extracted by BRANDT to $\tau_{th,i} = 500\,ns$ [14], which is consistent with the time-constant $\tau_{th,i} = 100\,ns$ for the diodes with the new design in this work.

$$U = U_0 + A_1 \cdot e^{-\frac{(t-t_0)}{\tau^{th}}} \tag{6.4}$$

$$U = U_0 + A_1 \cdot e^{-\frac{(t-t_0)}{\tau^{th,1}}} + A_2 \cdot e^{-\frac{(t-t_0)}{\tau^{th,2}}} \tag{6.5}$$

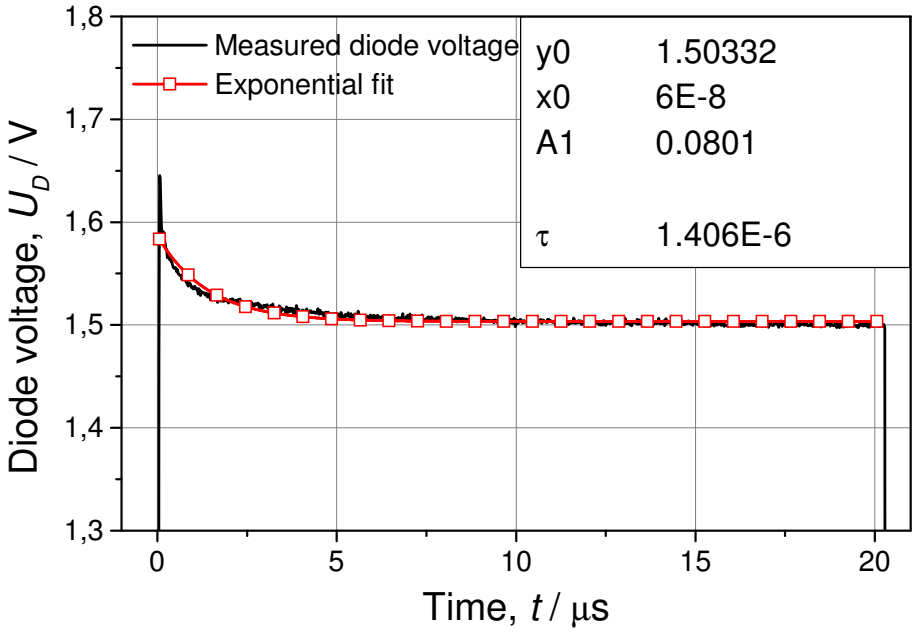


Figure 6.29: Thermal time constant for a whisker-contacted mixer diodes with $d = 5\ \mu m$.

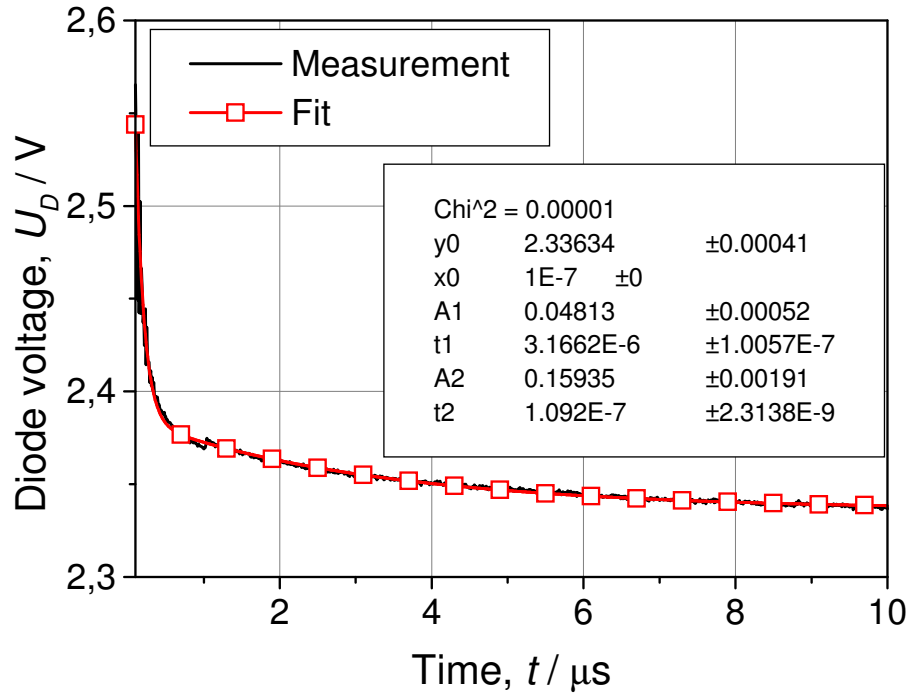


Figure 6.30: Two thermal time constant for planar mixer diodes with $d = 1\ \mu m$ for $U_D > U_{bi}$.

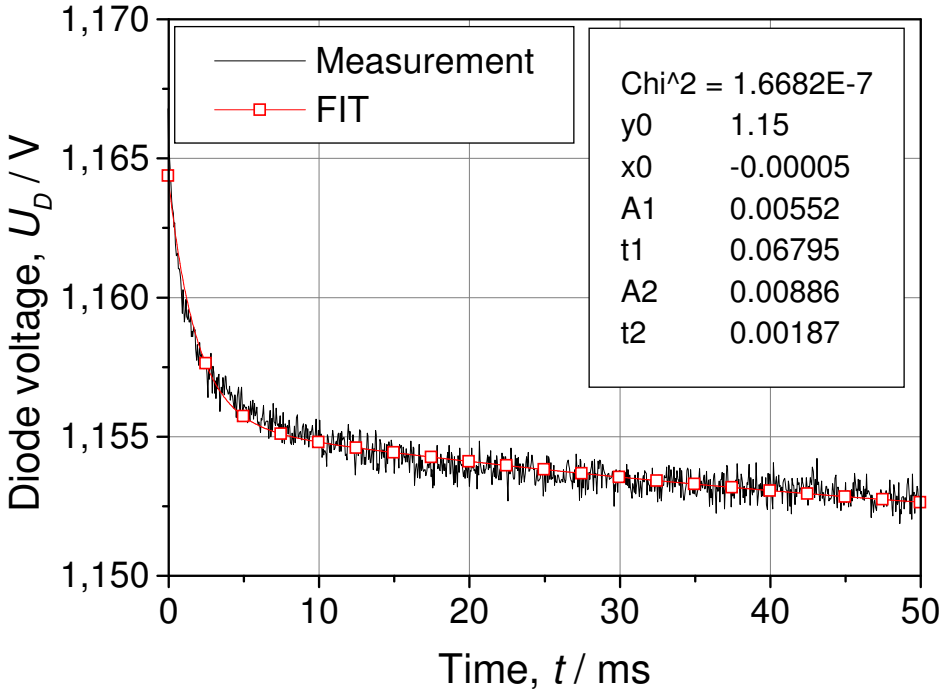


Figure 6.31: Two thermal time constant for planar mixer diodes with $d = 1\ \mu m$ for $U_D \approx U_{bi}$.

6.5.3 Pulsed step-stress test

This section shows the degradation threshold for current- and field induced effects extracted from pulsed-step stress tests, cf. section 3.3.2, with whisker-contacted process control diodes and planar THz Schottky mixer diodes.

The degradation threshold for whisker-contacted mixer diodes $d_a = 5\ \mu m$ is extracted to $U_{threshold} = 11.6\ V$, corresponding to a critical current density of $J_{crit} = 8.15 \cdot 10^5\ A/cm^2$. In the case of a mixer control diodes, $d = 1.2\ \mu m$, the threshold is determined to $U_{threshold} = 5.6\ V$, corresponding to a critical current density of $J_{crit} = 3 \cdot 10^5\ A/cm^2$. In the case of planar mixer-Schottky diodes, $d = 0.8\ \mu m$, the threshold voltage is determined to $U_{threshold} = 5.9\ V$, corresponding to a critical current density of $J_{crit} = 4 \cdot 10^5\ A/cm^2$. These results from the different diodes are in good agreement even though the degradation threshold is not identical due to the imperfect scaling of the pulse currents.

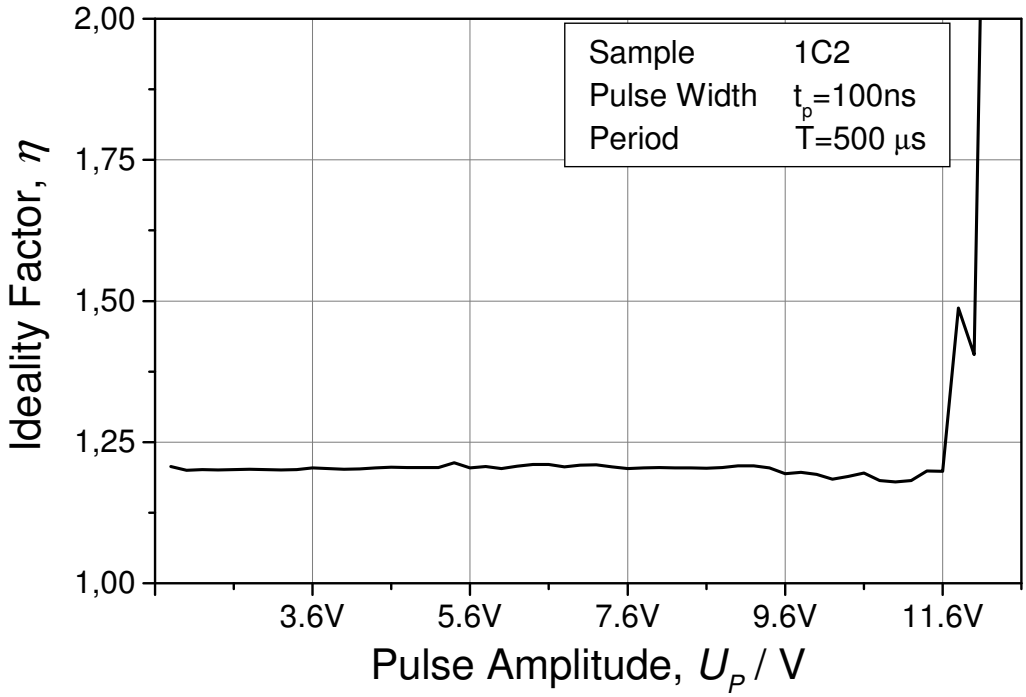


Figure 6.32: Degradation threshold for whisker-diodes.

Figure 6.32 shows the ideality factor of a whisker-contacted mixer diode versus pulse amplitude. It is evident that there is a sharp threshold for the occurring degradation mechanism. The degradation is assumed to be current-induced as it scales with the current density.

Figure 6.33 shows the modification of the corresponding IV-characteristics. Starting with $U_p = 11.6\ V$ there is an initial increase of the saturation current. This is reported in [14] to take effect at temperatures T=150 °C. At $U_p = 11.8\ V$, a strong shift of the IV-characteristic is visible indicating a significant modification of the Schottky interface properties. This degradation is observed to take place for T=400 °C. Finally, with $U_p = 13\ V$, the typical Schottky-diode characteristics vanished and the device is entirely destroyed.

Figure 6.34 shows the ideality factor of a planar diode vs. the pulse amplitude. It is evident that there is a sharp threshold for the occurring degradation mechanism. Figure 6.35 shows the modification of the corresponding IV-characteristics. The initial heating of the device is not as

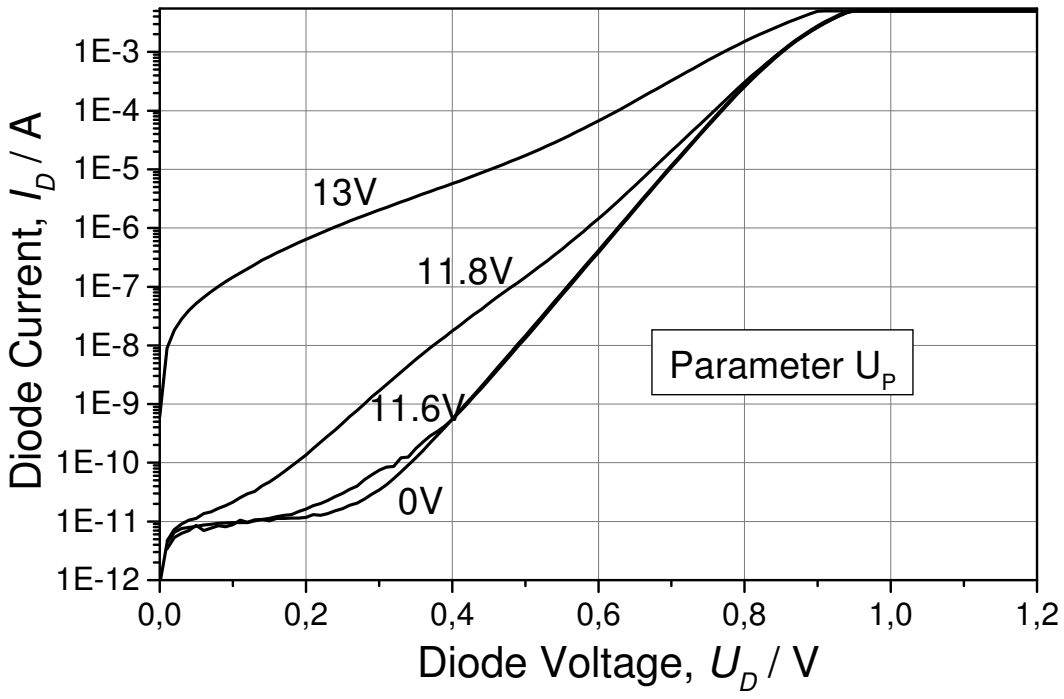


Figure 6.33: Change of the IV-characteristic for whisker-contacted process control mixer diodes.

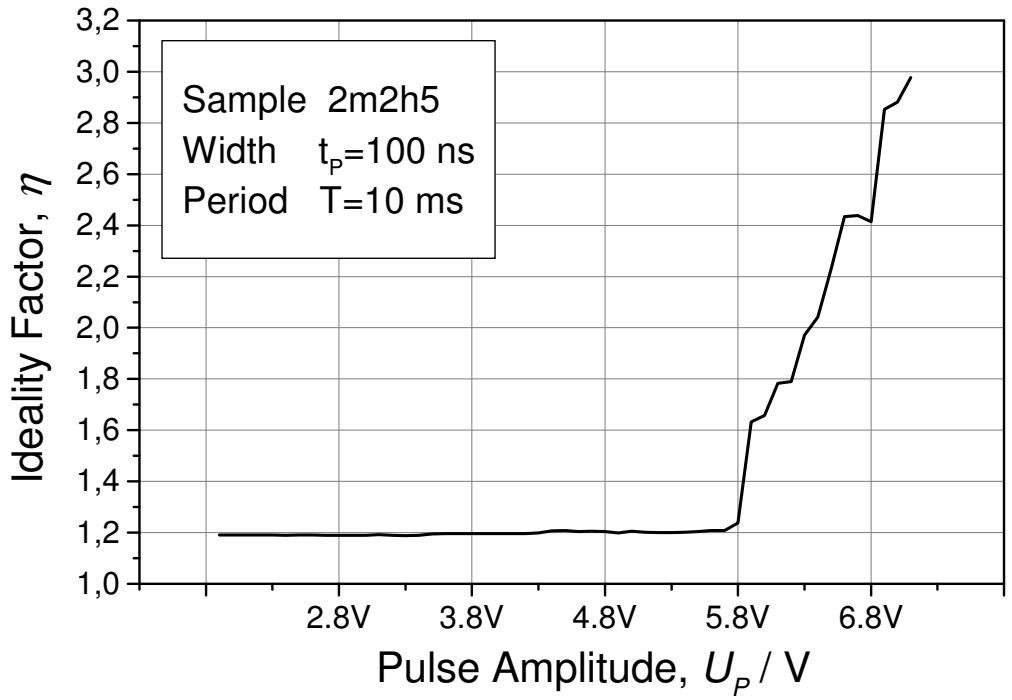


Figure 6.34: Degradation threshold for planar diodes.

significant as with whisker-diodes, which is due to the good thermal heat sink (the ohmic backside contact) directly next to the interface. A slight shift of the IV-characteristic is observed after

$U_p = 5.8\,V$. The typical Schottky diode characteristic vanishes with $U_p = 6\,V$.

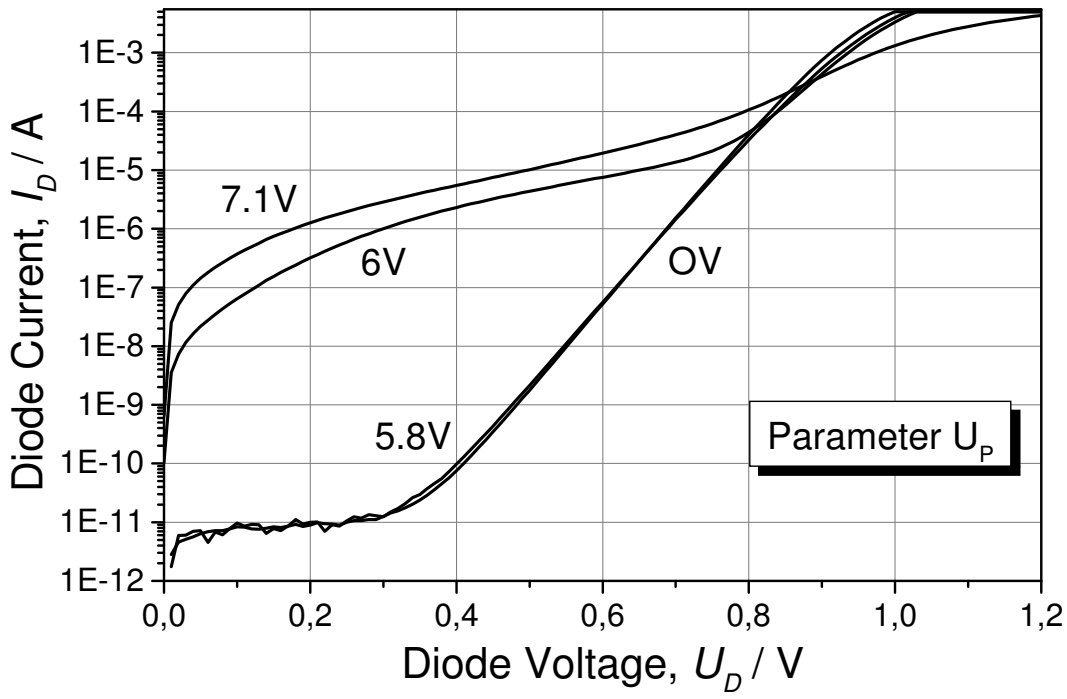


Figure 6.35: Change of the IV-characteristic for planar diodes.

6.5.4 Stress test with consecutive pulses

Figure 6.36 shows the ideality factor of a planar diode vs. the number of applied pulses. With this approach, monitoring of the degradation evolution is possible. In this case, there is only a slight increase of the ideality factor visible before device failure occurs. Figure 6.37 shows the modification of the corresponding IV-characteristics. There is a shift in the IV-characteristic starting with $N_p = 1 \cdot 10^7$ pulses before device failure occurs at $N_p = 2 \cdot 10^8$ pulses. This indicates beginning modification of the barrier due to current-induced diffusion mechanisms. Due to the good thermal heat sink, no initial temperature effect, e.g. burn-in, is observed.

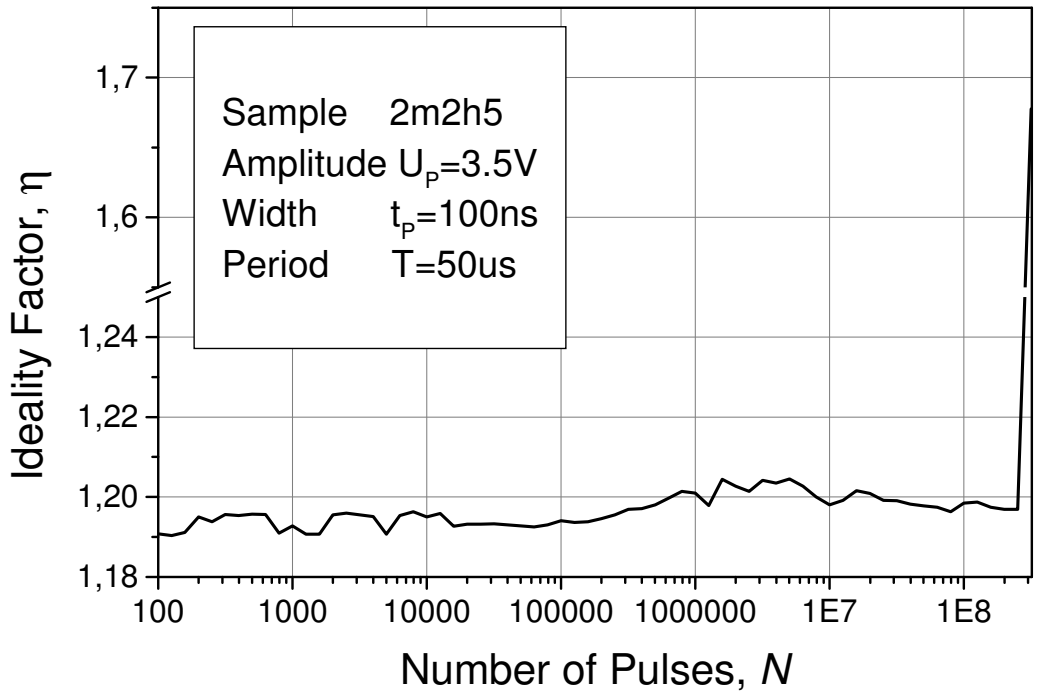


Figure 6.36: Change of the ideality factor as a function of the number of applied pulses for planar diodes.

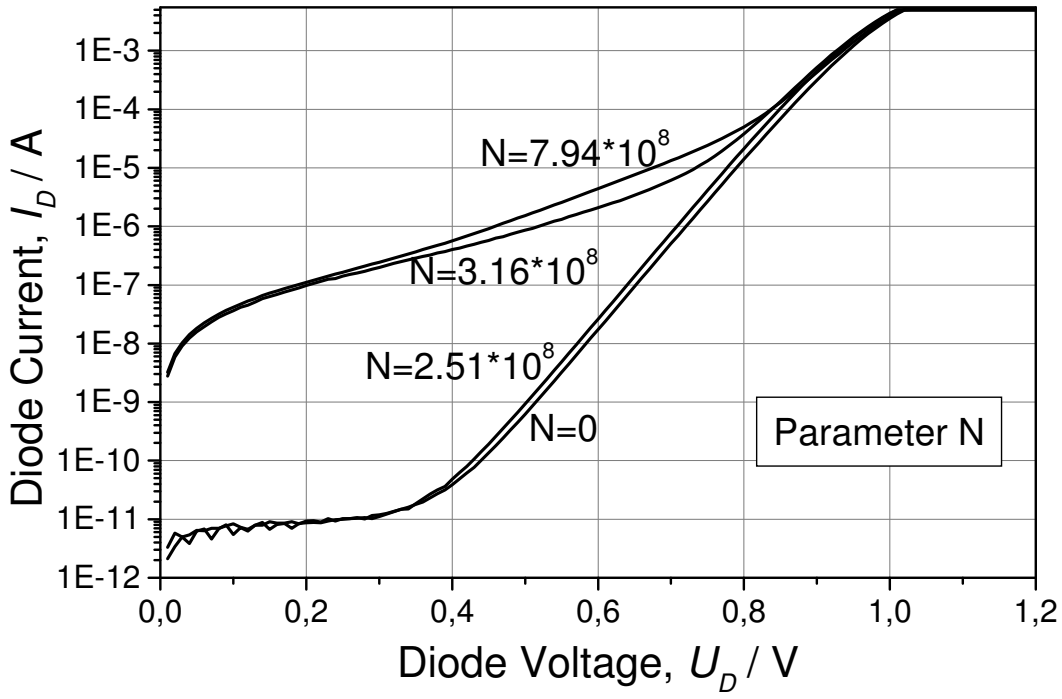


Figure 6.37: Change of the IV-characteristic as a function of the number of applied pulses for planar diodes.

6.5.5 Influence of TLP-parameters and technology

The first part of this section experimentally verifies the influence of the different TLP-parameters denoted in section 3.2 on the degradation evolution. The second part determines the influence of different technology parameters on the degradation evolution.

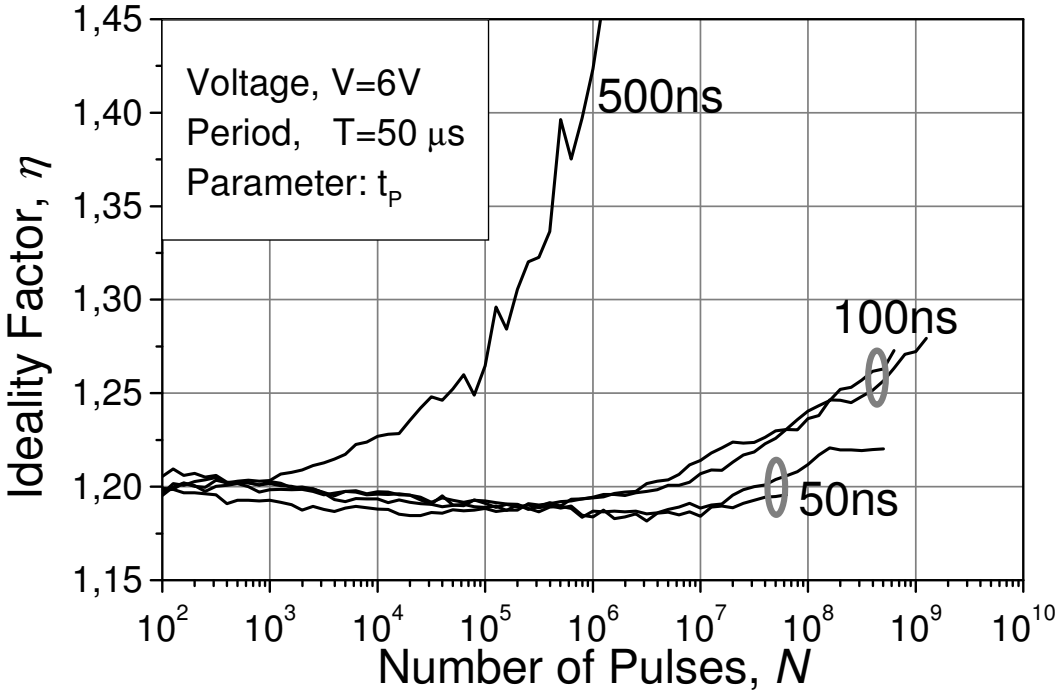


Figure 6.38: Degradation characteristics for different pulse lengths and different samples.

Figure 6.38 shows a comparison of the degradation characteristics for $t_p \ll \tau_{th}$ and for t_p being in the range of τ_{th}. Firstly, device lifetime is inverse-proportional to the pulse-length. In the case of $t_p = 50\,ns$ and $t_p = 100\,ns$ an electrically activated burn-in effect is visible. For $t_p = 500\,ns$ an additional thermally activated degradation mechanism superposes this effect.

A further experiment clearly identifies the thermally activated "burn-in" from the change in the ideality factor η using different pulse-pause-ratios. This effect is more pronounced for short pulse periods $T_p = 500\,ns, 5\,\mu s, 10\,\mu s$ than for longer pulse periods. Additionally, the slope for device degradation starting with $N_p = 10^6$ pulses changes.

The burn-in effect does not occur for rapid-thermally annealed (RTA)-samples. This supports the interpretation of a thermal activation of this degradation mechanism. In the following, the adiabatic case is chosen for accelerated stress tests, which compare the influence of the anode opening process, in this case CHF_3-RIE-etching or SF_6-Plasma etching, and show the transfer to a planar diode, cf. figure 6.40. A quasi-in-situ approach for the metal deposition directly after etching reduces the oxidation, cf. figure 6.42, of the GaAs surface. The oxidation reduction positively affects device lifetime as shown in figure 6.40. The quasi-in-situ diodes withstand significantly more pulses than the ones from standard processes.

The abrupt degradation and failure is typical for the CHF_3 RIE-etched whisker-contacted and planar diodes. Additionally, one can recognize the absence of a burn-in effect for the RTA-samples, of which the junction is already annealed before stress. This supports the assumption of a ther-

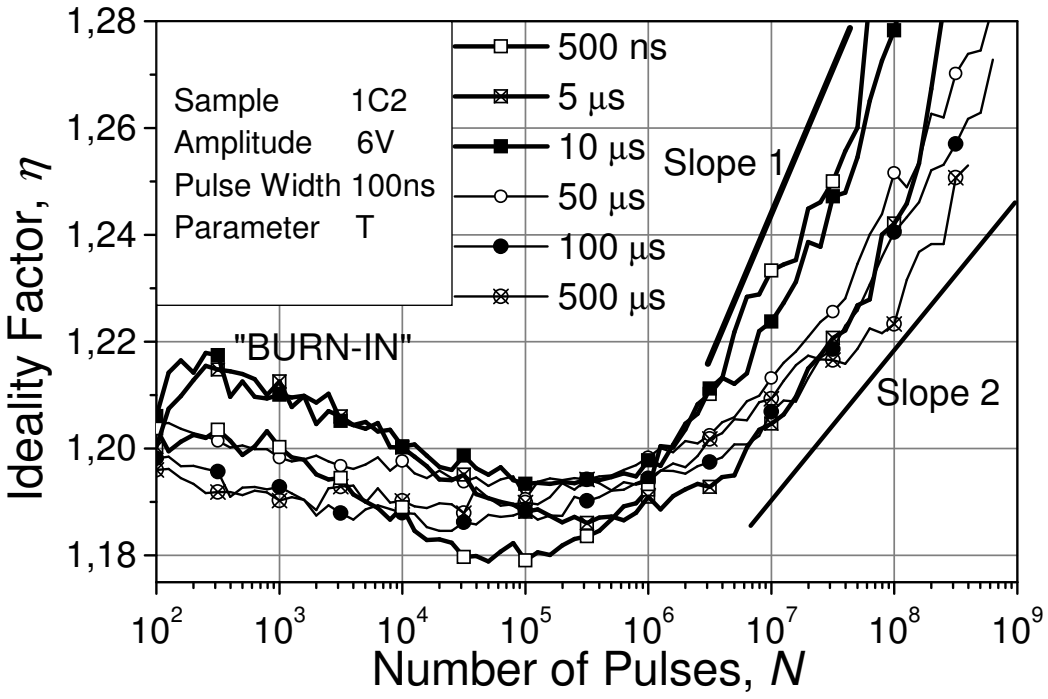


Figure 6.39: Degradation characteristics for different pulse periods and different samples.

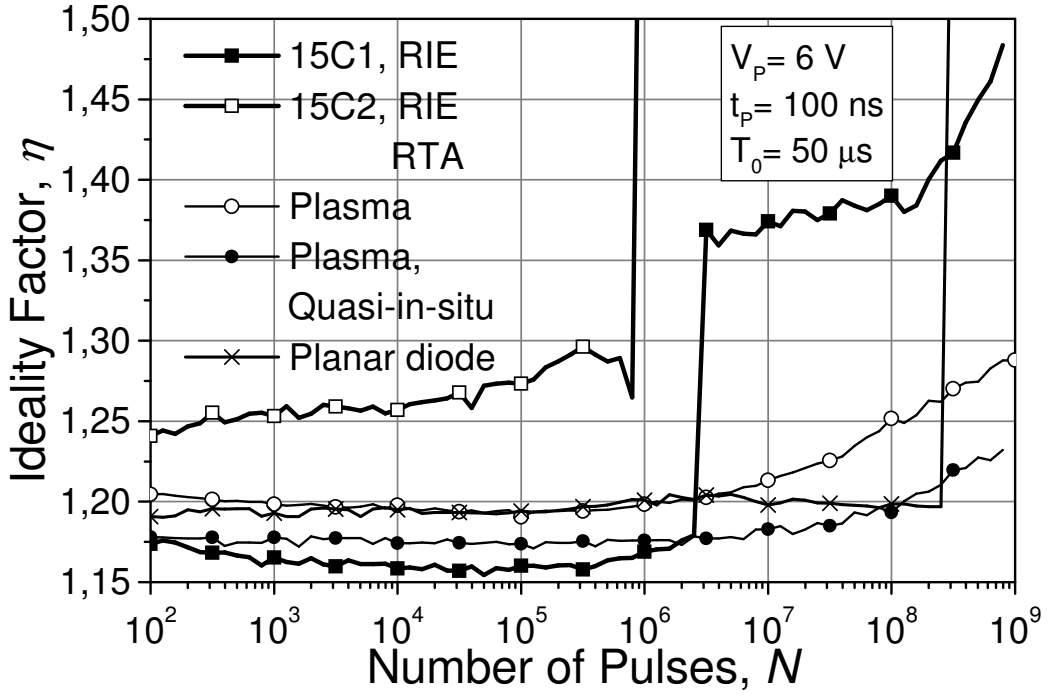


Figure 6.40: Degradation behavior for CHF3-RIE-etched diodes with and without RTA, SF6-Plasma etched anodes and Quasi-in-situ approach.

mal activation of the burn-in effect which takes place at temperatures $T_j < 150$ °C. Additionally, the degradation evolution is comparable between whisker-contacted control diodes and the planar diodes under test. The planar diode does not show the burn-in effect, which is consistent with the fabrication process including RTA.

6.5.6 Degradation and failure mechanisms with Schottky devices

The degradation mechanisms for semiconductor devices are coarsely classified as interface related and metalization related mechanisms as introduced in section 2.2. In the case of Schottky diodes, metal is integral part of the interface, so that this distinction does not hold without limitations. Degradation mechanisms for this device are e.g. ESD-like failure, field induced degradation and failure and current induced degradation, cf. section 2.2.2. In the case of the electrical ageing with the TLP-method, the dominating degradation and failure mechanisms are diffusion, migration, alloy formation and dislocations as detailed in section 2.2.4.

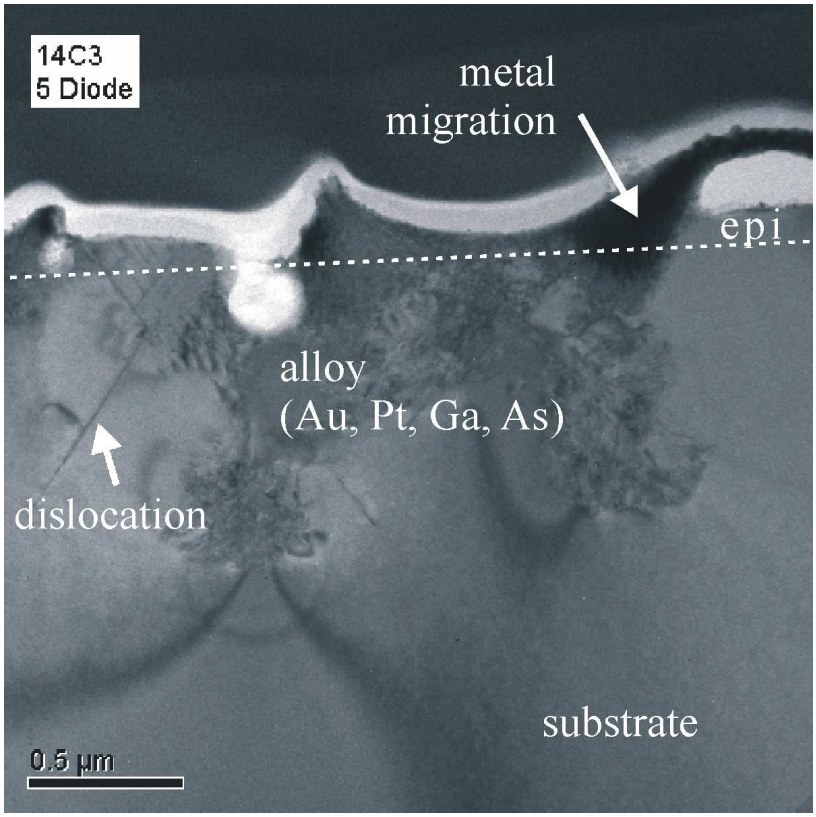


Figure 6.41: TEM image of the Schottky interface coarse degradation (current density $J = 8.15 \cdot 10^5 \frac{A}{cm^2}$), comparable to ESD damage.

Figure 6.41 shows a TEM image of a FIB-prepared Schottky control anode, $d = 5\ \mu m$, after pulse-step stress testing. One can clearly identify dislocation propagation in the semiconductor on the left side of the TEM image, regions with metal migration from the contact into the semiconductor due to local current crowding, interdiffusion and regions with alloy formation from Au, Pt, Ga and As directly at the interface. Figure 6.41 shows an interface, which failed after coarse degradation using the voltage pulsed-step stress test. This degradation is based on field induced material transport mechanisms (e.g. by hot electrons) resulting in metal spikes and migration into the semiconductor material.

In contrast to this coarse degradation, figure 6.42 shows a TEM-image of the Schottky interface after FIB preparation of a mixer diode Schottky interface, which was electrically stressed using consecutive pulses. The FIB-preparation and the TEM image is arranged at AMD, Dresden.

One can clearly identify an alloy between the GaAs lattice and the Schottky metalization due to metal interdiffusion. Figure 6.43 shows an energy dispersive x-ray (EDX)-scan of the interface. A metallic alloy forms at the interface due to current induced Ga interdiffusion [54]. On the other side, excess As remains on the GaAs side of the interface before the stoichiometric GaAs region starts. The thickness of the modified interface is approximately 5 nm, which corresponds to estimately 10 atomic layers without stoichiometry. This modification of the interface results in an increase of white noise.

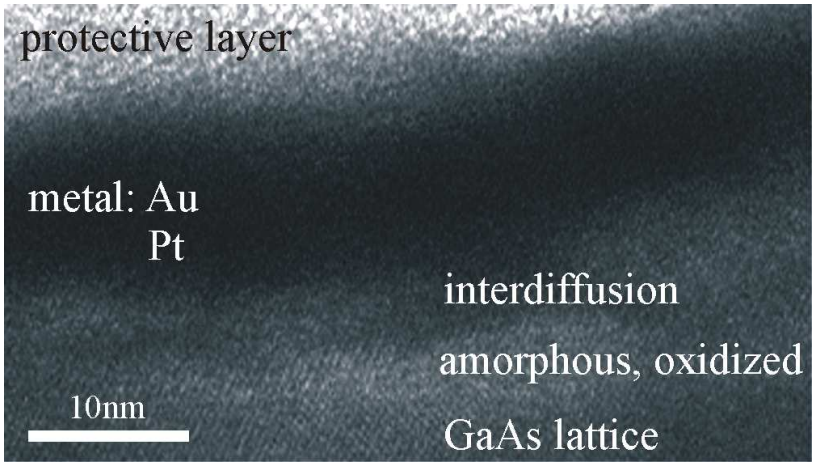


Figure 6.42: TEM image of the Schottky interface after pulsed stress with a current density $J = 4 \cdot 10^5 \frac{A}{cm^2}$.

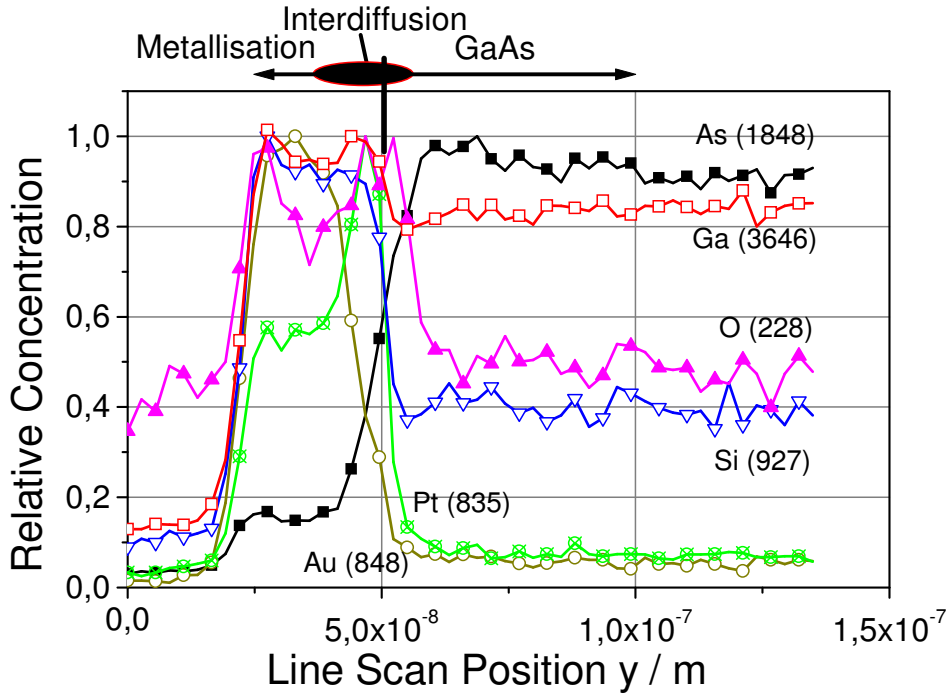


Figure 6.43: Vertical EDX-Scan of the stressed interface, cf. figure 6.42.

Chapter 7

Conclusion and Outlook

The presented work interrelates three major actual research topics in the area of III/V- based semiconductor technology development for high frequency devices, namely:

- the reliability analysis using electrical pulses (TLP-method) for very fast acceleration of degradation mechanisms and corresponding physics,
- the identification of degradation mechanisms with HBT using the TLP method and the comparison with results from Arrhenius-based lifetime tests,
- the THz-Schottky device and process development with respect to RF properties and reliability and introduction of a process control system.

The objective of this thesis was the implementation of a very fast accelerated reliability test method (TLP method) and the demonstration of the concept with high-frequency devices with respect to technology and process development. The process development was a prerequisite for planar Schottky diodes because reliability tests are only justifiable for devices with excellent performance. The following sections give a short conclusion of the achieved results and an outlook on further developments.

7.1 Conclusion

Reliability is a major concern for highest-frequency compound semiconductor devices, which are applied in security, medical or space applications. The accelerated determination of failure and degradation mechanisms is a key issue for device and technology development. The first part of this work describes a new test methodology for accelerated degradation excitation. The test methodology presented in this work is demonstrated to allow a very fast feedback to technology and therefore short optimization cycles for corresponding devices. This Transmission Line Pulsed (TLP)-method is implemented as a new testing methodology for very fast accelerated excitation of degradation mechanisms with high-frequency compound semiconductor devices (e.g. HBT, Schottky diode). A measurement setup is realized for this purpose, which is based on NATIONAL INSTRUMENTS LABVIEW for hardware control and allows stress and analysis cycles for degradation monitoring directly on-wafer without re-contacting the device under test (DUT) in a very short time. The realized hardware offers on the one hand very sensitive low-current IV-, CV-, or S-parameter measurements and on the other hand high-current/voltage conditions for the application of electrical pulses.

Reliability characterization with the TLP-method applies electrical square pulses to the device with a pulse length shorter than the respective thermal time constant, which is extracted in the first step of the test approach. After thermal characterization, The test methodology allows the separation of field- or current-induced degradation effects, which are excited with the pulsed-step stress approach, from diffusion effects, which are excited with the approach using consecutive pulsed. The capabilities of this method and the comparability to Arrhenius-based stress tests is demonstrated for an industrial Hetero Bipolar Transistor (HBT)-process and in-house designed and fabricated THz-Schottky diodes. The very fast feedback to the fabrication process, among many other research efforts from other research laboratories, enabled the establishment of an European HBT source on the one hand and the development of a "state-of-the-art European" planar Schottky-diode technology for THz-frequencies. With respect to the introduced methodology, the dominating degradation mechanism are presented for the investigated devices. The presented metal migration and interdiffusion effects are typical for high-frequency devices with small lateral dimensions and metal contact systems.

Results for HBT, their PCM- and TLM-structures, which are degraded by different types of electrical stress (i.e. pulsed step-stress test, stress test with consecutive pulses for electrical ageing) are shown excluding thermal effects. This method demonstrated to be a sensible and fast diagnostic tool for the accelerated excitation and detection of defects at the HBT metal contacts and in the device interfaces. A direct comparison of different devices regarding electrically induced defect mechanisms is performed directly on wafer within short time. The observed TLP-degradation behavior is shown to be comparable to Arrhenius-based lifetime prediction stress tests. With HBT, pulsed stress proves to be an alternative for accelerated reliability tests and process control, which requires less testing time and allows faster technology optimization. Within this work, the lifetime of HBT has been improved to more than 6000h under a junction temperature $T_j = 294\,^{\circ}C$ and a current density $J_E = 40\,KA/cm^2$. Simulations show, that the degradation mechanisms are mainly excited in the base-emitter region. With pulsed stress, the base-emitter is stressed selectively and that is why the formation of defects in this interface is accelerated to a high degree.

The second part of this work helps to reveal potential process weaknesses in the planar IHF THz-Schottky process. A systematic control and optimization approach leads to a proper understanding of lifetime limiting degradation mechanisms of devices using IV- and noise-measurements as well as TEM and EDX. The TLP method is found to excite RF-operation relevant degradation mechanisms in a well-directed very fast way and allows a fast feedback to the in-house fabrication process and proves its applicability in a process control system. With the TLP-approach, the dominating degradation mechanisms are field- and current induced metal migration and interdiffusion processes comparable to those reported for Arrhenius-based accelerated reliability tests. Further work is in progress for a comparison of Arrhenius-based methods and the TLP-method considering planar THz-Schottky diodes. The THz-capabilities of these devices are enhanced using a new diode design for the reduction of parasitic capacitances down to $C_p = 8.6\,fF$. The realized diodes are modeled using a commercial RF-simulation tool (AGILENT ADS) and simulation results are compared to DC- and S-parameter measurements. With these devices, the realization of uncooled mixer- and multiplier systems is possible for highest frequency applications. Currently, these devices are integrated with mixer systems for 150 GHz and offer excellent noise temperatures, which agrees with noise measurements at 5 GHz.

7.2 Outlook

The presented results give an excellent perspective for the application of the TLP-method in process and technology optimization for III/V-based high-frequency devices. The devices under test require a measurement setup with a high degree of flexibility. This can be achieved by the realization another control software, e.g. based on MATLAB, which offers a modular programming approach and easy extraction of characteristic device parameters due to implementation of analytic formulas (e.g. for fit algorithms). This is a mandatory condition for administration of the measurement data, which accumulates during measurements. The ULNA section was too slow for integration with very-fast accelerated stress tests, which is mainly due to the long settling time of the amplifier. Here, one must find a tradeoff between different requirements, such as low 1/f-noise floor, high amplification and fast onset. The pulse generator is already at its limit with respect to maximum output voltage, current and minimum pulse length. New devices with either wide bandgap or small dimensions require stress tests with a high level of electrical stress or very short stress duration. For this reason, the integration of a new pulse generator, which fulfills these requirements, is a future task The presented measurements set-up in combination with the proposed modification allows its commercialization, which is still an issue.

Further work on Schottky diodes includes a comparison of TLP-results and Arrhenius-based test results. These are required tests for space qualification of these devices. Additionally, further reduction of the parasitic capacitance requires detailed modeling of its constituent parts using Microwave Studio or Momentum. With this knowledge, a new diode concept can be realized. This design must include a new wafer design with an additional AlGaAs etch-stop layer for the reduction of ohmic backside contact dimensions and respective parasitic capacitance. In a next step, the hybrid integration with filter structures on quartz substrate and with conventionally manufactured or micro-machined waveguides is possible. These efforts will allow the extraction of further noise temperatures and give information on device capabilities for even higher frequencies. Finally, this will lead to the realization of radiometric instruments and opens the path to new developments in medical and security-related applications (e.g. biometry, exhaust gas control or cancer diagnostic). At last the path to monolithic integration should be followed.

From the reliability point of view, the test of FET-devices like MESFET or HEMT is the next logical step, based on the experiences with HBT and Schottky devices. For these devices, effects like gate-metal sinking (diffusion of Ti-gates into semiconductor) or the hydrogen-effect are reported with Arrhenius-based stress tests. The gate-metal sinking effect is comparable to the Schottky interface degradation reported in this work, while hydrogen is an impurity in any compound semiconductor process. Comparative Arrhenius-based stress tests will allow the validation of TLP results and increase industrial acceptance. The research efforts with the TLP method and high-frequency compound semiconductor devices showed a lack of computational tools for the calculation of coupled problems with semiconductor devices, which are in detail:

- a coupled electro-thermally semiconductor solver,
- a coupled physical-semiconductor RF solver.

The realization of these simulation tools or the enhancement of existing numerical solving algorithms would ease the understanding of reliability lifetime bottlenecks in semiconductor devices (e.g. by beforehand identification of hot spots). These research topics are a precondition for future effective design and realization of devices for frequencies up to 6 THz.

Symbols

A	Area	
$A**$	Effektiv Richardson-constant	
A_{eff}	Effektiv area of the Schottky diode	
c	Speed of light, $2.99792458 \cdot 10^{10}$	$[\frac{cm}{s}]$
C_j	Space charge capacity of the Schottky diode	
C_{j0}	Space charge capacity of the Schottky diode without bias	
C_{jmin}	Minimum space charge capacity of the Schottky diode without bias	
C_{jmax}	Maximum space chafge capacity of the Schottky diode without bias	
C_{mod}	Capacity modulation	
d	Diameter	$[m]$
e	Electron charge	[C]
E_f	Fermi energy	[eV]
E	Electric field	$[\frac{V}{m}]$
E_g	Bandgap between valence- and conduction band	
E_v	Energy level of the valence band	
$f(E)$	Fermi-distribution	[F]
f	Frequency	$[Hz]$
f_g	Cutoff-frequency of a device	$[Hz]$
g_m	Differential conductivity	
h	Planck's constant	[J·s]
I_d, i_d	Diode current	$[A]$
I_{sat}	Saturation current by velocity saturation of electrons	$[A]$
I_p	Pulse current	$[A]$
J_{sat}	Saturation current density	$[\frac{A}{m^2}]$
k	Boltzmann's constant	$[\frac{J}{K}]$
m_0	Free electron mass	$[kg]$
N_c	equivalent energy state density at the conduction band	
N_D	Doping concentration of the active n-layer	$[\frac{1}{cm^3}]$
n_i	Intrinsic carrier concentration	
N_p	Number of pulses	
r_a	Anode radius	$[m]$
R_B	Resistance of the diode	[Ω]
R_{epi}	Resistance of the epi-layer	[Ω]

R_j	Depletion layer resistance of a diode	$[\Omega]$
R_k	Sum of all contact resistances	$[\Omega]$
R_{sub}	Resistance of the substrate	$[\Omega]$
R_s	Series resistance of the diode	$[\Omega]$
t	Time	$[s]$
T_0	Ambient temperature	$[^\circ C]$
T_j	Junction temperature	$[^\circ C]$
t_p	Pulse duration	$[s]$
T_p	Pulse period	[s]
U	Voltage	$[V]$
$\hat{u}$	Amplitude of alternating voltage	$[V]$
U_{bi}	Built in potential	$[V]$
U_{bias}	Bias voltage	$[V]$
U_{br}	Diode breakdown voltage	$[V]$
U_D	Diode voltage	$[V]$
U_p	Pulse voltage	$[V]$
U_T	thermal voltage	$[V]$
v_{sat}	Saturation velocity of electrons	$[\frac{m}{sec}]$
w_{depl}	Effective depletion layer width	$[m]$
β	Current gain	
ε_0	Permittivity of the free space, $8.8542 \cdot 10^{-12} \frac{F}{m}$	
ε_r	Relative permittivity	$[\frac{A \cdot s}{V \cdot m}]$
η	Diode ideality factor	
μ_0	Permeability of the free space, $1.256637 \cdot 10^{-6} \frac{Vs}{Am}$	
μ_r	Relative permeability	$[\frac{V \cdot s}{A \cdot m}]$
ρ	Spezific resistance	$[\frac{\Omega}{m}]$
$\underline{\sigma}_s$	Complex conductivity of a semiconductor	$[\frac{S}{m}]$
Φ_0	Surface state energy level	$[eV]$
Φ_0	Workfunction for electrons	$[eV]$
Φ_{B0}	Schottky potential barrier without lowering	$[eV]$
Φ_{Bn}	Schottky potential barrier with lowering	$[eV]$
$\Delta\Phi$	Schottky potential barrier lowering	$[eV]$
σ	Specific conductivity	$[\frac{m}{\Omega}]$
τ	Time constant	$[s]$
τ_{th}	Thermal time constant	$[s]$
χ_H	Electron affinity of a semiconductor	

Acronyms

AC	Alternating current
AD	Analog Digital Conversion
As	Arsenic
AlGaAs	Aluminumgalliumarsenide
Au	Gold
Be	Berryllium
$B-E$	Base-Emitter
$B-C$	Base-Collector
C	Carbon
CH	Carbonhydroxid
C/V	Capacity/Voltage
DC	Direct current
DUT	Device under test
e-beam	Elektron beam
EDX	Energy dispersive x-ray
Epi, Epi-layer	Epitactically grown layer
ESA	European Space Agency
ESD	Electrostatic discharge
FET	Field effect transistor
FIB	Focussed ion beam
Ga	Gallium
GaAs	Gallium arsenide
Ge	Germanium
GHz	Gigahertz
H_2O_2	Hydrogenperoxide
HCl	Hydrochloric acid
HBT	Heterostructur Bipolar Transistor
HBV	Heterostructur Barrier Varactor
HEMT	High electron mobility transistor
HF,RF	High-frequency, Radiofreqeuency
IHF	Institut für Hochfrequenztechnik
I/V	Current/Voltage
InGaAs	Indium gallium arsenide
InGaP	Indium gallium phosphide

InP	Indium phosphide
ISO	International Standards Organisation
kHz	Kilohertz
MBE	Molecular beam epitaxy
MDS	Microwave Design System
MEMS	Micro Electro Mechanical Systems
MESFET	Metal semiconductor FET
MHz	Megahertz
MMIC	Microwave monolithic integrated circuits
MOCVD	Metal organic chemical vapour deposition
NH_3	Ammonium
Ni	Nickel
PECVD	Plasma enhanced chemical vapour deposition
PCM	Process control model
Pt	Platinum
REDR	Reaction enhanced defect reaction
RIE	Reactive ion etching
RLZ/SCR	Depletion layer / Space charge region
RTA	Rapid thermal annealing
SCR	Space charge region
S.I.	Semi-insulating
SiGe	Silicon Germanium
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
$SiON$	Phase from Silicon oxide and -nitride
TEM	Transmission electron microscopy
THz	Terahertz
Ti	Titan
TLM	Transmission line model
TLP	Transmission line pulse
ULNA	Ultra low noise amplifier

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Appendix A

Simulation

A.1 ADS-model following Dickens

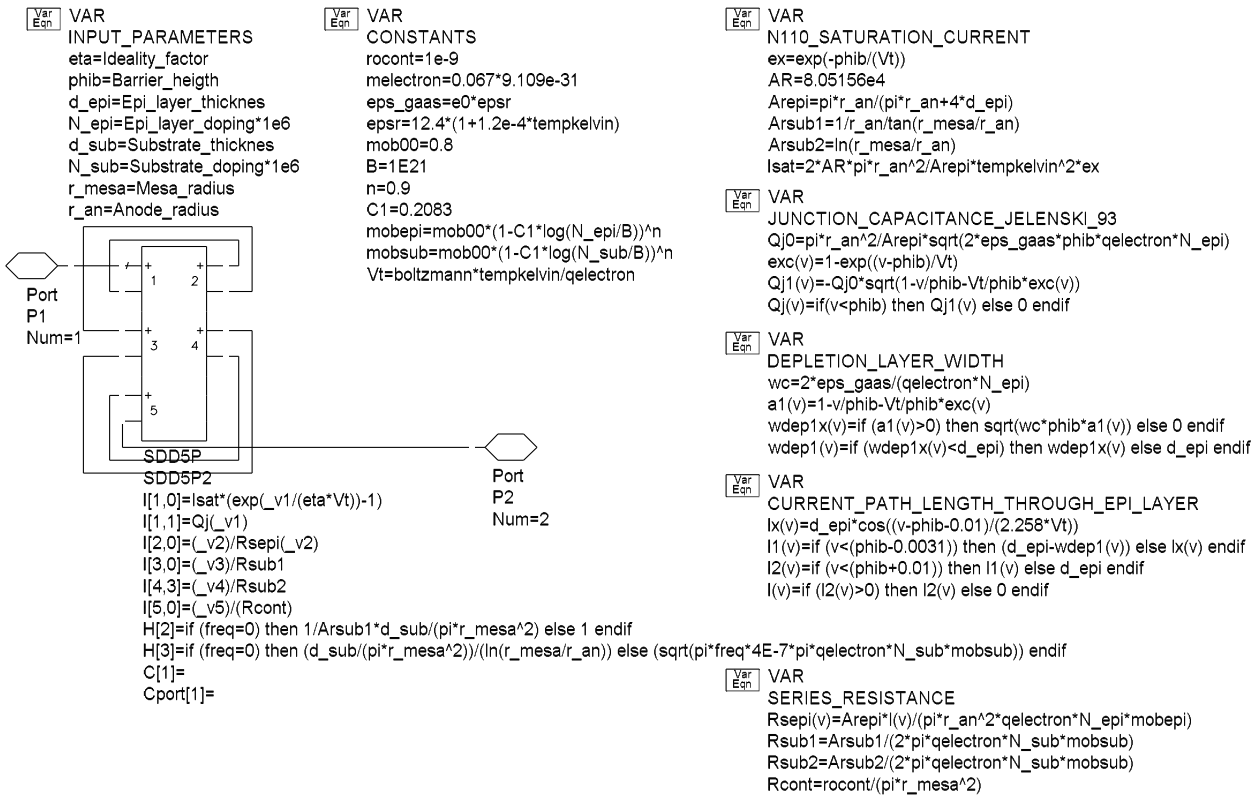


Figure A.1: ADS2003C-*Model of the IHF THz-Schottky diode following Dickens.*

A.2 ADS-model following Calviello

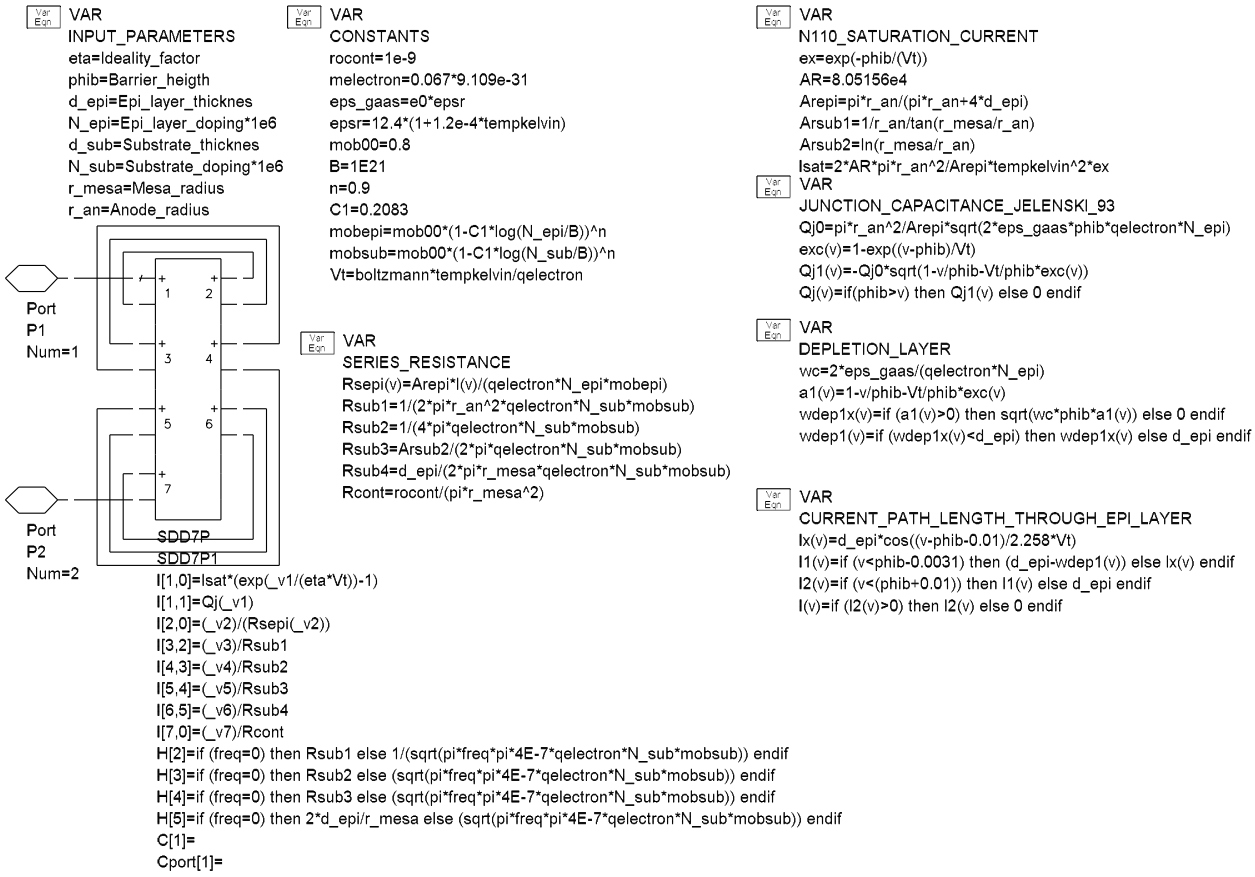


Figure A.2: ADS2003C-*Model of the IHF THz-Schottky diode following Calviello.*

Appendix B

Wafer Material

B.1 Planar Schottky diode wafer structure

Structure A is the wafer design for mixer diodes, structure B the one for varactor diodes. The two different wafer designs differ in the epi-layer thickness, which is designed for a low epi-layer resistance in the case of mixer diodes and acceptable reverse breakdown voltage in the case of varactor diodes. The wafers are passivated with a SiOx-layer. The etch-stop layer is mandatory for the realization of the ohmic contact on the backside. The total thickness of the 4-inch wafer EE2285 is 2800 nm, the sheet resistance 4.6 Ω/sq, the thickness of the 4-inch wafer EE2286 3310 nm and the sheet resistance 4.7 Ω/sq.

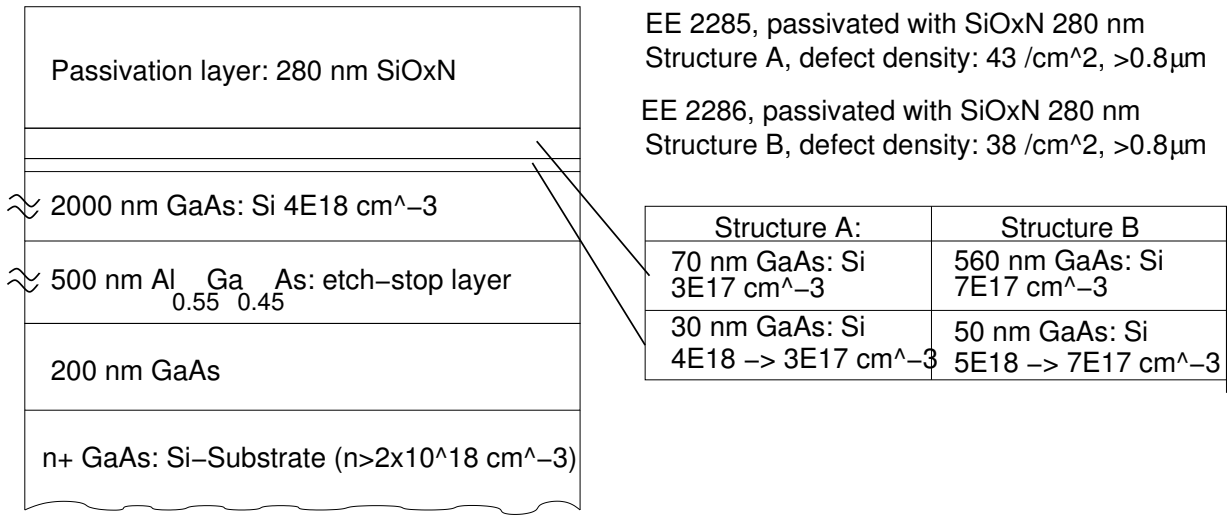
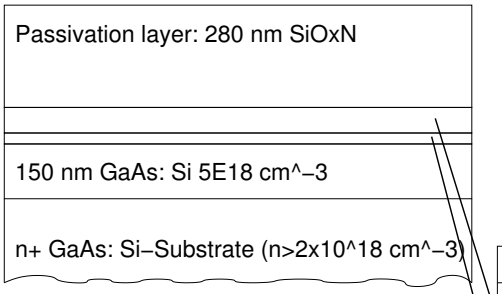


Figure B.1: Wafer design for planar Schottky diodes

B.2 Whisker-contacted Schottky diode wafer structure

The different wafer designs are used for mixer diode technology optimization using whisker-contacted diodes. The difference between the different structures is the epi-layer doping. The epi-layer is grown on 3-inch n^+ GaAs-substrate. The wafers are passivated with a SiOx-layer and thinned to a thickness of $70 \ldots 90 \mu m$, before further processing



EE 1983, passivated with SiOxN Run 2 on 17.05.2001
Structure A, defect density: 8.9 /cm^2, Dicke=220 nm

EE 1984, passivated with SiOxN Run 2 on 17.05.2001
Structure B, defect density: 4.4 /cm^2, Dicke=230 nm

EE 1985, passivated with SiOxN Run 1 on 17.05.2001
Structure C, defect density: 3.7 /cm^2, Dicke=250 nm

Structure A:	Structure B	Structure C
40 nm GaAs: Si 1E18 cm^–3	50 nm GaAs: Si 7E17 cm^–3	70 nm GaAs: Si 3E17 cm^–3
30 nm GaAs: Si 5E18 –> 1E18 cm^–3	30 nm GaAs: Si 5E18 –> 7E17 cm^–3	30 nm GaAs: Si 5E18 –> 3E17 cm^–3

Figure B.2: Wafer design for whisker-contacted Schottky diodes

B.3 HBT wafer structure

HBT-Wafer EPI-3302 (EPI, UK)

No.	Layer	Material	Thickness	Doping, cm^{-3}
1	InGaAs-contact	n^+-InGaAs	≈60 nm	$n \approx 2 \cdot 10^{19}$
2	Emitter-contact I	n^+-GaAs	200 nm	$n \approx 2 \cdot 10^{18}$
3	Emitter-contact II	n^+-InGaP	100 nm	$n = 9.2 \cdot 10^{17}$
4	Emitter-ballast	n-InGaP	250 nm	$n = 9.4 \cdot 10^{16}$
5	Emitter	n-InGaP	150 nm	on request*
6	Base	p^+-GaAs	on request*	$p = 2.5 \cdot 10^{19}$
7	Collector	n-GaAs	1000 nm	on request*
8	Sub-collector I	n^+-GaAs	100 nm	$n = 3.1 \cdot 10^{18}$
9	Etch-stop layer	n^+-InGaP	25 nm	$n > 1 \cdot 10^{18}$
10	Sub-collector II	n^+-GaAs	800 nm	$n = 3.5 \cdot 10^{18}$
11	Substrat	GaAs	100 µm	s.i.

Table B.1: *EPI-3302 wafer structure: The * marked details are available on request*

HBT-Wafer LCR-1146 (Thomson LCR, France)

No.	Layer	Material	Thickness	Doping, cm^{-3}
1	InGaAs-contact	n^+-InGaAs	≈50 nm	$n \approx 6 \cdot 10^{18}$
2	Emitter-contact I	n^+-GaAs	192 nm	$n \approx 2 \cdot 10^{18}$
3	Emitter-contact II	n^+-InGaP	97,5 nm	$n \approx 8 \cdot 10^{17}$
4	Emitter-ballast	n-InGaP	244 nm	$n \approx 1 \cdot 10^{17}$
5	Emitter	n-InGaP	146 nm	on request*
6	Base	p^+-GaAs	on request*	$p = 3.5 \cdot 10^{19}$
7	Collector	n-GaAs	1000 nm	on request*
8	Sub-collector I	n^+-GaAs	100 nm	$n = 3.1 \cdot 10^{18}$
9	Etch-stop layer	n^+-InGaP	25 nm	$n \approx 3 \cdot 10^{18}$
10	Sub-collector II	n^+-GaAs	800 nm	$n = 2.2 \cdot 10^{18}$
11	Substrat	GaAs	100 µm	s.i.

Table B.2: *LCR-1146 wafer structure: The * marked details are available on request*

The metalization of the single contacts and the passivation is identical for both wafers, listed as follows:

- Collector-and emitter contact system: AuGe/Ni/Au, 35/15/1000 nm (alloyed)
- Base-contact system: Ti/Pt/Au, 50/50/100 nm (not alloyed)
- Backside metalization: 10 µm Au, electrolytically deposited
- Passivation: SiO_2, 100 nm, SiN_4, 50 nm

Appendix C

Electrochemical Plating

C.1 Plating setup, plating pulse response and pulse monitor

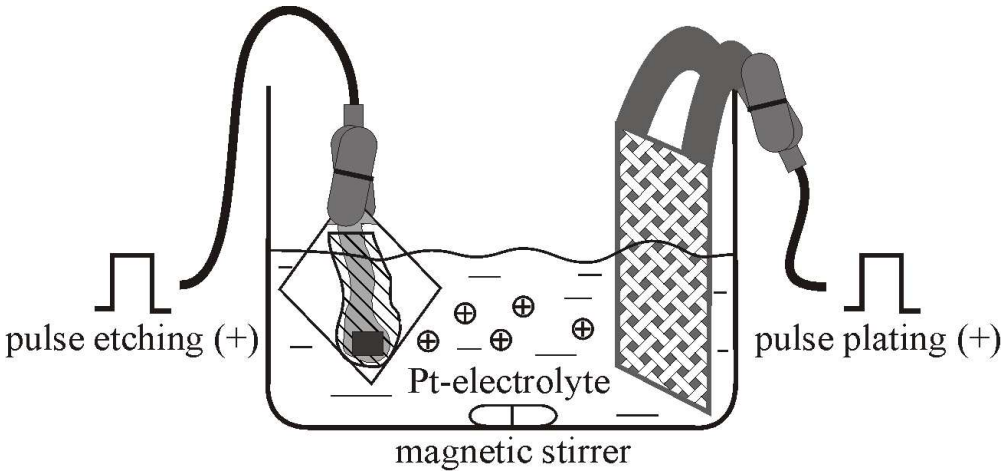


Figure C.1: Basic setup for electrochemical deposition of Schottky contacts.

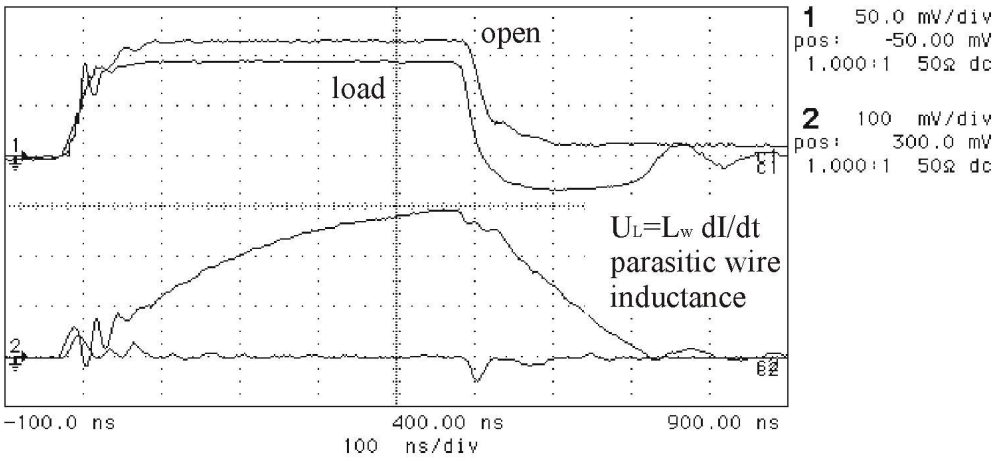


Figure C.2: Online plating pulse response.

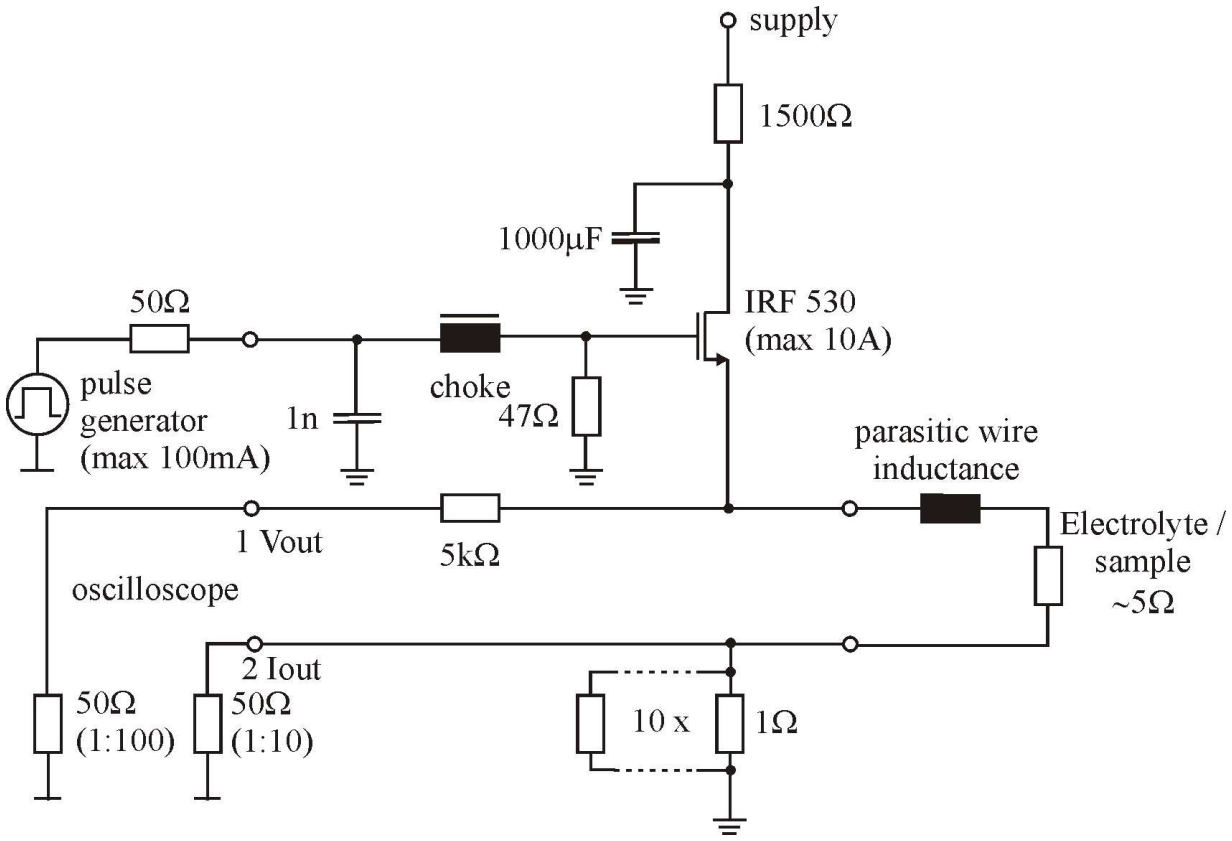


Figure C.3: Current amplifier and plating monitor for online monitoring of the plating pulse response.

Appendix D

TLP measurement setup

Measurement setup, on-wafer probe station and matrix switch

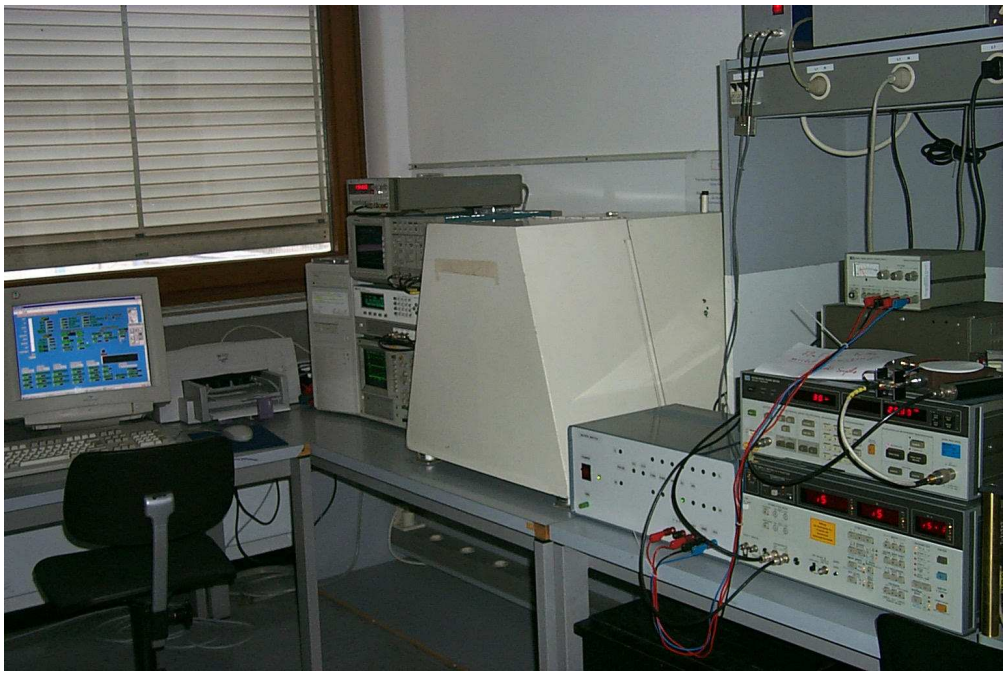


Figure D.1: Measurement setup for TLP measurements.

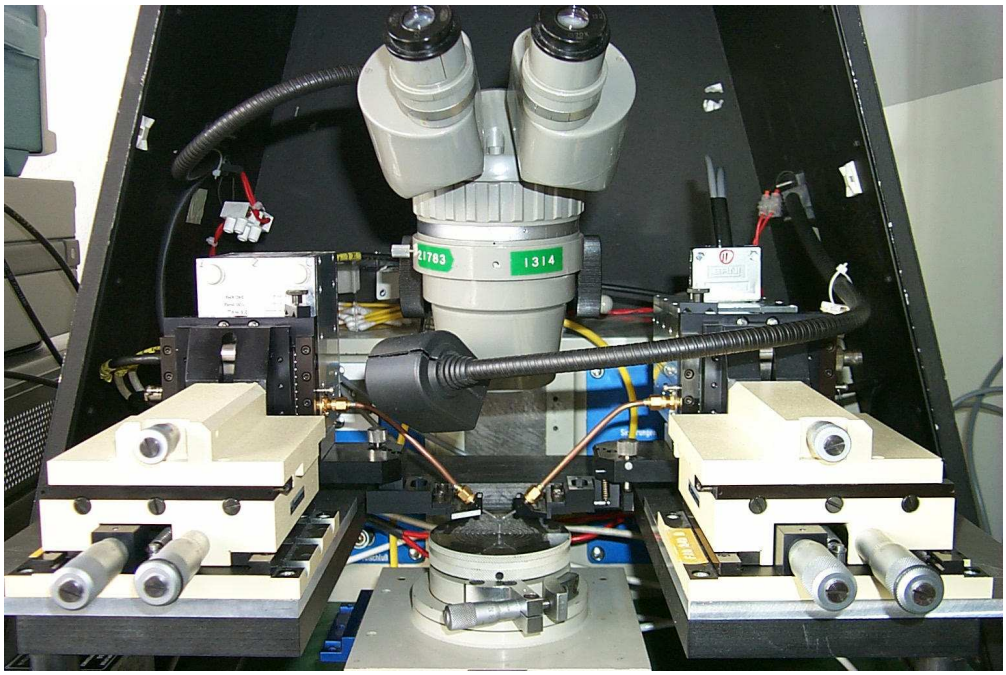


Figure D.2: On-wafer probe station with TUC probe heads and coplanar pico-probes.

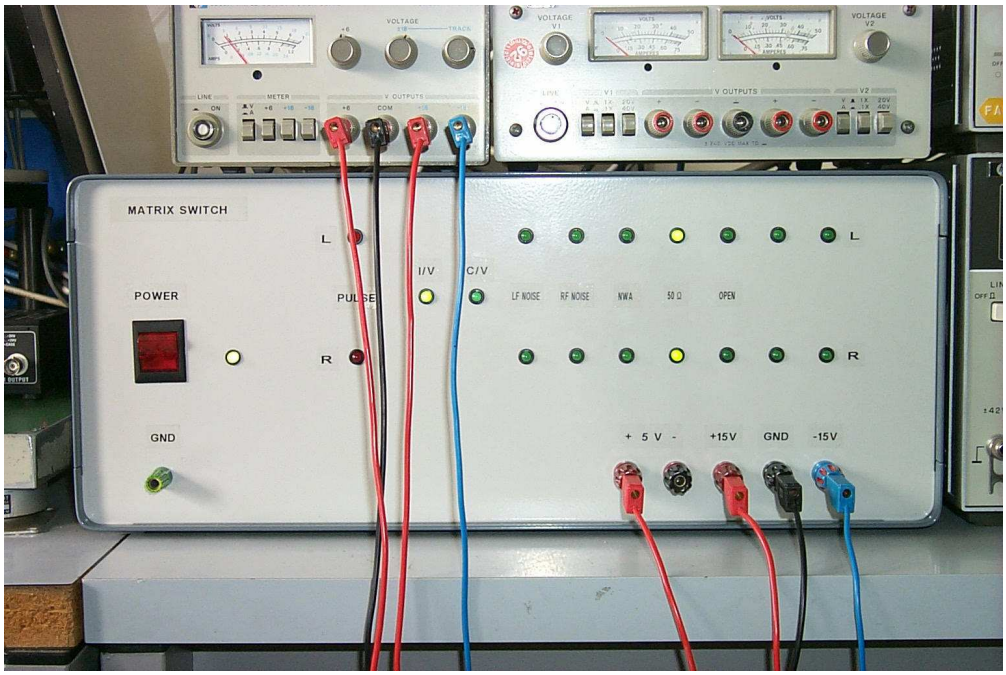


Figure D.3: Realised matrix switch.

Appendix E

Mask Set

E.1 Overview

The presented mask set is designed following the available technology for planar Schottky-diodes at the IHF TU DARMSTADT which was used e.g. in the former Master B Breadboard project. These diodes are fabricated using the „Quasi-Vertical-Approach“. This results in the basic necessity of a backside Ohmic contact and therefore a backside process. The critical dimensions of the anode and the mesa are not changed and thus, the electrical properties are expected to be comparable to the formerly manufactured planar diodes. Some modifications in the technological process and in the diode design are included which result from the experiences gained in various projects. The modifications mainly concern the backside processing, the seed-layer formation and the air-bridge formation, for which two designs are foreseen.

A major point for this mask design was the proper implementation of process control structures for alignment, exposure, ohmic contact quality, Schottky contact quality, adhesion and calibration structures for S-Parameter measurements. In general, the control structures are designed to be compatible with the fabrication process (e.g. the same via-holes as for the diodes are used). The control structures are presented in section 5.3. Further on, high precision alignment marks are used for critical alignment processes, which is e.g. the alignment of the mesa-mask on the anodes or the seed-layer- / air-bridge-masks on the anodes. The mask set is strongly correlated to the fabrication process for planar diodes at the IHF TUD (Master B Breadboard), which consequently gives the order of the following mask description. In this description, the term „sample“is used for the semiconductor piece (8 x 6 mm) under process and a part of the mask with a special purpose, e.g. anode-formation, is called anode-formation mask. Thus, the mask consists of a total of 20 different fields. These correspond to 12 different process layers and alternative solutions for a certain layer. Figure 4.5 shows a 3-dimensional preview of the final diode and clearly demonstrates the quasi-vertical design approach. In this figure, one side of the GaAs-substrate is removed to enable the view on the backside ohmic contact. Figure 4.6 shows a cut-out of the entire mask with all layers for only one diode and gives information on the dimensions of the final device.

The fabrication process for planar Schottky diodes at the IHF TUD is divided into the following steps, which are precisely described by PID's:

1. Backside processing
    - Etching of a first hole on the backside
    - Etching of the via-hole on the backside

- Ohmic contact formation on the backside

2. Front-side processing
    - Front-to-backside alignment
    - Dummy anode mask
    - Anode opening and formation (7 different diameters)
    - Mesa etching
    - Thin-film formation for 50 Ω NiCr-resistor
    - Seed layer formation (2 different designs)
    - Air-bridge formation (2 different designs)
    - Pillar formation
3. Separation
    - Standard etch step for separation
    - Etch step for fabrication of beam-lead diodes)

Curriculum vitae

Name	Bastian Mottet

Birth

06.03.1974	born in Krefeld Hüls, today Krefeld

Family status

Married	Wife: Andrea Mottet, née Paul 1st child: Yanneck Elias Mottet

School/Study

1980-84	Buscher-Holzweg Primary School in Krefeld-Traar
1984-90	Moltke-Grammar school in Krefeld
1990-93	Christian-Wirth-School (Grammar-school) in Usingen; Abitur
1994-99	Studies in electrical engineering, Technische Universität Darmstadt majoring in communications engineering Summerterm '96: preliminary diploma after 4th semester Diploma / majoring in RF-engineering, grade: gut
1999-2004	PHD thesis at Institut für Hochfrequenztechnik, TU Darmstadt

Military service

1993-94	Military service with 2nd company of 101st infantry battalion in Pfullendorf (3 months with Eurocorps in Strasbourg), Unteroffizier in the reserves

Practical

1994	Practical at Deutsche Telekom in Frankfurt a.M.
1998	3 month, Center for Wireless Communications (CWC), Singapore

Work experience

1999-2004	Research assistant at IHF, FB18, TU Darmstadt