Compact Modelling in RF CMOS Technology

by

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Declaration

I hereby certify that this material, which I now submit for assessment on the programme of study leading to the award of Doctor of Philosophy is entirely my own work, that I have exercised reasonable care to ensure that the work is original, and does not to the best of my knowledge breach any law of copyright, and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

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Publication List

This work has been and will be disseminated through the following publications:

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1. Jun Liu, Lingling Sun, Liheng Lou, Huang Wang and Charles McCorkell, "A Simple Test Structure for Directly Extracting Substrate Network Components in Deep n-Well RF CMOS Modeling", *IEEE Electron Device Letters*, Vol.30, No.11, pp.1200-1202, November 2009.

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Abstract

With the continuous downscaling of complementary metal-oxide-semiconductor (CMOS) technology, the RF performance of metal-oxide-semiconductor field transistors (MOSFETs) has considerably improved over the past years. Today, the standard CMOS technology has become a popular choice for realizing radio frequency (RF) applications. The focus of the thesis is on device compact modelling methodologies in RF CMOS. Compact models oriented to integrated circuit (ICs) computer automatic design (CAD) are the key component of a process design kit (PDK) and the bridge between design houses and foundries. In this work, a novel substrate model is proposed for accurately characterizing the behaviour of RF-MOSFETs with deep n-wells (DNW). A simple test structure is presented to directly access the substrate parasitics from two-port measurements in DNWs. The most important passive device in RFIC design in CMOS is the spiral inductor. A 1-pi model with a novel substrate network is proposed to characterize the broadband loss mechanisms of spiral inductors. Based on the proposed 1-pi model, a physics-originated fully-scalable 2-pi model and model parameter extraction methodology are also presented for spiral inductors in this work. To test and verify the developed active and passive device models and model parameter extraction methods, a series of RF-MOSFETs and planar on-chip spiral inductors with different geometries manufactured by employing standard RF CMOS processes were considered. Excellent agreement between the measured and the simulated results validate the compact models and modelling technologies developed in this work.

Abbreviations

MMIC	microwave monolithic integrated circuits
BJT	bipolar junction transistor
HBT	hetero-junction bipolar junction transistor
CMOS	complementary metal-oxide-semiconductor
RF	ratio frequency
PSP	Philips surface potential
EKV	C. C. Enz, F. Krummenacher and E. A. Vittoz
BSIM	Berkeley short-channel IGFET model
IGFET	insulated gate field effect transistor
NF_{min}	minimum noise figure
SOC	system-on-chip
IC	integrated circuit
ADS	Agilent Advanced Design Systems
CMC	compact model council
RFIC	radio frequency integrated circuit
MiM	metal-insulate-metal
LNA	low noise amplifier
VCO	voltage controlled oscillator
PA	power amplifier
NQS	non quasi-static
DNW	deep n-well
Q-factor	quality factor
SRF	Self-Resonance Frequency
EM	electromagnetic
SiO2	insulating silicon dioxide
HF	high frequency
S-parameters	scattering parameters
GSG	ground-signal-ground

SOLT	short-open-load-thru
LRRM	line-reflect-reflect-match
TRL	thru- reflect-line
DUT	device-under-test
ANN	artificial neural network
RMS	root-mean-square
ESR	effective series resistance
SMIC	Semiconductor Manufacturing International Corporation
HHNEC	Shanghai Hua Hong NEC Electronics Company, Limited
ICRD	Shanghai Integrated Circuit Research & Development Center
CAD	computer automatic design
PDK	process design kit
QS	quasi-static
NQS	nonquasi-static
IC-CAP	Integrated Circuit Characterization and Analysis Program

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Introduction

1.1 Application and Problem Overview

In order to meet the explosion in market demand for ubiquitous wireless access, a rapid proliferation of wireless communication standards has taken place in many areas of application such as wireless local area networks (HYPER-LAN, IEEE 802.11), wireless access in vehicular environments (WAVE, IEEE 1609), wireless personal area networks (Bluetooth, IEEE 802.15) and the 3rd (3G) and 4rd (4G) generations of cellular mobile communication. It is expected that a large amount of information access and data processing capabilities should be realized in modern individual wireless communication systems regardless of their location. This is only possible if high performance and low power wireless communication systems can be manufactured at low cost [1]. Traditionally, wireless transceivers were constructed with discrete single-transistors, inductors, capacitors, resistors and transmission lines. However, around 30 years ago, one started to witness some serious attempts to integrate certain functions of the radio into a single chip. Early microwave monolithic integrated circuits (MMIC) were predominantly fabricated in III-V compounds (GaAs MESFETs/HEMTs, GaAs HBTs technologies). Taking advantage of the high-speed carrier mobility, the low-loss substrate and the high break-down voltage, a larger scale of integration was achieved with the advent of silicon bipolar junction transistor (BJT) technology, especially when the SiGe hetero-junction bipolar junction transistor (HBT) became available where the transistor cut-off frequency (f_t) can be tens of GHz.

The complementary metal-oxide-semiconductor (CMOS) technology has long been considered slow and noisy [2] and therefore unsuitable for ratio frequency (RF) applications. Since the middle 1980s, when CMOS technology took over from that of NMOS in the fields of DRAM and microprocessors, it has dominated the technologies of digital integrated circuits. In fact, its simple planar structure and normally off type complimentary logic gate make CMOS the most suitable technology for high-density integration with high-speed and low-power operation as the downsizing of the transistor proceeds. In the field of high-frequency analog circuits for telecommunications

especially those for RF front-end circuits, CMOS has not been the major vehicle except for some specially designed systems. In spite of the fact that it has been predominantly used for the digital baseband portion, RF CMOS characteristics have been traditionally regarded as poorer than those of Si-bipolar and compound devices.

However, the aggressive scaling of the feature size, even though solely driven by digital applications, has resulted in a continuous improvement in RF characteristics of silicon MOSFETs and some of them have already exceeded some of Si-bipolar and GaAs transistors. For example, the 0.18-μm generation exhibits a peak f_t value in excess of 50 GHz [3–5]. A f_t of 115 GHz and a maximum oscillation frequency f_{max} of 80 GHz have been realized by using a 0.13-μm low-voltage logic-based technology node with a minimum noise figure (NF_{min}) of around 2.2 dB at 10 GHz [6–9]. At the 90-nm technology node, f_t and f_{max} have been increased to 150 and 200 GHz, respectively [10–12]. At the 65-nm technology node, f_t and f_{max} have been increased to 250 and 220 GHz, respectively [13]. Since the early 1990's, increasing investment and research has been attracted into RF CMOS radio design [14-18]. RF CMOS is considered more favorable primarily for the following reasons: First, the fabrication maturity and manufacture volume means the lowest possible cost. Second, it offers the best potential for wireless system-on-chip (SOC) as it would be compatible with the digital baseband circuit fabrication process. With the rapid improvement of the RF performance of MOSFETs, CMOS technology also has the potential to enable low-power mm-wave applications as well [19-21].

As modern circuits are usually very complex, the performance of such circuits is difficult to predict without accurate computer models. Most design work related to integrated circuit designs has a very large tooling cost, primarily for the photomasks used to create the devices, and there is a large economic incentive to get the design working without any iteration. Complete and accurate models allow a large percentage of designs to work the first time. These models traditionally fall into three types [22, 23]:

Tabular models: This type of model is a form of look-up table containing a large number

of values for common device parameters such as drain current and device parasitics. These values are indexed in the table by corresponding bias voltage combinations. Thus, model accuracy is increased by inclusion of additional data points within the table. The main advantage of this type of model is short simulation time. A limitation of these models is that they work well for interpolation of values in the table but are unreliable for extrapolation beyond the table values.

Physical models: These models are based upon device physics. Parameters of these models are based upon physical properties such as oxide thicknesses, substrate doping concentrations, carrier mobility, etc. In the past, these models were used extensively, but the complexity of modern devices mean simplifications have to be made to make them computationally practical and they are therefore inadequate for detailed design. Nonetheless, they find a place for initial analysis and estimation. Inclusion of all physical phenomena would render these models impractical in terms of computing requirements [24-28].

Empirical models: The third type of model is entirely based upon curve fitting, using arbitrary functions and parameter values to fit measured data so as to enable simulation of device operation. Unlike a physical model, the model parameters in an empirical model need have no physical basis. The fitting procedure is of the utmost importance for these models to be successfully used to extrapolate to data lying outside the range of the original fitting.

The integrated circuit (IC) design tools, such as the Cadence, H-SPICE, Agilent Advanced Design Systems (ADS), use compact models to predict the behaviour of a design. These models are commonly a hybrid of physical and empirical models. Compact models are the interface between the technology and the design [29]. A circuit designer iterates the design process by varying the compact model, rather than running expensive and time consuming experiments. Therefore compact models should be scalable with geometry and accurate across a wide temperature and bias voltage range. Compact models for devices are continuously evolving to keep up with changes in

technology. To attempt to standardize the model parameters used in different simulators, an industry working group, the compact model council (CMC), was formed to choose, maintain and promote the use of standard models. An elusive goal in such modelling is to predict the performance of the next generation, so as to identify the direction the technology should be taken before it is actually developed [30].

Despite the advantages brought about by RF CMOS technology use, CMOS RF design poses new design problems and implementation challenges when compared to the past alternatives. The development of low cost radio frequency integrated circuits (RFICs) in CMOS continues to move towards advanced technology nodes. First pass design success is expected, and the time window for a new product to enter the market is short. Robust RF compact models of both active and passive devices are therefore in great demand. The accurate characterization of the high-frequency behaviour is a major difficulty in RF CMOS modelling. Si substrate loss characteristics result in the performance degradation of active / passive devices. This therefore requires a model with more precise characterization. The improvement of the model accuracy usually means more complex modelling technology. In addition, new devices, such as spiral inductors, metal-insulate-metal (MiM) capacitors, varactors, are unique to RF CMOS technology. The device model and model parameter extraction method are still in development for these devices. Another issue is that RFIC design often requires non-linear, noise and other behaviour analysis, which poses new demands for the model simulation capability.

As regards the MOSFET, besides the well known requirements for a compact MOSFET model for low frequency application, such as accuracy and scalability of the DC model [31], there are additional important requirements for the RF models [32]: (1) the model should accurately predict the bias dependence of small signal parameters at high frequencies; (2) the model should correctly describe the nonlinear behaviour of the devices in order to permit accurate simulation of inter-modulation distortion and high-speed large-signal operation; (3) the model should correctly and accurately predict HF noise, which is important for the design of low noise amplifiers (LNA); (4) the

components in the developed sub-circuit should be physics-based and geometrically scaleable so that it can be used in predictive and statistical modelling for RF applications.

Composite (e.g. DC core model + RF sub-circuits) modelling technology alleviates to a certain extent the above mentioned design difficulties [31], but many issues should be considered in developing a MOSFET model for RF applications:

1) The extrinsic source and drain resistances (e.g. R_s and R_d) should be modeled with parameters for the real external resistors, instead of only with a correction to the drain current.
2) Substrate coupling in a MOSFET, that is, the contribution of substrate resistance and capacitance, needs to be modeled physically and accurately using a proper substrate network for the model be used in RF applications [26].
3) A bias dependent overlap capacitance model, which accurately describes the parasitic capacitive contributions between the gate and drain/source, needs to be included.
4) The distortion behaviour of MOS compact models should be evaluated, and advanced models with better predictability for distortion might be required.
5) Not only the accuracy of the model in DC or low frequency should be guaranteed, but the model accuracy should also be ensured in RF range. It requires an accurate frequency and bias dependence of small-signal parameters, such as transconductance and transcapacitance.
6) Besides the model accuracy for a single device, the model scalability needs also to be considered, at least over a certain channel length and width range.
7) The high frequency noise performance of the MOSFET model needs to be examined experimentally.
8) A methodology for worst-case model generation or better statistical modelling for RF applications needs to be developed.
9) Physics-based parameter extraction methodologies need to be developed.

With the emergence of the new generation MOSFET models, such as the Philips surface potential (PSP) model [33], (C. C. Enz, F. Krummenacher and E. A. Vittoz) EKV model [34], and (Berkeley short-channel IGFET (insulated gate field effect transistor) model 5) BSIM5 [35], many advanced problems with RF-MOSFET modelling have been solved such as a distortion simulation model, non quasi-static (NQS) model, the bias dependent overlap capacitance model and so on. However, there are still issues, such as the characterization of the substrate coupling in a MOSFET. The substrate network in CMOS is of the utmost importance in predicting the device output characteristics at radio frequencies. In particular, when employing a new substrate structure / process, such as the deep n-well (DNW) implantation, the traditional model is no longer valid. Since the coupling between the DNW and the p-well exists no matter what the electrical configuration is, as well as between the DNW and the original substrate, conventional substrate networks and corresponding extraction methods become too simple to accurately extract the substrate network parameters of DNW RF-MOSFETs. Advanced layout techniques [36-37] can bring great improvements to the high frequency characteristics of a MOSFET. However, the characterization of RF-MOSFET behaviour considering layout changes is rarely reported.

As a critical passive component, integrated spiral inductors have been widely used in CMOS RFIC design such as in RF amplifiers, voltage controlled oscillators, mixers, filters and impedance matching circuits. Therefore, an accurate equivalent circuit based model suitable for scalable spiral inductor library building is essential for reliable circuit implementation and design optimization. Though, considerable research work for on-chip spiral inductors modelling has been published in recent years, a rigorous physics-based scalable model for planar spiral inductors is still lacking.

This thesis focuses on the compact modelling techniques for RF-MOSFETs, on-chip spiral inductors and devices with novel layout structures in RF designs. In particular, it develops a physics-based fully scalable on-chip spiral inductor modelling method and a compact modelling methodology based on a PSP model for DNW RF-MOSFETs. The

behaviour and modelling methodologies for devices with advanced layout structures, such as RF-MOSFETs with non-average gate finger spacing are also investigated.

1.2 Thesis Contributions

There are two main contributions in this thesis. The first part is the analysis and modelling of the planar on-chip spiral inductors manufactured in RF CMOS technology. The second part is the compact modelling of DNW RF-MOSFETs. The avalanche breakdown performance of MOSFETs with different gate finger spacing and a compact modelling method are also investigated in this part. The developed compact modelling techniques for RF CMOS devices in this thesis can be applied to various other semiconductor processes which are similar in nature such as BiCMOS technologies.

1.2.1 Physics-Based Fully Scalable Spiral Inductor Model

This thesis defines a novel substrate network, consisting of R/L/C, to model the broadband loss mechanisms in the silicon substrate. A novel double-π equivalent circuit model for on-chip spiral inductors is presented. A hierarchical structure, similar to that for MOS models is introduced. This enables a strict partition of the geometry scaling in the global model and the model equations in the local model. The major parasitic effects, including the skin effect, the proximity effect, the inductive and capacitive loss in the substrate, and the distributed effect, are analytically calculated with geometric and process parameters at the local-level. As accurate values of the layout and process parameters are difficult to obtain, a set of model parameters is introduced to correct the errors caused by using these given inaccurate layout and process parameters at the local level. Scaling rules are defined to enable the formation of models that describe the behaviour of the inductors of a variety of geometric dimensions. A series of asymmetric inductors with different geometries are fabricated on a standard 0.18-μm SiGe BiCMOS process with 100 ohm/cm substrate resistivity to verify the proposed model. Excellent agreement has been obtained between the measured results and the proposed model over a wide frequency range.

1.2.2 Deep N-Well RF CMOS Modelling

This thesis also demonstrates a compact modelling technique for DNW RF-MOSFETs based on the PSP model. A simple test structure is developed for accurately extracting the substrate network parameters of RF-MOSFETs with DNW implantation from two-port measurements. The test structure with the source, drain and gate terminals all connected together is used as port one, while the bulk terminal is port two, making the substrate network accessible in measurements. A methodology is developed to directly extract the parameters for the substrate network from the measured data. Novel scalable models of substrate components for RF-MOSFETs with DNWs with different number of fingers are also derived and extracted by using the proposed test structure.

In addition to the content mentioned above, the effect of a non-uniform gate-finger spacing layout structure on the avalanche breakdown performance of RF CMOS technology is investigated. A novel compact model is also proposed to accurately predict the variation of BV_{ds} with the total area of devices which is dependent on the different finger spacing sizes. The model is verified and validated by the excellent match between the measured and simulated avalanche breakdown characteristics for a set of uniform and non-uniform gate finger spacing arranged nMOSFETs manufactured in a standard DNW RF CMOS technology.

1.3 Thesis Organization

Chapter 2 provides the background to the work addressed in the thesis.

Chapter 3 presents the analysis and modelling of the on-chip spiral inductors. The recent modelling approaches for RF CMOS spiral inductors are extensively investigated and compared. The key features of the models, including 1-π models, 2-π models and T-models are analyzed in detail. By actual implementation of each model's parameter extraction procedure, the pros and cons of the equivalent circuit topologies, parameter extraction techniques and fitting capacity of models are provided. A physics-based fully

scalable on-chip spiral inductor model is introduced. This model is further used to develop the spiral inductor model libraries for the asymmetric, symmetric and differential octagonal spiral inductors fabricated on a standard 0.18-μm SiGe BiCMOS process.

Chapter 4 describes the basic requirements for a compact MOSFET model in RF applications. A simple test structure developed for directly extracting substrate network components in DNW RF CMOS modelling is described. A physics-based scalable model of substrate components in DNW RF-MOSFETs with different number of fingers is also introduced in this chapter. The proposed test structure and scalable model are also suitable for modelling RF-MOSFETs without DNW implantations. The method for large-signal modelling of RF-MOSFETs based on the PSP model is described and examined. A method for modelling the avalanche break-down effect for RF-MOSFETs with non-average gate finger spacing is also presented.

Finally, Chapter 5 summarizes the contributions of the thesis and makes suggestions for future research.

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2

Background

2.1 Introduction

In addition to active devices (nMOSFET, pMOSFET) that are available in a CMOS process, most foundries provide mixed-signal options with high quality metal-insulate-metal (MiM) capacitors and high performance sheet resistance. However, their design, characterization and modelling are rather straight-forward. Hence, this thesis will thus focus on active devices and spiral inductors to discuss some specific issues in their modelling and implementation. The background to the techniques used in the work is described in this chapter.

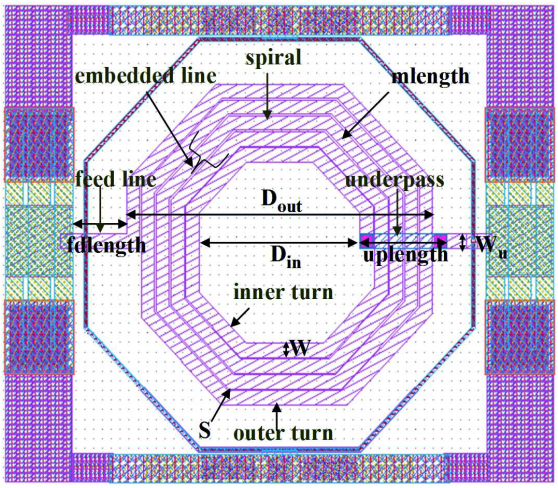
2.2 Spiral Inductors in Silicon Substrate

The first on-chip spiral inductor suitable for CMOS RFIC designs was first reported in 1990 [1]. Since then, much work has been done to improve its performance and characterize its behaviour. Inductors find application mainly in two areas, one is in tuned-amplifiers, and the other is in voltage controlled oscillators (VCOs).

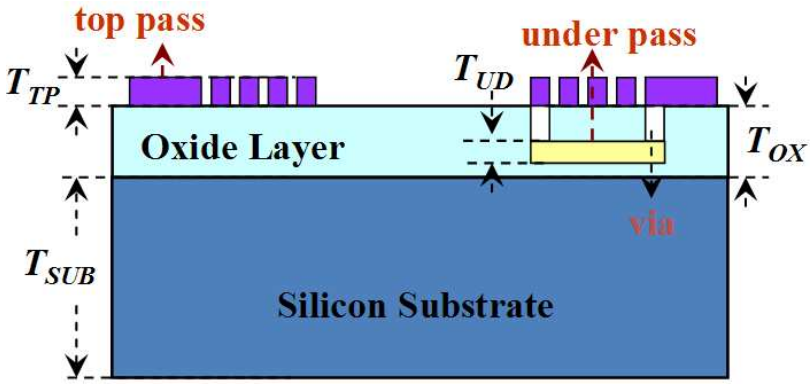
Design goals depend strongly on the application. On-chip inductor implementations entail a myriad of trade-offs between the vertical and lateral geometries of the layout. For example, when an inductor is designed for a tuned-amplifier, it is not uncommon to trade off the quality factor (*Q-factor*) for a smaller area. However, when an inductor is designed for a VCO, it is often most desirable to achieve the highest possible *Q*, limiting the designer to the top-most metal layer, which is the furthest layer from the lossy substrate, or to employ multi-metal levels to obtain high-*Q* inductors. In either case, a patterned substrate shield is often used to reduce the substrate loss due to both the capacitive and inductive coupling. [2]

The most commonly used inductor configuration in RF CMOS technologies is the planar spiral. It can be shaped into circular, square, hexagonal or octagonal metal stripe loops with average or gradient turn width [3-4], and constructed as asymmetric or symmetric structures. A simplified layout and cross-section view of an asymmetric planar

octangular spiral inductor are given in Figure 2.1(a) and (b), respectively. The inductor is isolated from the substrate by a layer of insulator, and it is usually made of silicon oxide in RF CMOS technologies. Generally speaking, a planar inductor with a given shape manufactured in a given process can be completely specified by the following lateral parameters as shown in Figure 2.1 (a): 1) the number of turns, *N*. 2) the metal width, *W*. 3) the edge-to-edge spacing between adjacent turns, *S*. 4) any one of the following: the outer diameter D_{out}, the inner diameter D_{in}, the average diameter $d_{avg} = 0.5(D_{out} + D_{in})$, or the fill ratio, defined as $\rho = (D_{out} - D_{in})/ (D_{out} + D_{in})$. Note that $D_{out} = D_{avg} + N(W + S) - S$ and that $\rho = (N(W + S) - S)/d_{avg}$.



(a)



(b)

Figure 2.1: (a) Layout of an octangular spiral inductor and the definition of the lateral parameters D_{out}, D_{in}, *W* and *S* and (b) Cross-section view of the on-chip spiral inductor and its vertical parameters, the thickness of metal spiral T_{TP}, thickness of oxide layer T_{OX}, the thickness of the metal underpass T_{UD} and the thickness of the substrate.

2.2.1 Definition of Inductance

Inductance is the electric dual of capacitance. A capacitor stores electrical energy, while an inductor stores magnetic energy. According to Faraday's law, we know that a changing magnetic field induces an electrical field. By using Lenz's law, we know that the induced electric field always opposes further change in the current. In quantitative form, consider an arbitrary closed circuit formed by conductors with a carried current I_i, as shown in Figure 2.2 (a). The magnetic flux of this circuit ψ is defined as the magnetic field crossing the cross-sectional area S

$$\psi = \iint_S \vec{B} \cdot d\vec{S} \tag{2.1}$$

As there is no other current in the system, the self-inductance of the circuit can be defined as

$$L = \frac{\psi}{I} \tag{2.2}$$

By Faraday's Law, the voltage induced in a loop is related to the flux by

$$V = \frac{d\psi}{dt} \tag{2.3}$$

Substituting equation (2.2) into (2.3), we have

$$V = L\frac{dI}{dt} \tag{2.4}$$

Then, if we now consider an arrangement of loops as shown in Figure 2.2 (b), current flow in Loop i and there is some flux linkage between the two loops, we have the following definition of mutual inductances

$$M_{ij} = \frac{\psi_i}{I_j} \tag{2.5}$$

where

$$\psi_i = \left[\iint_{S_i} \vec{B} \cdot d\vec{S}\right]_{I_i = 0 \forall i \neq j} \tag{2.6}$$

If the surrounding medium is linear, we have $M_{ij} = M_{ji}$. The mutual inductances can be positive or negative, depending on whether the magnetic fluxes from different circuits will enhance or cancel each other.

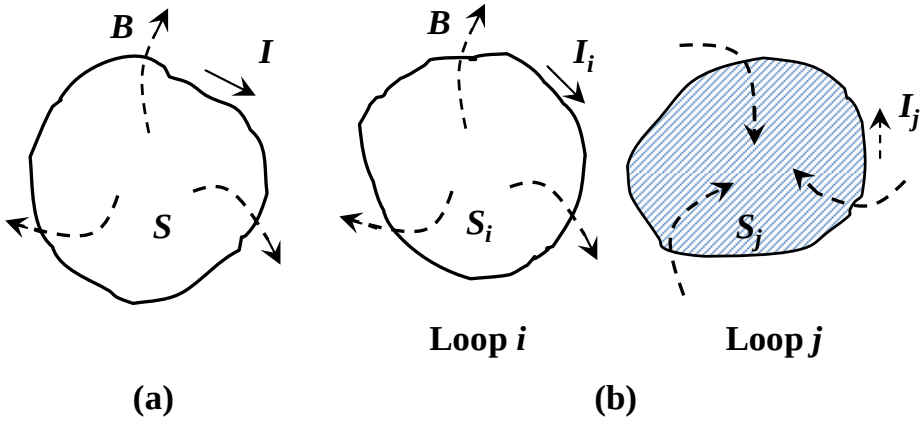


Figure 2.2: (a) An isolated current loop. (b) A magnetically coupled pair of loops. Current only flows in Loop *i*. It is magnetically linked with Loop *j*. S_i and S_j are the area of the Loop *i* and Loop *j*, respectively.

2.2.2 Estimations of Performance

1) Quality Factor

The performance of a passive element is usually measured by its quality factor (*Q*-factor). A simple definition of the *Q*-factor is that it is the ratio of the total energy in a system to the energy lost per cycle [5]

$$Q = \omega \frac{energy \quad stored}{average \quad power \quad dissipated} \tag{2.7}$$

As an inductor stores magnetic energy, the *Q*-factor for spiral inductors can also be defined as the ratio of the net magnetic energy (equal to the difference between the peak magnetic energy and the peak electric energy) stored in a system to the energy lost per cycle

$$Q = \omega \frac{net \quad magnetic \quad energy \quad stored}{energy \quad lost \quad per \quad cycle}$$

$$= \omega \frac{peak \quad magnetic \quad energy - peak \quad electric \quad energy}{energy \quad lost \quad per \quad cycle} \tag{2.8}$$

In RF applications, *S*-parameters are the characteristics that we can measure directly from a sample device and they can be converted into *Y*- or *Z*- parameters easily. The *Q*-factor of on-chip inductors can be directly evaluated from the measured two-port characterization of devices, using the following expression, valid up to the self-resonating frequency of the inductor [6][34]

$$Q = \frac{imag\left(1/Y\right)}{real(1/Y)} \tag{2.9}$$

At low frequency, it is equivalent to $\omega L/R$ for inductors (L and R are the series inductance and series resistance, respectively). But at RF, it would also include parasitic effects. Energy is not only lost in the metal but also in the substrate through the parasitic capacitors. To a certain extent, Q can be interpreted as the difference between the average stored magnetic energy and average stored electric energy divided by the total energy dissipated in one signal cycle.

$$Q = \frac{2\omega \cdot \left(\left|\bar{W}_m\right| - \left|\bar{W}_E\right|\right)}{P_{\text{loss}}} \tag{2.10}$$

A typical characteristic of the quality factor of a spiral inductor versus frequency is illustrated in Figure 2.3. Due to the simplicity of its calculation, equation (2.9) is employed through out this research, which is also the most widely used definition of the *Q*-factor for spiral inductors.

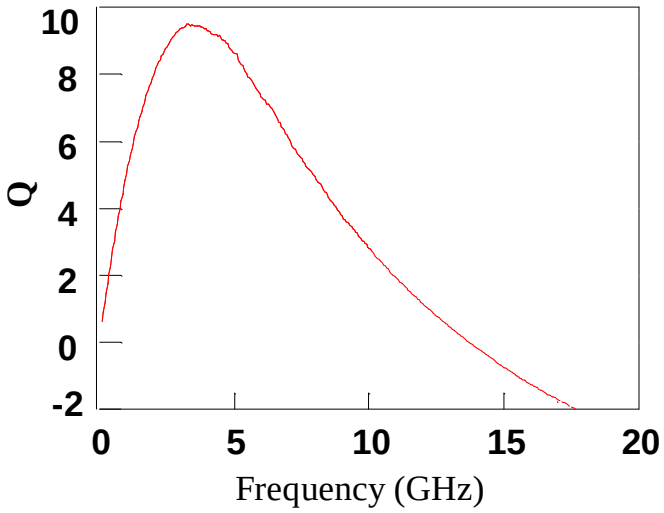


Figure 2.3: Q factor versus frequency.

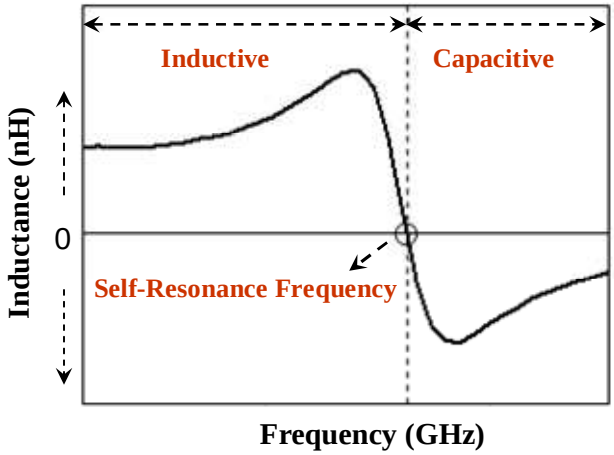


Figure 2.4: Inductance versus frequency.

2) Self-Resonance Frequency (*SRF*)

Since the spiral inductor has both inductive and capacitive behaviour, the parasitic capacitances will resonate with the inductance at a certain frequency, roughly given by [5]

$$\omega_o = \frac{1}{\sqrt{LC_{total}}} \tag{2.11}$$

where L is the inductance of the spiral inductor, C_{total} represents the parasitic capacitance of the spiral inductor. The frequency ω_o is defined as the self-resonance frequency. A typical diagram of the frequency behaviour of a spiral inductor is illustrated in Figure

2.4. At frequencies above ω_o , the inductor will look capacitive. Generally, a spiral inductor that is closer to the substrate or is larger in size has higher total parasitic capacitance and a lower self-resonant frequency.

3) Inductance and Resistance

Inductance and resistance [5] are two other important features to estimate the performance of a spiral inductor. The characteristics of the inductance and resistance of a typical on-chip spiral inductor versus frequency is illustrated in Figure 2.5 (a) and (b), respectively. In a manner similar to that for the *Q*-factor, the inductance and resistance are determined directly from the *Y*-parameters (converted from the measured *S*-parameters) as follows [34]

$$L = -\frac{imag(1/Y)}{\omega} \tag{2.12}$$

$$R = -real(\frac{1}{Y}) \tag{2.13}$$

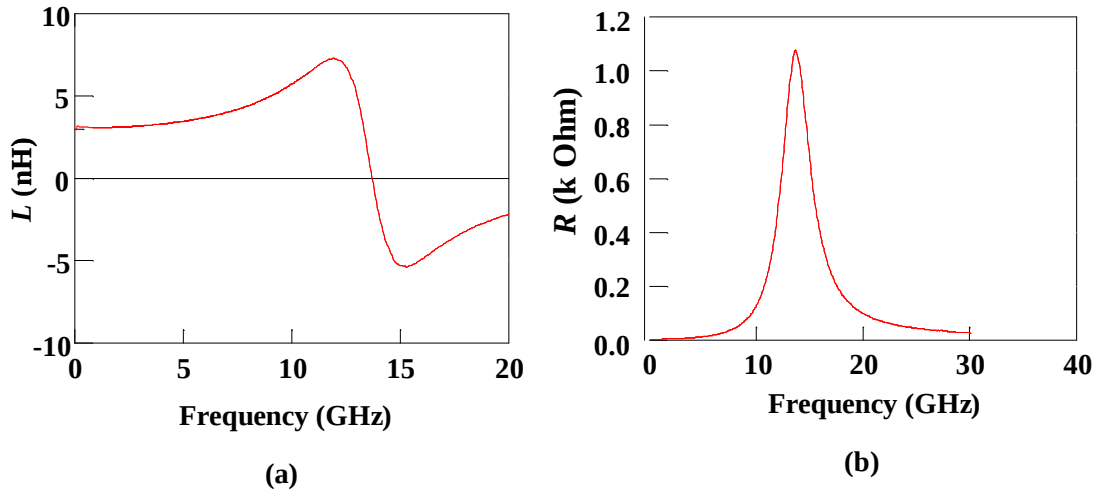


Figure 2.5: Characteristics of (a) the inductance and (b) resistance of a typical spiral inductance versus frequency

2.2.3 Overview of the Loss Mechanisms

Spiral inductors implemented on silicon substrate suffer from several loss mechanisms, leading to poor inductor quality factors. The *Q*-factor of on-chip spiral inductors is strongly dependent on the metallization and characteristics of the substrate used to build

the device. The various loss mechanisms of on-chip RF CMOS spiral inductors include skin and proximity effects, I^2R losses from eddy currents circulating below the spiral in the semiconducting substrate, from displacement currents conducted through the turn-to-substrate capacitances and the underlying substrate material, and from the primary inductor current flowing through the thin metal traces of the spiral itself [7]–[10]. They can be categorized into two groups: metal loss and substrate loss. They are briefly discussed as follows

1) Metal Loss

Spiral inductors manufactured in CMOS technologies are constructed with one or more metallization layers, typically polysilicon and aluminum layers. Since real metals always have finite conductivities, energy is lost when a current is flowing in the spiral. The conductivities of such layers play an integral part in determining the *Q*-factor of devices, which is the main limiting factor to the performance of devices at low frequencies.

In general, the DC resistance of a conductor is given by

$$R = \rho \frac{l}{A} \tag{2.14}$$

where ρ is the resistivity, l is the length and A is the conductor area.

With an increase in frequency, the current distribution in the metallization changes due to eddy currents in the metal layers, also known as skin and proximity effects, and current crowding. Since magnetic fields of the device penetrate the conductors and produce opposing electric fields within the volume of conductors, currents tend to accumulate near the skin of conductors. Thus, the effective cross-section area of the conductors decreases, and the resistance goes up at high frequencies.

The influence of the skin effect follows a $\sqrt{f}$ function dependence, which is usually evaluated by means of the skin depth δ

$$\delta = \sqrt{\frac{2}{\mu\sigma\omega}} \tag{2.15}$$

where σ is the conductivity of the conductor, μ is the magnetic permeability and ω is the angular frequency. The parameter is defined as the equivalent wall thickness of a hollow conductor having the same DC resistance as the AC resistance at the frequency of interest.

In a multi-conductor system, the magnetic field in the vicinity of a particular conductor can be considered as the sum of two terms, namely the self-magnetic field and the neighbour-magnetic field. The effects of nearby conductors thus can be attributed to proximity effects. In inductors, the proximity effect is apparent because multiple metal strips are placed close to each other and the operating frequency is high. The magnetic field in the inner area of a spiral is particularly strong. This makes the resistance higher for the inner turns.

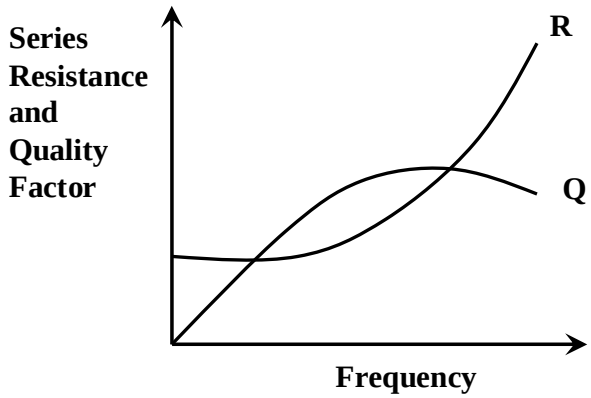


Figure 2.6: General form of resistance and *Q*-factor for a spiral with current crowding [13].

The limitation on the *Q*-factor of on-chip spiral inductors can be traced to an increase in effective resistance of the metal traces at high frequencies due to skin effect and current crowding [11], [12]. For frequencies below about 2 GHz, skin effects are relatively small in most processes since the trace metal thickness is typically less than or equal to the skin depth. Above 2 GHz, resistance increases with the growing skin effect, slowly approaching an asymptote proportional to the square root of frequency [13]. In contrast,

the proximity effect is a strong function of frequency, resulting in resistance increases at a rate that is much higher than a linear growth rate, and a function that is concave downward, as shown in Figure 2.6.

2) Substrate Induced Losses

The conducting nature of the silicon substrate is a major source of loss and frequency limitation for on-chip spiral inductor design. The silicon substrate resistivity varies from 10 kOhm-cm for lightly doped silicon to 0.001Ohm-cm for heavily doped silicon processes. The low resistivity of the substrate leads to various forms of loss, often dominating and masking the effects of the capacitive coupling and magnetic coupling. The substrate capacitive coupling can easily be understood by realizing that the top surface of silicon substrate and the bottom surface of metal layer act like the two plates of a capacitor which are separated by a dielectric. This has an adverse effect on the inductor performance because energy is stored in the electrical field of the capacitor instead of the magnetic field of the inductor. Beyond the self-resonance frequency, an on-chip inductor would act as a capacitor.

Magnetic coupling is the major loss mechanism for inductors on a silicon substrate. However, there exist other electromagnetic fields which result in losses and decrease the performance of inductors. Figure 2.7 shows a three dimensional cross-sectional view of an on-chip spiral inductor. The different possible E-field and B-field paths inside an on-chip inductor are summarized. One fundamental property of an inductor is that it generates a B-field. The B-field reaching neighboring strips ($B_1(t)$ as shown in Figure 2.7) results in skin and proximity effects. The B-field penetrates into the substrate ($B_2(t)$ as shown in Figure 2.7) inducing an eddy current. The eddy current will generate a B-field to oppose the inducing one. From the point of view of inductors, the eddy current will increase the series resistance of the spiral. Furthermore, the eddy current acts as a mirror inductor, which contributes a negative mutual inductance to the spiral inductor and consequently, reduces the total inductance.

Each of the electric field components $E_1(t)$ - $E_4(t)$ in Figure 2.7 results in the loss of

energy in the whole structure. $E_1(t)$ is the electric field along the metal trace. It is caused by the current in the winding and the finite conductivity. The current, in association with ohmic losses, causes a voltage drop along the whole winding and hence a voltage difference between each turn. This difference maintains the field denoted by $E_2(t)$ which is present between each turn. Due to the finite resistance and capacitive coupling, a leakage current flows from turn to turn. In the same manner the electric field components $E_3(t)$ and $E_4(t)$ force leakage currents from the metal traces to the oxide and ground, respectively. In addition to the described electromagnetic fields, many other high-order effects should be considered. [65]

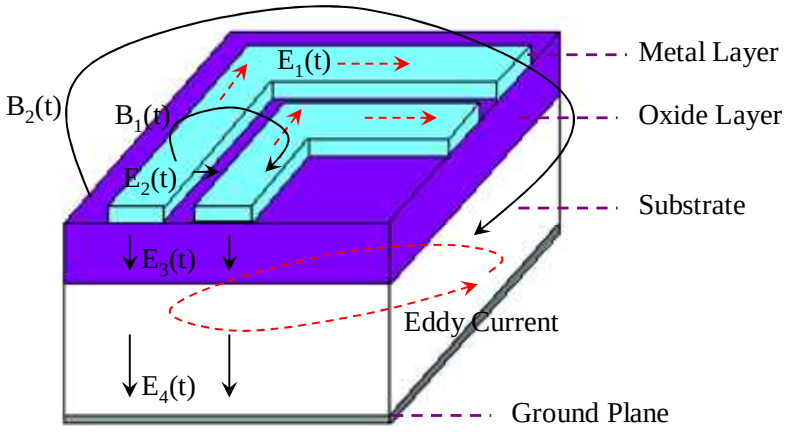


Figure 2.7: Three dimensional cross-section view of an on-chip spiral inductor showing different E-field and B-field paths.

2.2.4 Modelling

The modelling of on-chip inductors can be categorized into three groups: numerical techniques, segmented circuit models and compact models.

1) Numerical techniques

The method for modelling a distributed electrical system is to solve Maxwell's equations subject to boundary conditions. Commercial 3-D electromagnetic (EM) simulators, such as HFSS, ANSYS Multiphysics, Maxwell [14], EM-Sonnet [15], operate by solving Maxwell's equations numerically. They have been widely used to model on-chip spiral inductors. These EM simulators are suitable for accurate prediction of simple passive

structures, while they are unsuitable for simulating large three dimensional structures with multiple segments, such as spiral inductors.

On-chip spirals require a long simulation time, access to fast processors and the availability of substantial memory. As numerical techniques require both the lateral and vertical geometries be specified, considerable experience is required on the part of the user to simulate on-chip inductors. Thus, full EM field solvers are not a practical option for on-chip inductor design. Custom field solvers [16] also suffer from several drawbacks, though they can achieve faster simulation speeds by ignoring retardation effects so that magneto static and electrostatic approximations may be used to quickly solve the field matrices. The use of these tools complicates the interface between the inductor model and the circuit simulator.

The best way to incorporate numerical techniques in the design flow is to use them first to generate a library of inductor models that span a wide design space, and then link this library to the circuit simulator. Unfortunately, this requires new libraries to be generated for every process or, worse, an existing library to be updated even if only a few process parameters are changed. Another disadvantage is that each involves the transfer of simulation data from the EM simulators to the circuit simulator to achieve the optimum design. Furthermore, this approach offers no design insight about engineering trade-offs. Thus, numerical techniques are best suited to verify rather than design and optimize inductor circuits. EM simulators are generally sufficient to predict the inductance, parasitic capacitance and self-resonance frequency of a spiral inductor. However, the challenge resides in simulating the substrate induced losses without knowing the doping profile.

2) Segmented Circuit Models

Many segmented circuit models for spiral inductor modelling have been proposed. This approach entails the use of a separate equivalent circuit for each segment of a spiral inductor [17-22]. For example, a square inductor with N turns can be separated into $4N$ segments, each with a single-pi equivalent circuit model [17]. Additional terms are

needed to characterize the coupling effects between different segments and any associated bends.

A typical segmented circuit model for a single turn of a square spiral is illustrated in Figure 2.8. Four segments are used to describe the characterization of the single turn. In this model, each segment contains the self inductance, series resistance and the associated capacitances. A dependent current source is used to account for the mutual inductance between segments. The self and mutual inductances are calculated using the method proposed by Greenhouse [23]. The resistances and capacitances are determined from process parameters and frequency information.

Although simpler than a field solver, the segmented model is very bulky and complicated. Since the number of segments is determined by the product of the number of turns and the number of sides per turn, optimization of the complete circuit requires a script that can dynamically add or remove segments to the model. Thus, although it may be integrated into a circuit simulator environment, the complexity of the inductor model could easily surpass that of the remainder of the circuit, thereby compromising the speed of the circuit simulation.

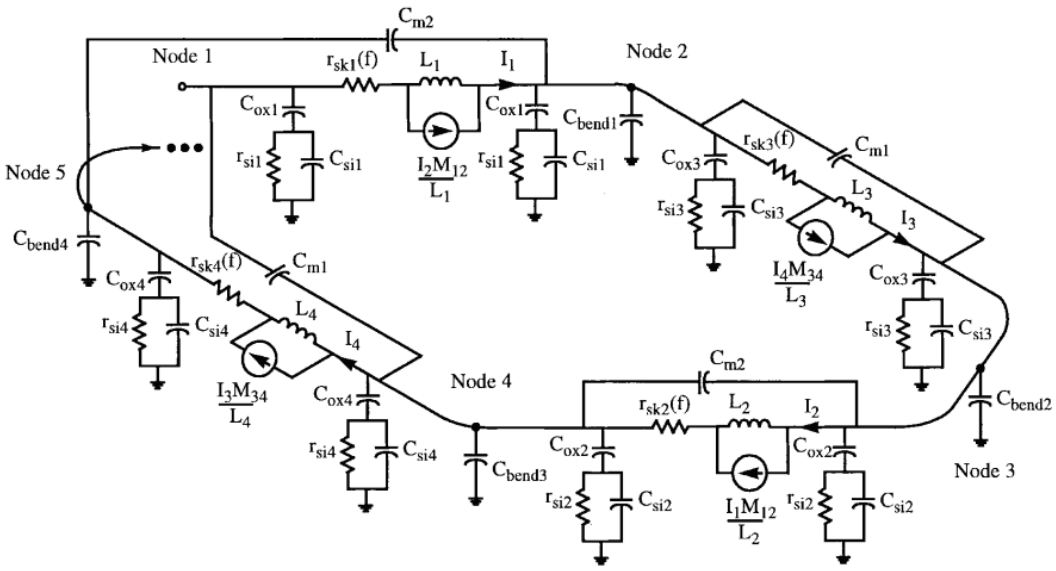


Figure 2.8: Segmented model for a single turn square spiral inductor introduced in [17].

3) Compact Equivalent Circuit Models

The disadvantages of numerical techniques and segmented circuit models indicate the need for simpler models that can be conveniently integrated into circuit simulators for design. This brought compact equivalent circuit models to the attention of CMOS RFIC designers and EDA vendors. Significant work has gone into modelling spiral inductors using such compact equivalent circuit models [24-37]. Though the accuracy of the lumped circuit approximation breaks down at higher frequencies [38] in the modelling of any distributed system, the lumped models exhibit sufficient accuracy up to the self-resonant frequency of the spiral. The speed, convenience and compactness of these lumped models make them ideal candidates for use in circuit design and optimization. It is also a common practice for a designer to build a scalable library with a limited number of devices with well characterized reliable equivalent circuit models.

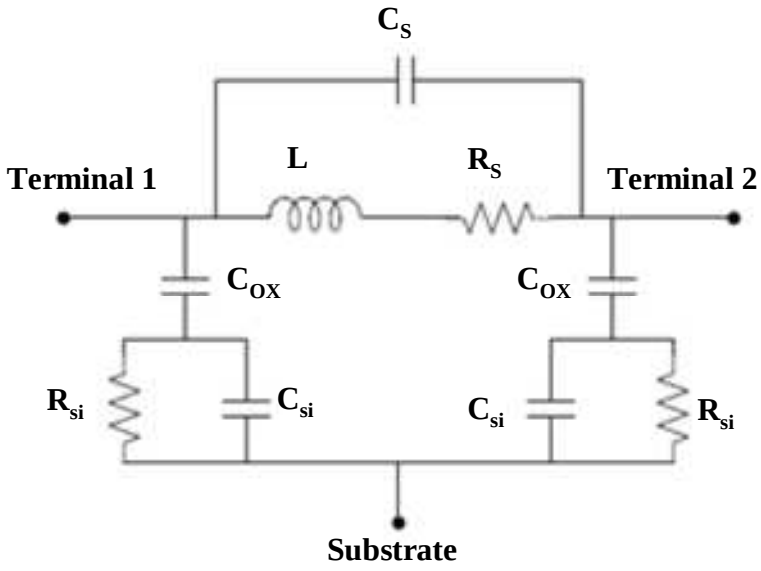


Figure 2.9: Single-pi circuit model for a spiral inductor proposed in Ref. [8]

A typical compact equivalent circuit model [8] for a spiral inductor is shown in Figure 2.9. The model includes the series inductance (L), the series resistance (R_s), the feedforward capacitance (C_s), the spiral-substrate oxide capacitance (C_{ox}), the substrate capacitance (C_{si}) and the substrate spreading resistance (R_{si}). As the topology is simple, analytical expression based methods [26, 29-31] can be used to obtain the values of model parameters in such a topology as given in Figure 2.9. All the model parameters can be directly calculated from measurements. However, this method may not be

applicable to complex topologies, as clear relationships between the model parameters and measurements can be hard to derive. Therefore, it is difficult to extract most of the model parameters from measurement analytically. These model parameters have to be determined through optimization procedures. This may lead to physically meaningless values of model parameters.

Since most of the elements used in an equivalent circuit topology are physically meaningful, the value of electrical lumped elements can also be directly calculated from the geometry and material constants of the structure. The key to accurate modelling in this way is the ability of the model equations to describe the behaviour of the inductance and the parasitic effects precisely. Each lumped element of the model should be consistent with the physical phenomena occurring in the part of structure it represents. And each model equation for the model element calculation should have high accuracy to describe the corresponding physical effect. As accurate process parameters are hard to obtain (depend on foundries), approximations and assumptions should be used in model equation derivation, and the values of model elements calculated by using the model equations can only be treated as initial values. An optimization procedure is generally needed to achieve better agreement between the measured and simulated results. In this work, the method will be studied and applied to building model libraries for asymmetric and symmetric spiral inductors manufactured in a SiGe BiCMOS technology based on a scalable double-π model topology.

Here is an example as follows, which gives physical expressions to initially determine the model elements of the model illustrated in Figure 2.9.

L: The series inductance *L* consists of the inductance of spiral coils (L_{spiral}) and the extending metal lines (L_{extend}). They are calculated according to the dc inductance [66]

$$L_{\text{spiral}} = b\, d_{\text{out}}^{a_1} W^{a_2} d_{\text{avg}}^{a_3} N^{a_4} S^{a_5} \tag{2.16}$$

$$L_{\text{extend}} = 2l_3\left[\ln\frac{2l_3}{W+t} + 0.50049 + \frac{W+t}{3l_3}\right]\times 10^{-7} \tag{2.17}$$

$$L = L_{\text{spiral}} + L_{\text{extend}} \tag{2.18}$$

The coefficients β and α_1, α_2, α_3, α_4, α_5 are dependent on the fabrication process. These are further tuned to obtain an optimal fit between the extracted values and scalable model. d_{out} is the outer diameter of the coil, t is the thickness of the conductor, d_{avg} is the average of the inner and the outer diameters, and l_3 is the total length of extending lines. W, t, S, d_{out}, d_{avg} and l_3 are in m, and L_{spiral}, L_{extend} and L are in H. N is the number of turns.

R_S: The series resistance of the spiral is given by

$$R_S \approx \frac{l}{\sigma W \delta\left(1-e^{-t/\delta}\right)} \tag{2.19}$$

where σ is the conductivity, l refers to the length of the spiral, and t is the turn thickness, δ is the skin length, which is given by

$$\delta = \sqrt{\frac{2}{\omega\mu_0\sigma}} \tag{2.20}$$

where ω is the frequency, and μ is the magnetic permeability of free space ($\mu=4\pi 10^{-7}$ H/m). This expression models the increase in resistance with frequency due to the skin effect.

C_{ox}: The spiral-substrate oxide capacitance accounts for most of the inductor's parasitic capacitance. It is well approximated by

$$C_{\text{OX}} \approx \frac{1}{2}\frac{\varepsilon_{\text{OX}}}{t_{\text{OX}}} lW \tag{2.21}$$

where ε_{OX} is the oxide permittivity (3.45×10^{-13} F/cm) and t_{OX} is the oxide thickness between the spiral and the substrate.

C_S: This capacitance is mainly due to the capacitance between the spiral and the metal underpass required to connect the inner end of the spiral inductor to external circuitry. It is modeled by

$$C_S \approx \frac{\varepsilon_{OX}}{t_{OX,M1\text{-}M2}} nW^2 \tag{2.22}$$

where $t_{OX,M1\text{-}M2}$ is the oxide thickness between the spiral and the underpass.

C_{si}: The substrate capacitance is given by

$$C_{si} \approx \frac{1}{2} C_{sub} lW \tag{2.23}$$

where C_{sub} is the substrate capacitance per unit area. Since the substrate impedance is difficult to model, C_{sub} is generally treated as a fitting parameter that is constant for a given substrate and distance between the spiral and the substrate.

R_{si}: The substrate resistance can be expressed as

$$R_{si} \approx \frac{2}{G_{sub} lW} \tag{2.24}$$

where G_{sub} is the substrate conductance per unit area. Since the substrate impedance is difficult to model, G_{sub} is generally treated as a fitting parameter. It is also constant for a given substrate material and distance between the spiral and the substrate.

2.3 RF-MOSFET and Compact Modelling

2.3.1 RF-MOSFET

The idea of the depletion mode MOSFET and the notion of the inversion-mode

MOSFET were proposed by Lilienfeld in 1928 [39] and Heil in 1935 [40], respectively. However, the first MOSFET was not fabricated until 1960 by Kahng and Atalla [41, 42] because of the technical difficulties to obtain a good oxide and the lack of basic semiconductor notions. Kahng and Atalla presented the first successful realization of a silicon inversion-channel MOSFET using thermally grown oxide for the gate insulator. Three years later, the MOSFET dramatically increased its importance when Wanlass and Sah invented the CMOS circuit [43–45]. Due to their compactness and low power dissipation, MOSFETs have been the most widely used semiconductor device since the 1980s.

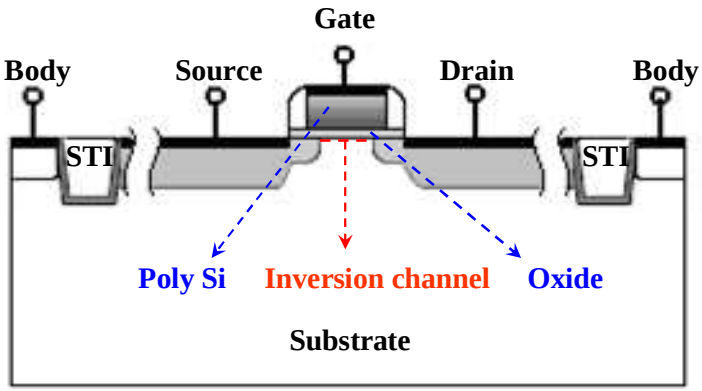


Figure 2.10: Schematic of a typical bulk MOSFET structure in CMOS technology.

The basic structure of MOSFETs is shown in Figure 2.10, consisting of a single gate, a semiconducting substrate, and heavily doped source and drain regions. The gate contact is separated from the channel by an insulating silicon dioxide (SiO2) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of a *p*- type substrate (*n*-channel device) or holes in the case of an *n*- type substrate (*p*- channel device), induced in the semiconductor at the silicon-insulator interface by the voltage applied to the gate electrode. The electrons enter and exit the channel at *n*+ source and drain contacts in the case of an *n*- channel MOSFET, and at *p*+ contacts in the case of a *p*- channel MOSFET. The structure has not changed much in the past 20 years [46]. Only the dimensions and other features have been scaled down continuously to meet the demands of higher speed and increased compactness.

For RF applications, an important measure of a transistor is the cutoff frequency f_t. This is the frequency at which the small signal current gain h_{21} of the transistor rolls off to unity (i.e. 0 dB). For today's 65 nm gate-length MOSFETs, the cutoff frequency can reach 250 GHz [47]. Applying a frequently used rule of thumb that the cutoff frequency should be around 10 times the transistor's operating frequency, one could use these devices to design integrated circuits operating up to 20 GHz which is high enough for most of the applications in modern RF electronics.

Besides f_t, other figures of merit have to be considered for a good RF-MOSFET. For example, the maximum oscillation frequency f_{max} is often desirable, which is the frequency when the transistor's unilateral power gain rolls off to unity (i.e. 0 dB),. the minimum noise figure NF_{min}, the third order intercept voltage point ip3 and the thermal noise current i_d^2 are all critical for RF noise and power applications, respectively.

The performance parameters mentioned above can be simply calculated as follows [48, 49]

$$f_t = \frac{1}{2\pi} \frac{g_m}{C_{gg} + C_{par} + C_{gso} + C_{gdo}} \tag{2.25}$$

$$f_{max} = \frac{1}{2\sqrt{\left(R_g + R_i\right)\left(g_{ds} + 2\pi f_t C_{gdo}\right)}} \tag{2.26}$$

$$NF_{min} = 1 + K \frac{f}{f_t} \sqrt{g_m \left(R_g + R_i + R_s\right)} \tag{2.27}$$

$$V_{ip3} = \sqrt{\frac{24 g_m}{g_m''}} \tag{2.28}$$

$$\overline{i_d^2} = 4KT\gamma g_{d0}\Delta f \tag{2.29}$$

where K is the boltzmann's constant, g_m is the transconductance, g_m'' is the 2nd-order derivative of g_m versus gate bias. g_{ds} is the output conductance. The capacitances C_{gg}, C_{par},

C_{gso} and C_{gdo} are the intrinsic input capacitances, the parasitic gate-bulk capacitance and the gate-source and gate-drain overlap capacitances. R_g and R_i are the gate resistance and the real part of the input impedance due to non-quasistatic effects, respectively. R_s is the source resistance.

2.3.2 RF-MOSFET Modelling

In most of the commercially available circuit simulators, the MOS transistor models have originally been developed for digital and low-frequency analog circuit design, which focus on the DC drain current, conductance, and intrinsic charge/capacitance behaviour up to the megahertz range. However, as the operating frequency increases to the gigahertz range, the importance of the extrinsic components rivals that of the intrinsic counterparts. Therefore, an RF model considering the high frequency (HF) behaviour of both intrinsic and extrinsic components in MOSFETs is extremely important to achieve accurate and predictive results in the simulation of a designed circuit.

As shown in Figure 2.11, a four terminal MOSFET can be divided into two portions [50]: intrinsic part and extrinsic part. The extrinsic part consists of all the parasitic components, such as the gate resistance R_G, gate/source overlap capacitance C_{GSO}, gate/drain overlap capacitance C_{GDO}, gate/bulk overlap capacitance C_{GBO}, source series resistance R_S, drain series resistance R_D, source/bulk junction diode D_{SB}, drain/bulk junction diode D_{DB}, and substrate resistances R_{SB}, R_{DB}, and R_{DSB}. The intrinsic part is the core of the device without those parasitics. Even though it would be desirable to design and fabricate MOSFETs without those parasitics, they are inevitable in reality. Some of them may be unnoticeable in DC and low-frequency operation. For example, the impedance of the junction capacitance is so large that the substrate impedance may not be seen from the drain terminal at low frequencies. However, the distributed *R–C* network (composed of the depletion capacitances and the substrate resistances) and the ac current flowing through this *R–C* network will influence the device performance at HF significantly.

An effective modelling approach for RF applications is to build sub-circuits based on the intrinsic MOSFET models that have been well established for DC and analog applications. This approach commonly makes use of a commercially available MOSFET model core, such as BSIM from UC Berkeley [51], MOS models from Philips Laboratories [52], and EKV model [53]. By adding lumped element extensions, the HF behaviour of devices is captured. In other words, the core model and lumped element extensions compose an equivalent circuit representing an RF-MOSFET. One of these lumped components is the gate resistance, which consists of the distributed gate electrode resistance as well as the non-quasistatic element. The effect of substrate should also be incorporated into the model by using lumped components. Figure 2.12 shows a RF MOS model [54] consisting of the gate resistance and the sub-circuit (two capacitances and five resistances) accounting for the effect of the substrate.

For simulation, the model parameters are needed, which are determined by extraction techniques based on measured data of devices at different bias conditions and frequencies. Usually, parameters of the core model are extracted with DC *I-V* and low-frequency *C–V* measurements using the same procedures available in the commercial model. The extraction of the extrinsic elements is then carried out using measured *S*-parameters at given DC bias conditions. By terminating the port with a cable of characteristic impedance (50 Ω), the *S*-parameter technique measures power waves propagating into and being reflected by the device, which is the easiest and the most reliable way to characterize high-frequency networks. For RF-MOSFETs, two-port configured test structures, with the gate terminal serving as port one, the drain terminal serving as port two and the source shorted to the substrate serving as the common terminal [55]–[58], are commonly employed to capture the characteristics of devices at high-frequencies.

The macro-modelling approach discussed above provides a useful compromise between accuracy and efficiency. These models, accompanied by appropriate parameter extraction processes, show fairly good agreement with measured RF data. However, this

approach cannot overcome some of the limitations inherited in the MOSFET core model. For example, g_m and g_{ds} predicted by commercial models are not yet sufficiently accurate, which is especially troublesome for RF circuit simulation where the higher order derivatives of the current should be smooth and correct. There are also errors in predicting the intrinsic *C–V* characteristics of short-channel MOSFETs. Moreover, scalable models for the added lumped elements are needed for the whole model to be scalable and predictive [50].

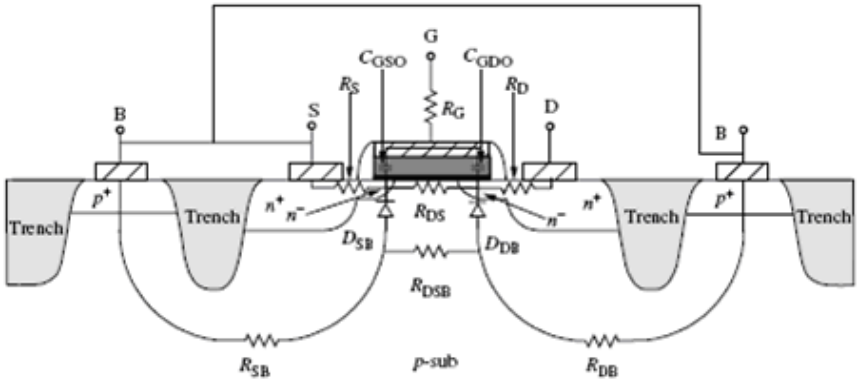


Figure 2.11: A MOSFET schematic cross section view with parasitic components. Reproduced from Ref. [50].Cheng *et al*. (2000b) MOSFET modelling for circuit design, 2000 Third IEEE international caracas conference on device, Circuits and Systems, D23/1-8.

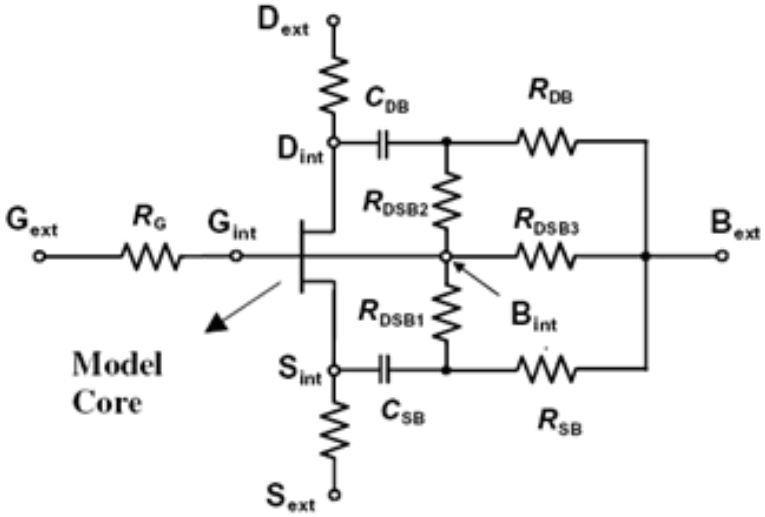


Figure 2.12: Four-terminal RF-MOSFET model based on the DC model core. Reproduced from Ref. [54]

2.3.3 Philips Surface Potential (PSP) MOSFET Model [59-62]

The PSP model is the advanced compact model jointly developed by Arizona State University (formerly at the Pennsylvania State University) and Philips Research and selected by the Compact Modeling Council as a new standard MOSFET model for the next generation of MOSFETs. PSP is a surface-potential based MOS Model, containing all relevant physical effects (mobility reduction, velocity saturation, gate current, lateral doping gradient effects, stress, etc.) to model current and upcoming deep-submicron bulk CMOS technologies. The source/drain junction model is fully integrated in PSP. PSP gives an accurate description of currents, charges and their first order derivatives (i.e. trans-conductance, conductance and capacitances). It also gives accurate higher order derivatives resulting in an accurate description of electrical distortion behavior. The latter is especially important for analog and RF circuit design. The detailed description of the theory and modeling techniques used in the model can be found in Ref. [59][60].

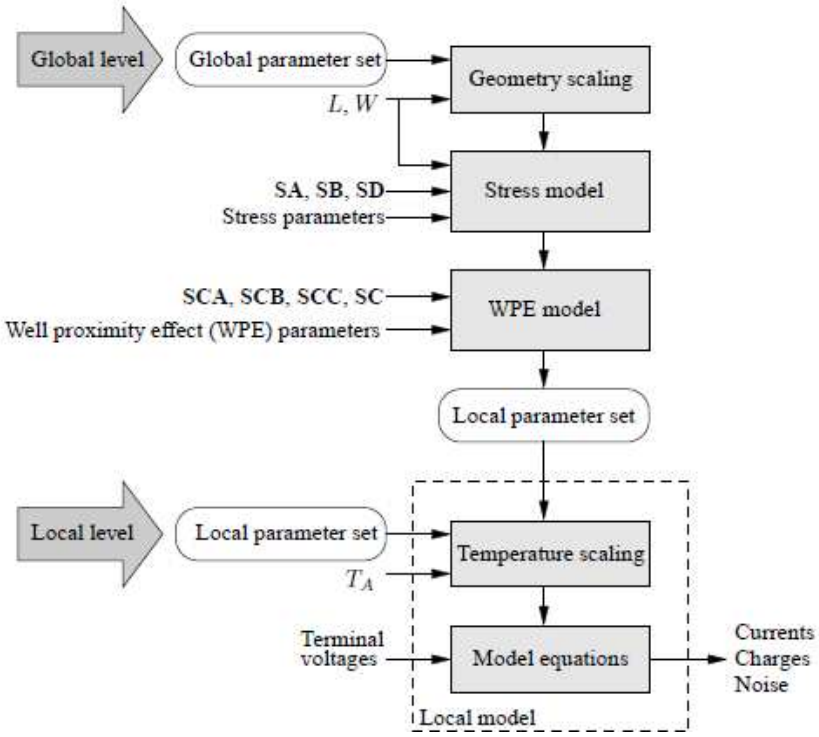


Figure 2.13: Simplified schematic overview of PSP's hierarchical structure. Reproduced from Ref. [61]

For industry application, the PSP model as defined has a hierarchical structure, similar to

that of MOS Model 11 and SP. This means that there is a strict separation of the geometry scaling in the global model and the model equations in the local model. As a consequence, PSP can be used at either one of two levels.

•**Global level:** One uses a global parameter set, which describes a whole geometry range. Combined with instance parameters (such as L and W), a local parameter set is internally generated and further processed at the local level in exactly the same way as a custom-made local parameter set.

• **Local level:** One uses a custom-made local parameter set to simulate a transistor with a specific geometry. Temperature scaling is included at this level.

The model structure described above is schematically depicted in Figure 2.13.

In the thesis, the Local Level model core is employed for DNW RF MOSFET modeling. The local model parameter set and the model core parameter extraction procedure can be found in Ref. [61].

2.4 Two-Port Measurement and De-embedding

2.4.1 Two-port Measurement

Compact modelling and characterization based on an equivalent circuit, always involve expensive setups (such as a network analyzer, high-frequency probe station and probes) and a tedious calibration and de-embedding process. As it is easier to measure the voltage or current with open or short circuits, electrical characteristics of low-frequency electronic devices are typically done by measurement of voltage, current and the phase angle between them. However, at RF, voltage and current are difficult to define and measure. High frequency characterizations are usually done by using scattering parameters (*S*-parameters) measurements. Figure 2.14 gives a two-port network for *S*-parameters, and (2.30)–(2.35) are the equations describing the network [63].

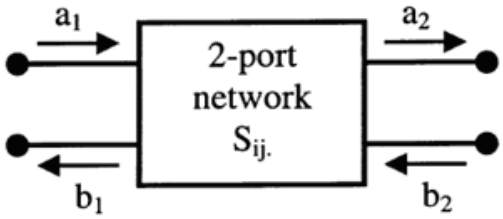


Figure 2.14: A two port network illustrating S-parameters measurement

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{2.30}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2.31}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{2.32}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a1=0} \tag{2.33}$$

$$b_1 = s_{11}a_1 + s_{12}a_2 \tag{2.34}$$

$$b_2 = s_{22}a_2 + s_{21}a_1 \tag{2.35}$$

where a_1 and a_2 are the incident electromagnetic waves at port 1 and port 2, respectively. b_1 and b_2 are the reflected electromagnetic waves from port 1 and port 2, respectively. s_{11} and s_{22} are the input and output reflection coefficients, and s_{21} and s_{12} are forward and reverse transmission coefficients, respectively.

The measurement setup consists of an Agilent E-8363B network analyzer (50MHz to 40GHz), an Agilent 4156C precision semiconductor parameter analyzer which provides bias, a probe station and ground-signal-ground (GSG) microprobes from Cascade Microtech.

2.4.2 Calibration and De-embedding

Typically, the measurement reference planes are defined by means of a standard calibration using methods such as short-open-load-thru (SOLT), line-reflect-reflect-match (LRRM) and thru- reflect-line (TRL). As GSG probes were used, corresponding PADs, interconnects between the PADs and the device-under-test (DUT), and ground ring structures were fabricated along with the DUT. It is often impossible to set the reference planes directly at the measured devices for on-wafer measurements. Thus, proper de-embedding techniques have to be applied to remove the impact of any error network between the calibration reference plane and the DUTs.

In this work, Impedance Standard Substrate (ISS) from Cascade Microtech and SOLT procedures were given priority to calibrate the whole setup. For on wafer testing, test PADs were designed. As for the corresponding GSG probes, the distance between neighboring probe tips is 100 μm and the designed PAD size is 75 μm×75 μm. In order to reveal the true performance of the DUTs, the parasitics associated with the probe structures are subtracted from the readings obtained by applying the OPEN + SHORT de-embedding technique [64] to devices.

S-parameters can be converted into *Y*- and *Z*-parameters in CAD tools or by equations [63] as follows

$$Y_{11} = \frac{1}{Z_0}\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{2.36}$$

$$Y_{12} = \frac{1}{Z_0}\frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{2.37}$$

$$Y_{21} = \frac{1}{Z_0}\frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{2.38}$$

$$Y_{22} = \frac{1}{Z_0}\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{2.39}$$

$$Z_{11} = Z_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \tag{2.40}$$

$$Z_{12} = Z_0\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \tag{2.41}$$

$$Z_{21} = Z_0\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \tag{2.42}$$

$$Z_{22} = Z_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \tag{2.43}$$

Figure 2.15: depicts a typical test structure for MOSFETs and the equivalent circuit of the whole test structure. In Figure 2.15, C_{12}, C_{23}, and C_{13} represent the parallel capacitive parasitics, while the inductors L_1, L_2, and L_3 represent the series parasitic components introduced by the test structure. The OPEN and SHORT test structures and their equivalent circuits are given in the Figure 2.16 and Figure 2.17 respectively.

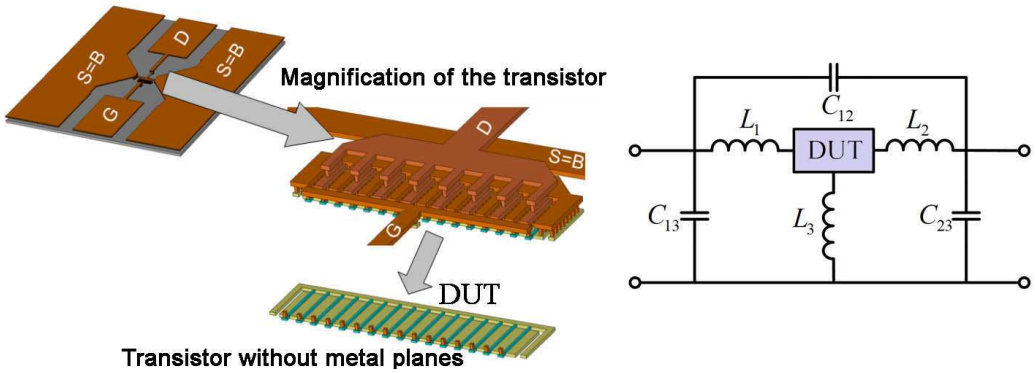


Figure 2.15: The whole test structure and its equivalent circuit.

According to the equivalent circuit of the OPEN test structure given in Figure 2.16, the *Y*-parameters of parallel parasitic components Y_{parallel} can be calculated by

$$Y_{parallel} = Y_{\text{OPEN}} = \begin{pmatrix} j\omega(C_{13}+C_{12}) & -j\omega C_{12} \\ -j\omega C_{12} & j\omega(C_{12}+C_{23}) \end{pmatrix} \tag{2.44}$$

where Y_{OPEN} is the Y-parameter matrix of the OPEN test structures.

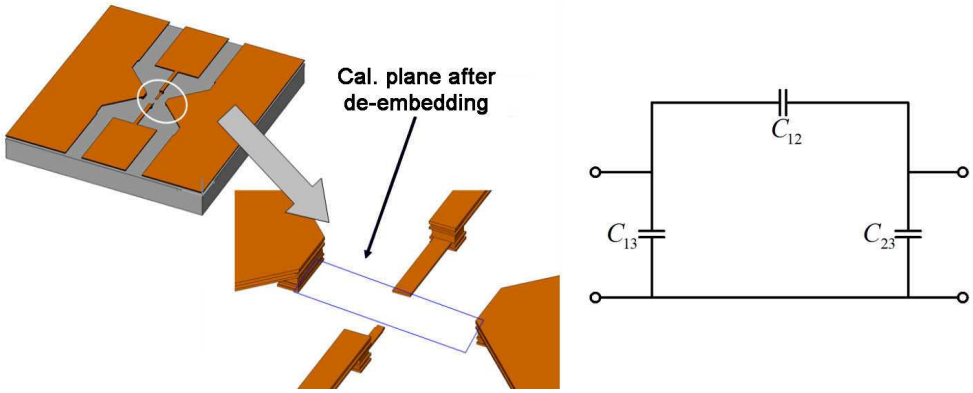


Figure 2.16: The OPEN test structure and its equivalent circuit.

According to the equivalent circuits of the short test structures shown in Figure 2.17, the Z-parameters of series parasitic components Z_{series} can be calculated by

$$Z_{\text{series}} = Z_{\text{SHORT}} - Z_{\text{OPEN}} = \begin{pmatrix} j\omega(L_1+L_3) & j\omega L_3 \\ j\omega L_3 & j\omega(L_2+L_3) \end{pmatrix} \tag{2.45}$$

where Z_{OPEN} is the Z-parameter of the OPEN test structures, Z_{SHORT} is the Z-parameter matrix of the SHORT test structures.

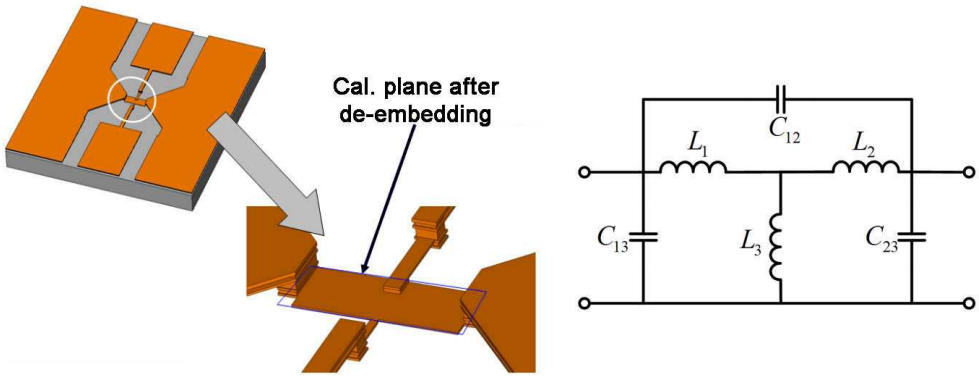


Figure 2.17: The SHORT test structure and its equivalent circuit.

The deembedding steps are depicted in Figure 2.18. Firstly, transform the measured

S-parameters of the DUT to *Y*-parameters Y_{TOTAL}, because a *Y* matrix represents a π structure of components. A simple subtraction will deembed the parallel parasitic components.

$$Y_{\text{deembed parallel}} = Y_{\text{TOTAL}} - Y_{\text{parallel}} \tag{2.46}$$

Now, the "outer" parasitic components are the three inductors, which are in series with the DUT. As series parasitics can be easily eliminated by subtracting a *Z* matrix, the pure *Z*-parameters of the DUT Z_{pure} can be obtained by

$$Z_{pure} = Z_{\text{deembed parallel}} - Z_{\text{series}} \tag{2.47}$$

Finally, these *Z*-parameters (Z_{pure}) are transformed back into *S*-parameters which describe the performance of the "inner" DUT.

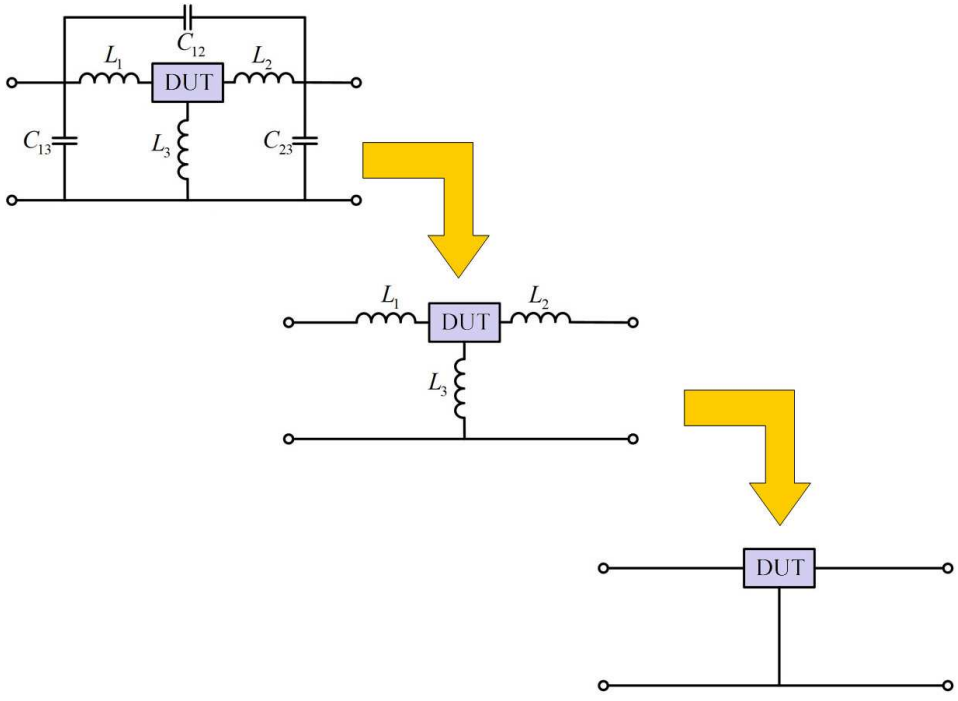


Figure 2.18: Stripping off the parasitic components gives the performance of the DUT.

2.5 Summary

The background knowledge about spiral inductors and MOSFETs and two-port

measurement techniques used in the work is described in this chapter. The commonly used inductor configuration is discussed. The key indicators for inductor characterization are introduced, including inductance, quality factor, SRF, and resistance. Then, the loss mechanisms for spiral inductors implemented on a silicon substrate are discussed, including metal loss and substrate induced losses. The approaches for inductor modelling are categorized into three groups: numerical techniques, segmented circuit models and compact models. The pros and cons of these modelling techniques are provided. The popular modelling approaches for the RF MOSFET are discussed, as well as the commercially available MOSFET model cores. Finally, the measurement, calibration and de-embedding techniques used in the work are described in detail.

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3

Modelling of On-Chip Spiral Inductors

3.1 Introduction

As a critical passive component, on-chip spiral inductors have been widely used in CMOS RFIC design such as in RF amplifiers, VCOs, mixers, filters and impedance matching circuits [1]-[5]. Therefore, an accurate equivalent circuit based model suitable for building a scalable spiral inductor library is essential for reliable circuit implementation and design optimization. Considerable research work on modelling on-chip spiral inductors has been published in recent years [6]-[19]. These methods are generally categorized into two types: numerical and compact circuit modelling techniques. Numerical techniques are generally based on EM field solvers and consequently, are time consuming. Hence, Spice-format compact models (e.g. equivalent circuit models) are preferred by the IC designers.

Most of the efforts into the development of equivalent circuit models for spiral inductors in the past years were focused on different topologies (such as the 1-π model [6]-[13], 2-π model [14]-[17], T-model [18], [19]) for accurate prediction of the characteristics of spiral inductors over a wide frequency range, for characterization of parasitic effects (skin and proximity and the capacitive and inductive coupling in the substrate), and on model parameter extraction methods (such as the measured data based analytic parameter extraction techniques, physical equation based model parameter extraction methods). Scalable models with scaling rules which can be used to describe the behaviour of spiral inductors over a complete geometry range are rarely presented.

In general, a scalable modelling procedure for inductors manufactured in a specified manufacture process is as follows – firstly, parameters are extracted for devices of various dimensions and secondly, a function is fitted to each parameter variation with the geometry. For scalable fitting, a unique parameter extraction solution and physically meaningful scaling expressions for each parameter are of the utmost importance to ensure the accuracy of the extracted scalable model. Among the reported parameter extraction approaches are the numerical optimization method, the analytic [11]-[12],

[16]-[18] and physical based [10], [13], [19] model parameter extraction techniques. The numerical optimization method is difficult to render scalable because the optimized parameters are not always unique. The availability of an analytic parameter extraction technique is strongly dependent on the complexity of the equivalent circuit used, e.g. whether every parameter can be directly determined from measurements or not. The errors introduced by the assumptions used to simplify the parameter extraction at high frequencies tend to hinder the scalability of the models. On the contrary, physics-based model parameter extraction methods are expected to be unique, benefiting from the strictly defined calculation method based on the layout and process parameters.

In this Chapter, the recent compact models proposed for RF CMOS spiral inductors are reviewed and extensively investigated in Section 3.2. The key features of these models, including 1-π models, 2-π models and T-models are analyzed in detail. By actual implementation of each model's parameter extraction procedure, the pros and cons of equivalent circuit topologies, parameter extraction techniques and fitting capacity of models are analyzed and compared by using devices manufactured on a standard 0.18 μm RF CMOS process.

2-π models have been widely employed in model library building to achieve wideband accuracy. However, an acceptable method for forming a scalable model for on-chip spiral inductors is still lacking. A physics-based 2-π equivalent circuit model suitable for on-chip spiral inductors is proposed in Section 3.3. The major parasitic effects, including the skin effect, the proximity effect, the vertical and lateral high frequency losses in the substrate and the distributed effect are analytically calculated with layout and process parameters. By using the complex effective thickness of the substrate for eddy currents flowing in the substrate, novel equations of the high frequency lateral substrate losses are proposed. A series of asymmetric, axially symmetric and centrally symmetric spiral inductors with different geometries are fabricated on a standard 0.18 μm SiGe BiCMOS process with 100 ohm/cm substrate resistivity to verify the model. Excellent agreement has been obtained between the measured results and the proposed model over a wide

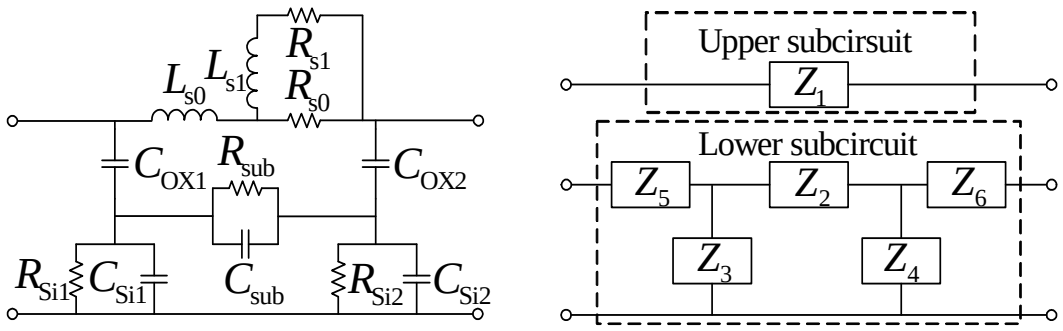
frequency range. Finally, a summary is given in Section 3.4.

3.2 Overview of Spiral Inductor Models

Inductors have frequency-dependent behaviour caused, for example, by the conductive substrate (eddy currents, capacitive coupling), and by skin and proximity effects. All of these frequency-dependent effects account for the degradation of the quality factor *Q*. This requires the elemental R-L-G-C model to be expanded to capture the frequency-dependence of the series and shunt components [20]. In addition, the measured *S*-parameters also indicate the distributed nature of metal windings and their capacitive coupling. In the past, only 2-π models were considered to be adequate for modelling distributed effects [14], [16], [17].

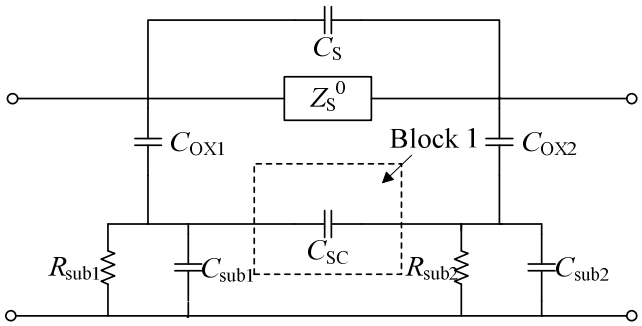
Table 3.1: Comparison of the key features of spiral inductor models. ("√" for taken into account, "×" for not taken into account)

Previous models	Topology	Element number	Analytically extracted elements	Skin effect	Proximity effect
[7]	1-π	9	9	√	×
[8]	1-π	12	12	√	√
[11]	1-π	12	11	√	√
[12]	1-π	14	3	√	√
[15]	2-π	20	20	√	√
[17]	2-π	23	23	√	√
[18]	T	13	13	×	×
[19]	T	10	8	√	×

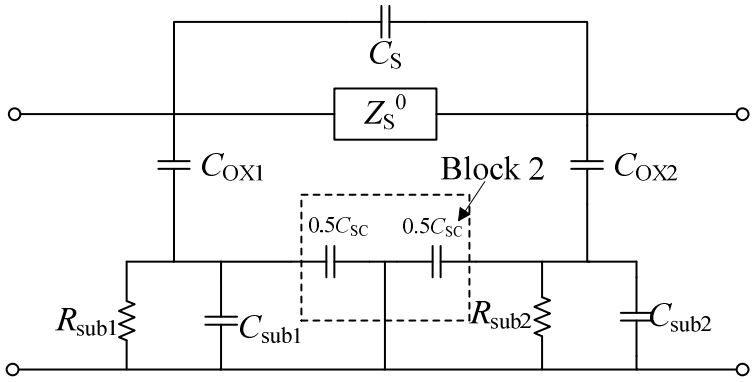


(a) (b)

Figure 3.1: (a) Equivalent circuit schematic of 1-π model [6] and [8]. (b) The lateral partition presented by [8].



(a)



(b)

Figure 3.2: Partition of the substrate coupling capacitance into two equal capacitances in the substrate branch proposed in [11].

Former parameter extraction techniques, such as those based on electromagnetic (EM) calculations [21], are normally estimated solutions and much optimizing work still needs to be done. Measurement-based parameter extraction techniques provide an alternative solution. Mathematical techniques for curve fitting, such as the genetic algorithm, particle swarm optimization, artificial neural network (ANN) and a vector fitting procedure, turn out to be resource and time consuming, and the extracted results often have poor physical meaning. Analytical extraction techniques based on network analysis, are much more efficient and capable of providing physical aspects of the inductor behaviour. In these analytical approaches, approximations that are valid at relatively low or high frequencies are usually utilized to decompose the complicated circuit model into several sub-circuits. The elements are then extracted step by step from the simplified sub-circuits. Thus, the selection of a valid frequency range for proper network partition is critical for extraction. The key features of eight models are listed in Table 3.1.

A. 1-π Model

Figure 3.1 depicts the 1-π model in [6] and [8]. L_{s0} and R_{s0} are used to model series inductance and resistance. The *L*-*R* ladder series branch formed by L_{s1} and R_{s1} in parallel with R_{s0} is used to capture the increase in the series resistance due to both skin and proximity effects at high frequency. C_{ox}, C_{si} and R_{si} represent the oxide capacitance, substrate capacitance and resistance to ground, respectively. The parallel network R_{sub} and C_{sub} is used to model the lateral substrate coupling among the spiral metal lines.

Ref. [8] proposed a novel method to determine the frequency bands quantitatively. The enhanced model was treated as a parallel combination of upper and lower sub-circuits. This lateral partition of the topology made it feasible to extract L_{s0}, R_{s0}, L_{s1} and R_{s1} directly from measured *Y*-parameters at low frequencies. Then, C_{ox1} and C_{ox2} are evaluated in an intermediate frequency range by approximating C_{sub} as behaving like an open circuit. Then C_{si1}, C_{si2}, R_{si1}, R_{si2}, R_{sub} and C_{sub} are extracted from the slopes of the linear regression of related experimental functions versus ω at higher frequencies [8]. Due to the exact frequency band determination and reasonable circuit topology approximation, the parameter extraction procedure in [8] has proven to be of high accuracy. As shown in Table 3.2, the deviation of root-mean-square (*RMS*) errors between extracted and optimized effective series resistance (*ESR*), *L* and *Q* of [8] is much smaller than in the case of [6] (In this Section, *ESR*, *L* and *Q* are calculated by the following equations, $ESR = \mathrm{Re}(-1/Y_{21})$, $L = \mathrm{Im}(1/Y_{11})/\omega$, and $Q = -\mathrm{Im}(Y_{11})/\mathrm{Re}(Y_{11})$ respectively). Note that the optimized *RMS* errors of [6] and [8] are almost the same. The reason is that they employed the same circuit model.

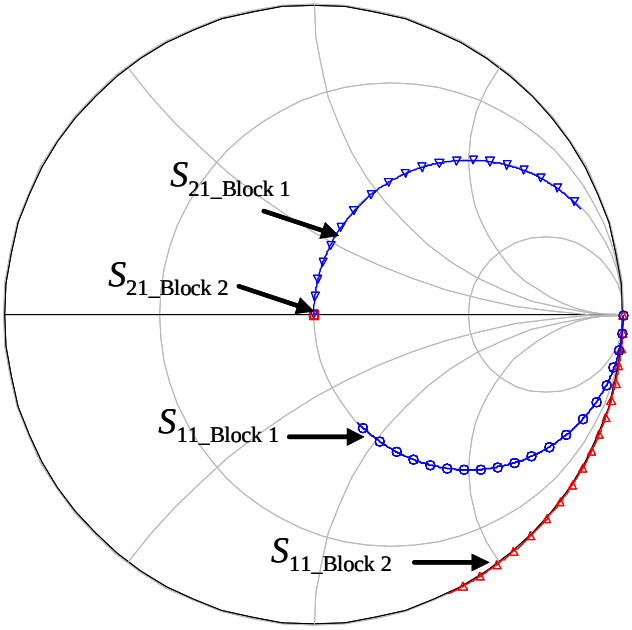


Figure 3.3: Comparison of simulated *S*-parameters between the two networks in the dashed line blocks in Figure 3.2.

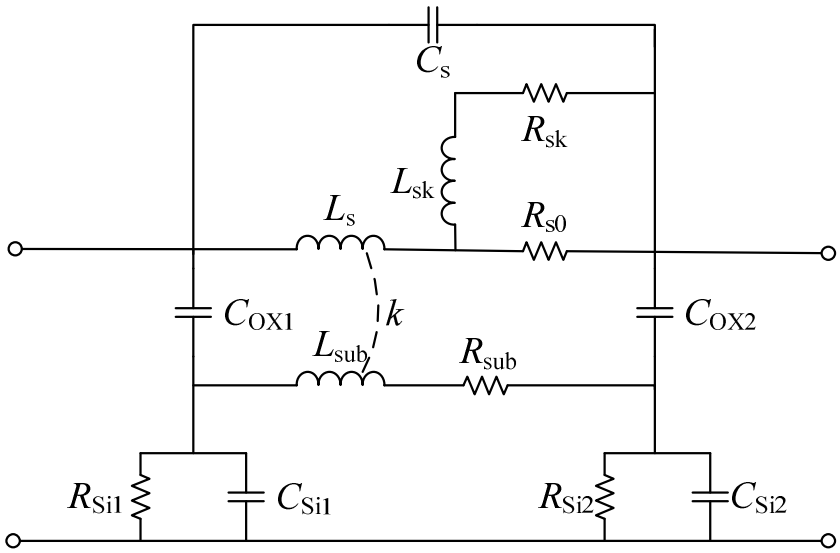


Figure 3.4: Equivalent circuit model of an inductor in [9].

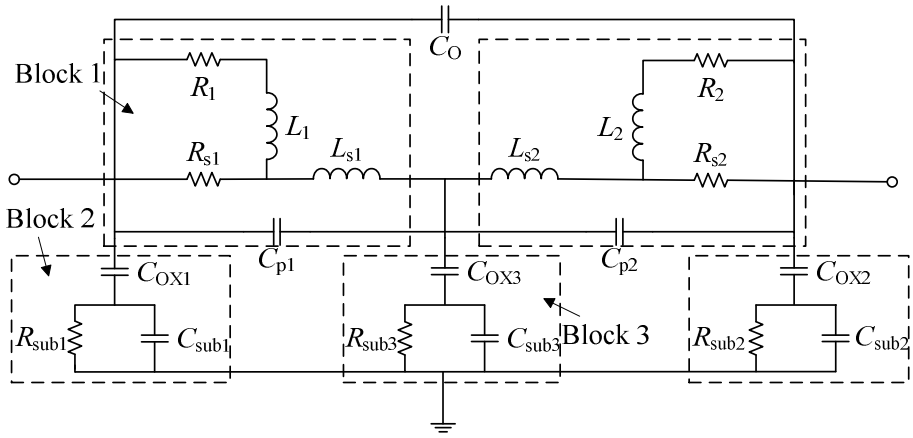


Figure 3.5: Asymmetric 2-π equivalent circuit proposed in [15].

Table 3.2: Comparison of resistance (*R*), inductance (*L*) and quality factor (*Q*) RMS (%) deviation employing parameter-extraction procedure from Ref. [6] and [8], respectively

Fabrication Parameter		[6]					
R	*N*	*ESR*		*L*		*Q*	
		Ext.	Opt.	Ext.	Opt.	Ext.	Opt.
30	2.5	24.5	6.56	30.4	7.09	25.0	8.01
30	3.5	26.1	8.67	28.2	10.3	30.5	6.55
30	4.5	30.2	13.5	32.8	5.56	42.5	7.33
30	5.5	34.7	11.6	45.2	7.28	34.3	12.7
30	6.5	33.8	13.8	42.9	9.96	39.7	11.8
		[8]					
30	2.5	21.7	7.50	18.7	6.91	15.3	7.16
30	3.5	26.8	11.7	15.3	9.51	14.2	7.73
30	4.5	19.9	10.4	13.4	4.90	10.4	5.07
30	5.5	28.7	11.1	22.5	6.55	17.5	9.90
30	6.5	29..3	14.7	23.5	8.09	15.8	10.2

In Figure 3.1, the coupling is dominated by R_{sub} at low frequencies and by C_{sub} at high frequencies. It is reasonable to eliminate R_{sub} at high-frequency measurements. During the parameter extraction process, we found that the extraction technique that partitions C_{sc} into two equal $C_{sc}/2$ segments proposed by [11] is inappropriate. To verify this, two-port *S*-parameters of the two circuits in dashed line blocks in Figure 3.2 have been simulated. According to the results shown in Figure 3.3, the small-signal characteristics are quite different. In fact, our extractions with this technique gave a minus value for C_{sub} for all of the fabricated inductors. In view of the previous discussion, it is observed that the lateral partition presented by [8] is a better solution, as depicted in Figure 3.1(b).

The model in Ref. [9] considers the lossy substrate as a current sheet and utilizes an L_{sub} and R_{sub} series branch to model lateral substrate coupling, as shown in Figure 3.4. This plays a similar role to the central grounded branch (block 3 in Figure 3.5) and consequently, has the capability to model *ESR* correctly.

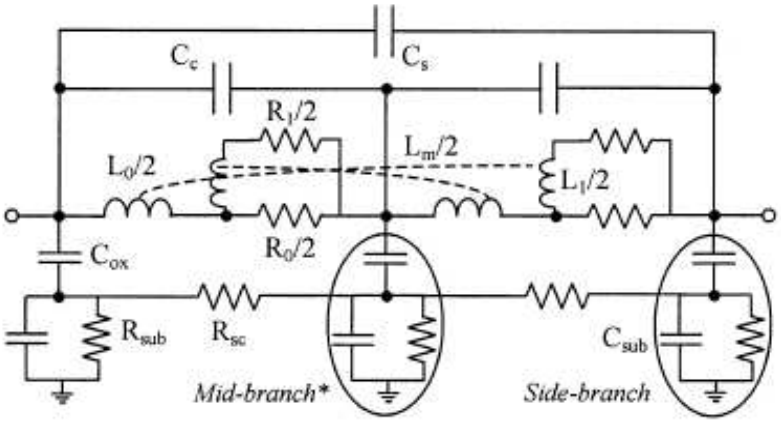


Figure 3.6: Symmetric 2-π equivalent circuit proposed in [17].

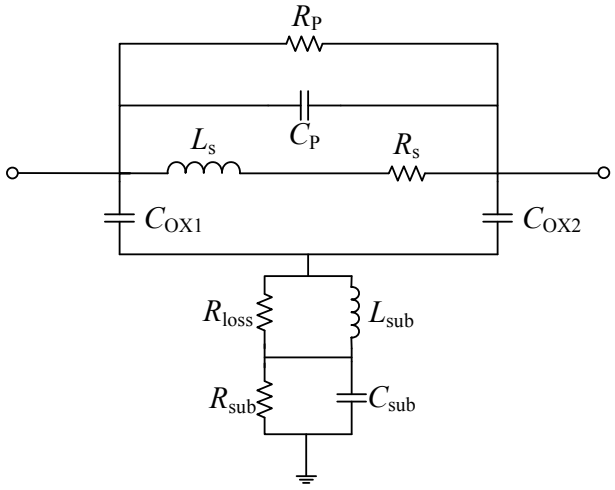


Figure 3.7: Equivalent circuit schematic of T-model [19].

B. 2-π Model

The high accuracy of 2-π models which are extended from 1-π models has long been emphasized. By adding a central grounded branch (*C-R-C* oxide-substrate three-element sub-circuit, see Block 3 in Figure 3.5), the distributed nature of spiral inductors can be well modeled [16].

Figure 3.5 presented an asymmetric 2-π model [15], to deal with the non-symmetric

inductor layouts which are the standard offering from most CMOS foundries. The skin and proximity effects are still captured by the three-element *LR* ladder series branch (Block 1 in Figure 3.5).

Another symmetric 2-π model is reported by [17]. As shown in Figure 3.6, a mutual inductance L_m is introduced to capture the inductive coupling among metal lines, which is cross coupled between the two series ladder networks. The lateral substrate coupling is modeled by C_c and R_{sc}. All element values can be analytically calculated based on the inductor layout parameters (i.e. geometric parameter). However, this analytical calculation is only an initial value evaluation, which may deviate largely from the final value after the necessary optimization.

Since there is one more node in the circuit model topology of a 2-π model than in a 1-π model, a singular point exists in complex frequency domain in the 2-π model.

C. T-Model

The T-model was first proposed by Horng *et al.* in [18] and was extensively improved by Guo *et al.* [19]. The physical reasoning that underlies the model is that the distributed spiral inductor can be viewed as a transmission line which can be modeled by a T-topology lumped element network [22]. Ref. [20] has presented a scalable model for millimeter-wave inductors and transmission lines for CMOS designs. The parameter extraction technique proposed in [18] requires the frequency locations that correspond to zeros and poles of two measured *Y*-parameter functions. However, we found that according to measured data, most of the inductors do not present these zeros and poles even with frequencies up to 40 GHz. Thus, the use of the extraction technique is limited.

Figure 3.7 shows the model proposed in [19]. The model is composed of two *RLC* networks to account for spiral coils, a lossy substrate, and their mutual interaction. All of the elements are constants independent of frequency and can be expressed in a closed form derived from circuit analysis. By introducing R_p which accounts for the spiral coil's conductor loss originating from the lossy substrate return path, the quality factor *Q* can

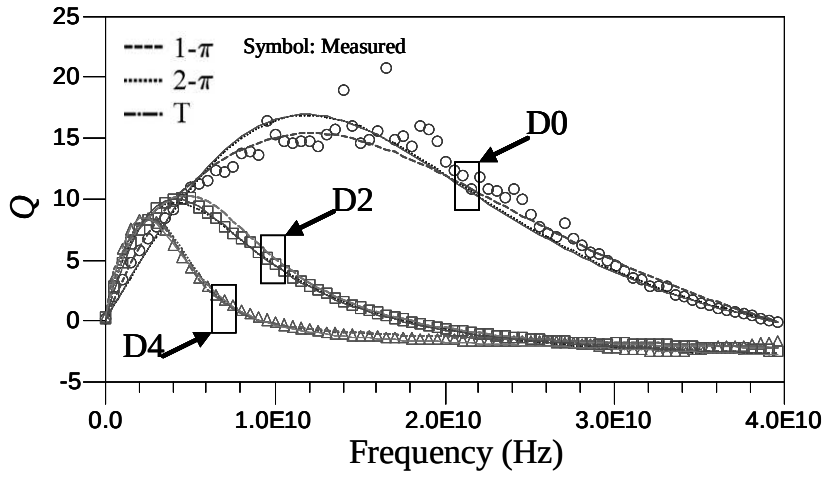
be precisely described around the peak area.

Table 3.3: Comparison of inductance (*L*) and quality factor (*Q*) RMS (%) deviation for fabricated inductors with different geometries

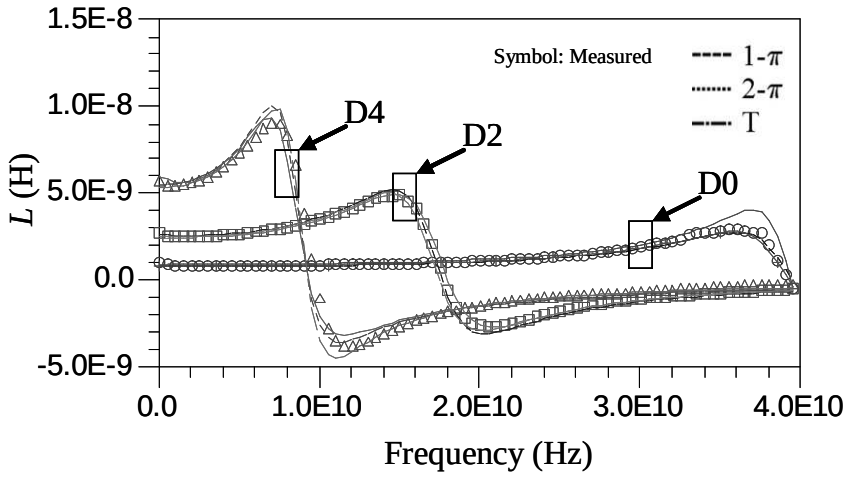
Name	Fabrication Parameter		[7]		[8]		[11]		[12]	
			1-π		1-π		1-π		1-π	
	R (Radius)	*N (Turns)*	*L*	*Q*	*L*	*Q*	*L*	*Q*	*L*	*Q*
D0	30	2.5	15.3	22.9	6.91	7.16	7.53	8.15	6.21	5.52
D1	30	3.5	16.5	21.3	9.51	7.73	12.4	11.9	10.5	8.32
D2	30	4.5	24.8	30.9	4.90	5.07	15.4	14.1	15.2	9.69
D3	30	5.5	26.5	33.2	6.55	9.90	11.2	10.5	11.5	13.2
D4	30	6.5	30.1	35.2	8.09	10.2	15.2	17.1	10.2	12.5
D5	60	2.5	12.8	23.5	6.07	5.35	5.02	6.58	8.33	7.51
D6	60	3.5	17.9	25.7	5.63	7.32	9.09	10.2	6.72	9.57
D7	60	4.5	27.6	34.1	6.58	6.46	14.5	16.8	13.7	15.3
D8	60	5.5	23.5	29.6	14.3	8.69	15.9	15.2	16.7	19.8
D9	60	6.5	35.1	39.2	13.2	12.8	17.3	19.5	18.5	26.6

Continued Table 3.3: Comparison of inductance (*L*) and quality factor (*Q*) RMS (%) deviation for fabricated inductors with different geometries

Name	Fabrication Parameter		[15]		[17]		[19]	
			2-π		2-π		T	
	R (Radius)	*N (Turns)*	*L*	*Q*	*L*	*Q*	*L*	*Q*
D0	30	2.5	3.64	5.25	8.54	7.03	10.2	8.31
D1	30	3.5	4.38	6.33	10.5	9.56	14.1	11.3
D2	30	4.5	5.02	4.11	8.65	10.3	15.3	12.4
D3	30	5.5	7.21	5.51	14.2	17.1	17.2	16.5
D4	30	6.5	9.02	9.33	16.9	19.0	20.1	18.2
D5	60	2.5	9.57	8.31	10.0	12.5	13.3	16.1
D6	60	3.5	18.9	23.0	14.3	10.7	15.8	16.2
D7	60	4.5	17.5	24.1	16.6	19.7	19.1	21.4
D8	60	5.5	30.1	29.7	28.5	25.8	25.4	25.1
D9	60	6.5	31.4	32.7	35.4	37.3	24.7	29.5


Symbol: Measured
1-π
2-π
T
D0
D2
D4
Q
Frequency (Hz)

(a)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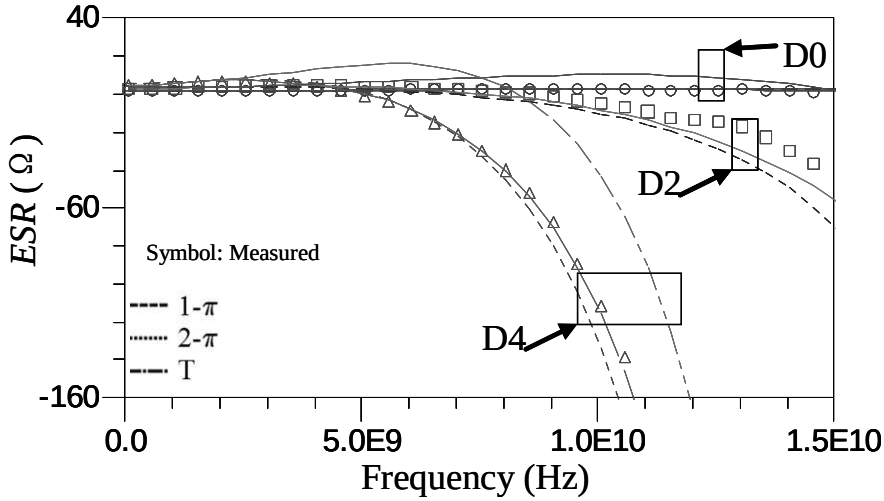
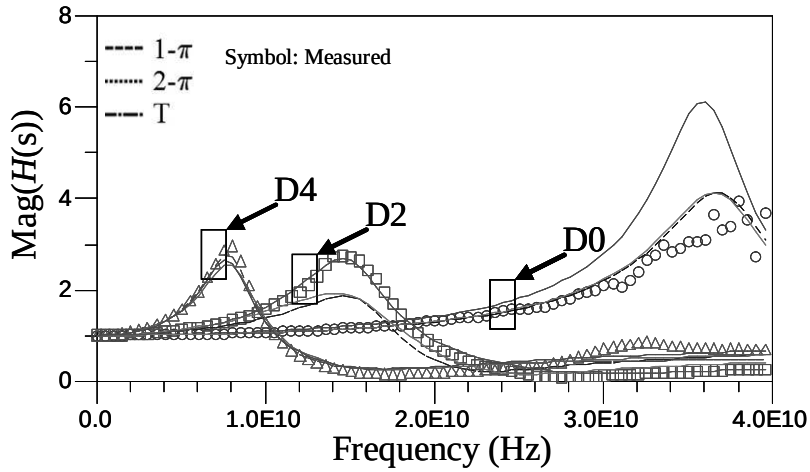
(b)


Symbol: Measured
1-π
2-π
T
D0
D2
D4
ESR (Ω)
Frequency (Hz)

(c)



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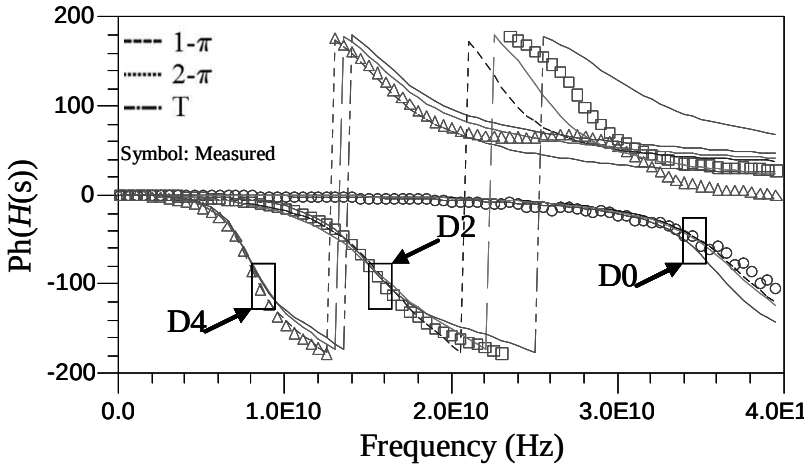


(e)

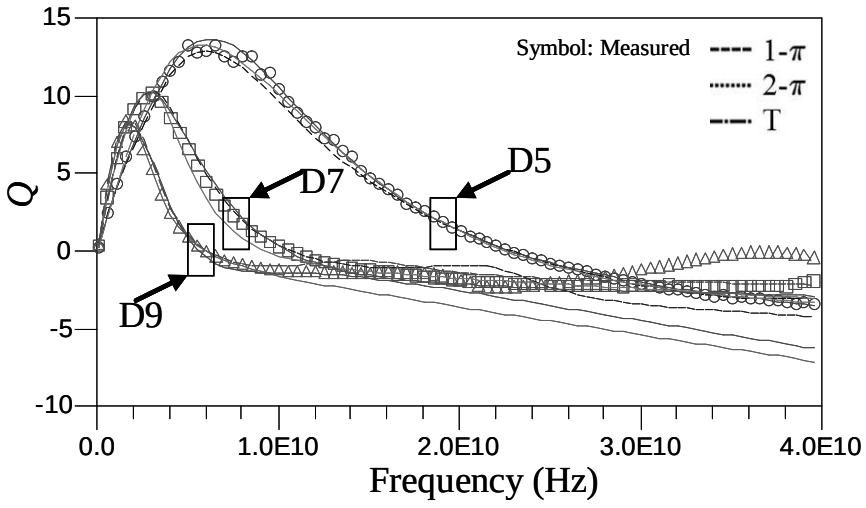
Figure 3.8: Comparisons of measured (R = 30 μm) and simulated *Q* (a), *L* (b), *ESR* (c), and *H*(*s*) (d and e) by 1-π model [8], 2-π model [15] and T-model [19].

For the verification and comparison of the analyzed models, test structures of circle spiral inductors with various geometrical configurations were fabricated using Semiconductor Manufacturing International Corporation (SMIC) 0.18μm 1P6M RF CMOS technology. In this process, the inductor's windings are made of M6 (Metal level 6). In this work, 10 spiral inductors were investigated. Two-port *S*-parameters up to 40GHz were measured by the GSG PAD using an Agilent E-8363B Network Analyzer and a CASCADE Summit probe station. The layout parameters are outlined in Table 3.3. For clarity, results for D0, D2, D4, D5, D7 and D9 as well as the simulated results from the models in [8], [15], and [19] are presented in Figure 3.8 and Figure 3.9.

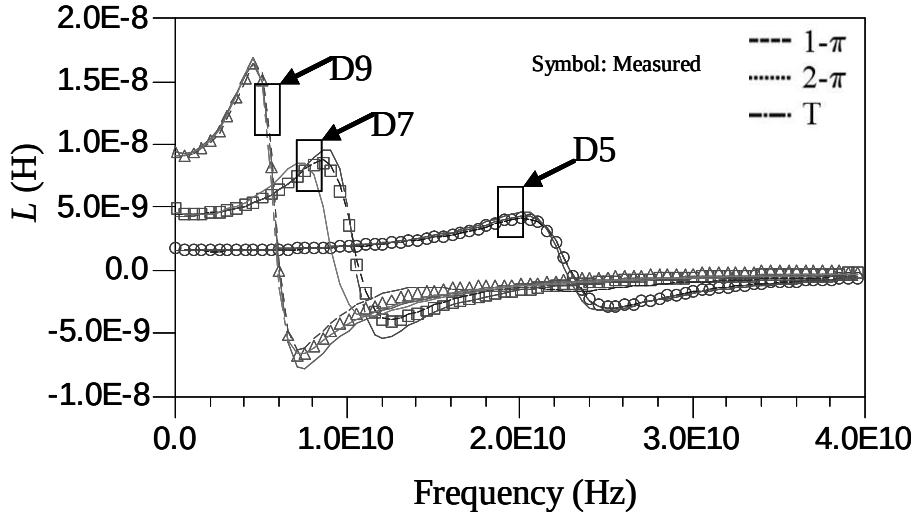
The *RMS* (%) errors in the inductance and the quality factor for the fabricated inductors with different geometries are listed in Table 3.3. It can be observed that the accuracy of 2-π models is relatively higher than the others. Note that the *RMS* errors of the D8 and D9 inductors simulated by [15] and [17] are much higher than the previous ones. This results from the singularity in the 2-π models [12]. As D8 and D9 have relatively more turns than the other measured inductors, their electromagnetic mechanisms are consequently more complicated. This may introduce a singularity to their measured *S*-parameters through electromagnetic coupling.

Figure 3.8 (a) and (b) demonstrate that all of the three models can give an exact description in the low frequency range, while for inductors with R = 60 μm, the quality factors simulated by the 1-π [8] and the 2-π [15] cannot match the measured results at high frequencies. The T-model in [19] can still follow closely with the measured results but fails to catch the hump above the *SRF*.

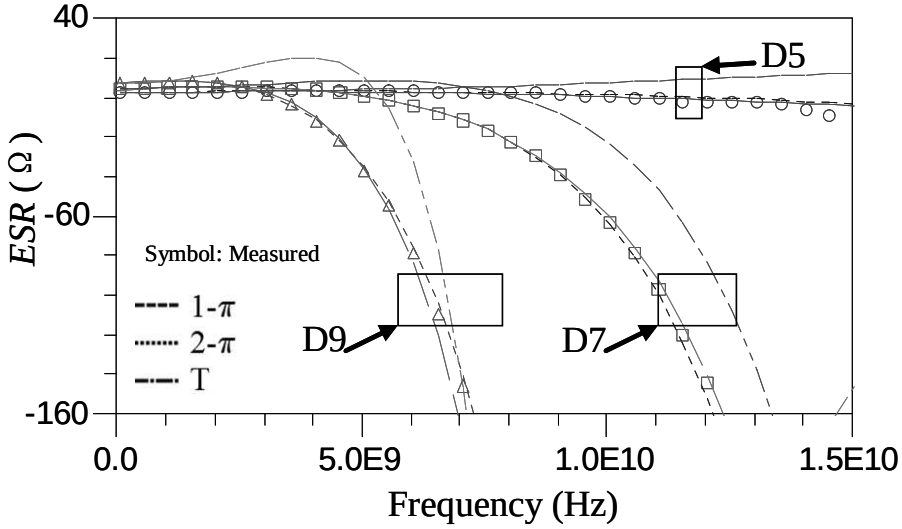
Figure 3.8 (c) and Figure 3.9 (c) show that all of the three models have the potential to model the frequency-dependent *ESR*, whereas the 1-π model and 2-π model exhibit much better fitting capacity. However, while the 2-π model has a high accuracy, its number of parameters is nearly double that of the 1-π model and T-model. These are the better solutions if efficiency and accuracy need to be taken into account simultaneously.



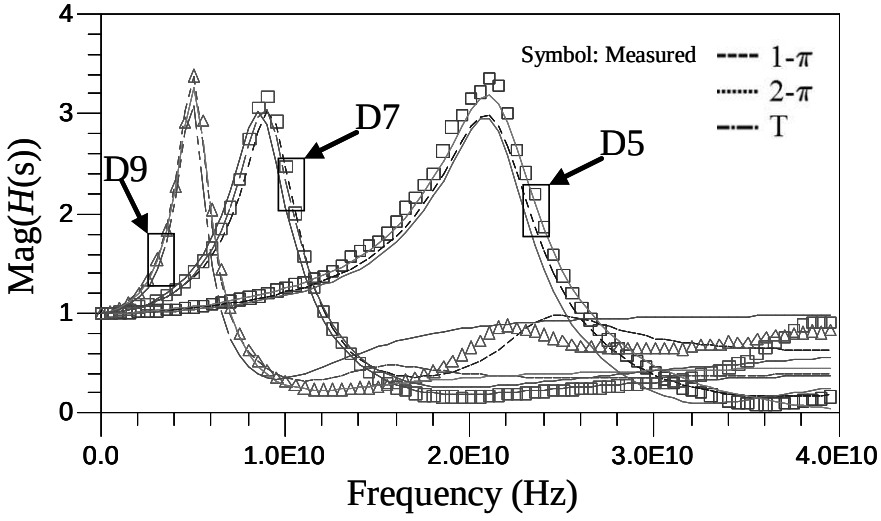
(a)


2.0E-8
1.5E-8
1.0E-8
5.0E-9
0.0
-5.0E-9
-1.0E-8
L (H)
D9
D7
D5
Symbol: Measured
1-π
2-π
T
0.0
1.0E10
2.0E10
3.0E10
4.0E10
Frequency (Hz)

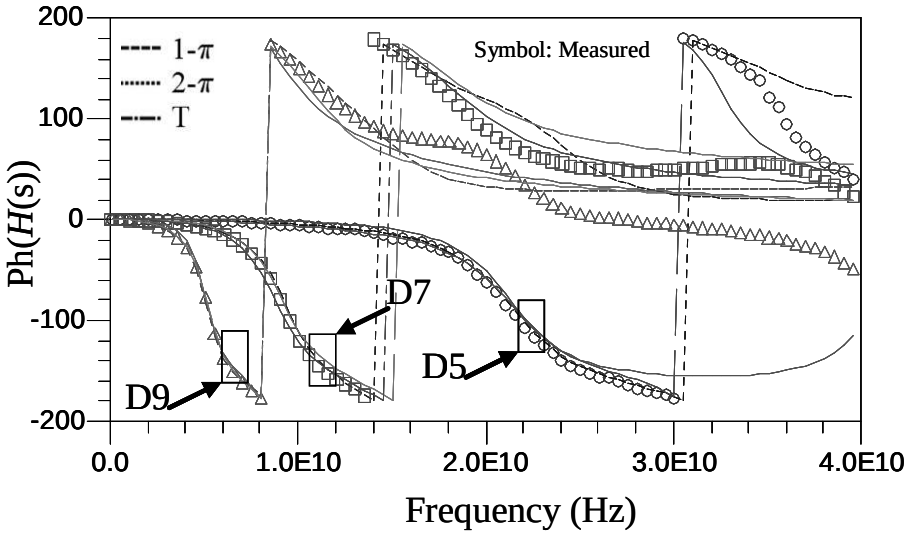
(b)


40
-60
-160
ESR (Ω)
D5
Symbol: Measured
1-π
2-π
T
D9
D7
0.0
5.0E9
1.0E10
1.5E10
Frequency (Hz)

(c)


4
3
2
1
0
Mag(H(s))
Symbol: Measured
1-π
2-π
T
D9
D7
D5
0.0
1.0E10
2.0E10
3.0E10
4.0E10
Frequency (Hz)

(d)

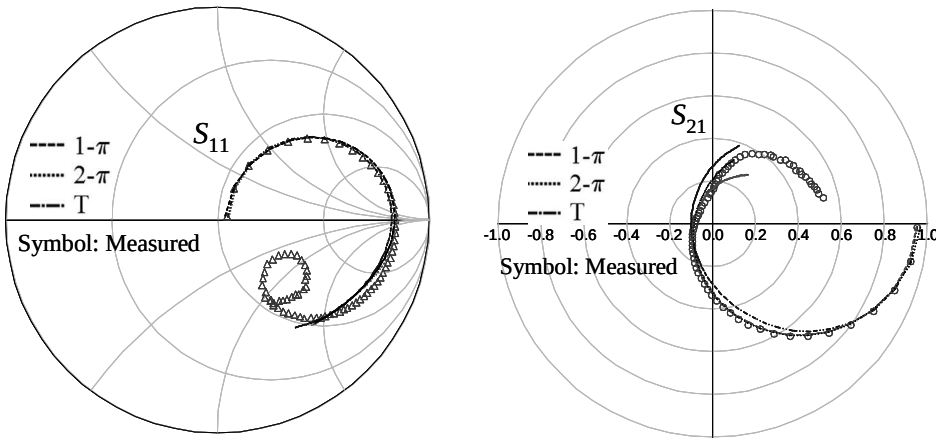


(e)

Figure 3.9: Comparisons of measured (R = 60μm) and simulated Q (a), L (b), ESR (c), and H(s) (d and e) by 1-π model [8], 2-π model [15] and T-model [19].

Figure 3.10 depicts the *S*-parameter results of the three models for the D4 and D9 inductors. These are more difficult to fit than for the other inductors. Therefore, it is better to use them to examine the fitting capacity of these models.

The magnitude and phase of the transfer function are shown in Figure 3.8 (d), Figure 3.8 (e), Figure 3.9 (d) and Figure 3.9 (e), respectively. Note that the measured magnitudes of inductors with larger geometries may form another smaller peak above the frequency of the main peak. Only the 2-π model can generate a second peak. In view of these phenomena, the 2-π model may actually be the best one to model the physical nature of spiral inductors among the three types of models.



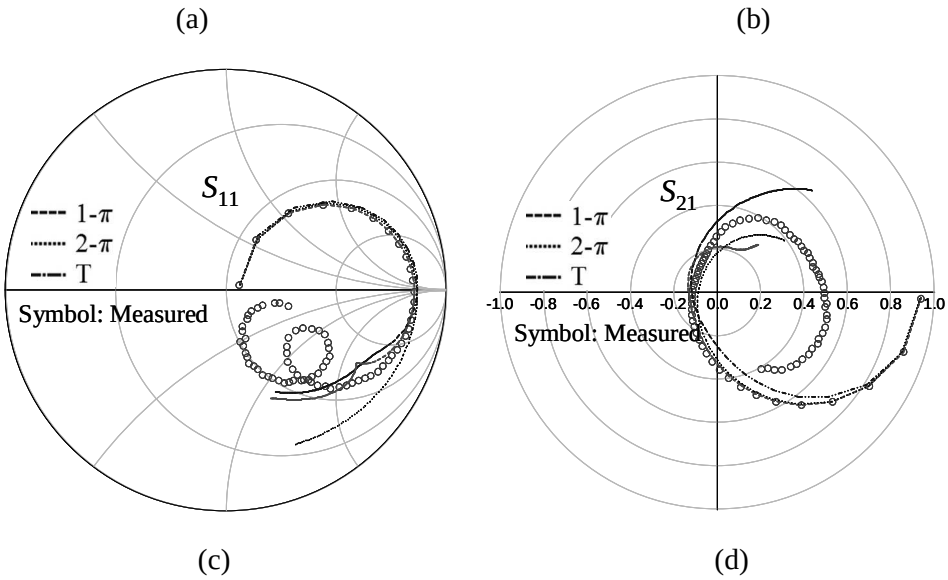


Figure 3.10: Comparisons between the measured and simulated *S*-parameters (for (a) and (b), R =30 μm; for (c) and (d), R =60 μm) by 1-π model [8], 2-π model [15] and T-model [19].

3.3 Physics-Based 2-π RF CMOS Spiral Modelling

3.3.1 Model and Model Parameter Extraction Method

A. Model Structure

The proposed spiral inductor model has a hierarchical structure, which is similar to that of standard transistor models such as BSIM3v3.2 and PSP. A strict separation of the geometry scaling in the global model and the model equations in the local model is introduced. Consequently, the model can be used at either one of the two levels. The described model structure is schematically depicted in Figure 3.11. Figure 3.12 shows the structures of on-chip spiral inductors fabricated in this work.

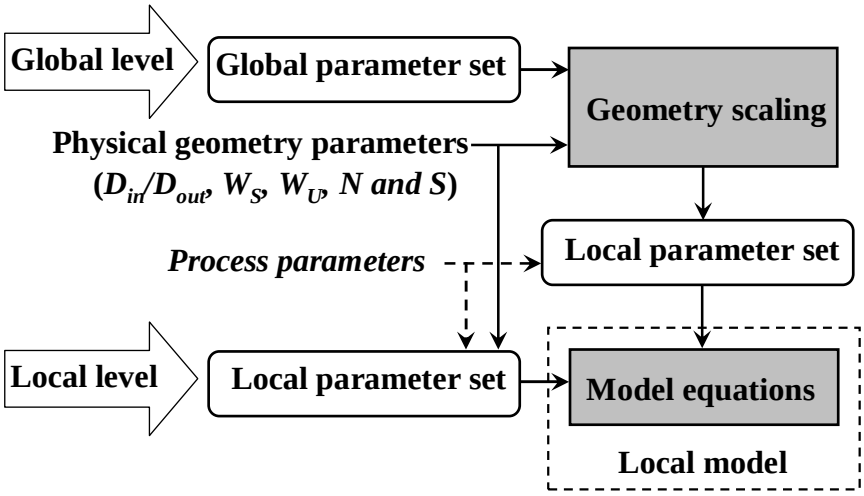
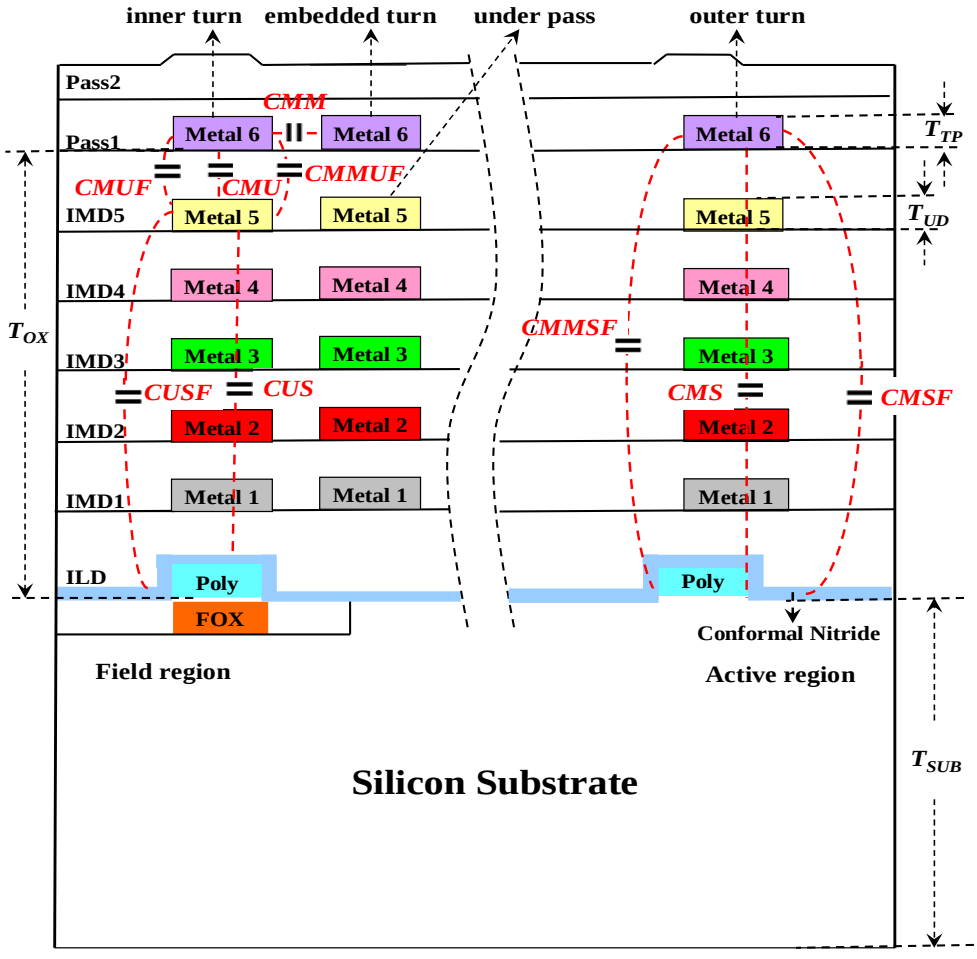
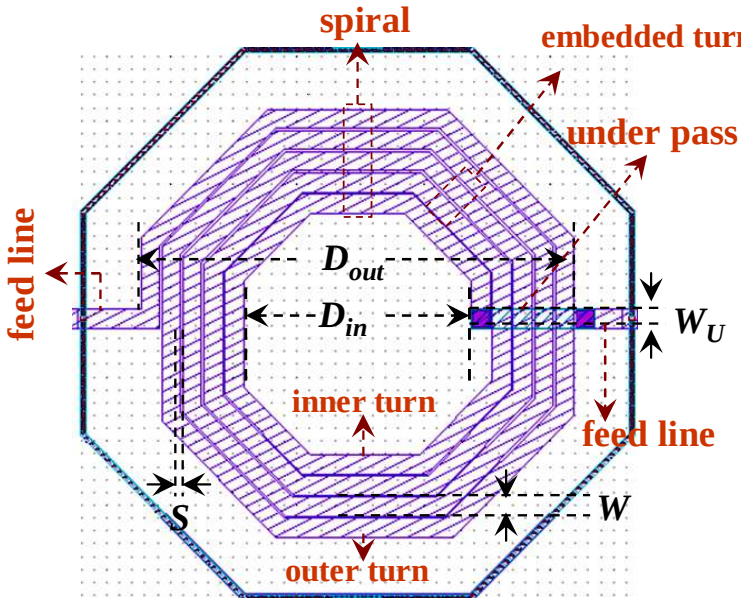


Figure 3.11: Simplified schematic overview of the proposed model's hierarchical structure.



(a)



(b)

Figure 3.12: Structures of on-chip spiral inductors. (a) Cross-section view of an on-chip spiral inductor. (b) Top view of a single-end octangular inductor. As seen from the Fig. 3.12 (a), an inductor with a given shape can be completely specified by the number of turns N, the spiral turn width W_S, the under-pass width W_U, the turn spacing S, and any one of the following: the inner diameter D_{in} or the outer diameter D_{out}.

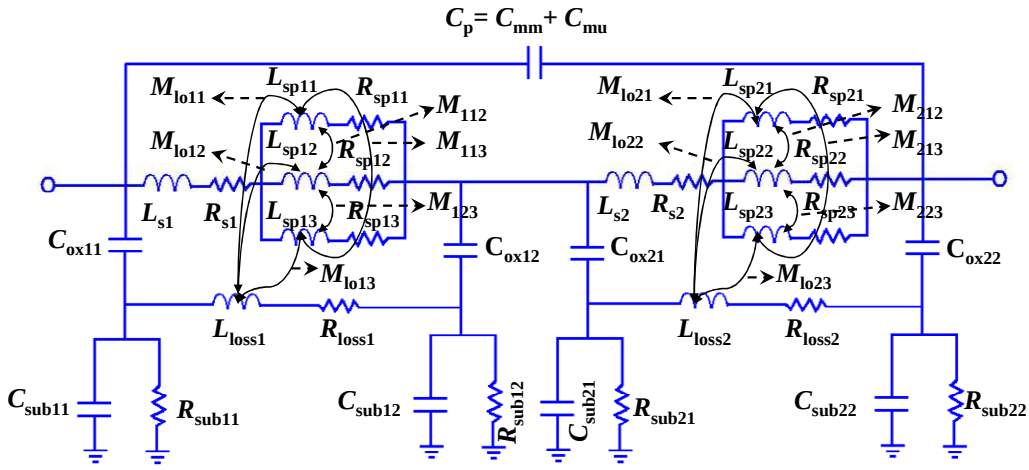


Figure 3.13: Proposed double-□□equivalent circuit model for asymmetric spiral inductors.

B. Model topology

The topology of the proposed 2-π equivalent circuit model is shown in Figure 3.13. In the circuit, L_{si} and R_{si} (i=1, 2) are the DC inductance and resistance, respectively. The L_{spij} - R_{spij} (i = 1, 2; j = 1, 2, 3) ladders with the mutual inductances M_{i12}, M_{i13}, and M_{i23}, (i = 1, 2) are used to capture the skin and proximity effects. C_p is the forward capacitance,

which includes the overlap capacitance C_{mu} and the coupling capacitance C_{mm} between the neighboring turns. C_{oxij} (i = 1, 2; j = 1, 2) represents the oxide-capacitance between the inductor and the substrate [24]. R_{subij} and C_{subij} (i = 1, 2; j = 1, 2) are the vertical substrate resistance and capacitance of the substrate, respectively. R_{lossj} and L_{lossj} (i = 1, 2) are introduced to represent the lateral resistive and inductive losses caused by the eddy current in the substrate.

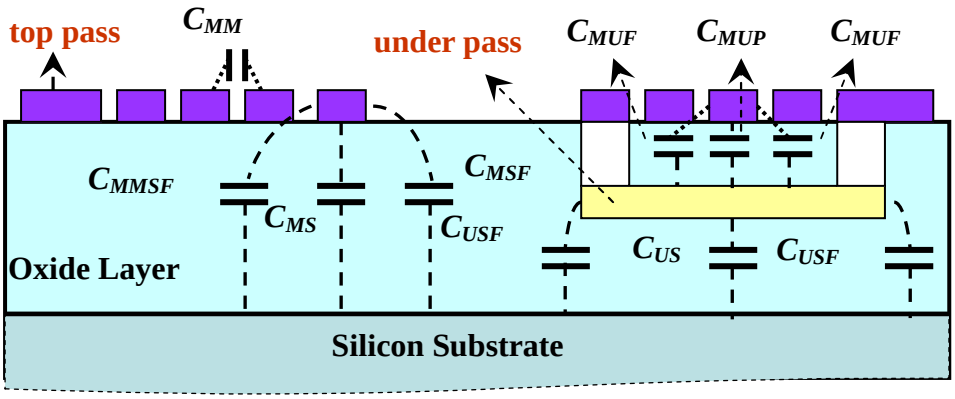


Figure 3.14: Simplified schematic overview of the capacitive parasitics in an asymmetric spiral inductor. The fringing capacitances are considered.

C. Model Parameter Set and Model Features

The definition of the physical geometry parameters needed in the model is described in this section. As accurate values of the layout and process parameters are difficult to obtain, a set of model parameters is introduced to correct the errors caused by using these given inaccurate layout and process parameters at the local level. For one specific instance of an inductor, a local parameter set is internally generated using the relevant geometric (as given in Table 3.4) and process parameters (as given in Table 3.5).

Since most of these local parameters scale with geometry, all inductors of a particular process can be described by a set of parameters, called the global parameter set. A set of scaling rules relates the local and global parameter set. By applying the set of scaling rules, a local parameter set can be obtained from a global parameter set. An overview of the local and global parameters in the model is given in the first and second column of Table 3.6.

Table 3.4: Physical geometry parameters

Name	Unit	Default	Description
D_{in}/D_{out}	μm	60	Inner/Outer diameter
W_S	μm	10	Width of spiral turn
W_U	μm	10	Width of underpass
N	/	2.5	Number of turns
S	μm	2	Turns spacing

Table 3.5: Process parameters

Name	Unit	Default	Description
R_{TP}	Ohm/□	0.015	Sheet resistance of spiral
T_{TP}	μm	2.9	Thickness of spiral
R_{UD}	Ohm/□	0.028	Sheet resistance of underpass
T_{UD}	μm	0.85	Thickness of underpass
C_{MU}	μF/m^2	34.2	Spiral to underpass capacitance
C_{MUF}	pF/m	21	Spiral to underpass fringing capacitance
C_{MM}	pF/m	89.8	Spiral turn to turn capacitance
C_{MS}	μF/m^2	4.307	Spiral to substrate capacitance
C_{MSF}	pF/m	3.91	Spiral to substrate fringing capacitance
C_{MMSF}	pF/m	2.3	metal windings to substrate fringing capacitance for embedded lines
C_{US}	μF/m^2	5.357	Underpass to substrate capacitance
C_{USF}	pF/m	6.25	Underpass to substrate fringing capacitance
T_{SUB}	μm	700	Substrate thickness
R_{SUB}	Ω-cm	100	Substrate resistivity
T_{OX}	μm	6.664	Oxide layer thickness

In the next sub-section, all of the initial values of the components in the topology shown in Figure 3.13 are calculated by the above parameters, which also bring many advantages to the model. 1) The use of process parameters provides the basis for building a direct process-tolerances-based statistical model. The deviations in the behaviour of actual manufactured spiral inductors results primarily from the deviation of the process parameters. 2) All of the elements in the model are calculated using the process parameters, physical design parameters and physical behavior so as to avoid the inaccuracy introduced by the analytical extraction algorithm. Therefore, more reliable values for the model parameters are obtained. This provides the basis for building more

simplified scalable models. More simplified scalable models mean fewer model parameters and a much easier extraction process. This can greatly reduce the time for building models and model libraries. In addition, the two-pi models have a higher broad-band accuracy and exhibit closer behavior to the real physical mechanisms of the device when compared to single-pi, and T-topologies. This is the reason for the choice of the 2-pi topology in our study.

D. Model Equations for Local Level

Physics-based equations are carefully investigated and employed for the local model determination in this section. The set of local parameters as given in the first column of Table 3.6 are used to correct the errors introduced by the using the inaccurate values of the geometric and process parameters for determination of the model elements in this work.

Figure 3.14 shows the simplified schematic overview of the capacitive parasitics in an asymmetric spiral inductor. The fringing capacitances are considered. The model equations for all of the elements shown in Figure 3.13 are given as follows:

1) Skin and Proximity Effects: L_{spij}, R_{spij} and Mutual Inductances, M_{i12}, M_{i13}, and M_{i23}, (i=*1, 2;* j=*1, 2, 3)*

With increasing frequency, the skin effect causes current crowding towards the surface of the conductor. The current density decreases from the surface to the center of the conductor. If the cross-section of the conductor is partitioned into many smaller subsections (in this work, three subsections are used), the current distribution in each subsection can be taken as uniform [20]. A simplified partitioning and modelling method as seen in Figure 3.15 is used to accurately capture the skin and proximity effects. The thickness and width for the partitioned three subsections of a metal line with a thickness T_h, width W_i, and length l_e are defined as h_{1s}, h_{2s} and h_{3s}, and w_{1s}, w_{2s} and w_{3s}, respectively.

At the frequency $f_{\max}$ (the interest modeled frequency, normally set to the highest test frequency, 20 GHz is used in this work), the skin depth of metal winding line, $\delta_{\max}$ can be calculated as:

$$\delta_{\max} = \sqrt{\frac{1}{\pi f_{\max} \mu \sigma_m}} \tag{3.1}$$

where, μ and σ_m are the permeability and conductivity of metal line, respectively. σ_m is defined as:

$$\sigma_m = \left(R_{\square} T_h \right)^{-1} \tag{3.2}$$

where $R_{\square}$ is the metal sheet resistivity.

In this work, experimental relationships between h_{js} (j=1,2,3) and $\delta_{\max}$ defined as (3.3) - (3.5) are used to determine the thicknesses (h_{1s}, h_{2s} and h_{3s}) of the three subsections, respectively:

$$h_{1s} = \delta_{\max} / 3 \tag{3.3}$$

$$h_{2s} = 2\delta_{\max} / 3 \tag{3.4}$$

$$h_{3s} = T_h - 2\delta_{\max} \tag{3.5}$$

Once h_{1s}, h_{2s} and h_{3s} are known, the width of the three subsections for the metal line can be calculated as follows:

$$w_{1s} = 2\left(W_i + T_h - 2h_{1s} \right) \tag{3.6}$$

$$w_{2s} = 2\left(W_i + T_h - 4h_{1s} - 2h_{2s} \right) \tag{3.7}$$

$$w_{3s} = W_i - 2\delta_{\max} \tag{3.8}$$

By using the DC resistance and self-inductance calculation method [26] for rectangular conductors, the six equivalent circuit model parameters as shown in the upper-right hand corner in Figure 3.15, R_{1s}, R_{2s}, R_{3s}, L_{1s}, L_{2s} and L_{3s} can be determined as follows:

$$R_{js} = \frac{1}{\sigma_m}\frac{l_e}{h_{js}w_{js}},\ j = 1,2,3 \tag{3.9}$$

$$L_{js} = 2l_e\left[\begin{array}{l}\log\left(\dfrac{2l_e}{w_{js}+h_{js}}\right)\\ +0.50049+\dfrac{w_{js}+h_{js}}{3l_e}\end{array}\right]\cdot 10^{-7},\ j = 1,2,3 \tag{3.10}$$

The mutual inductances M_{s12}, M_{s13} and M_{s23} can be calculated as follows:

$$M_{s12} = 2l_e\left[\begin{array}{l}\ln\left(\dfrac{l_e}{gmd_{12s}}+\sqrt{1+\dfrac{l_e^{\,2}}{gmd_{12s}^{\,2}}}\right)\\ -\sqrt{1+\dfrac{gmd_{12s}^{\,2}}{l_e^{\,2}}}+\dfrac{gmd_{12s}}{l_e}\end{array}\right]\cdot 10^{-7} \tag{3.11}$$

$$M_{s13} = 2l_e\left[\begin{array}{l}\ln\left(\dfrac{l_e}{gmd_{13s}}+\sqrt{1+\dfrac{l_e^{\,2}}{gmd_{13s}^{\,2}}}\right)\\ -\sqrt{1+\dfrac{gmd_{13s}^{\,2}}{l_e^{\,2}}}+\dfrac{gmd_{13s}}{l_e}\end{array}\right]\cdot 10^{-7} \tag{3.12}$$

$$M_{s23} = 2l_e\left[\begin{array}{l}\ln\left(\dfrac{l_e}{gmd_{23s}}+\sqrt{1+\dfrac{l_e^{\,2}}{gmd_{23s}^{\,2}}}\right)\\ -\sqrt{1+\dfrac{gmd_{23s}^{\,2}}{l_e^{\,2}}}+\dfrac{gmd_{23s}}{l_e}\end{array}\right]\cdot 10^{-7} \tag{3.13}$$

where rad_{1s}, rad_{1s} and rad_{1s} are defined as the equivalent radii of the three subsections, gmd_{12s}, gmd_{13s}, and gmd_{23s} are the geometric mean distances between the three parts, which can be calculated as follows:

$$rad_{1s} = 0.2235\left(W_i + T_h\right)/0.7788 \tag{3.14}$$

$$rad_{2s} = 0.2235\left(W_i + T_h - 4h_{1s}\right)/0.7788 \tag{3.15}$$

$$rad_{3s} = 0.2235\left[W_i + T_h - 4\left(h_{1s} + h_{2s}\right)\right]/0.7788 \tag{3.16}$$

$$gmd_{12s} = e^{\left[\frac{rad_{1s}^{\,2}\cdot\ln(rad_{1s}) - rad_{2s}^{\,2}\cdot\ln(rad_{2s})}{rad_{1s}^{\,2} - rad_{2s}^{\,2}} - 0.5\right]} \tag{3.17}$$

$$gmd_{13s} = e^{\left[\frac{rad_{1s}^{\,2}\cdot\ln(rad_{1s}) - rad_{3s}^{\,2}\cdot\ln(rad_{3s})}{rad_{1s}^{\,2} - rad_{3s}^{\,2}} - 0.5\right]} \tag{3.18}$$

$$gmd_{23s} = e^{\left[\frac{rad_{2s}^{\,2}\cdot\ln(rad_{2s}) - rad_{3s}^{\,2}\cdot\ln(rad_{3s})}{rad_{2s}^{\,2} - rad_{3s}^{\,2}} - 0.5\right]} \tag{3.19}$$

So following this approach, the metal segments used in a spiral inductor can be divided into three segments: the spiral, which has the length of l_m, the feed line, which has the length of l_{fd}, and the underpass, which has the length of l_{up}, respectively. In this work, the

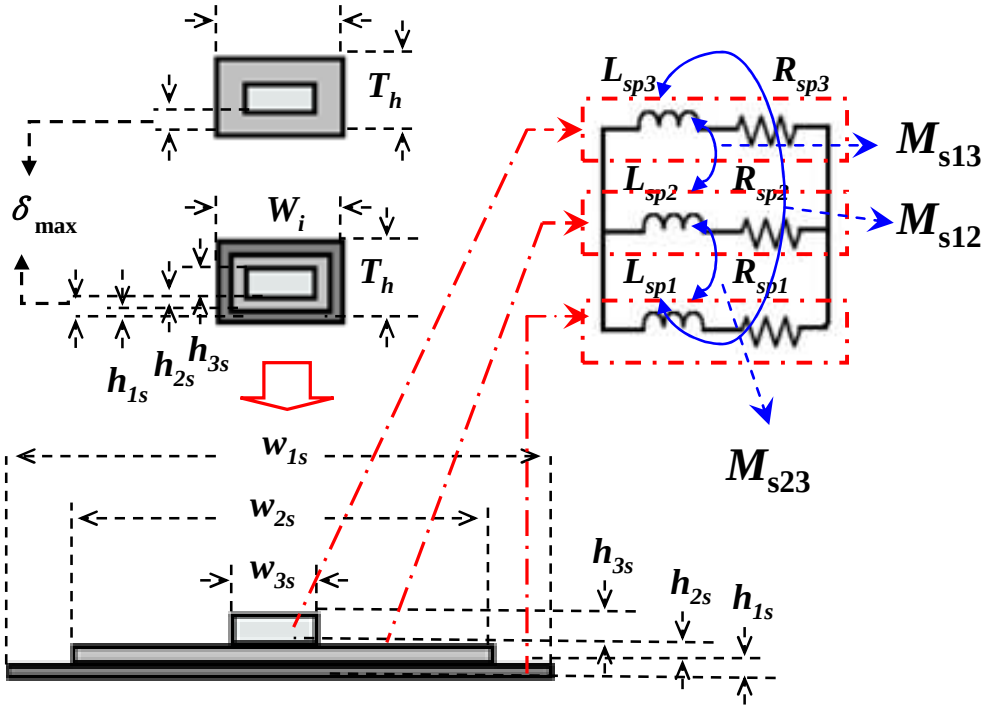


Figure 3.15: Schematic of the skin effect modelling.

width of feed line equals to that of the metal winding lines. $R_{\square}$, T_h, W_i and l_e are replaced with R_{TP}, T_{TP}, W_S, l_{total} (the total length of the spiral), for the spiral and with R_{UD}, T_{UD}, W_U, l_{up}, for the underpass. L_{spij} R_{spij}, M_{i12}, M_{i13}, and M_{i23}, *(*i=*1, 2;* j=*1, 2, 3)* can be determined by using (3.1) – (3.19), respectively, as follows:

$$R_{spij} = \frac{1}{2} r_{spcorr} \left(R_{wj} + R_{uj} \right), \left(i = 1, 2;\ j = 1, 2, 3\ \right) \tag{3.20}$$

$$L_{spij} = \frac{1}{2} l_{spcorr} \left(L_{wj} + L_{uj} \right), \left(i = 1, 2;\ j = 1, 2, 3 \right) \tag{3.21}$$

$$M_{i12} = \frac{1}{2} \left(M_{w12} + M_{u12} \right), \left(i = 1, 2 \right) \tag{3.22}$$

$$M_{i13} = \frac{1}{2} \left(M_{w13} + M_{u13} \right), \left(i = 1, 2 \right) \tag{3.23}$$

$$M_{i23} = \frac{1}{2} \left(M_{w23} + M_{u23} \right), \left(i = 1, 2 \right) \tag{3.24}$$

where r_{spcorr} and l_{spcorr} are local model parameters, R_{wj} and R_{uj} represent the DC resistances of the metal winding lines and the under-pass, respectively. L_{wj} and L_{uj} are the self-inductances of spiral and underpass, respectively. M_{w12}, M_{w13}, M_{w23} and M_{u12}, M_{u13}, M_{u23} represent the mutual inductances of the metal winding lines and the under-pass, respectively. For the layout given in Figure 3.12 (b), l_{total} can be calculated as

$$l_{total} = l_m + 2 l_{fd} \tag{3.25}$$

The proximity effect may be considered simultaneously by introducing the mutual inductances, M_{i12}, $M_{i13,}$ and M_{i23}, between the three different inductances L_{spij} (i=1,2; j=1,2,3). These are calculated with the mutual coefficients K_{i12}, $K_{i13,}$ and K_{i23}, (i=1, 2) which are calculated by an empirical method.

$$K_{i12} = \min \left[\frac{M_{i12}}{\sqrt{\mathrm{L}_{spi2} \mathrm{L}_{spi1}}}, 0.99 \right], i = 1, 2 \tag{3.26}$$

$$K_{i13} = \min \left[\frac{M_{i13}}{\sqrt{\mathrm{L}_{spi3} \mathrm{L}_{spi1}}}, 0.99 \right], i = 1, 2 \tag{3.27}$$

$$K_{i23} = \min \left[\frac{M_{i23}}{\sqrt{\mathrm{L}_{spi3} \mathrm{L}_{spi2}}}, 0.99 \right], i = 1, 2 \tag{3.28}$$

Table 3.6: Model parameter set and the geometry scaling rules. A total of 17 local parameters and 68 global model parameters are used for asymmetric on-chip spiral inductors.

Local Parameter Set	Global Parameter Set	Geometry Scaling for Local Parameter Set	Default Values of the global parameters
l_{spcorr}	l_{sp1}, l_{sp2}, l_{sp3}, l_{sp4}	$l_{spcorr} = l_{sp1} h_p^{l_{sp2}} N^{l_{sp3}} D_{in}^{l_{sp4}}$	*0.7945, -0.9205, 0.6433, 0.3471*
r_{spcorr}	r_{sp1}, r_{sp2}, r_{sp3}, r_{sp4}	$r_{spcorr} = r_{sp1} h_p^{r_{sp2}} N^{r_{sp3}} D_{in}^{r_{sp4}}$	*0.0218, -1.368, -0.1977, 0.0967*
c_{pcorr}	c_{p1}, c_{p2}, c_{p3}, c_{p4}	$c_{pcorr} = c_{p1} h_p^{c_{p2}} N^{c_{p3}} D_{in}^{cp4}$	*1.438, -0.9049, -1.299, 0.1428*
$c_{oxcorr11}$	c_{ox11}, c_{ox12}, c_{ox13}, c_{ox14}, c_{ox15}	$c_{oxcorr11} = c_{ox11} h_p^{c_{ox12}} N^{c_{ox13}} D_{in}^{c_{ox14}} W_S^{c_{ox15}}$	*0.005237, -0.5084, -0.3639, 0.215, -0.562*
$c_{oxcorr12}$	c_{ox121}, c_{ox122}, c_{ox123}, c_{ox124}, c_{ox125}	$c_{oxcorr12} = c_{ox121} h_p^{c_{ox122}} N^{c_{ox123}} D_{in}^{c_{ox124}} W_S^{c_{ox125}}$	*0.2437, -0.2584, -0.7202, 0.05421, -0.05775*
$c_{oxcorr22}$	c_{ox21}, c_{ox22}, c_{ox23}, c_{ox24}, c_{ox25}	$c_{oxcorr22} = c_{ox21} h_p^{c_{ox22}} N^{c_{ox23}} D_{in}^{c_{ox24}} W_S^{c_{ox25}}$	*0.001061, 0.1896, -0.3967, 0.1706, -0.6638*
$c_{subcorr11}$	c_{sub11}, c_{sub12}, c_{sub13}, c_{sub14}	$c_{subcorr11} = c_{sub11} h_p^{c_{sub12}} N^{c_{sub13}} D_{in}^{c_{sub14}}$	*15.74, 0.4367, -0.6414, 0.2686*
$c_{subcorr12}$	c_{sub121}, c_{sub122}, c_{sub123}, c_{sub124}	$c_{subcorr12} = c_{sub121} h_p^{c_{sub122}} N^{c_{sub123}} D_{in}^{c_{sub124}}$	*0.003289, 1.031, -1.298, -0.8483*
$c_{sbucorr22}$	c_{sub21}, c_{sub22}, c_{sub23}, c_{sub24}	$c_{subcorr22} = c_{sub21} h_p^{c_{sub22}} N^{c_{sub23}} D_{in}^{c_{sub24}}$	*9.295, 0.7762, -0.8756, 0.1861*
$r_{subcorr11}$	r_{sub11}, r_{sub12}, r_{sub13}, r_{sub14}	$r_{subcorr11} = r_{sub11} h_p^{r_{sub12}} N^{r_{sub13}} D_{in}^{r_{sub14}}$	*32.76, -0.5752, 1.71, 0.7687*
$r_{subcorr12}$	r_{sub121}, r_{sub122}, r_{sub123}, r_{sub124}	$r_{subcorr12} = r_{sub121} h_p^{r_{sub122}} N^{r_{sub123}} D_{in}^{r_{sub124}}$	*12.69,-0.8495, 0.3311, 0.3437*
$r_{sbucorr22}$	r_{sub21}, r_{sub22}, r_{sub23}, r_{sub24}	$r_{subcorr22} = r_{sub21} h_p^{r_{sub22}} N^{r_{sub23}} D_{in}^{r_{sub24}}$	*5.058, 0.4124, 1.715, 0.5148*
$r_{losscorr1}$	r_{lo11}, r_{lo12}, r_{lo13}, r_{lo14}	$r_{losscorr1} = r_{lo11} h_p^{r_{lo12}} N^{r_{lo13}} D_{in}^{r_{lo14}}$	*4.23, -0.036, 0.35, 0.08537*
$r_{losscorr2}$	r_{lo21}, r_{lo22}, r_{lo23}, r_{lo24}	$r_{losscorr2} = r_{lo21} h_p^{r_{lo22}} N^{r_{lo23}} D_{in}^{r_{lo24}}$	*4.36, -0.03455, 0.3547, 0.089*
$l_{losscorr1}$	l_{lo11}, l_{lo12}, l_{lo13}, l_{lo14}	$l_{losscorr1} = l_{lo11} h_p^{l_{lo12}} N^{l_{lo13}} D_{in}^{l_{lo14}}$	*1.737, -0.4737, 0.262, 0.1918*
$l_{losscorr2}$	l_{lo21}, l_{lo22}, l_{lo23}, l_{lo24}	$l_{losscorr2} = l_{lo21} h_p^{l_{lo22}} N^{l_{lo23}} D_{in}^{l_{lo24}}$	*1.642, -0.4776, 0.256, 0.1854*
r_{dccorr}	rl_{dc1}, r_{dc2}, r_{dc3}, r_{dc4}	$r_{dccorr} = r_{dc1} h_p^{r_{dc2}} N^{r_{dc3}} D_{in}^{r_{dc4}}$	*1.474, -0.2628, -0.1162, 0.03109*

l_{dccorr}	l_{dc1}, l_{dc2}, l_{dc3}, l_{dc4}	$l_{dccorr} = l_{dc1} h_p^{l_{dc2}} N^{l_{dc3}} D_{in}^{l_{dc4}}$	*0.2788, 0.2942, -0.03423, -0.1537*

2) DC Inductance and Resistance: L_{si} and R_{si}, *(i=1, 2)*

The DC resistance R_{dc} of a spiral inductor can be calculated as

$$R_{dc} = R_{UD} \frac{l_{up}}{W_U} + R_{TP} \frac{l_{total}}{W_S} \tag{3.29}$$

The distributed DC inductance L_{dc} of a spiral inductor can be calculated using [26] as follows:

$$L_{dc} = \beta D_{out}^{\alpha 1} W_S^{\alpha 2} d_{avg}^{\alpha 3} N^{\alpha 4} S^{\alpha 5} \tag{3.30}$$

where α_i (i = 1, 2, 3, 4, 5) and β are layout dependent coefficients. For octagonal inductors, α_i (i = 1, 2, 3, 4, 5) and β are -1.21, -0.163, 2.43, 1.75, -0.149 and 1.33×10^{-3}, respectively. The average diameter d_{avg} is defined as

$$d_{avg} = \frac{1}{2}(D_{in} + D_{out}) \tag{3.31}$$

As the partition method used in (3.3)-(3.5) for modeling the skin and proximity effects is experiential, this method causes differences between the total resistance of the resistances R_{spij}, (i=1, 2; j=1, 2, 3) and the DC resistance calculated by using (3.29), the total inductance of the inductances L_{spij}, (i=1, 2; j=1, 2, 3) and the DC inductance calculated by using (3.30) directly. L_{si} and R_{si} are introduced to account for this L_{si} and R_{si} are calculated as

$$L_{si} = \frac{1}{2} M_L L_{dc}, i = 1, 2 \tag{3.32}$$

$$R_{si} = \frac{1}{2} M_R R_{dc}, i = 1, 2 \tag{3.33}$$

where

$$M_R = 1 - 2\frac{R_{sp11} // R_{sp12} // R_{sp13}}{R_{dc}} = 1 - 2\frac{R_{sp11}R_{sp12}R_{sp13}}{R_{dc}\left(R_{sp12}R_{sp13} + R_{sp11}R_{sp13} + R_{sp11}R_{sp12}\right)} \quad (3.34)$$

$$M_L = 1 - 2\frac{L_{sp11} // L_{sp12} // L_{sp13}}{L_{dc}} = 1 - 2\frac{L_{sp11}L_{sp12}L_{sp13}}{L_{dc}\left(L_{sp12}L_{sp13} + L_{sp11}L_{sp13} + L_{sp11}L_{sp12}\right)} \quad (3.35)$$

3) Overlap and Coupling Capacitance: $C_p = C_{mm} + C_{mu}$

C_p represents the forward capacitance, which includes the overlap capacitance C_{mu} and the coupling capacitance C_{mm} between the neighboring segments. A simplified schematic overview of the capacitive parasitics in an asymmetric spiral inductor is illustrated in Figure 3.14. Considering the parallel-plate capacitance and the fringing capacitance from spiral turn to under pass, the overlap capacitance including the fringing effect can be calculated as follows

$$C_{mu} = c_{pcorr}\left[W_U N\left(C_{MU}W_S + 2C_{MUF}\right)\right] \quad (3.36)$$

The coupling capacitance between the neighboring turns is calculated as

$$C_{mm} = c_{pcorr}C_{MM}l_{sp} \quad (3.37)$$

where, c_{pcorr} is a local model parameter, l_{sp} is the length of turn spacing.

4) Metal-oxide Capacitance: C_{oxij}

The metal-oxide capacitances $C_{\mathrm{ox}11}$, $C_{\mathrm{ox}12}$, $C_{\mathrm{ox}21}$ and $C_{\mathrm{ox}22}$ are defined as

$$C_{ox1j} = c_{oxcorr1j}\left[\frac{1}{2}\left(C_{msp} + C_{msf}\right) + C_{mup} + C_{muf}\right],\ j = 1,2 \quad (3.38)$$

$$C_{ox2j} = \frac{1}{2}c_{oxcorr2j}\left(C_{msp} + C_{msf}\right),\ j = 1,2 \quad (3.39)$$

where C_{msp} and C_{msf} represent the parallel-plate capacitance and the fringing capacitance from the top pass to substrate, respectively. C_{mup} and C_{muf} are the parallel-plate capacitance and the fringing capacitance from the under pass to substrate, respectively.

C_{msp}, C_{msf}, C_{mup} and C_{muf} are defined as

$$C_{msp} = C_{MS} l_{total} W \tag{3.40}$$

$$C_{mup} = C_{US} l_{up} W_U \tag{3.41}$$

$$C_{msf} = 2C_{MS} l_m + 4C_{MSF} l_{fd} + \left(C_{MSF} - C_{MS}\right)\left(l_{inner} + l_{outer}\right) \tag{3.42}$$

$$C_{muf} = 2l_{up} C_{USF} \tag{3.43}$$

where, l_{inner} and l_{outer} are the length of the inner and outer spiral turn, respectively. c_{oxcorrij} (i=1, 2; j=1, 2) are local model parameters. $c_{\text{oxcorr12}} = c_{\text{oxcorr21}}$ is used in this work.

5) The Vertical Substrate Loss Model: R_{subij} and C_{subij}

The displacement current loss that resulted from the capacitive coupling effect of the silicon substrate is highly dependent on the process parameters and the working frequency. For multi-turn inductors, due to the fringing electric field of the neighboring metal segments [22], the electric field of the embedded turns is much smaller than that of the outer turn, inner turn and the feed lines. Consequently, the effective thicknesses of the substrate relative to the embedded turns and the inner turn/outer turn/feed lines are different. The thickness of the substrate relative to the embedded turns is much smaller than the original value $T_{\text{SUB.}}$ A substrate effect factor γ_{sub} is defined here to take this effect into account. By using the modelling method for substrate capacitive and resistive coupling effects proposed in [23]-[24], the substrate capacitance and conductance of the embedded turns per unit-length can be calculated as

$$C_{sub\_e} = \varepsilon_0 \varepsilon_{eff\_e} \Big/ \left\{ \frac{1}{2\pi} \ln\left[8h_{r\_e} + 1 \Big/ \left(4h_{r\_e}\right) \right] \right\} \tag{3.44}$$

$$G_{sub\_e} = \frac{\pi \sigma_{sub}}{\ln\left[8h_{r\_e} + 1 \Big/ \left(4h_{r\_e}\right) \right]} \left[1 + \left(1 + 10h_{r\_e}\right)^{-1/2} \right] \tag{3.45}$$

where σ_{sub} is the conductivity of substrate. h_{r_e} is the ratio of the effective thickness of the substrate relative to the embedded turns to the width of spiral turn. ε_{sub} and ε_{eff_e} are the dielectric constant and the effective dielectric constant of substrate, respectively. $\sigma_{sub,}$ h_{r_e} and ε_{eff_e} are defined as

$$\sigma_{sub} = \left(T_{SUB} R_{SUB}\right)^{-1} \tag{3.46}$$

$$h_{r\_e} = \gamma_{sub} T_{SUB} / W_S \tag{3.47}$$

$$\varepsilon_{eff\_e} = \frac{1}{2}\left[\left(\varepsilon_{sub}+1\right) + \frac{\varepsilon_{sub}-1}{\sqrt{1+10h_{r\_e}}}\right] \tag{3.48}$$

The substrate capacitance and conductance of the inner turn, the outer turn and the feed lines per unit-length can be calculated as

$$C_{sub\_o} = \varepsilon_0 \varepsilon_{eff\_o} \Big/ \left\{\frac{1}{2\pi} \ln\left[8h_{r\_o} + 1 \Big/ \left(4h_{r\_o}\right)\right]\right\} \tag{3.49}$$

$$G_{sub\_o} = \frac{\pi \sigma_{sub}}{\ln\left[8h_{r\_o} + 1/\left(4h_{r\_o}\right)\right]_o} \left[1 + \left(1 + 10h_{r\_o}\right)^{-1/2}\right] \tag{3.50}$$

where h_{r_o} is the ratio of the thickness of the substrate to the width of spiral turn, ε_{eff_o} is the dielectric constant of substrate respectively. h_{r_o} and ε_{eff_o} are defined as

$$h_{r\_o} = T_{SUB} / W_S \tag{3.51}$$

$$\varepsilon_{eff\_o} = \frac{1}{2}\left[\left(\varepsilon_{sub}+1\right) + \frac{\varepsilon_{sub}-1}{\sqrt{1+10h_{r\_o}}}\right] \tag{3.52}$$

The vertical substrate capacitance C_{subij} and resistance R_{subij}, (i=1, 2; j=1, 2) can be calculated as

$$C_{subij} = \frac{C_{subcorrij}}{2}\left[l_m \left(1 - l_{ratio}\right) C_{sub\_e} + \left(l_m l_{ratio} + 2 l_{fd} \right) C_{sub\_o} \right], i = 1, 2;\ j = 1, 2 \tag{3.53}$$

$$R_{subij} = 2 r_{subcorrij} \left[l_m \left(1 - l_{ratio}\right) G_{sub\_e} + \left(l_m l_{ratio} + 2 l_{fd} \right) G_{sub\_o} \right]^{-1}, i = 1, 2;\ j = 1, 2 \tag{3.54}$$

where, l_{ratio} is defined as $l_{ratio} = \frac{l_{inner} + l_{outer}}{l_m}$, $\gamma_{\text{sub,}}$ $r_{\text{subcorrij}}$ and $c_{\text{subcorrij}}$ (i=1, 2; j=1, 2) are local model parameters. For single or half turn spiral inductors, the calculation of (3.51)-(3.54) can be omitted.

6) The Lateral Substrate Loss Model: R_{lossi} and L_{lossi}

As the eddy current is generally flowing in the lateral direction in the substrate, and the impedance caused by the geometric and frequency-dependent effects is complex, the eddy current effect can be taken as the major mechanism of the lateral substrate losses for spiral inductors manufactured in a specified process. For compact modelling, the concept of the complex effective height [25] of the substrate is introduced to determine the lateral resistances and inductances, R_{lossi} and L_{lossi} in this work.

The complex effective thickness of the substrate for the eddy current flowing in the substrate can be defined as

$$h_{eff} = h_{ox} + \frac{\delta}{2}(1 - j)\coth\left[\frac{h_{si}}{\delta}(1 + j) \right] \tag{3.55}$$

where h_{ox} and h_{si} are the thicknesses of oxide layer and the silicon substrate, respectively. δ is defined as the skin depth of substrate at f_{max}, which can be calculated as

$$\delta = \frac{1}{\sqrt{\pi f_{\max} \mu_{si} \sigma_{si}}} \tag{3.56}$$

where μ_{si} and σ_{si} are the permeability and conductivity of the silicon substrate, respectively.

According to the method introduced in [25], the per-unit-length series impedance of the substrate can be calculated as

$$L^*(\omega) = \frac{\mu_0}{4\pi} \ln\left\{1 + 32\left(\frac{h_{eff}}{\omega}\right)^2 \cdot \left[1 + \sqrt{1 + \left(\frac{\pi\omega}{8h_{eff}}\right)^2}\right]\right\} \tag{3.57}$$

By using the real and imaginary part of (3.57), R_{lossi} and L_{lossi} are determined as

$$L_{lossi} = -l_{lossi} l_{total} \frac{\omega}{2} \mathrm{Im}\left[L^*(\omega)\right], i = 1, 2 \tag{3.58}$$

$$R_{lossi} = \frac{1}{2} r_{lossi} l_{total} \mathrm{Re}\left[L^*(\omega)\right], i = 1, 2 \tag{3.59}$$

where l_{lossi} and r_{lossi} (i=1, 2) are local model parameters. For compact modelling, the results of $L^*(\omega)$ at $\omega=2\pi f_{\max}$ is used in this work.

In order to consider the geometric effect on the strength of the eddy current, mutual inductances, M_{loij} (i=1, 2; j=1, 2, 3) calculated with the mutual coefficients K_{loij} (i=1, 2; j=1, 2, 3), between L_{lossi} and L_{spij} (i=1, 2; j=1, 2, 3) are introduced into the topology as shown in Figure 3.13 for capturing this effect. K_{loij} (i=1, 2; j=1, 2, 3) is experientially defined as follows:

$$K_{loij} = \min\left[\frac{\mathrm{L}_{lossi}}{\sqrt{\mathrm{L}_{si}\mathrm{L}_{spij}}}, 0.99\right], i = 1, 2; j = 1, 2, 3 \tag{3.60}$$

Table 3.7: Geometric parameters of asymmetric inductors manufactured on a standard 0.18-μm SiGe BiCMOS process with 100 Ohm-cm substrate resistivity. $W = W_{\mathrm{u}} = W_{\mathrm{s}}$ is used for these devices. The extracted results of the global parameter set for these devices are given as the default values listed in Table 3.6.

DUT #	W_s (μm)	D_{in} (μm)	N	S (μm)
D1	8	80	1.5	2
D2, D3		120	1.5, 2.5	
D4~D9		200	1.5, 2.5, 3.5, 4.5, 5.5, 6.5	
D10, D11		240	1.5, 6.5	
D12~D17		280	1.5, 2.5, 3.5, 4.5, 5.5, 6.5	
D18, D19		320	1.5, 6.5	
D20, D25		400	1.5, 2.5, 3.5, 4.5, 5.5, 6.5	
D26, D27	10	160	1.5, 2.5	
D28~D31		200	1.5, 2.5, 3.5, 4.5	
D32, D33		240	1.5, 6.5	

D34~D36		280	1.5, 3.5, 6.5	
D37			3.5	3
D38			3.5	4
D39~D41		360	1.5, 3.5, 6.5	2
D42~D44		400	1.5, 3.5, 6.5	
D45, D46	15	200	1.5, 3.5	
D47~D51		280	1.5, 2.5, 3.5, 4.5, 5.5	
D52, D53		320	1.5, 4.5	
D54~D56		400	1.5, 4.5, 5.5	
D57	20	280	3.5	
D58		400	3.5	
D59	30	360	3.5	

E. Geometry Based Scaling Rules and the Global Model

The local parameter set can be viewed as a correction of the model determined from the local model equations and the employed process and geometric parameters. The global parameters account for geometric scaling. The complete geometry scaling rules developed for the local parameter set is listed in Table 3.6. All of the local model parameters are considered as a function of the N, D_{in} and h_p. h_p is the hollowness of an inductor with a specified geometry, which is defined as:

$$h_p = \frac{D_{in} + W_S}{D_{out} - W_S} \tag{3.61}$$

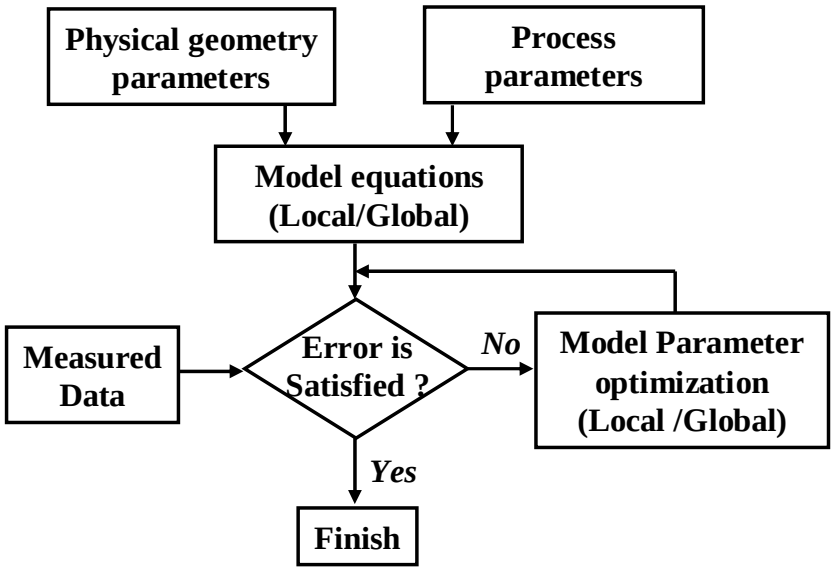


Figure 3.16: Local/Global model extraction flow.

Table 3.8: *RMS* errors between the simulated and measured inductance (*L*), Quality Factor (*Q*) and *S*-parameter for the devices listed in table 3.7

DUT	*L* (%)	*Q* (%)	S_{11} (%)		S_{12} (%)	
			real	imag	real	imag
D5	1.675	3.885	2.049	1.991	1.361	4.320
D9	4.771	2.175	3.140	2.899	1.725	4.540
D13	2.268	5.391	2.246	3.076	1.273	4.625
D21	1.761	3.718	0.794	1.638	1.511	1.808
D25	4.604	2.332	2.836	2.612	1.675	5.202
D30	1.557	1.933	0.781	1.425	1.149	1.378
D32	3.270	7.161	0.724	2.417	1.641	2.852
D36	2.546	6.524	3.870	4.126	0.611	5.896
D41	2.108	4.865	3.139	2.725	2.287	3.627
D43	1.826	2.081	2.924	2.991	0.574	5.280
D49	3.967	4.819	3.723	2.941	1.164	3.843
D53	1.469	2.070	0.998	1.238	1.255	2.389
D59	3.515	2.542	0.621	1.267	1.163	1.585

3.3.2 Model Extraction and Verification

A simplified global/local model extraction flowchart is given in Figure 3.16. Once the process and geometry parameters needed in the equations (3.1)-(3.61) are given (the required process parameters are generally obtained from the foundry), the local parameter set given in Table 3.6 can be extracted using an optimization procedure. For global model parameter determination, a set of measurements from inductors with different geometric parameters are required. In this work, the local model parameters for the devices with different geometric parameters are first extracted. The extracted results are then used to determine the global model parameters by using a simple optimization procedure.

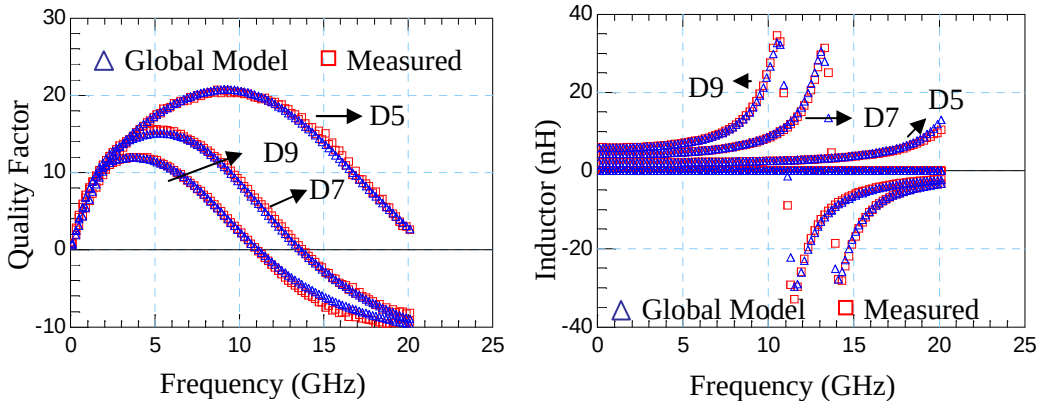
In order to verify the accuracy of the proposed scalable model, a set of 59 asymmetric octagonal spiral inductors with different geometric parameters fabricated on a standard 0.18-μm SiGe BiCMOS technology are modelled using the global model proposed in the thesis. The geometric parameters of the 59 devices are outlined in Table 3.7. Two-port *S*-parameters were measured and de-embedded (Open + Short) for parasitics

introduced by the GSG PAD using an Agilent E8363B Network Analyzer and a CASCADE Summit probe station. The feed lines connected at the right and left side of inductors are finally deembedded from test structures for model extraction. The model parameter extraction procedure is executed by using Agilent Integrated Circuit Characterization and Analysis Program (IC-CAP) device modeling software. The Random Optimization Package and HSPICE simulator implanted in IC-CAP are employed for the model simulation and optimization.

Measurements are taken of the S-parameters and the quality factor and inductance are determined. These are compared to the results from the scaled global models. The *RMS* errors of the *S*-parameters, quality factor (*Q*) and inductance (*L*) for the measured and simulated results are given in Table 3.8. The *RMS* error is defined as follows:

$$RMS\_error = 100 \cdot \sqrt{\left[\frac{1}{n} \sum_{1}^{n} \frac{\left(X_{mea} - X_{sim} \right)^2}{\left(\sum_{1}^{n} X_{mea}^2 / n \right)} \right]} \tag{3.62}$$

where, n is the total number of data points. The *RMS* error calculation is executed over the frequency range from 50 MHz to the *SRF* of devices.



(a) (b)

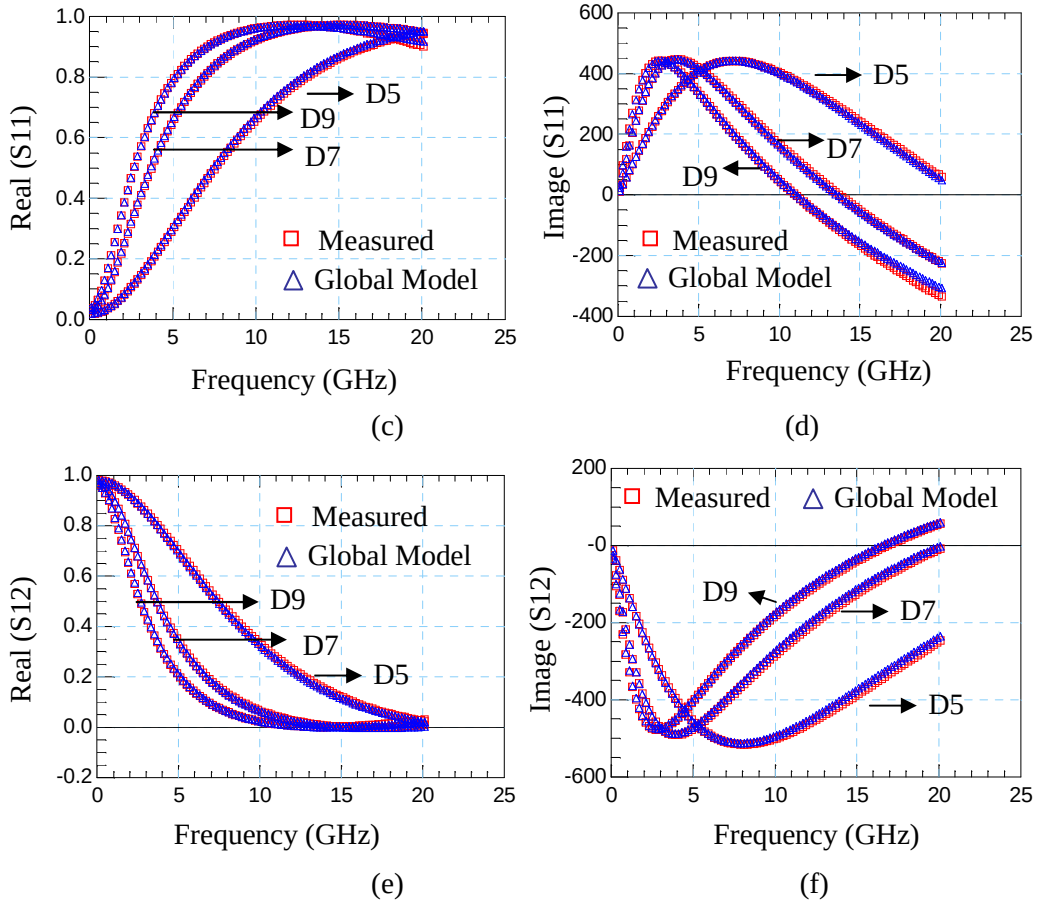
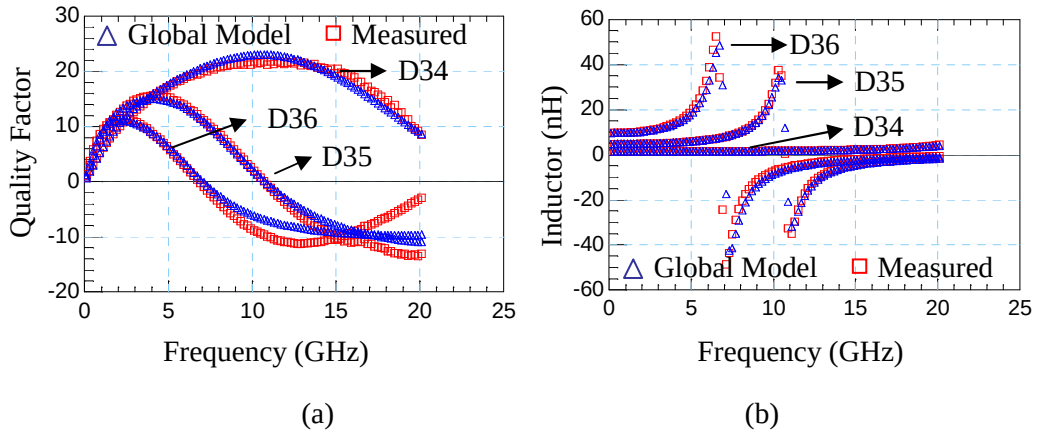


Figure 3.17: Comparison between measured and double-π scalable model for asymmetric inductors with W=8μm, D_{out}=200μm, S=2μm, : (a) Quality factor, (b) Inductance, (c) Real parts of S_{11}, (d) Imaginary parts of S_{11}, (e) Real parts of S_{12}, (f) Imaginary parts of S_{12}.



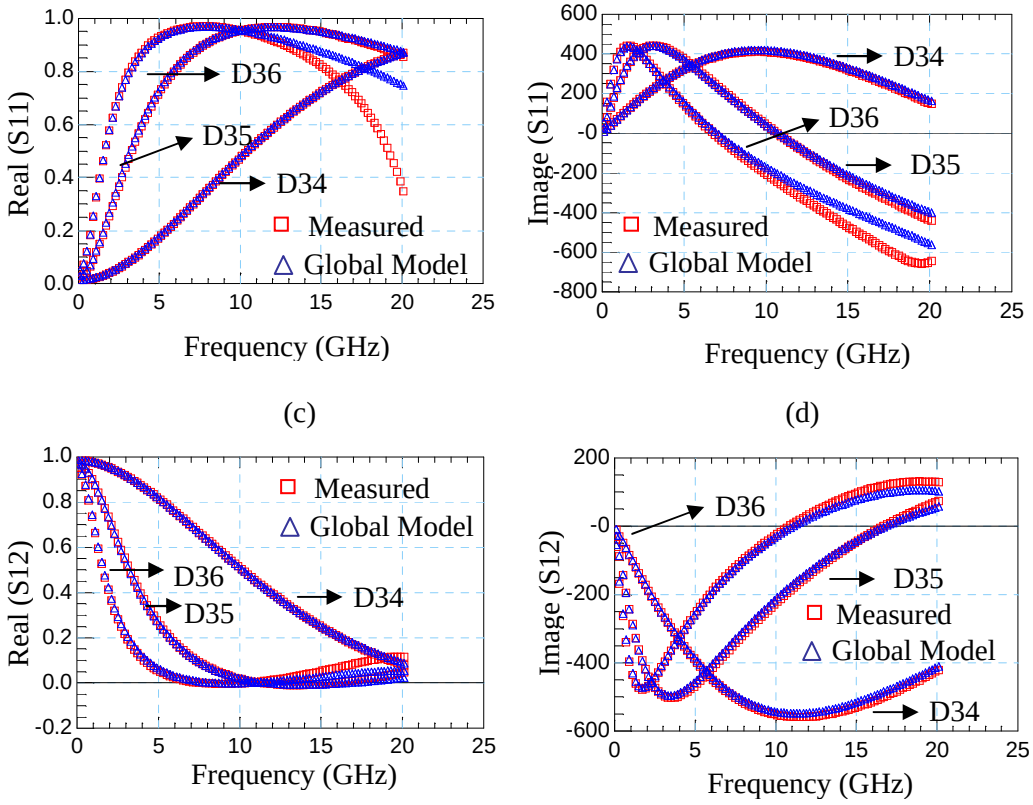
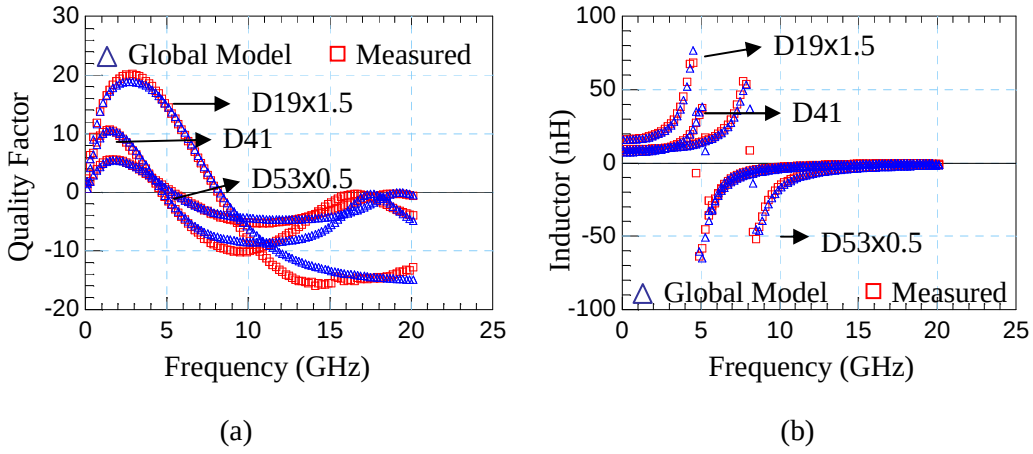


Figure 3.18: Comparison between measured and double-π scalable model for asymmetric inductors with W=10μm, D_{out}=280μm, S=2μm, : (a) Quality factor, (b) Inductance, (c) Real parts of S_{11}, (d) Imaginary parts of S_{11}, (e) Real parts of S_{12}, (f) Imaginary parts of S_{12}.



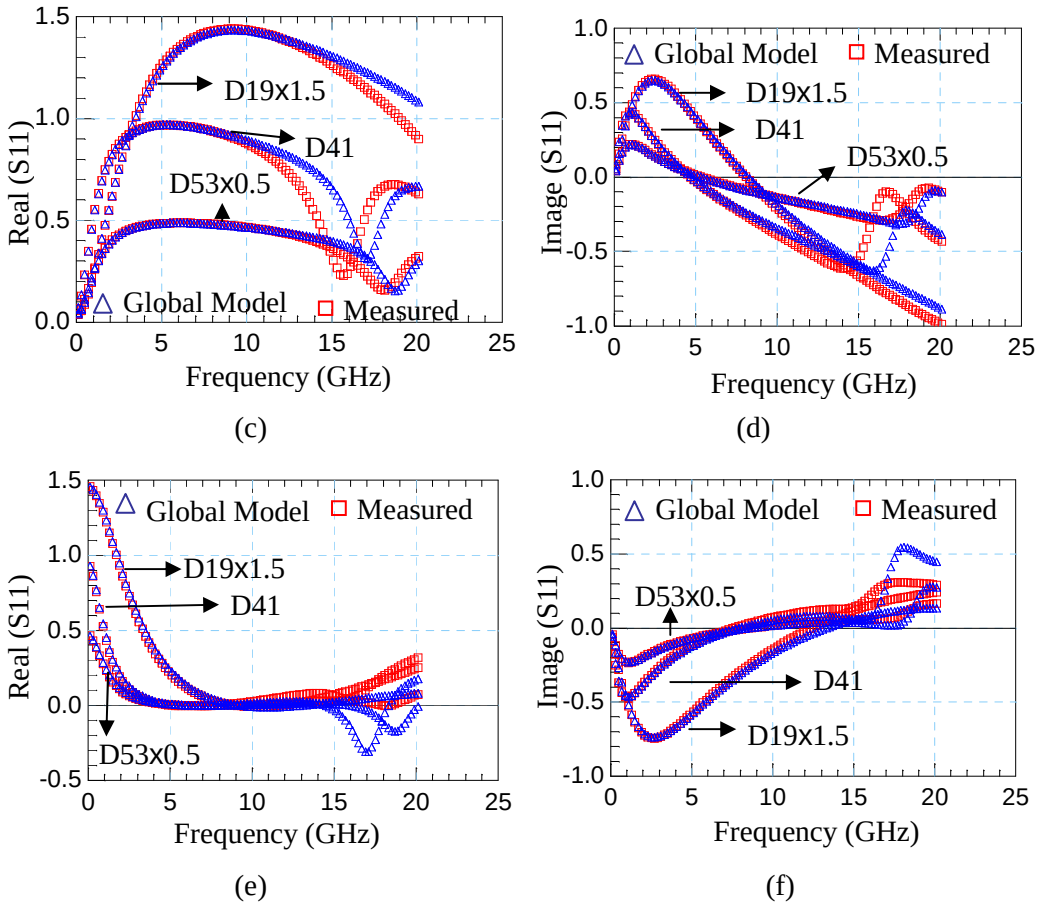
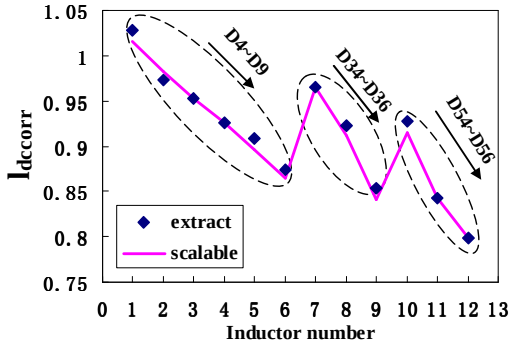
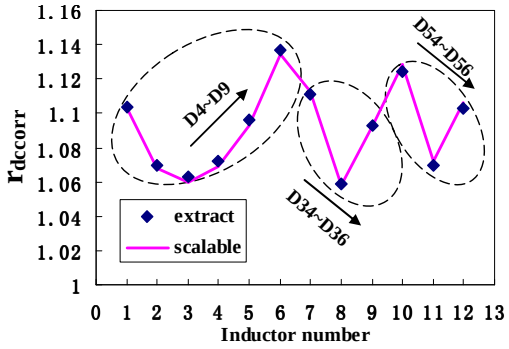


Figure 3.19: Comparison between measured and double-π scalable model for asymmetric inductors with N=6.5, D_{out}=360μm, S=2μm, : (a) Quality factor, (b) Inductance, (c) Real parts of S_{11} (d) Imaginary parts of S_{11}, (e) Real parts of S_{12}, (f) Imaginary parts of S_{12}.

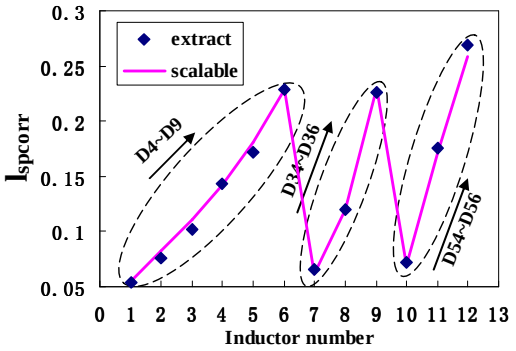
The measured and simulated Q, L, $real(S_{11})$, $real(S_{12})$, $imag(S_{11})$ and $imag(S_{12})$ characteristics of the asymmetric on-chip inductors, with W fixed at 8 μm, 10 μm and 15μm, S fixed at 2 μm while changing D_{out} and N, are shown in Figure 3.17 , Figure 3.18 and Figure 3.19, respectively. The *RMS* errors in L between the measured and simulated data for the inductors are below 5%. The average *RMS* error of L is 2.291%. For most of these devices, the *RMS* errors of Q are below 5%, and the average error of Q is 3.511%. The average *RMS* errors of the real and imaginary parts of S_{11} and S_{12} are 2.339%, 2.387%, 3.429% and 2.516%, respectively. The excellent agreement between the measured and simulated results verified and validated the accuracy of the proposed on-chip spiral inductor modelling technique. The accuracy of the proposed scalable rules are verified by the excellent agreement between the extracted data and the results from the scaled models of inductors with typical geometries, as shown in Figure 3.20.


1.05
1
0.95
0.9
0.85
0.8
0.75
l_{dccorr}
D4~D9
D34~D36
D54~D56
extract
scalable
0 1 2 3 4 5 6 7 8 9 10 11 12 13
Inductor number

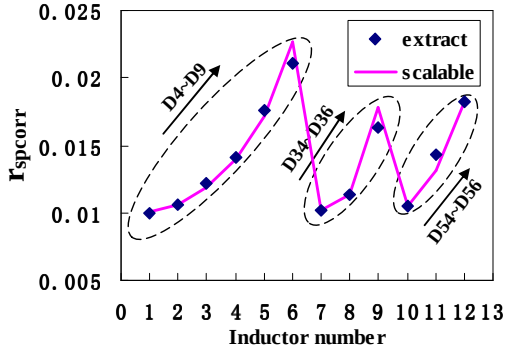
(a)


1.16
1.14
1.12
1.1
1.08
1.06
1.04
1.02
1
r_{dccorr}
D4~D9
D34~D36
D54~D56
extract
scalable
0 1 2 3 4 5 6 7 8 9 10 11 12 13
Inductor number

(b)


0.3
0.25
0.2
0.15
0.1
0.05
l_{spcorr}
extract
scalable
D4~D9
D34~D36
D54~D56
0 1 2 3 4 5 6 7 8 9 10 11 12 13
Inductor number

(c)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0.02
0.015
0.01
0.005
r_{spcorr}
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scalable
D4~D9
D34~D36
D54~D56
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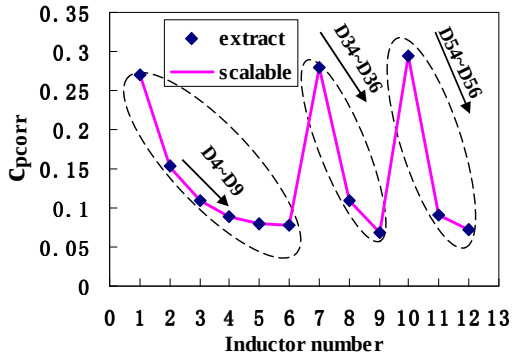
Inductor number

(d)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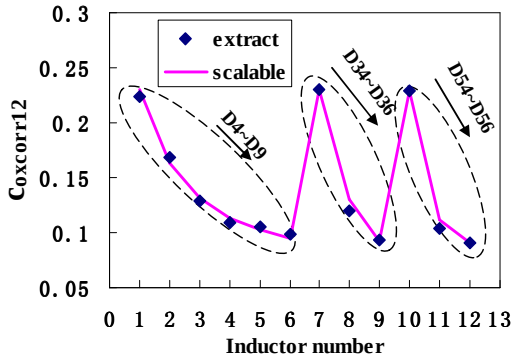
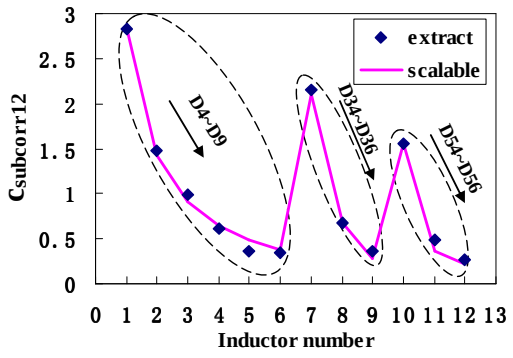
0.3
0.25
0.2
0.15
0.1
0.05
0
c_{pcorr}
extract
scalable
D4~D9
D34~D36
D54~D56
0 1 2 3 4 5 6 7 8 9 10 11 12 13
Inductor number

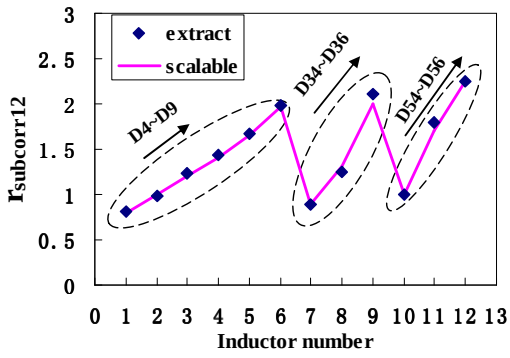
(e)


0.3
0.25
0.2
0.15
0.1
0.05
$c_{oxcorr12}$
extract
scalable
D4~D9
D34~D36
D54~D56
0 1 2 3 4 5 6 7 8 9 10 11 12 13
Inductor number

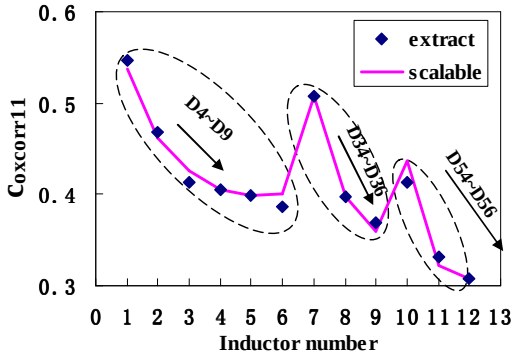
(f)


3
2.5
2
1.5
1
0.5
0
$c_{subcorr12}$
extract
scalable
D4~D9
D34~D36
D54~D56
0 1 2 3 4 5 6 7 8 9 10 11 12 13
Inductor number

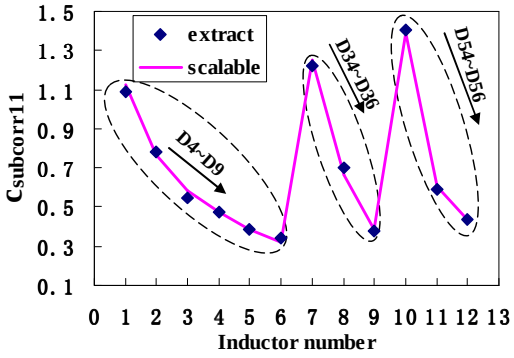
(g)


3
2.5
2
1.5
1
0.5
0
$r_{subcorr12}$
extract
scalable
D4~D9
D34~D36
D54~D56
0 1 2 3 4 5 6 7 8 9 10 11 12 13
Inductor number

(h)


extract
scalable
D4~D9
D34~D36
D54~D56
Coxcorr11
Inductor number

(i)


extract
scalable
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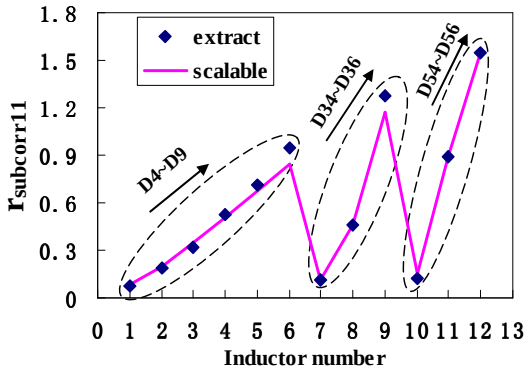
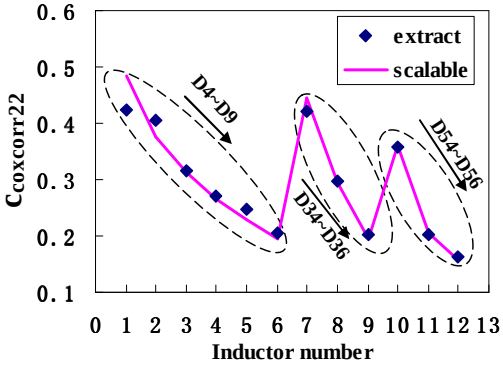
D34~D36
D54~D56
Csubcorr11
Inductor number

(j)


extract
scalable
D4~D9
D34~D36
D54~D56
rsubcorr11
Inductor number

(k)


extract
scalable
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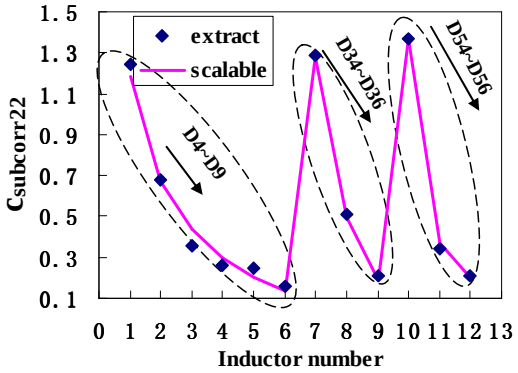
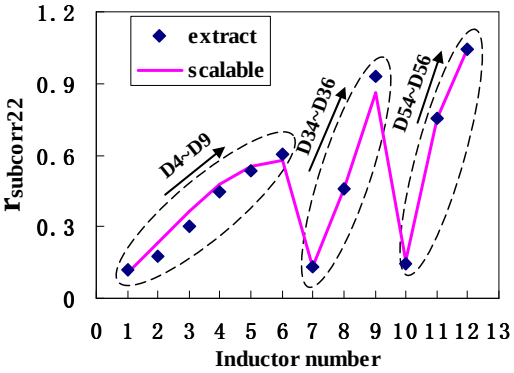
D34~D36
D54~D56
Ccoxcorr22
Inductor number

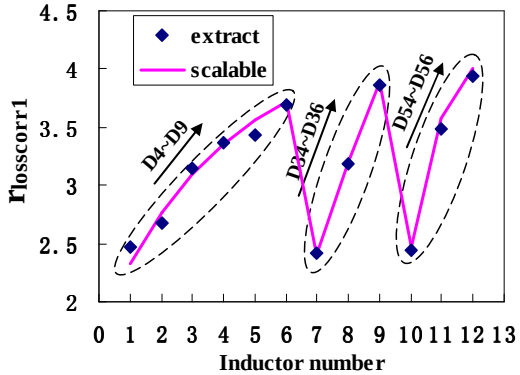
(l)


extract
scalable
D4~D9
D34~D36
D54~D56
Csubcorr22
Inductor number

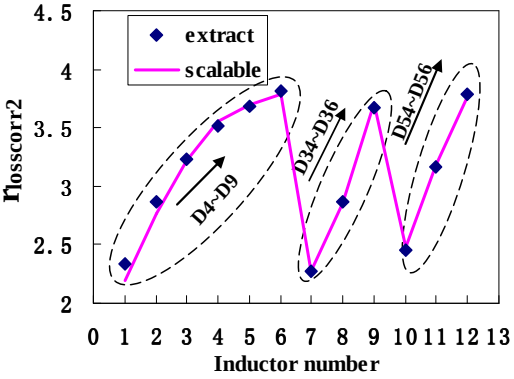
(m)


extract
scalable
D4~D9
D34~D36
D54~D56
rsubcorr22
Inductor number

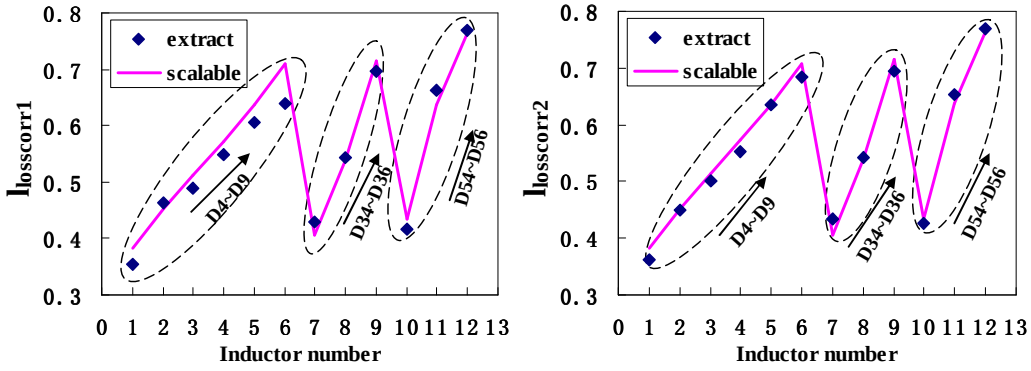
(n)


extract
scalable
D4~D9
D34~D36
D54~D56
rlosscorr1
Inductor number

(o)


extract
scalable
D4~D9
D34~D36
D54~D56
rlosscorr2
Inductor number

(p)



(q) (r)

Figure 3.20 (a) to (r): Scalable and extracted data of the model parameters.

3.4 Summary

In this chapter, the modelling approaches for RF CMOS spiral inductors are extensively investigated. Comparisons have been made through actual implementation of each model's parameter extraction procedure. The key features of the models are analyzed. The pros and cons of equivalent circuit topologies, parameter extraction techniques and fitting capacity of models are summarized. The proposals are verified by measurement of the *S*-parameters of 10 fabricated CMOS spiral inductors up to 40 GHz.

An industry-oriented fully scalable compact circuit model for on-chip spiral inductors has been proposed. The model is developed with a hierarchical structure, in which a strict partition of the geometry scaling in the global model and the model equations in the local model is defined. The major parasitic effects, including the skin effect, the proximity effect, the inductive and capacitive loss in the substrate and the distributed effect are considered and calculated using physics-based equations. The accuracy of the proposed method is validated through the excellent agreement observed up to the *SRF* between the simulated and measured results of asymmetric inductors with different geometries fabricated by a standard 0.18-μm SiGe BiCMOS technology.

3.5 References

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4

Deep N-Well RF CMOS Modelling

4.1 Introduction

The incorporation of DNW implantation into a standard CMOS technology has become a popular choice for reducing undesired interference in RF CMOS [1], [2], [3], [4]-[6]. A DNW implant is generally formed by inserting a high-energy ion implantation step before n-well formation [7]. In contrast to an RF-MOSFET without DNW implantation, the DNW actually partitions the substrate of a DNW RF-MOSFET into three parts (as seen in Figure 4.1): the DNW itself, p-well in the DNW, and the original substrate where the DNW is formed. Consequently, a back-to-back diode pair is thus formed as illustrated in Figure 4.2. When the diodes operate in the off state, there is significant resistive parasitics in the substrate. This greatly suppresses the cross-talk in the substrate [1].

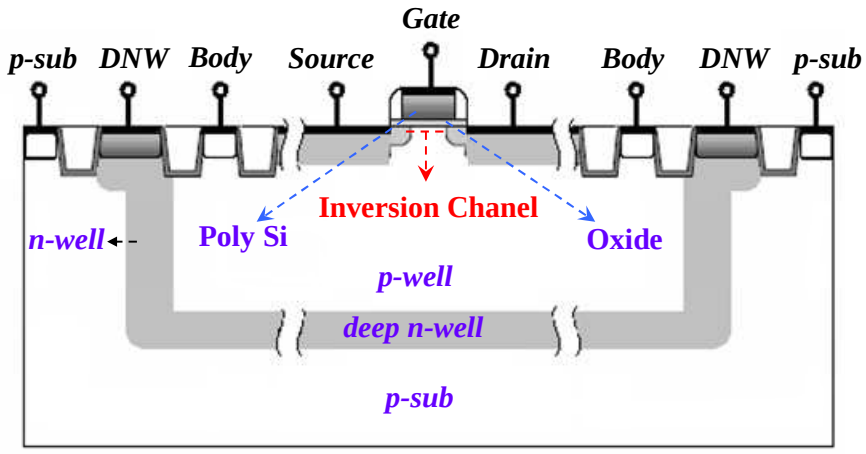


Figure 4.1: Cross section of an n-channel transistor with DNW.

It has been reported that f_t and f_{max} will be enhanced and that DC characteristics are almost not altered [8]. The DNW can also significantly improve the linearity of power amplifiers (PAs) without disturbing the power performances [5], and appears to be useful for enhancing the dc performance of CMOS RFICs [2]. Although, the many advantages of DNW implantation in CMOS technologies have been validated, a reasonable methodology for accurately extracting the substrate network parameters of DNW RF-MOSFETs has not been reported. The substrate network in CMOS is of the utmost importance in predicting the device output characteristics at radio frequencies.

Since the coupling between the DNW and the p-well, as well as between the DNW and the original substrate, exists no matter what the electrical configuration is, it must be taken into account in any realistic model. However, most previous works [9]-[21] have dealt with substrate parasitic effects in RF-MOSFETs by using resistance networks only. The capacitive coupling effect, which is physically in existence, is always neglected. Hence, the previously reported substrate models and corresponding extraction methods become too simple to accurately extract the substrate network parameters of DNW RF-MOSFETs.

Furthermore, most test structures used in measuring the substrate characteristics of RF-MOSFETs have a two-port configuration with the gate terminal serving as port one, the drain terminal defining port two and the source shorted to the p-substrate serving as the common terminal [2]–[4][8]. This configuration fails to capture the interaction between the source and bulk terminals and that between the source and the drain terminals through the bulk. Different test structures have been proposed for characterizing the distributed substrate network [5-6] [10-11], and some have employed three-port [6] or four-port measurement [11]. A common gate arrangement can help access the substrate from both the source and the drain side [5], whereas the gate network is also included during measurement via the gate-source and gate-drain admittances. Employing the on-probe capacitance of a Ground-Power-Ground (GPG) probe to ac short the extrinsic gate and bulk [10] does not suffer from the problem in [5]. However, this approach is valid only at low frequencies as the GPG probe provides a non-ideal short at higher frequencies. Furthermore, all of the test structures and measurement setups in [2]-[6][8][10-11] are developed for modelling RF-MOSFETs without DNW implantation.

In this Chapter, a simple test structure which can make the substrate network of DNW RF-MOSFETs distinctly accessible in measurement is proposed in Section 4.2. A scalable model for the substrate network of DNW RF-MOSFET with different number of fingers is developed in Section 4.2.1. Section 4.2.2 gives the model parameter

extraction method. The method and the substrate model are further verified and validated by matching the measured and simulated output admittances. Excellent agreement up to 40GHz for devices manufactured in SMIC 0.18um RF CMOS technology has been achieved in Section 4.2.3. Section 4.3 is an investigation into the avalanche breakdown effect of DNW RF-MOSFETs with non-uniform gate-finger spacing layout structures. An accurate compact modelling method is also proposed. Finally, a summary is given in Section 4.4.

4.2 Model and Extraction Method for the DNW Substrate Network

4.2.1 Equivalent Circuit Model for DNW

As seen from Figure 4.2(a), the implantation of the DNW into the nMOSFET forms a *p-well – DNW – p-sub* structure in the substrate. This is similar to a pair of back-to-back diodes (D_1 and D_2, as shown in the dashed box of the Figure 4.2(a)). These two diodes connect the p-well and p-sub. The outer terminal of the DNW is usually connected to V_{dd}. The high potential provided by V_{dd} keeps both diodes (D_1 and D_2) in turn-off status, and thereby achieves the purpose of substrate cross-talk isolation. At certain V_{dd}, the influences of D_1 and D_2 on the output characteristics of the transistor are mainly decided by their ac performance. D_1 and D_2 can be characterized by the equivalent circuit depicted in Figure 4.2(b), where C_{dnwu} and C_{dnwd} are the equivalent capacitance of D_1 and D_2, respectively, when the DNW is biased by V_{dd}. It is observed in the extracted results of a 64-finger DNW n-MOSFET (W_f= 0.18μm and L_f = 2.5μm) in Section 4.2.2 that as long as V_{dd} is kept higher than the conduction voltage of the junction diode of the transistor, C_{dnwu} and C_{dnwd} stay bias-independent.

4.2.2 Directly Extraction Method of the DNW Substrate Network

For model parameter extraction, a simple test structure is used to directly access the substrate characteristics of DNW RF-MOSFETs from two-port measurements. This test

configuration also enables one to perform a more detailed analysis of DNWs. A methodology is further developed to directly extract the parameters for the substrate network from the measured data.

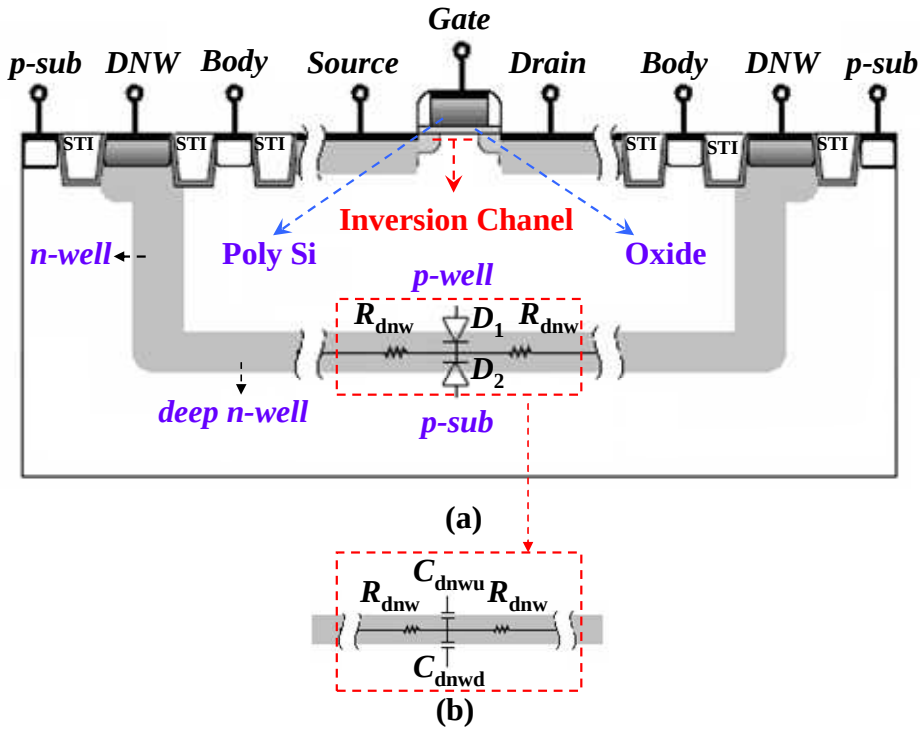


Figure 4.2: (a) Equivalent circuit model of the DNW implantation and (b) the simplified model of the DNW when the voltage of the terminal *DNW* (V_{dnw}) is connected to high V_{dd}.

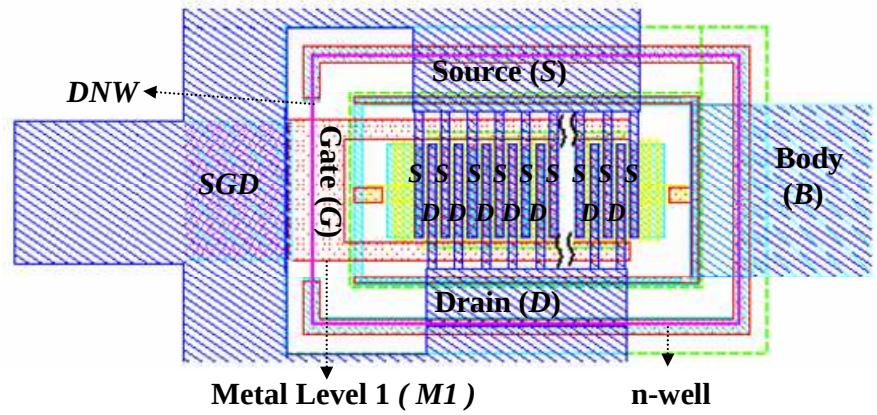


Figure 4.3: Simplified layout plane figure of the proposed test structure for DNW nMOSFETs. Two different DNW configuration methods, the DNW floating and the DNW grounded are used for the two-port measurement in substrate network component extraction in this work.

A simplified layout plane figure of the proposed test structure for DNW nMOSFETs is

given in Figure 4.3. The test structure with the *S*, *D* and *G* terminals all connected together is used as port one, while the bulk terminal is port two, and the p-substrate is grounded, making the substrate network distinctly accessible in measurements.

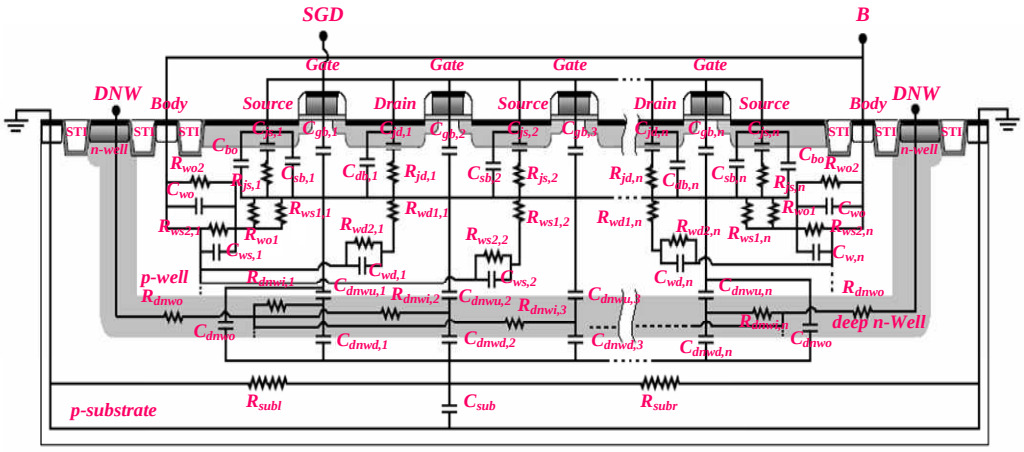


Figure 4.4: Equivalent circuit for substrate resistance and capacitance networks of a multi-finger (N_f) DNW RF-MOSFET with all the source (*S*), drain (*D*) and gate (*G*) terminals for different fingers connected together when the junction diodes are turned off. Source, drain, and gate resistances are ignored for their slight contribution to the output impedance.

Figure 4.4 shows the substrate network of devices under the proposed test configuration when the junction diodes are turned off. In Figure 4.4, $C_{js,i}$, $C_{jd,i}$ are each *S/D* junction region capacitors, $R_{js,i}$, $R_{js/jd,i}$ are each *S/D* junction resistors. C_{dnwo}, which combined with C_{wo}, C_{bo}, $R_{\text{wo1,}}$ R_{wo2} and $R_{\text{wo,}}$ is used to capture the difference between the inner and outer *S/D* regions in this work. $C_{\text{dnwu,i}}$ and $C_{dnwd,i}$ represent the p-well-to-DNW and the DNW-to-p-substrate capacitors under each finger region. $C_{\text{ws,i}}$ and $C_{\text{wd,i}}$ are each finger capacitors from the bottom of the *S/D* regions to *B* within the deep n-well. $R_{\text{ws1,i}}$, $R_{\text{wd1,i}}$, $R_{\text{ws2,i}}$ and $R_{\text{wd2,i}}$ represent the single finger resistors between the bottom of the *S/D* region and *B*. $C_{\text{sb,i}}$, $C_{\text{db,i}}$ and $C_{\text{gb,i}}$ are the *S*-to-*B*, *D*-to-*B* and *G*-to-*B* and capacitors of each finger region, R_{subl}, R_{subr} and C_{sub} are the capacitor and the resistor of the p-substrate, $R_{\text{dnw,i}}$ represent the resistors of the DNW under each finger region. R_{dnwo} represents the n-well ring resistor.

Based on the equivalent circuit identified in Figure 4.4, the following relationships can

be obtained for any number of fingers

$$C_{js/jd} = \sum_{i=1}^{N_{s/d}} C_{js/jd,i} \tag{4.1a}$$

$$R_{js/jd}^{-1} = \sum_{i=1}^{N_{s/d}} R_{js/jd,i}^{-1} \tag{4.1b}$$

$$C_{sgdb} = \sum_{i=1}^{N_f} \left[C_{sb,i} + C_{gb,i} + C_{db,i} \right] \tag{4.1c}$$

$$C_{ws/wd} \approx \sum_{i=1}^{N_{s/d}} C_{ws/wd,i} \tag{4.1d}$$

$$R_{ws1/wd1}^{-1} = \sum_{i=1}^{N_{s/d}} R_{ws1/wd1,i}^{-1} \tag{4.1e}$$

$$R_{sub}^{-1} = R_{subl}^{-1} + R_{subr}^{-1} \tag{4.1f}$$

$$R_{ws2/wd2}^{-1} = \sum_{i=1}^{N_{s/d}} R_{ws2/wd2,i}^{-1} \tag{4.1g}$$

$$C_{dnwu} = \sum_{i=1}^{N_f} \left[C_{dnwu,i} \right] \tag{4.1h}$$

$$C_{dnwd} = \sum_{i=1}^{N_f} \left[C_{dnwd,i} \right] \tag{4.1i}$$

$$R_{dnw} = 2R_{dnwo} + \left[\sum_{i=1}^{N_f} \left[R_{dnw,i}^{-1} \right] \right]^{-1} \tag{4.1j}$$

where C_{js} and C_{jd} represent the total *S/D* junction region capacitances. R_{js} and R_{jd} represent the total *S/D* junction resistances. R_{sub} represents the total resistance of the p-substrate. C_{dnw} represents the total capacitance caused by the DNW. C_{ws} and C_{wd} are the total capacitances from the bottom of the *S/D* regions to *B* within the deep n-well. $R_{\text{ws1/wd1}}$ and $R_{\text{ws2/wd2}}$ are the total resistances between the bottom of the *S/D* regions and *B* within the deep n-well. N_s and N_d represent the numbers of source and drain diffusion regions, respectively. In our model, when the number fingers is odd, $N_s = N_d = (N_f + 1)/2$,

while $N_s = N_f/2+1$ and $N_d = N_f/2$ when the number of fingers is even.

Assuming that there are no differences in the inner *S/D* regions, the above equations, (4.1a)-(4.1j), can be simplified as

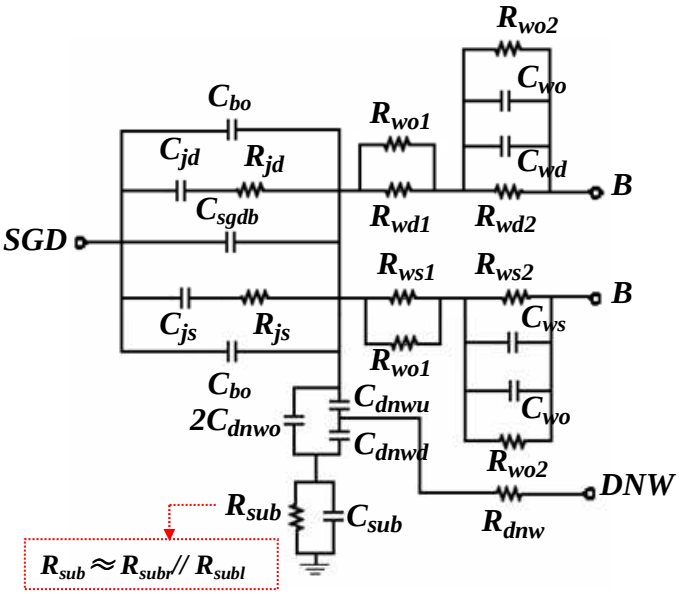


Figure 4.5: Simplified equivalent circuit of multi-finger RF-MOSFETs with S/G/D terminals connected together.

$$C_{js/jd} = N_{s/d} C_{j,i} \tag{4.2a}$$

$$R_{js/jd} = R_{j/i} / N_{s/d} \tag{4.2b}$$

$$C_{sgdb} = N_f \left[2C_{sdb,i} + C_{gb,i} \right] \tag{4.2c}$$

$$C_{ws/wd} = N_{s/d} C_{w,i} \tag{4.2d}$$

$$R_{ws1/wd1} = \frac{R_{w1,i}}{N_{s/d}} \tag{4.2e}$$

$$R_{ws2/wd2} = \frac{R_{w2,i}}{N_{s/d}} \tag{4.2f}$$

$$C_{dnwu} = N_f C_{dnwu,i} \tag{4.2g}$$

$$C_{dnwd} = N_f C_{dnwd,i} \tag{4.2h}$$

$$R_{dnw} = 2R_{dnwo} + \frac{R_{dnwi}}{N_f} \tag{4.2i}$$

where $C_{j,i} = C_{js,i} = C_{jd,i}$, $R_{j,i} = R_{js,i} = R_{jd,i}$, $C_{sdb} = C_{sb,i} = C_{db,i}$, $C_{w,i} = C_{ws,i} = C_{wd,i}$, $R_{w1,i} = R_{ws1,i} = R_{wd1,i}$ and $R_{w2,i} = R_{ws2,i} = R_{wd2,i}$.

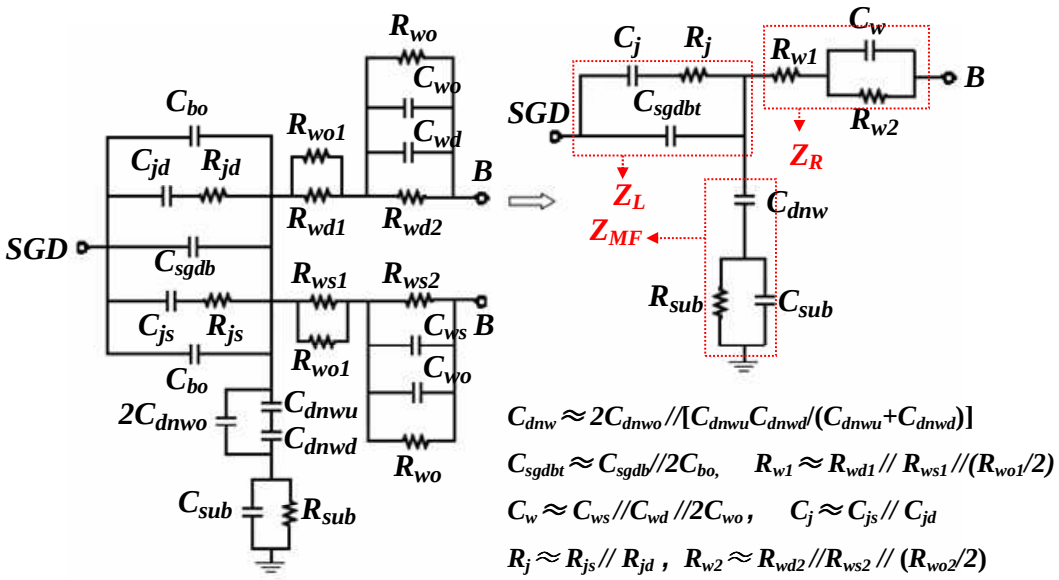


Figure 4.6: (a) Equivalent circuit for multi-finger DNW RF-MOSFETs with the DNW floating and S/G/D terminals connected together. R_{dnw} is ignored for its slight influence on two-port measurement. (b) Simplified equivalent circuit for parameter extraction.

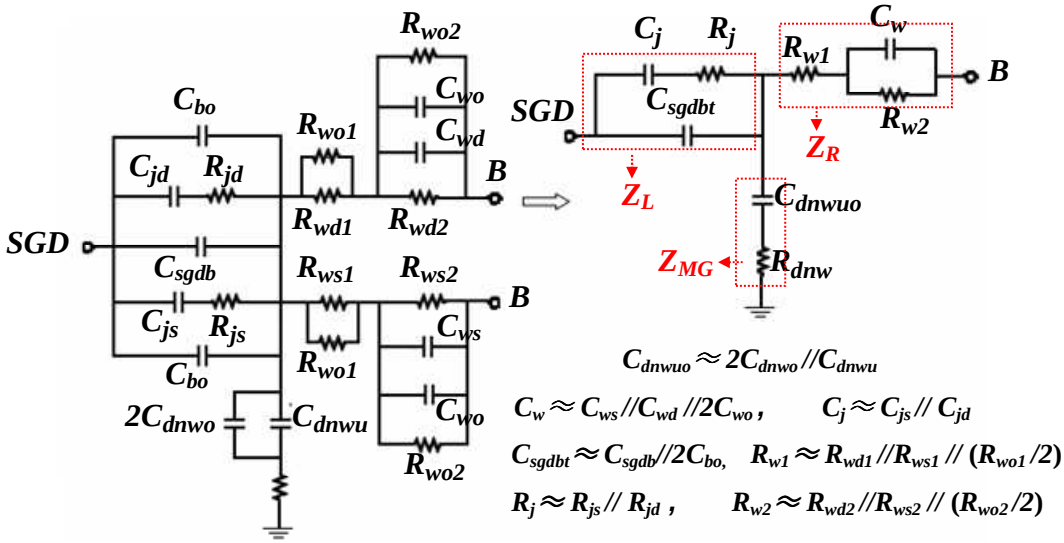


Figure 4.7: (a) Equivalent circuit model for DNW RF-MOSFETs with the DNW grounded and S/G/D terminals connected together. (b) Simplified equivalent circuit for parameter extraction.

In this section, the following equations are used to empirically model the N_f-dependence of R_{sub} and C_{sub}

$$R_{sub} = R_{subI} + N_f R_{subunit} \tag{4.2j}$$

$$C_{sub} = C_{subI} + N_f C_{subunit} \tag{4.2k}$$

where R_{subI} and C_{subI} represent the p-substrate resistance and capacitance of a one-finger device. $R_{subunit}$ and $C_{subunit}$ are used to explain the increase of R_{sub} and C_{sub} with an increase in the number of gate fingers.

In order to accurately predict the scalability of the substrate elements, a direct parameter extraction methodology is of the utmost importance. In this work, two different test configurations are employed to extract all of the parameters of the scalable model derived above. One has the DNW floating and the other has the DNW grounded. In each case, all *S/D/G* terminals for different fingers are connected together as port one, the *B* terminal is port two, and the p-substrate is grounded. The equivalent circuits shown in Figure 4.6 (a) and Figure 4.7 (a) can easily be derived from the complete equivalent circuit shown in Figure 4.5, and used for modelling the above two test structures (e.g., with the DNW in grounded or float configuration, respectively).

As seen from Figure 4.6 (a) and Figure 4.7 (a), since the topology from *S* to *B* is the same as that from *D* to *B*, both of the equivalent circuits shown in Figure 4.6 (a) and Figure 4.7 (a) can be reduced to *T*-networks by using simple approaches as shown at the bottom of Figure 4.6 (b) and Figure 4.7 (b). Based on (4.2a) - (4.2k) and the approaches used to simplify Figure 4.6 (a) and Figure 4.7 (a) to Figure 4.6 (b) and Figure 4.7 (b), respectively, the elements of the two *T*-networks shown in Figure 4.6 (b) and Figure 4.7 (b) can be calculated with the following equations

$$C_j = (N_f + 1)C_{j,i} \tag{4.3a}$$

$$R_j = R_{j,i} / \left(N_f + 1 \right) \tag{4.3b}$$

$$C_w = 2C_{wo} + \left(N_f + 1 \right) C_{w,i} \tag{4.3c}$$

$$R_{w1} = \frac{0.5 R_{wo1} R_{w1,i} / \left(N_f + 1 \right)}{0.5 R_{wo1} + R_{w1,i} / \left(N_f + 1 \right)} \tag{4.3d}$$

$$R_{w2} = \frac{0.5 R_{wo2} R_{w2,i} / \left(N_f + 1 \right)}{0.5 R_{wo2} + R_{w2,i} / \left(N_f + 1 \right)} \tag{4.3e}$$

$$C_{sgdbt} = 2C_{bo} + N_f \left[2C_{sdb,i} + C_{gb,i} \right] \tag{4.3f}$$

$$C_{dnwuo} = 2C_{dnwo} + N_f C_{dnwu,i} \tag{4.3g}$$

$$C_{dnw} = 2C_{dnwo} + N_f C_{dnw,i} \tag{4.3h}$$

where

$$C_{dnw,i} = \frac{C_{dnwu,i} C_{dnwd,i}}{C_{dnwu,i} + C_{dnwd,i}} \tag{4.3h.1}$$

Using (4.3h.1), $C_{\mathrm{dnwu,i}}$ can be calculated as

$$C_{dnwd,i} = \frac{C_{dnwu,i} C_{dnw,i}}{C_{dnwu,i} - C_{dnw,i}} \tag{4.3h.2}$$

(4.2c), (4.2g) - (4.2j) and (4.3a) - (4.3h) give the N_f-dependent equations of the equivalent circuit in Figure 4.5. This enables the direct extraction of the scalable substrate components as will become clear in the equivalent circuit analysis which follows later in this section.

As the Z_{L} and Z_{R} of the T-network shown in Figure 4.6 (b) is the same as the Z_{L} and Z_{R} shown in Figure 4.7 (b), with the ground terminal as reference, the Z-parameters of the T-networks shown in Figure 4.6 (b) and Figure 4.7 (b) can be calculated approximately with the following equations

$$[Z_L]^{-1} = [Z_{dnw\_floating,11} - Z_{dnw\_floating,12}]^{-1} = [Z_{dnw\_grounded,11} - Z_{dnw\_grounded,12}]^{-1}$$

$$= \frac{\omega^2 C_j^2 R_j}{1+\omega^2 C_j^2 R_j^2} + j\frac{\omega C_j}{1+\omega^2 C_j^2 R_j^2} + j\omega C_{sgdb} \tag{4.4a}$$

$$Z_R = Z_{dnw\_floating,22} - Z_{dnw\_floating,12} = Z_{dnw\_grounded,22} - Z_{dnw\_grounded,12}$$

$$= R_{w1} + \frac{R_{w2}}{1+\omega^2 R_{w2}^2 C_w^2} - j\omega\frac{R_{w2}^2 C_w}{1+\omega^2 R_{w2}^2 C_w^2} \tag{4.4b}$$

$$Z_{MF} = Z_{dnw\_floating,12} = \frac{R_{sub}}{1+\omega^2 R_{sub}^2 C_{sub}^2} - j\omega\frac{R_{sub}^2 C_{sub}}{1+\omega^2 R_{sub}^2 C_{sub}^2} - j\frac{1}{\omega C_{dnw}} \tag{4.4c}$$

$$Z_{MG} = Z_{dnw\_grounded,12} = R_{dnw} + \frac{1}{j\omega C_{dnwuo}} \tag{4.4d}$$

where $Z_{dnw\_floating}$ and $Z_{dnw\_grounded}$ are the measured Z-parameters of DNW RF-MOSFETs with the S/G/D terminals connected together and the DNW is floating or grounded, respectively.

Further, the real and imaginary parts of the above *Z*-parameter expressions can be rearranged as

$$\frac{\omega^2}{\mathrm{Re}\{[Z_L]^{-1}\}} = \omega^2 R_j + \frac{1}{C_j^2 R_j} \tag{4.5a}$$

$$C_{sgdb} = \omega^{-1}\left\{\mathrm{Im}\{[Z_L]^{-1}\} - \frac{\omega C_j}{1+\omega^2 C_j^2 R_j^2}\right\} \tag{4.5b}$$

$$-\frac{\omega}{\mathrm{Im}[Z_R]} = \omega^2 C_w + \frac{1}{R_{w2}^2 C_w} \tag{4.5c}$$

$$R_{w1} = \mathrm{Re}[Z_R] - \frac{R_{w2}}{1+\omega^2 R_{w2}^2 C_w^2} \tag{4.5d}$$

$$\{\mathrm{Re}[Z_{MF}]\}^{-1} = R_{sub}^{-1} + \omega^2 R_{sub} C_{sub}^2 \tag{4.5e}$$

$$C_{dnw} = -\{\omega[\mathrm{Im}[Z_{MF}] + \omega R_{sub}^2 C_{sub}/(1+\omega^2 R_{sub}^2 C_{sub}^2)]\}^{-1} \tag{4.5f}$$

$$R_{dnw} = \mathrm{Re}[Z_{MG}] \tag{4.5g}$$

$$[-\mathrm{Im}(Z_{MG})]^{-1} = \omega C_{dnwuo} \tag{4.5h}$$

By using (4.5a) and (4.5c), R_j and C_w can be extracted from the slopes of the plots of the

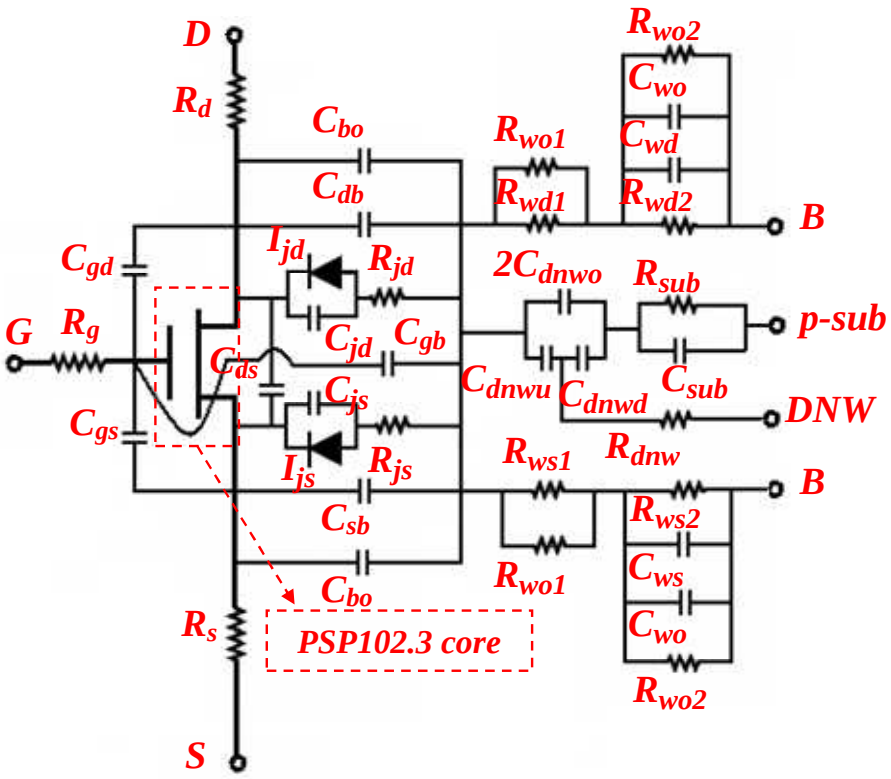


Figure 4.8: Macro-model for DNW RF-MOSFET modelling.

experimental $\omega^2 / \mathrm{Re}\{[Z_L]^{-1}\}$ and $-\omega / \mathrm{Im}[Z_R]$ versus ω^2, respectively. Equation (4.5a) and (4.5c) give C_j and R_{w2}, after inserting R_j and C_w,. Further, (4.5b) and (4.5d) give C_{sgdb} and R_{w1}. Using (4.5e), R_{sub} and C_{sub} can be determined from the intercept and slope of the plot of the experimental $1/\mathrm{Re}[Z_{MF}]$ versus ω^2. The slope gives C_{sub} after inserting R_{sub}. After inserting R_{sub} and C_{sub}, (4.5f) gives C_{dnw}. Using (4.5h), C_{dnwuo} can be extracted from the slope of the plot of the experimental Im(Z_{MG}) versus ω, while (4.5g) gives R_{dnw} directly. Thus, all elements of the equivalent circuit of Figure 4.6 (b) and/or Figure 4.7 (b) are extracted.

4.2.3 Macro-model, Model Parameter Extraction and Verification

For compact modelling, a macro-model for DNW RF-MOSFET modelling is given in Figure 4.8. The model consists of the PSP102.3 model core with the proposed new substrate-network. In Figure 4.8, R_g, R_d and R_s are the gate (*G*), drain (*D*) and source (*S*) resistors. C_{js} and C_{jd} are the junction capacitances of source/drain (*S/D*) regions with the embedded p-well. C_{gb}, C_{db}, C_{sb} and C_{bo} indicate the extrinsic gate-to-body (*G*-to-*B*), drain-to-body (*D*-to-*B*), source-to-body (*S*-to-*B*) capacitance and the edge drain/source-to-body (*D/S*-to-*B*) capacitance. R_{js} and R_{jd} are resistances of the p-well under the *S* and *D* regions, respectively. C_{dnwu} represents the capacitance between the p-well and the DNW, C_{dnwd} represents the capacitance between the DNW and the p-substrate, while C_{dnwo} represents the edge capacitance of the DNW. R_{wo1}, R_{wo2}, R_{wd1}, R_{wd2}, R_{ws1} and R_{ws2} are introduced to capture the Drain-to-Body and Source-to-Body resistive parasitics. R_{dnw} is the resistance caused by DNW itself. R_{sub} represents the p-substrate resistance. Capacitances, C_{wd} C_{ws}, C_{wo} and C_{sub} are introduced to capture the capacitive coupling effect in the p-well and p-substrate.

For model verification, two different test structures for nine devices with different number of fingers were fabricated using the SMIC 0.18µm 1P6M RF-CMOS process (N_f of each device is 1, 2, 4, 8, 16, 24, 32, 48 and 64. The length (L_f) and width (W_f) for each gate finger are fixed at 0.18µm and 2.5µm). The DNW is either floating or grounded. The metal level 1 (M1) is used to connect all the *S/D/G* terminals for different fingers together as port one, while the *B* terminal is port two for two-port RF measurement.

The two-port *S*-parameters were measured and de-embedded (Open + Short) for parasitics introduced by the GSG PAD using an Agilent E-8363B Network Analyzer and a CASCADE Summit probe station. Then, the de-embedded *S*-parameters were transformed to *Z*-parameters for directly extracting all of the parameters of the *T*-networks shown in Figure 4.6 (b) and Figure 4.7 (b) using the parameter extraction methodology developed in Section 4.2.2.

When the junction voltage of the *p-well – DNW – p-sub* diode becomes significant, the equivalent circuits in Figure 4.6 (a) and Figure 4.7 (a) and their corresponding parameter values are less reasonable. Therefore, it is recommended that the substrate network be extracted at a smaller voltage than V_{jth}. The extraction of the substrate network parameters at $V_B < (V_{jth} - 0.3V)$ and $V_{SGD} = 0V$, gives a more realistic value based on experimental evidence. The detailed extraction procedure is illustrated for a 64-finger DNW nMOSFET ($L_f = 0.18\mu m$ and $W_f = 2.5\mu m$ for each finger) in Figures 4.9 to Figure 4.12. Excellent linear regressions validated the accuracy of the parameter extraction methodology developed in this section. Similar extraction procedures are finally used for substrate parameter value extraction for the nine fabricated devices with different number of fingers at $V_B = -1V$ and $V_{SGD} = 0V$. The extracted results are plotted in Figure 4.13.

Once R_j, C_j, C_w, R_{w1}, R_{w2}, C_{sgdbt}, R_{dnw}, R_{sub}, C_{sub}, C_{dnwuo} and C_{dnw} are extracted, by using (4.3a)-(4.3h) and (4.2i), $R_{j,i}$, $C_{j,i}$, C_{wo}, $C_{w,i}$, R_{wo1}, $R_{w1,i}$, R_{wo2}, $R_{w2,i}$, C_{bo}, $(2C_{sdbi} + C_{gbi})$, R_{dnwo}, R_{dnwi}, R_{subI}, $R_{subunit}$, C_{subI}, $C_{subunit}$, C_{dnwo}, C_{dnwui} and C_{dnwi} can be obtained with a simple optimization procedure from the relationships between the total extracted results and N_f. After determining C_{dnwui} and C_{dnwi}, (4.3h.2) gives $C_{dnwd,i}$. Thus, (4.2a)-(4.2k) and (4.3a)-(4.3h) become only $N_{s/d}$ – and N_f – dependence equations. Table 4.1 gives the extracted scalable model parameter values. The comparisons between the extracted substrate resistances and capacitances of the nine DNW nMOSFETs and the modeled results simulated on the extracted parameter values shown in Table 4.1 are depicted in Figure 4.13. The excellent agreement between the extracted and modeled N_f - dependent substrate network components verifies that the proposed scalable model ((4.3a-4.3h)) can accurately describe the scalabilities of the substrate network components of DNW MOSFETs.

In Figure 4.8, the parameters of the PSP102.3 model core are extracted according to the standard model parameter extraction procedure as described in [22]. A conventional method developed in [23] is used to extract the initial values of three terminal series resistances R_g, R_d and R_s from de-embedded *Y*-parameters. By using the extraction

method proposed in [23], the following equations are employed for the remaining component extraction from the two-port measurement of devices with the *G* terminal defining port one, the *D* terminal defining port two and the *S*, *B*, *DNW* and the *p-substrate* connected together with ground serving as the common terminal (i.e. common-source test configuration) configurations:

$$C_{gd} = \frac{\mathrm{Im}(Y_{12}\})}{\omega} \tag{4.6a}$$

$$C_{gs} = C_{gd} \tag{4.6b}$$

$$C_{gb} = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega} - C_{gd} \tag{4.6c}$$

According to (4.1c), the total C_{gb} of an RF-MOSFET when the number of fingers is N_f can be calculated as follows:

$$C_{gb} = N_f C_{gb,i} \tag{4.6d}$$

Thus, $C_{gb,i}$ can be extracted for two or more devices with different number of fingers. Once $C_{gb,i}$ is obtained, (4.3f) gives $C_{sdb,i}$.

$$C_{sdb,i} = \frac{\left|C_{sgdbt} - 2C_{bo} - N_f C_{gb,i}\right|}{2N_f} \tag{4.6e}$$

The extracted value for $C_{sdb,i}$ for multi-finger devices with the length (*L)* and width *(W)* for each finger fixed at 0.18μm and 2.5μm, is 0.285 *f*F. C_{ds} in Figure 4.8 is calculated from de-embedded *Y*-parameters of the common-source connected nMOSFET as follows:

$$C_{ds} = \frac{\mathrm{Im}(Y_{22} - Y_{12})}{\omega} - \frac{C_d (C_s + C_t)}{C_d + C_s + C_t} \tag{4.6f}$$

where $C_d = C_{jd} + C_{bo} + C_{db}$, $C_s = C_{js} + C_{bo} + C_{sb}$,

$$C_t = 2C_{wo} + C_{wd} + C_{ws} + \frac{C_n C_{sub}}{C_n + C_{sub}} \text{ and } C_n = 2C_{dnwo} + \frac{C_{dnwu} C_{dnwd}}{C_{dnwu} + C_{dnwd}}.$$

Table 4.1: Extracted parameter values of the proposed model of the substrate network in DNW RF-MOSFETs

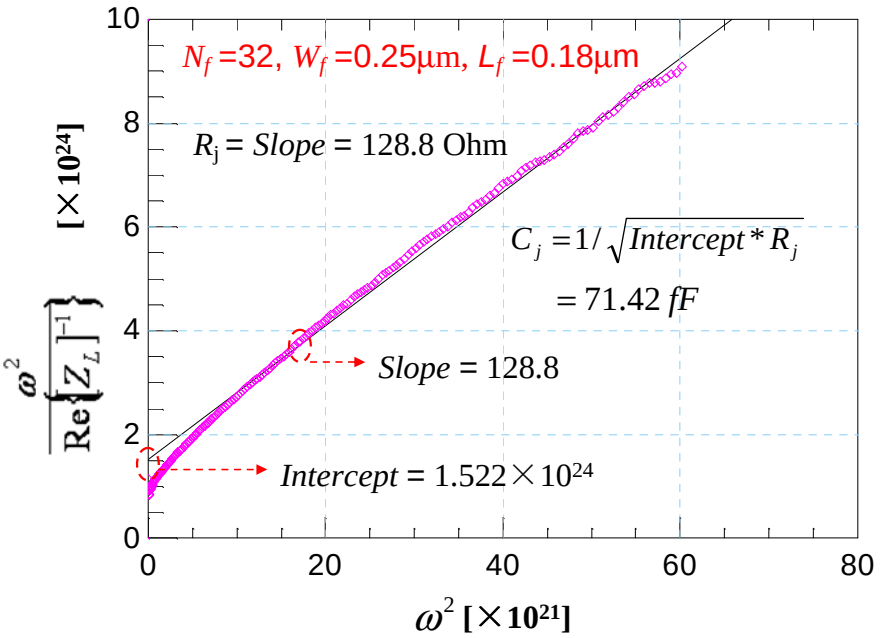
$R_{j,i}(\Omega)$	$C_{j,i}(fF)$	$C_{wo}(fF)$	$C_{w,i}(fF)$	$R_{wo1}(\Omega)$
4162	2.395	30.64	0.737	87.78
$R_{wo2}(\Omega)$	$R_{w2,i}(\Omega)$	$C_{bo}(fF)$	$2C_{sdbi}+C_{gbi}(fF)$	
203.7	2775	5.471	0.908	
$R_{dnwi}(\Omega)$	$R_{subI}(\Omega)$	$R_{subunit}(\Omega)$	$C_{subI}(fF)$	$C_{subunit}(fF)$
73.79	282.8	0.137	26.18	0.11
$C_{dnwui}(fF)$	$C_{dnwdi}(fF)$	$R_{w1,i}(\Omega)$	$R_{dnwo}(\Omega)$	$C_{dnwo}(fF)$
5.045	4.771	447.7	3.46	15.2

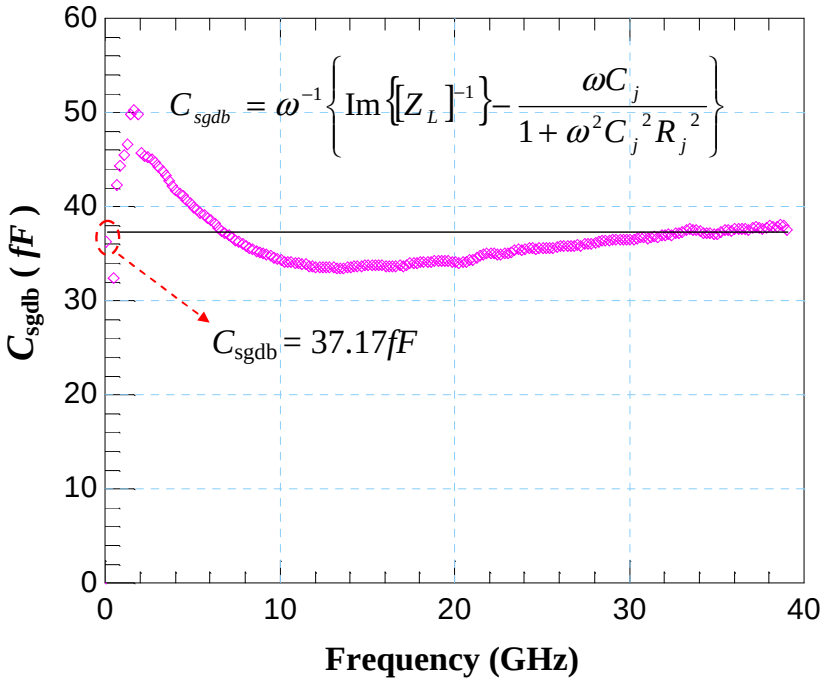
Table 4.2: Values of the extracted external capacitors from common source connected devices with different N_f at zero bias. (L_f = 0.18μm; W_f = 2.5μm)

N_f	$C_{gs/d}$ (*fF*)	C_{gb} (*fF*)	C_{ds} (*fF*)
1	0.66	3.4	0.68
2	3.5	4.2	1.02
4	3.9	7.2	3.1
8	8.6	8.5	10.7
16	18.4	10.3	24.1
24	28.3	13.2	41.2
32	36.1	15.5	54.6
48	55.4	16.2	83.4
64	72.2	17.5	110.2

The external capacitances in Figure 4.8 (i.e. C_{gd}, C_{gs} and C_{ds}) extracted from the nine devices with different N_f at zero-bias condition (V_G = 0V; V_D = 0V and $V_{S/B/DNW}$ = 0V) are listed in Table 4.2.

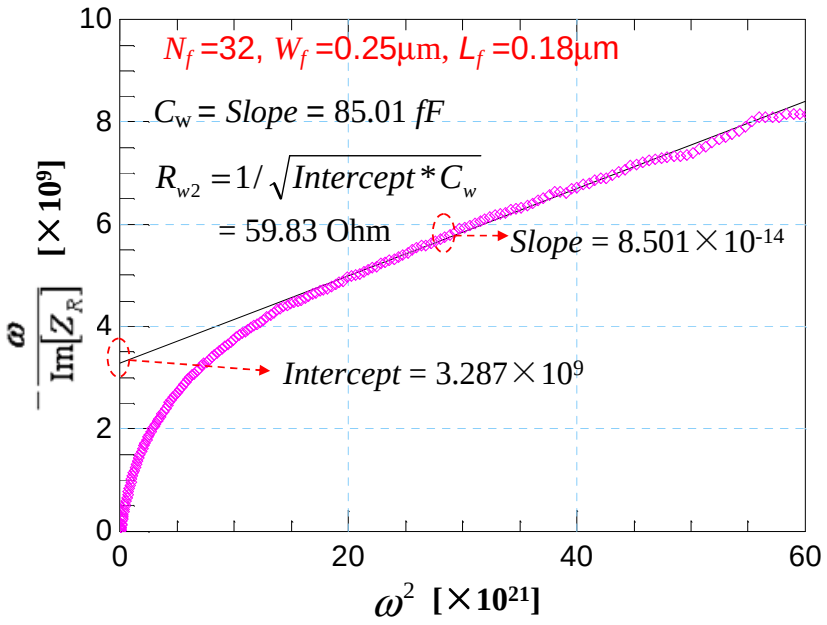
After all of the parameters have been extracted, the proposed macro-model is simulated based on the extracted parameters in Agilent Advanced Design System (ADS) directly.

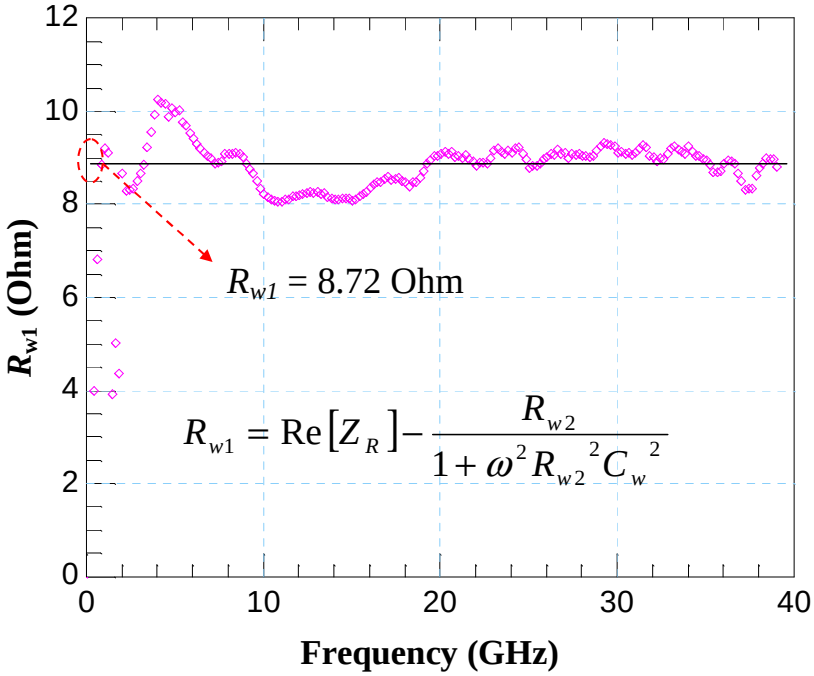




$$Z_L = Z_{dnw\_grounded,11} - Z_{dnw\_grounded,12}$$

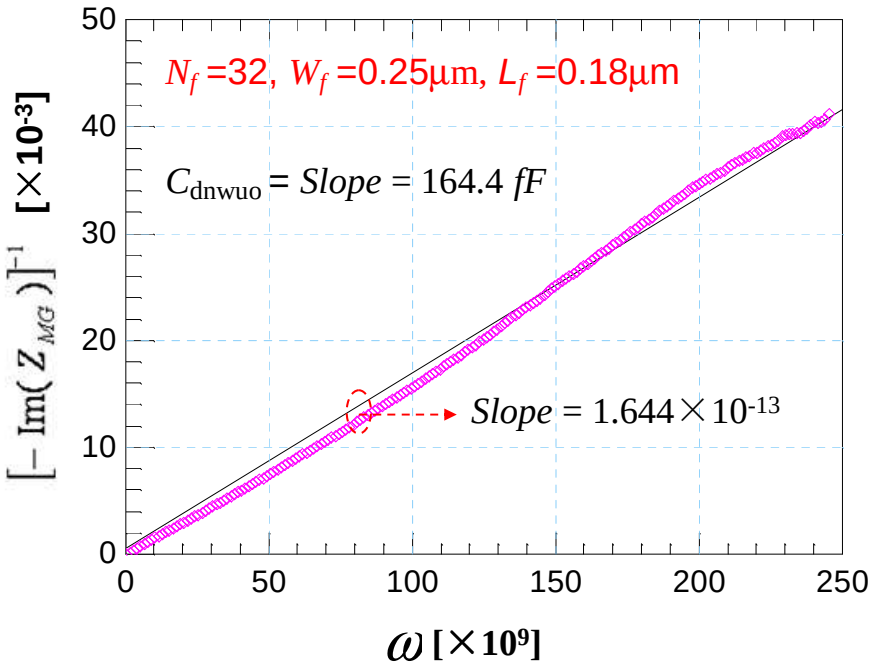
Figure 4.9: Determine R_j (top) from the slope of the linear regression of the experimental $\omega^2/\mathrm{Re}\{[Z_L]^{-1}\}$ versus ω^2. C_j can be calculated from the intercept. Once R_j and C_j are determined, (4.5b) gives C_{sgdb} (bottom).

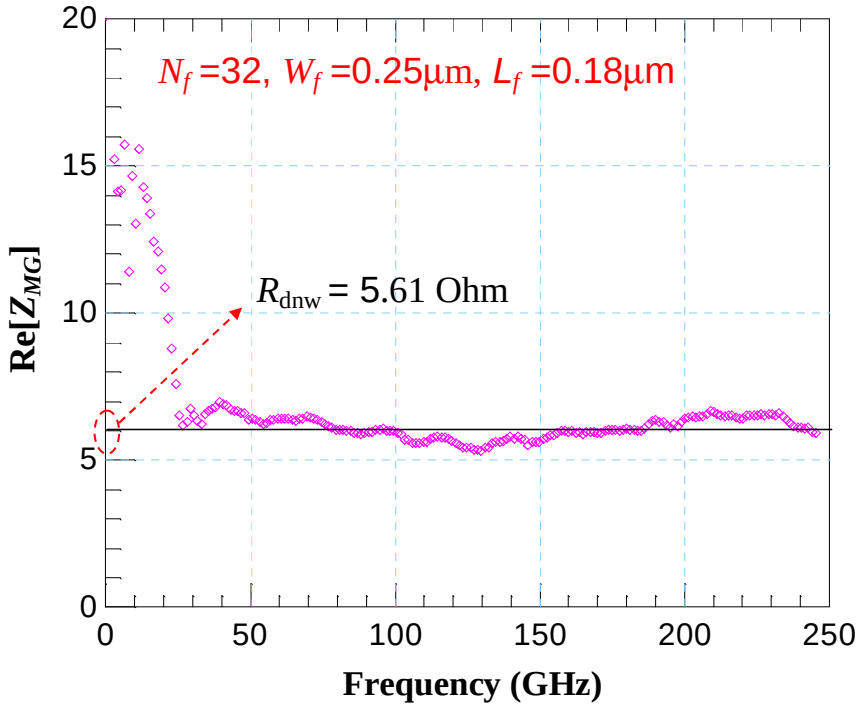




$$Z_R = Z_{dnw\_grounded,11} - Z_{dnw\_grounded,12}$$

Figure 4.10: Extract C_w (top) from the slope of the linear regression of the experimental versus $-\omega/\mathrm{Im}[Z_R]$ versus ω^2. R_{w2} can be extracted from the intercept. Once R_{w1} and C_w are determined, (4.5d) gives R_{w1} (bottom).





$$Z_{MG} = Z_{dnw\_grounded,12}$$

Figure 4.11: Extract C_{dnwuo} (top) from the slope of the linear regression of the experimental -Im[Z_{MG}]$^{-1}$ versus ω. R_{dnw} can be determined from the real part of Z_{MG} (bottom).

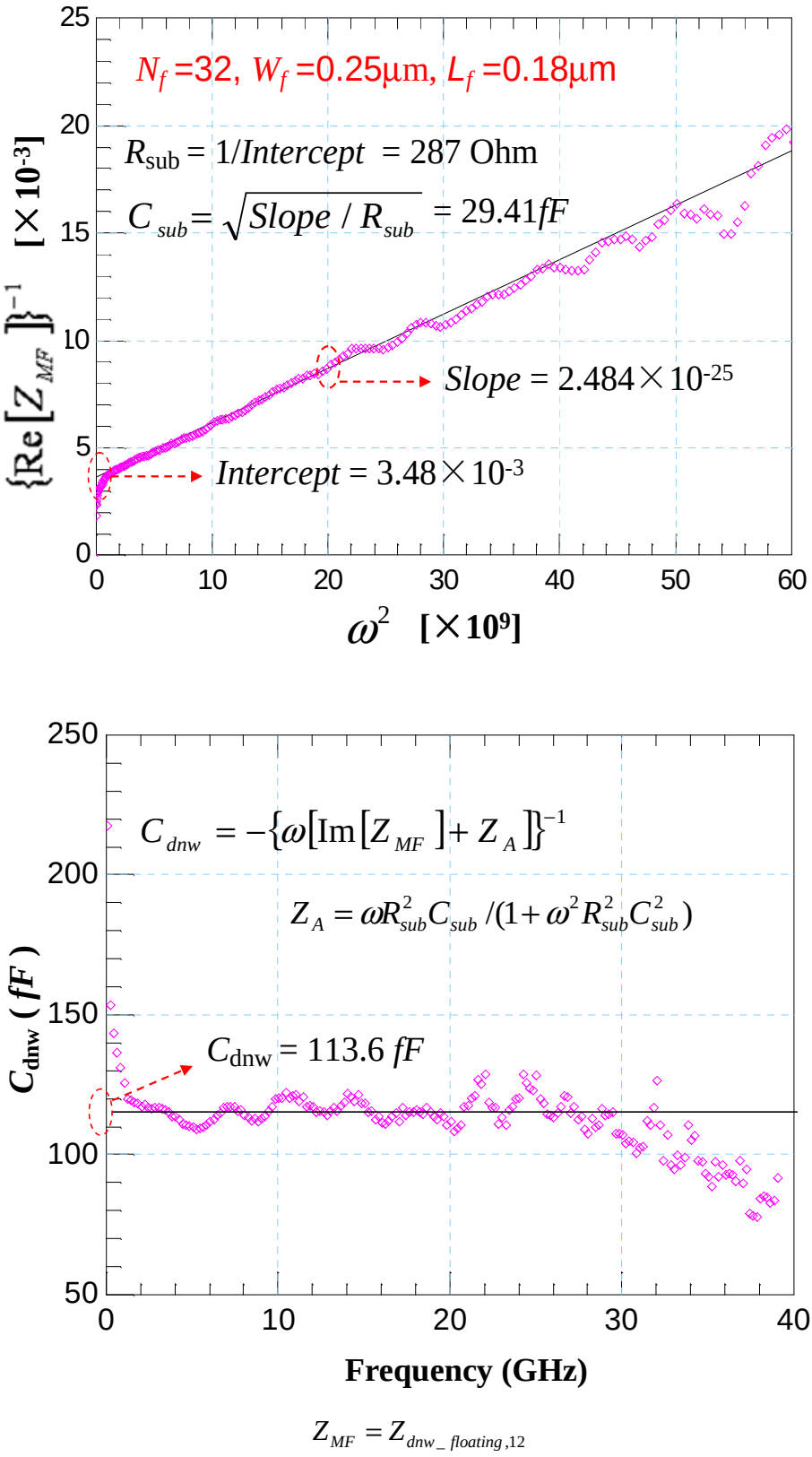


Figure 4.12: Extract R_{sub} (top) from the intercept of the experimental $\{\mathrm{Re}[Z_{MF}]\}^{-1}$ versus ω^2, and the slope gives C_{sub} after subtracting R_{sub}. Once R_{sub} and C_{sub} are determined, (4.5f) gives C_{dnw} (bottom).

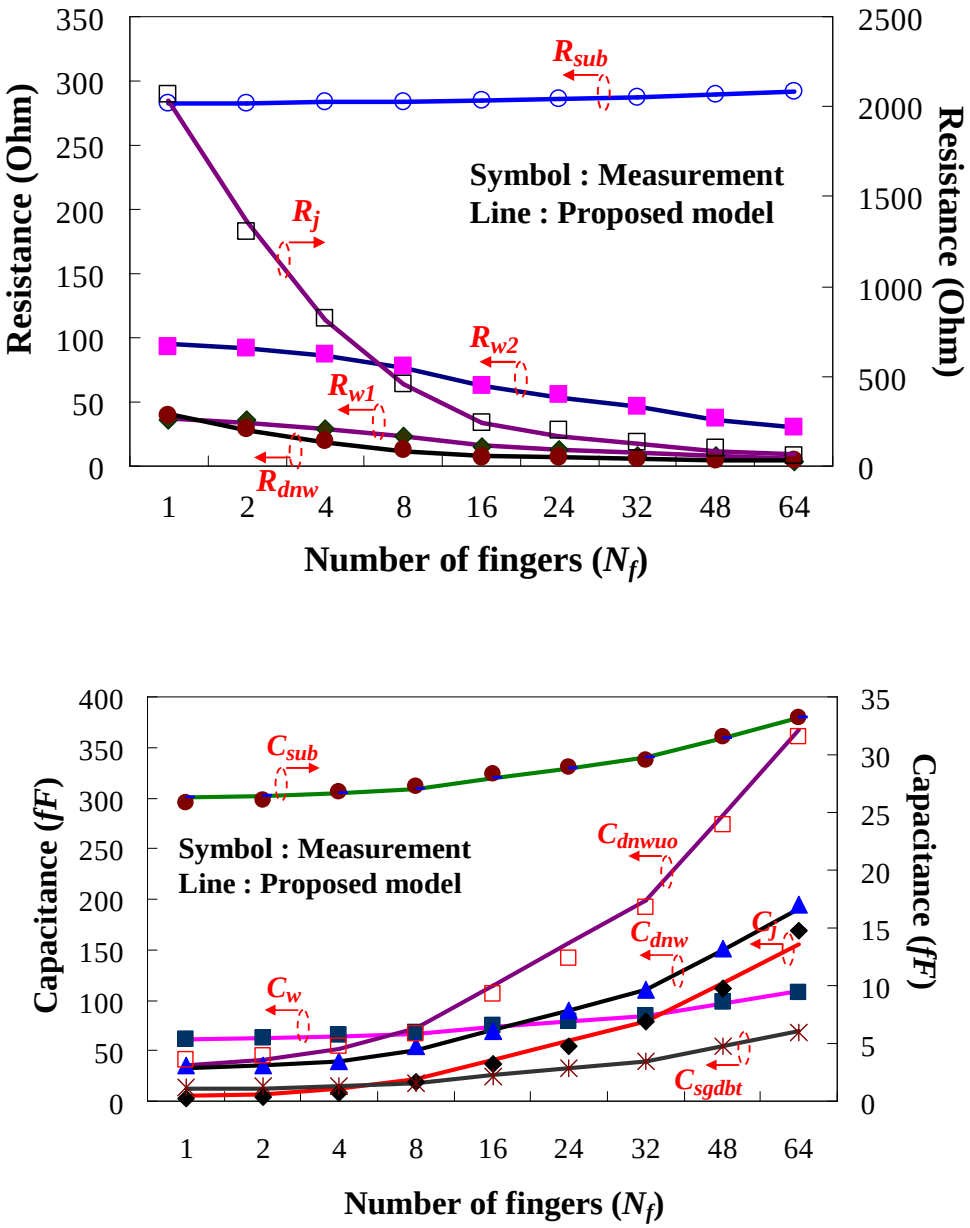
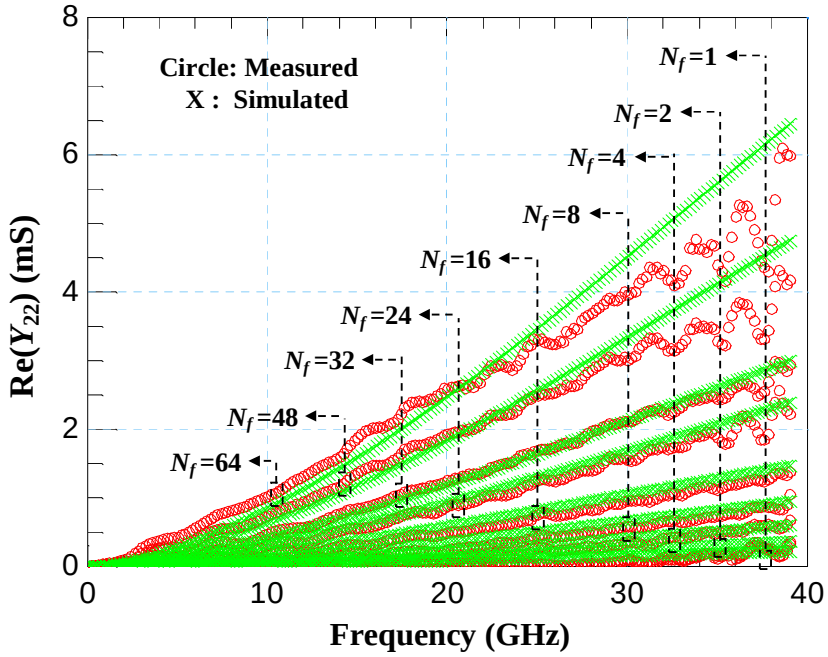


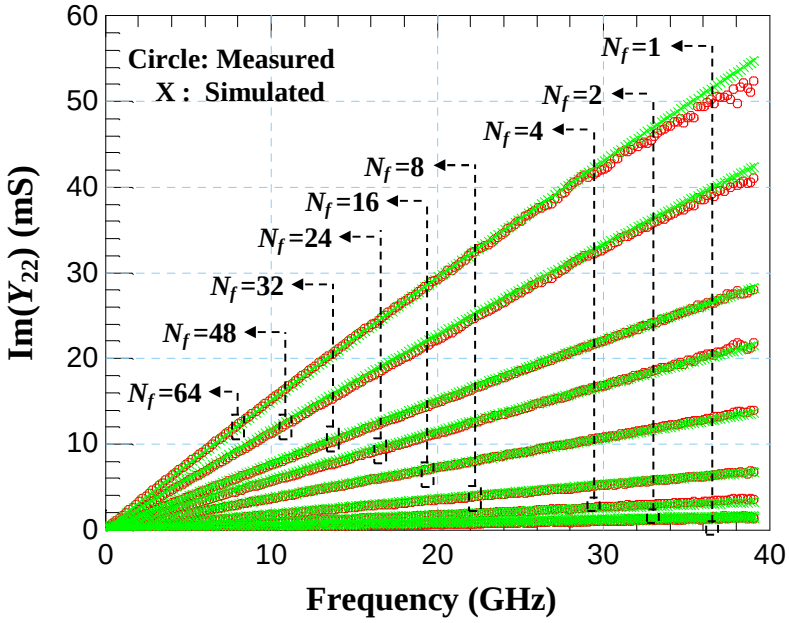
Figure 4.13: Extracted and modeled substrate resistances (top) and capacitances (bottom) of DNW nMOSFETs with different number of fingers.

Figure 4.14 depicts an excellent agreement between the measured and simulated output admittances of the 64-finger nMOSFET at different bias conditions with a common source configuration, while the DNW is grounded. The measured and simulated output admittances (Y_{22}) at zero-bias for the nine devices with different number of fingers are compared and plotted in Figure 4.14. Excellent agreement is achieved between the imaginary parts of the output admittances of devices. Due to the oscillation of the measurements at high frequencies, the resistive parasitics of the substrate are hard to be extracted accurately. This introduces errors between the measured and simulated results

of the real parts of the output admittances of transistors at high frequencies.



(a)



(b)

Figure 4.14: Measured and simulated output admittance of DNW nMOSFETs with different number of fingers at zero bias [(V_G = 0V; V_D = 0V; V_S = 0V]. All the devices are connected in common source configuration, while the DNW is grounded.

4.3 Investigation and Modelling of the Avalanche Effect in MOSFETs with Non-uniform Finger Spacing

4.3.1 Avalanche Effect in MOSFETs

There has been an increasing interest in designing RF power amplifiers (PAs) in CMOS technology, such as the 0.25-μm [24], 0.18-μm [25], 0.13-μm [26], 90-nm [27] and 65-nm [28] standard RF CMOS processes. Given that there is no restriction on the choice of drain bias, the break-down characteristics of the MOSFETs operated at high drain potentials determine the onset of gain compression and the maximum achievable output power. Using a MOSFET at best efficiency and full power often requires operation at the limit set by breakdown mechanisms [29]. Thus, novel layout structures which can improve the breakdown limit of MOSFETs without reducing the RF performance of devices are of utmost importance in RF power amplifier design based on standard CMOS processes.

As an advanced layout method, the non-uniform finger spacing layout is traditionally claimed as an effective layout method to provide a uniform junction temperature across the fingers, thus significantly enhancing the power performance of power transistors, such as the SiGe HBTs [30] and III-V FETs [31]. In this work, we propose that this kind of layout structure can also be used to effectively improve the breakdown limit of MOSFETs. In this work, characteristics of a non-uniform finger spaced layout structure, which has a variable pitch between the gate-fingers which decreases uniformly from the central portion of a multi-finger nMOSFET to two opposite outer end portions similar to [31], is investigated in 0.18-μm RF CMOS. The drain-source breakdown voltage (BV_{ds}) is the key limitation for realizing power amplifiers in RF CMOS technology, and the RF performance of devices is largely determined by the parasitic capacitances, in contrast to [30], [31], we specifically focus on the impact of changing of the spacing size (corresponding to the increasing of the area of the device) on the corresponding BV_{ds} and parasitic capacitances. For RF MOSFETs, a compact model for accurately

predicting the characteristics of the avalanche breakdown current of the devices with different gate-finger spacing is proposed. The measured BV_{ds} characteristics and the extracted equivalent circuit model parameters indicate that the employed layout approach can effectively improve the avalanche break-down effects, and only slightly reduce the cutoff frequency f_T and maximum oscillation frequency f_{max}, leading to an improvement in the design of high performance CMOS PAs.

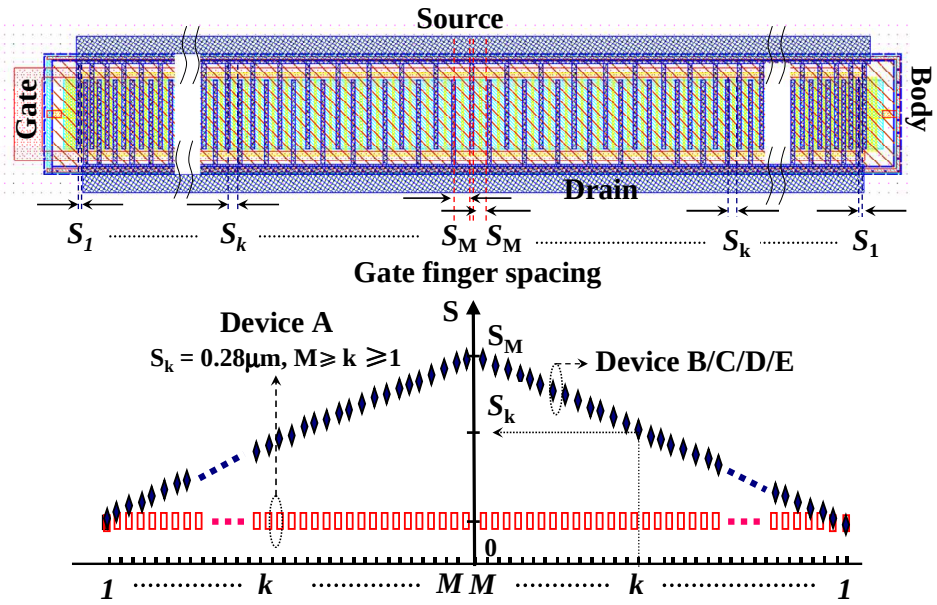


Figure 4.15: Simplified layout plane figure (up) and the gate-finger spacing sizes arrangement method (down) of the investigated layout structures of nMOSFETs with an odd number of gate-fingers. The layout is arranged as a symmetric structure. When the number of gate-fingers (N_f) is odd, M = (N_f -1)/2, while M =N_f/2+1 for N_f is even. S_k ($M \geq k \geq 1$) represents the k^{st} gate-finger spacing size. Device A is a uniformly gate-finger spacing arranged transistor, and the spacing size is 0.28μm. Devices B, C, D and E are non-uniformly gate-finger spacing arranged transistors, S_M represents the central portion spacing, 0.6μm, 0.92μm, 1.24μm and 1.56μm are used for the four devices, respectively.

4.3.2 Experimental Setup and Results

A simplified layout plane figure and the gate-finger spacing arrangement method of the investigated devices in this work are given in Figure 4.15. Four 65-finger n-MOSFETs with L_f = 0.18μm and W_f = 7.5μm, named Device B, C, D and E, which have step varied pitches with 0.01μm, 0.02μm, 0.03μm and 0.04μm between the adjacent gate-fingers and with S_M = 0.6μm, 0.92μm, 1.24μm and 1.56μm were fabricated using the SMIC

0.18μm 1P6M DNW RF-CMOS technolgoy, respectively. For comparison, a uniformly spaced 65-finger nMOSFET with the same L_f and W_f, named Device A, was also fabricated. The gate-finger spacing sizes between the two out end fingers of Device B, C, D and E are set equal to the spacing size used in Device A, 0.28μm.

Table 4.3: Description of nMOSFETs with different gate finger spacing arrangements including extracted gate resistance, parasitic capacitances, DC current, tranconductance, iso-thermal drain conductance and RF performance at V_{DS} = V_{GS} = 1.8V. Δg_{ds} is calculated as $\Delta g_{ds} = g_{dsT} - g_{ds}$.

Device / Parameters	Device A	Device B	Device C	Device D	Device E
R_g (Ω)	1.20	1.18	1.24	1.19	1.21
C_{gs} (*fF*)	332.5	339.1	342.2	345.2	350.8
C_{gd} (*fF*)	134.1	134.4	135.4	136.2	137.2
C_{total} (*fF*)	476.6	473.5	477.6	481.4	488.0
I_{ds} (*mA*)	117.3	114.8	114.9	113.9	112.3
g_m (*mS*)	143.4	142.7	143.8	144.1	143.1
g_{ds} (*mS*)	8.3	8.32	8.5	8.35	8.48
g_{dsT} (*mS*)	16.74	16.48	15.84	15.54	15.24
Δg_{ds} (*mS*)	8.44	8.16	7.34	7.19	6.76
f_T (GHz)	48.9	47.96	47.92	47.64	46.67
f_{max} (GHz)	100.3	99.91	96.93	98.52	96.12

The DC characteristics of transistors are measured with the Agilent 4156C precision semiconductor parameter analyzer. Two RF measurement systems, the Agilent E5071C and the E8364B network analyzer are used to characterize the RF behaviour of transistors from 100KHz - 1GHz and 1GHz - 50GHz, respectively. The breakdown voltage, BV_{ds}, is taken as the value of V_{ds} when dI_{ds}/dV_{ds} equal to $0.05(N_f W_f/L_f)$ [32] as illustrated in Figure 4.16. In this work, the BV_{ds} at V_{gs} = 1.8V for the five devices are taken for comparison. For quantitative analysis, small-signal parameters C_{gs}, C_{gd} and R_g are extracted based on the following [33], [34]

$$C_{gs} = \left[\mathrm{Im}(Y_{11} + Y_{12})\right]/\omega \tag{4.7}$$

$$C_{gd} = [-\mathrm{Im}(Y_{12})]/\omega \tag{4.8}$$

$$R_g = \mathrm{Re}(Y_{11})/[\mathrm{Im}(Y_{11})]^2 \tag{4.9}$$

g_{dsT} listed in Table 4.3 represents the iso-thermal drain conductance, which is extracted by using the frequency dependent characterization of the drain conductance [35].

The values of C_{gs}, C_{gd} and R_g listed in Table 4.3 were extracted from *S*-parameters and averaged in the range of 2 – 15GHz, and C_{total} equals C_{gs} + $C_{gd.}$ The f_T and f_{max} of the five devices are estimated from the equivalent circuit model parameters as follows (simplified from [36])

$$f_T = g_m/2\pi C_{total} \tag{4.10}$$

$$f_{\max} = f_T/2\sqrt{R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)} \tag{4.11}$$

The measured BV_{ds} characteristics of the five devices and the extracted equivalent circuit parameters are given in Figure 4.16 and Table 4.3, respectively. Although the drain current I_{ds} in Device E is reduced by ~4% compared with that in Device A, g_m and R_g of Device B, C, D and E keep close to those of Device A. Compared with that in Device A, C_{total} is slightly increased by ~2.4% for Device E, and there is only a small reduction of 2.23GHz and 4.18GHz in f_T and f_{max} of Device E as seen from Table 4.3, respectively. Two points worth mentioning are that the BV_{ds} in Device E is improved by ~8% compared with that in Device A, from 2.95V to 3.2V, and the thermally related drain conductance doublet (i.e. Δg_{ds} listed in Table 4.3) is improved by ~20% for Device E, compared with that in Device A. As seen from Figure 4.16, BV_{ds} of the four transistors with non-uniform finger spacing arrangement are higher than that of the Device A. This should be a joint result of the improved thermal characteristics and the change in g_{ds} of transistors with the increasing of S_M.

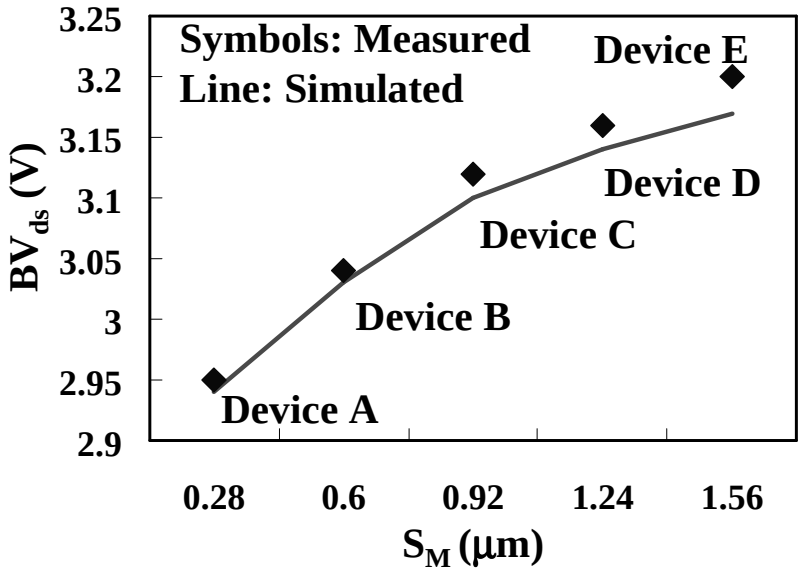


Figure 4.16: Comparison of the measured and scalable model BV_{ds} characteristics of the five devices at V_{gs} = 1.8V. BV_{ds} of transistors is increased with the increasing of $S_{M.}$

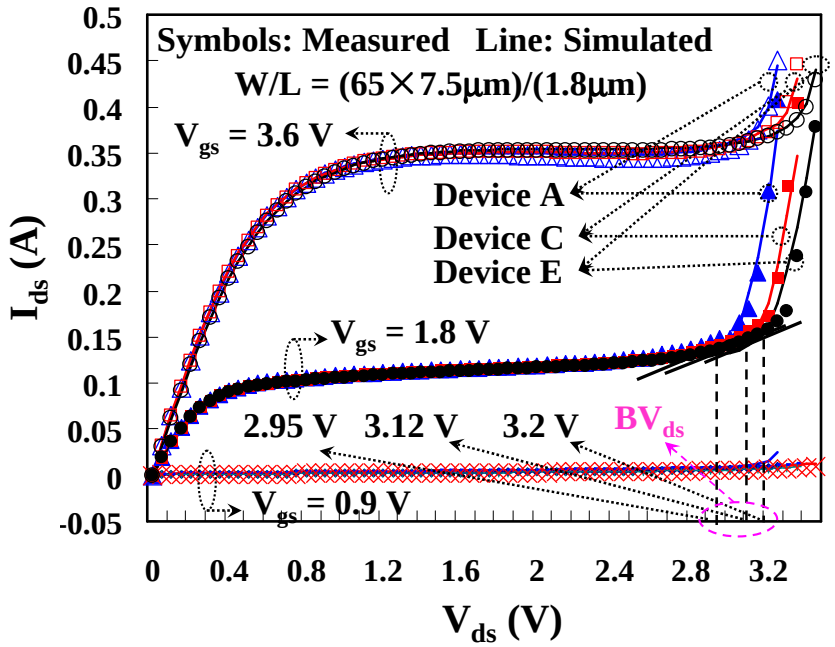


Figure 4.17: Comparison of simulated I_{ds}-V_{ds} characteristics including the breakdown region and the measured results for the Device A, C and E. BV_{ds} is taken be the value of V_{ds} when dI_{ds}/dV_{ds} equal to $0.05(N_f W_f/L_f)$.

4.3.3 Scalable Drain Current Modelling and Verification

The drain current model considering the breakdown effect proposed here is defined as follows,

Table 4.4: Values of the model parameters extracted from five devices with different gate-finger spacing arrangement.

M_{10}	M_{11}	B_{10}	B_{11}	B_{20}
5.04	1.344×10^{-2}	1.63×10^{-35}	9.178×10^{-3}	-6.83
B_{30}	B_{31}	B_{40}	B_{41}	B_{21}
-488	3.795	1.964	5.075×10^{-2}	4.52×10^{-2}

$$I_{ds} = \frac{I_{dse}}{1 + m_1 P_{diss}} \left(1 + b_1 e^{\frac{V_{gd}}{b_2 V_{tv}} + \frac{V_{gd}^2}{b_3 V_{tv}^2}} e^{\frac{V_{ds}}{b_4 V_{tv}}} \right) \tag{4.12}$$

where, V_{tv} is the thermal voltage, I_{dse} represents the drain current without the avalanche breakdown effect, which is modeled by using the PSP102.3 model core, m_1 is introduced to consider the thermal-related power dissipation effect of transistors, while b_1, b_2, b_3 and b_4 are introduced to consider the influence of the layout area change caused by the finger spacing size changes. The power dissipation, P_{diss}, is defined as follows:

$$P_{diss} = I_{dse} V_{ds} \tag{4.13}$$

For scalable modelling, the five parameters, m_1, b_1, b_2, b_3 and b_4 are dependent on the nominal active area of transistor (A_{nor}). For a layout structure with an odd number of gate-fingers, A_{nor} can be calculated as follows,

$$A_{nor} = A_0 W_f \left(L_f N_f + 2 \sum_{k=1}^{M} S_k \right) \tag{4.14}$$

$$S_k = \frac{k-1}{M-1} (S_M - S_1) + S_1, \quad M \geq k \geq 1 \tag{4.15a}$$

where A_0 is 1.0×10^{12}, which is used as the nominal active area of transistor. The functions used for the scalable m_1, b_1, b_2, b_3 and b_4 with regard to A_{nor} are defined as follows,

$$m_1 = (M_{10} + M_{11} A_{nor})^{-1} \tag{4.15b}$$

$$b_1 = B_{10} e^{B_{11} A_{nor}} \tag{4.15c}$$

$$b_2 = B_{20}^{-1} + \left(B_{21} A_{nor}\right)^{-1} \tag{4.15d}$$

$$b_3 = B_{30}^{-1} + \left(B_{31} A_{nor}\right)^{-1} \tag{4.15e}$$

$$b_4 = B_{40}^{-1} + \left(B_{41} A_{nor}\right)^{-1} \tag{4.15f}$$

where M_{10}, M_{11}, B_{10}, B_{11}, B_{20}, B_{21}, B_{30}, B_{31}, B_{40} and B_{41} are model parameters.

To verify the validity of the proposed model, the Verilog-A based PSP102.3 model is modified using (4.12) – (4.15), and implemented in Agilent Advanced Design System (ADS) for simulation. The model parameters for the five transistors are directly extracted by using a simple optimization procedure. The extracted parameters are listed in Table 4.4. An excellent agreement between the extracted and simulated BV_{ds} characteristics of all the five devices is achieved and illustrated in Figure 4.16. Figure 4.17 depicts an excellent agreement between the measured and simulated drain current avalanche break down characteristics of Device A, C and E, at V_{gs} = 0.9V, 1.8V and 3.6V, respectively.

4.4 Summary

In this chapter, a simple test structure and a novel compact model have been presented for predicting the characteristics of the substrate network of a DNW RF-MOSFET. An analytical extraction algorithm has been presented for the substrate network parameters. By using the proposed novel test structure, a physics-based scalable model for substrate components of DNW RF-MOSFETs is developed. All of the substrate components that are scalable are directly extracted from two-port measurements. The derived and extracted scalable model is finally directly used to capture the substrate characteristics of common-source connected devices. The model shows excellent agreement with

measured output admittances for frequencies up to 40 GHz for devices with different number of fingers. The performance of RF-MOSFETs with a non-uniform gate-finger spacing arrangement has been investigated. The employed non-uniform gate-finger spacing layout method demonstrated the enhanced breakdown voltage of transistors. A novel active area dependent avalanche breakdown model has been presented. The accuracy of the proposed scalable model is validated through the excellent agreement between the predicted and measured avalanche breakdown current and the breakdown voltage of uniformly and non-uniformly gate-finger spacing arranged RF-MOSFETs.

4.5 References

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5

Conclusions

5.1 On-chip Planar Spiral Inductor Modelling

The modeling of on-chip spiral inductors in RF CMOS processes is an important research area. Standards for on-chip inductor models have yet to be formed in the industrial community. However, there is one consensus among the academic and industrial community and it is that the on-chip spiral inductor models used for CMOS RFIC design should be compact models. Furthermore, in order to meet the requirements of IC designers, the developed models should be scalable.

As regards the formation of scalable models for on-chip spiral inductors, there are two distinct approaches. One is that the models involve expressions and parameters that have no direct correlation with the device physics or process parameters. In other words, the equations are merely mathematical relationships used for data analysis. Therefore, these equations can only reproduce the behaviour of the devices which are used to extract the equations themselves but cannot provide accurate simulation for other devices. The second approach is to develop mathematical expressions directly based on the device physics and process parameters of IC designs. Due to the physics basis of the model structure and behaviour, the equations can accurately predict the device behaviour with changes in the process parameters and design parameters. The scalable models constructed by this method not only accurately predict the behaviour of the devices used to extract the parameters of these equations, but also accurately predict the behaviour of other devices with different physical design parameters. Another advantage of this type of model is that it is not subject to specific restrictions on technology (e.g. bulk silicon RF CMOS / BiCMOS, and SiGe BiCMOS processes). By changing the process related parameters, the model can be easily applied for new processes.

The proposed on-chip spiral inductor modelling technique in this thesis has been employed by the HHNEC 0.18um SiGe BiCMOS process and the 45nm RF CMOS process which is developed by ICRD. The proposed model library presents excellent fitting accuracy, which also verifies the advantage and advancement of the proposed

on-chip spiral inductor model.

5.2 DNW RF CMOS Modelling

With the presence of the DNW, the bulk silicon MOSFET has changed from the traditional 4-terminal device to a 5-terminal device and consequently, modelling of the behaviour of the substrate has become more complex. The DNW is a popular choice for noise isolation in CMOS RFIC design. However, the frequency range where the DNW takes effect is closely related to the parasitic substrate capacitance and substrate resistance formed by the DNW structure, as well as the high-frequency parasitics formed by the p-well of the transistor. The DNW will significantly affect the device output characteristics within the frequency range where it takes effect. For the RF designers, it is important to know the exact values of parasitics. Consequently, compact models which can predict the characteristics of the DNW are greatly needed to guide the circuit design. Therefore, this thesis has developed a novel PSP-based compact model for the substrate structure after the implantation of a DNW and a novel test strategy to extract the model parameters. The proposed test structure has the S, D and G terminals all connected together to be used as port one, while the bulk terminal is port two, and the p-substrate is grounded. This makes the substrate network distinctly accessible in measurements and enables a direct extraction of the DNW parasitics. This test structure provides the basis for the exact extraction of the parasitics of the DNW. By using this test structure, we build the RF MOSFET model which is scalable with the number of fingers of the device and takes the DNW parasitics into account as well. The model is verified using a DNW RF MOSFET manufactured by the SMIC 0.18um RF CMOS process. The high accuracy fitting up to 40 GHz validates the utility and accuracy of the proposed model. The developed PSP-based DNW RF MOSFET model has been successfully used for building a model library for a SMIC 0.13um RF MOSFET and 65nm RF MOSFET, so as to support wireless transceiver design with a 30 ~ 40GHz frequency band using CMOS technology.

In addition to these works, special efforts are also focused on the investigation and modeling of the breakdown effects for RF MOSFET with non-uniform gate-finger spacing. Our investigation found that a device with non-uniform gate-finger spacing represents a considerable improvement for the drain-source break-down voltage (BV_{ds}). This characterization is useful for realizing RF power amplifier designs in RF CMOS technologies. A scalable model based on the area of the active region is also developed for accurately predicting the BV_{ds} characterization of devices. It is observed from the experimental data that the model has good accuracy.

5.3 Future Works

Future work on spiral inductors and DNW RF CMOS compact modelling would involve works such as:

1) Perform a feasibility study using the established double-π model for on-chip spiral inductors with a multi-layer metal series or parallel structure. The study would primarily be focused on the possible new physical effects of multi-metal series or parallel connections as well as the adjustments and additions to the corresponding models. Of specific importance would be to establish a physics-based scalable model for such structures. Such structures have a higher inductance when compared to the planar spiral inductors taking the same chip area.

2) The DNW structure improves the performance of the MOSFET. During the off state of the diode formed by the DNW, there is significant resistance in the substrate, which greatly reduces the high-frequency loss and improves the noise isolation features. These advantages can also be used to improve the performance of spiral inductors, transmission lines and other devices / structures. However, to use the DNW structure, the model and model parameter extraction method for these passive devices or structures is required. However, appropriate technologies and methods regarding this topic are rarely reported.