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Pulsed PECVD Growth of Silicon Nanowires on Various Substrates

David Parlevliet, and John C. L. Cornish
Physics & Energy Studies, Murdoch University, EEPE, DSE, Murdoch University, South St, Murdoch WA 6150, Murdoch, 6150, Australia

ABSTRACT

Silicon nanowires with high aspect ratio were grown using PPECVD and a gold catalyst on a variety of different substrates. The morphology of the nanowires was investigated for a range of crystalline silicon, glass, metal, ITO coated and amorphous silicon coated glass substrates. Deposition of the nanowires was carried out in a parallel plate PECVD chamber modified for PPECVD using a 1kHz square wave to modulate the 13.56MHz RF signal. Samples were analyzed using either a Phillips XL20 SEM of a ZEISS 1555 VP FESEM. The average diameter of the nanowires was found to be independent of the substrate used. The silicon nanowires would grow on all of the substrates tested, however the density varied greatly. It was found that nanowires grew with higher density on the ITO coated glass substrates rather than the uncoated glass substrates. Aligned nanowire growth was observed on polished copper substrates. Of all the substrates trialed, ITO coated aluminosilicate glass proved to be the most effective substrate for the growth of silicon nanowires.

INTRODUCTION

Silicon nanowires can be produced by techniques compatible with or already used in the thin film and semiconductor manufacturing industries making them attractive for applications in advanced photovoltaics. Silicon nanowires are often grown via the Vapour Liquid Solid (VLS) mechanism as first proposed by Wagner and Ellis [1]. Plasma Enhanced Chemical Vapor Deposition (PECVD) is a widely used technique for the growth of semiconductor thin films. When used with substrates covered with a metal catalyst such as gold, PECVD has been used to produce silicon nanowires and is known to improve their deposition rate [2]. A further modification of PECVD uses a square wave signal to produce Pulsed PECVD (PPECVD). We have previously shown [3] that the use of PPECVD improves nanowire density and overall sample coverage in comparison to PECVD. Silicon nanowires have been produced using a variety of substrates, although most interest is devoted to what is being grown, the substrate used can affect the ultimate usefulness of the silicon nanowires. The appropriate choice of crystalline silicon substrates can affect the direction of growth of the nanowires in relation to the substrate by using an epitaxial growth mechanism [4]. To take advantage of the epitaxial growth mechanism the native oxide must be removed from the silicon substrate. The treatment of the substrates with an HF etch to remove the native oxide layer before the addition of a gold layer is critical for epitaxial growth. It has also been found that the formation of SiO_2 on the gold deposited on silicon (111) substrates can have a detrimental effect on the epitaxial growth of silicon nanowires [5], hence was recommended that the silicon oxide over layer be removed from the gold before nanowire growth [5].

Non crystalline silicon substrates have also been used such as highly oriented pyrolytic graphite [6], indium-tin-oxide (ITO) [7] and silicon on insulator (SOI) [8]. In this work a series of materials were trialed as substrates for the growth of silicon nanowires using PPECVD and a gold catalyst via the VLS mechanism. The substrates used were polished c-Si(110), c-Si(100), c-Si(111), polished stainless steel, polished copper (poly-crystalline), microscope slides (borosilicate glass), Corning 7059 aluminosilicate glass, Corning ITO (corning 7059 coated in ITO), Asahi ITO, microscope slides coated in amorphous silicon (a-Si:H) and amorphous silicon coated Corning ITO. Scanning electron microscopy was used to compare the growth of silicon nanowires on each of these substrates.

EXPERIMENT

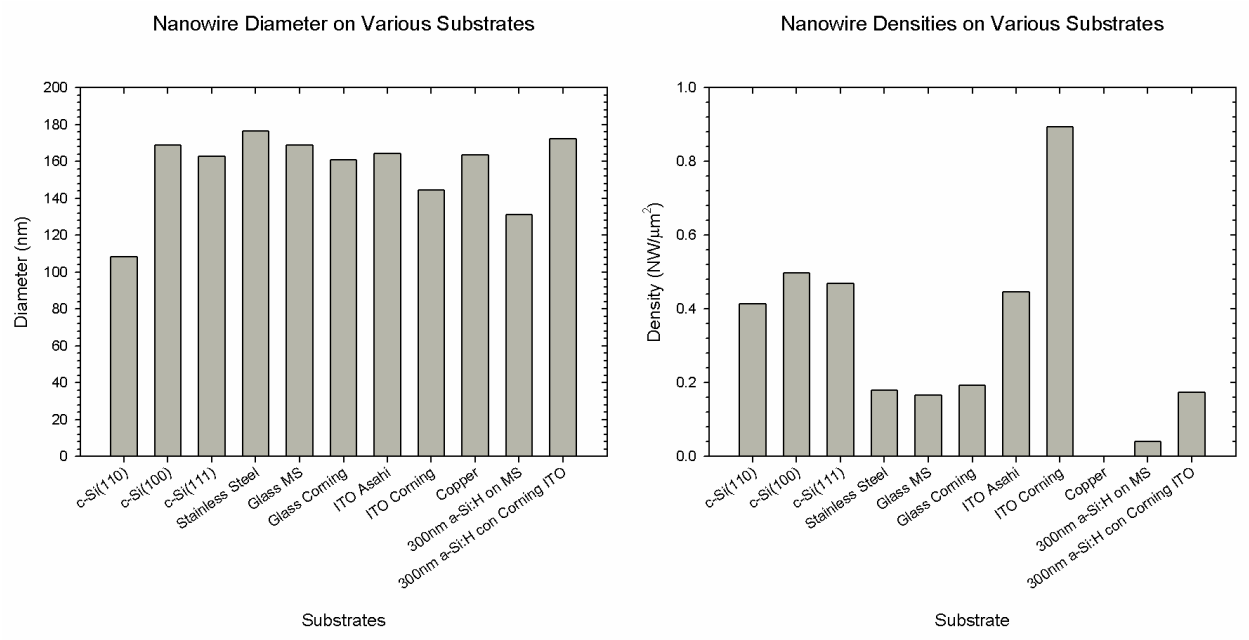
Gold catalyst layers of an average thickness of 100nm were deposited onto the substrates by thermal evaporation of the metal from a tungsten wire or boat under vacuum. The thickness of the catalyst layer was measured in-situ using a quartz crystal microbalance. Prior to the deposition of the catalyst, the substrates were cleaned in an ultrasonic bath in several steps using decon-90, ultra-pure water and propanol. After a final ultra-pure water rinse the substrates were dried using high purity nitrogen. Following this, some of the crystalline silicon substrates were subjected to a 1minute etch in 10% HF to remove the native oxide layer before being transferred into a vacuum system for deposition of the Au catalyst layer. Some crystalline silicon substrates were not given this etch before catalyst coating so as to preserve the native oxide layer. In addition, some crystalline silicon substrates previously treated with HF were given a second 30s HF etch immediately prior to being placed in the chamber for the deposition of silicon nanowires. Copper (poly-crystalline) and stainless steel substrates were polished to a mirror-like finish using increasingly finer grades of abrasives before being cleaned as per the glass and ITO substrates. The glass and ITO substrates to be coated with amorphous silicon were cleaned as above and were then placed in the PECVD chamber for the deposition of an approximately 300nm thick intrinsic amorphous silicon layer before coating with the catalyst layer. After coating with the metal catalyst and subsequent HF dip if required, the substrates were transferred to the PECVD chamber for the growth of silicon nanowires. The deposition was performed under 3.0 Torr of silane (100%) and at a temperature of ~340°C. A square wave generated by a pulse generator (SRS Model DG535) was used to modulate the 13.56MHz signal used to generate the plasma. A modulation frequency of 1000Hz was used and the mark space ratio was held at a constant ratio of 1:1. A control sample using a c-Si(100) substrate with intact native oxide layer was present during each deposition to ensure sample were deposited under comparable growth conditions. Deposition conditions had been previously optimized for the growth on crystalline silicon substrates. The samples were cooled to room temperature before the chamber was purged with Ar. Once cooled the samples were removed from the chamber and analyzed using a Philips XL20 SEM and some were given further analysis on a ZEISS 1555 VP FESEM. The orientation of individual silicon nanowires was not conducted as part of this work.

DISCUSSION

There are several factors that would influence the growth of silicon nanowires on various substrates. The temperature of the substrate directly influences the proportion of catalyst that is liquid on the surface, allowing the nanowires to grow via the VLS mechanism. The composition

of the substrate determines if the nanowires can grow at all, if the substrate reacts with the catalyst or amorphous silicon the growth of nanowires can be stifled. Additionally, some growth mechanisms such as the Solid-Liquid-Solid (SLS) mechanism, use the substrate as a source of silicon [9]. The VLS mechanism, using gold as a catalyst, at low temperatures requires a eutectic of gold and silicon to form. If in an available form, the substrate can be a source of silicon for this process.

The average diameter of the silicon nanowires grown during this work was 150nm although some as large as 380nm and as small as 80nm were observed. The diameter was largely unaffected by the change in substrate as shown in Figure 1a. This was to be expected as the diameter of silicon nanowires is known to depend primarily on the size of the catalyst droplet [10] and the silane partial pressure used during deposition [11]. There is no indication that the selection of the substrate alters the diameter of the silicon nanowires.

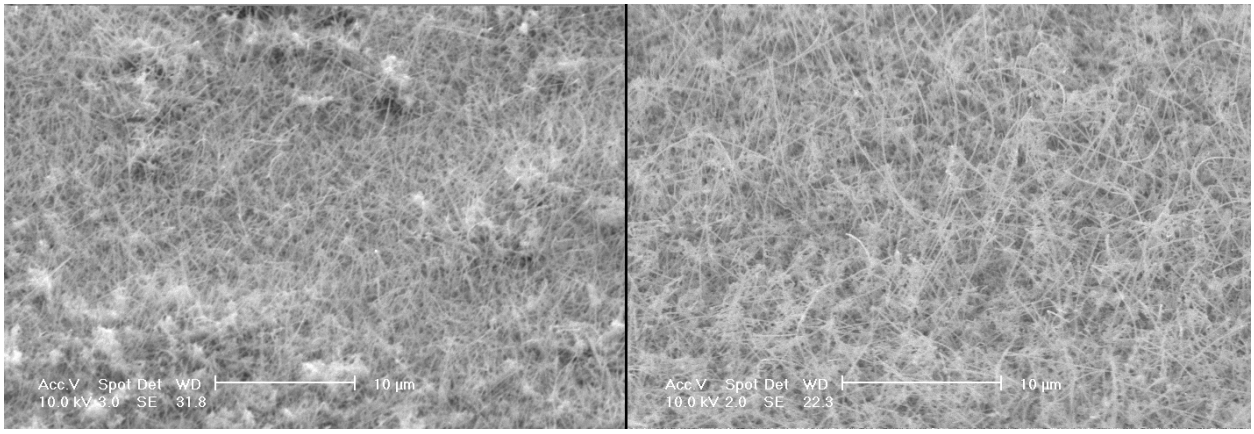


(a) **(b)**

Figure 1: **(a)** Average nanowire diameter on each of the substrates.
(b) Average nanowire densities on the substrates trialed.

The nanowires grown on crystalline substrates in this work did not exhibit any significant evidence of aligned or epitaxial growth. This was regardless of the removal of the native oxide layer via a HF etch or the removal of the oxide over layer on the gold as recommended by Jagannathan and Nishi *et al* by a second HF etch immediately before the growth of silicon nanowires [5]. For epitaxial growth gold catalyst thicknesses such as 3nm [5] are often used, or gold colloids with mean diameters of 20nm [12]. These lead to nanowires with diameters much smaller than the average 150nm produced in this work. Reliable epitaxial growth of silicon nanowires in this work did not occur, likely a result of the low substrate temperatures used or oxide formation after the HF etch, prior to the gold deposition. A sample of the nanowires produced on the c-Si(111) substrate is shown in figure 2. As can be seen the nanowires are protruding from the substrate but not otherwise showing any preferred orientation or alignment. The high aspect ratio

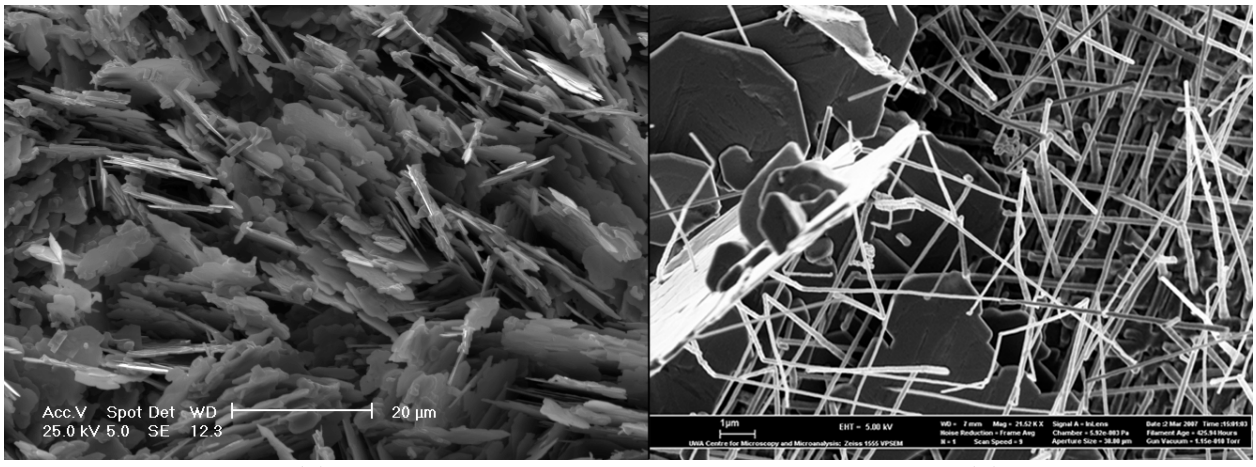
of the nanowires can also be observed in Figure 2a. Similar results were observed for the other orientations of crystalline silicon.



(a) **(b)**

Figure 2: **(a)** Nanowire grown on c-Si(111) substrate (45° tilt).
(b) High density nanowires grown directly on Corning ITO (45° tilt).

No alignment of the silicon nanowires was observed on glass substrates, ITO coated glass substrates or amorphous silicon coated substrates. An example of the nanowire growth directly on ITO is shown in Figure 2b. This result was expected as epitaxial growth requires a clean crystal surface to occur and the substrates used were amorphous in nature. The surface of the stainless steel and copper substrates were polished and non crystalline in nature, in addition, an oxide layer would have been present on the substrate before the deposition of the gold catalyst. As could be expected, stainless steel substrates did not show aligned growth. The copper substrate did demonstrate aligned growth in some regions as shown in Figure 3b, however the dominant growth was a platelet structure as shown in Figure 3a. The growth of silicon nanowires on this substrate is far from optimal given the extreme texturing that occurs upon deposition of the amorphous film by CVD during the preheat stage of the deposition either when Ar or silane was present, before the nanowire growth occurs.



(a) **(b)**

Figure 3: **(a)** Platelet like structures grown on copper substrates.
(b) Silicon nanowires on a copper substrate (FESEM).

As stated above, the growth of silicon nanowires via the VLS mechanism is highly dependant upon temperature. It is generally accepted that nanowire growth is promoted at higher temperatures, in excess of the gold-silicon eutectic point. The sample holder that holds the glass materials to the heater block in the deposition is designed to loosely hold pieces of ITO and glass, as such there is a gap of 0.1 to 0.2 mm between the surface of the ITO and the bottom of the heater block. The sample holder was designed for 1.1 and 0.5mm substrates, other thickness substrates make poor thermal contact with the heater block. However, under the pressures used there is significant conduction through the gas itself. The holder for crystalline and metallic samples is further from the centre of the heater block and is thinner leaving the crystalline samples in loose contact and the metallic samples in good contact with the heater block. As the microscope slides are thinner (0.1 mm) than the ITO coated materials and Corning glass the slide would be in poorer thermal contact with the heater block and hence at a slightly lower temperature. Given that the deposition temperature being used is close to the eutectic point of gold and silicon, a slight decrease in temperature has a large impact on the quality of nanowire growth and thus the nanowire density. This is shown in Figure 1b, where the density of nanowire growth on the microscope slides is less than that of the thicker glass based materials. This argument also applies for the amorphous silicon coated samples. The crystalline samples, being further from the heater centre of the heater block could again be at a slightly lower temperature than the glass substrates, resulting in a decreased nanowire density. From Figure 1b it can be seen that the conductive ITO coated materials, both Corning glass and Asahi ITO produce nanowires at a higher density than the uncoated corning glass of similar thickness. Previous work using PPECVD has indicated that part of the increase in density with using a 1kHz pulsed plasma is due to the induced heating in the substrate [3]. By introducing a conductive layer to the surface of the otherwise insulating glass substrate before the deposition of the gold catalyst layer this effect could be enhanced. The resulting raised temperature encouraged a higher density growth of silicon nanowires. By the same token, introducing a poorly conductive layer such as amorphous silicon between the ITO and gold layers appears to reduce this enhanced effect as shown by the poor densities of silicon nanowires on amorphous silicon coated substrates in Figure 1b. The reduced growth densities on amorphous silicon can also be explained by the gold and silicon forming a eutectic without forming catalyst droplets as is the case on crystalline or glass substrates

CONCLUSIONS

The growth density of silicon nanowires was compared for a number of different substrates. Due to the thickness of the gold catalyst layer used there was little evidence of aligned or epitaxial growth upon the crystalline silicon substrates despite HF etching. Copper and stainless steel substrate were found to be unsuitable substrates for the growth of silicon nanowires at the deposition temperature used, with only a few nanowires being observed. Of the glass based substrates it was found that the thickness of the substrate had an effect on the density of nanowire growth, this being directly linked to proximity with the heater block. Both plain and ITO coated Corning glass was used. It was found that nanowires grew with higher density on the ITO coated substrates. The reason for this was proposed to be the presence of a conductive layer immediately preceding the gold catalyst layer. For samples where a poorly conducting amorphous silicon layer was interposed between the ITO and Au layers, poorer growth resulted.

Of all the substrates trialed, ITO coated aluminosilicate glass was found to the most effective substrate to produce nanowires. This has many potential applications where nanowires need to be grown on transparent conductive substrates, such as solar cells and photodetectors.

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