Murdoch University
Facility of Minerals and Energy
School of Engineering and Energy

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Efficiency of Super Capacitor Banks Used in Regenerative Breaking in Hybrid Electric Vehicles

A report submitted to the School of Engineering and Energy, Murdoch University in partial fulfilment of the requirements for the degree of Bachelor of Engineering

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Abstract

The aim of this project was to build a supercapacitor bank, dc to dc converter, and testing rig to perform efficiency testing for various configurations of the super capacitor bank against various hybrid electric vehicle regenerative braking profiles.

A bank of 10 25F cells was constructed along with a bidirectional DC to DC converter allowing practical testing of two of the four possible bank configurations.

An average of 55% and 63% end to end efficiency was found for the two configurations respectively when tested under three different scaled regenerative braking profiles.

It was found that capacitor banks with a higher maximum voltage i.e. more cells in series were more efficient as there were lower input and output currents and most of losses were restricted to the converter.

Disclaimer

I declare that the following report is my own work unless otherwise referenced and has not been submitted for assessment in another unit.

David Napier

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1 Introduction

The purpose of this project was to evaluate the use of supercapacitors as storage devices for regenerative breaking in hybrid vehicles.

Supercapacitors are high capacitance capacitors with a large power density that are filling the gap between batteries and capacitors.

A lot of attention has been given in the last decade to using supercapacitors in hybrid vehicles to overcome the deficiencies of batteries especially when it comes to harnessing and releasing the power generated in regenerative breaking.

As supercapacitors have much higher power densities than batteries, the devices can successfully absorb the power produced by the regenerative braking, which is normally over a short time interval. To achieve this with batteries, large battery banks need to be installed which are costly, inefficient and heavy.

There has been a lot of work done on this topic but this thesis is going to focus on testing the efficiency of the charging and discharging of supercapacitor banks in different configurations with regenerative breaking profiles.

2 Aims

The aims of the proposed project are to

- Design a scaled down capacitor bank for regenerative breaking. i.e. size a capacitor bank based on the scaled powered requirements.
- Design a DC to DC converter to regulate the output of the capacitor bank and allows both charging and discharging of the capacitors.
- Test the capacitor bank and DC to DC converter efficiency by charging and then discharging the setup in line with various regenerative breaking profiles.
- Repeat efficiency testing with the capacitors in the capacitor bank in various setups i.e. various parallel/series arrangements.

When the project is complete, a capacitor bank with a corresponding DC to DC converter which is capable of charging and discharging should have been constructed. Also a test rig

with voltage and current monitoring with appropriate power for charging and load banks for discharging should have been constructed.

Various setups of the capacitor bank will be tested against a number of regenerative breaking profiles.

3 Project Management

A project plan was created at the start of the project covering the expected completion of the major milestones.

Figure 1 displays the plan for the completion of the major stages of the project. It is broken up into research, design, construction, testing (including experiments), analysis and report completion. Completion of these stages were defined as being the key milestones for the project and as can be seen in Figure 1 certain tasks are dependent on completion of other tasks, while other tasks can run in parallel.

ID	Task Name	Start	Finish	Duration
1	Research	3/08/2009	24/08/2009	16d
2	Design	17/08/2009	7/09/2009	16d
3	Construction	8/09/2009	15/09/2009	6d
4	Testing	16/09/2009	14/10/2009	21d
5	Analysis	28/09/2009	30/10/2009	25d
6	Completion of report	2/11/2009	9/11/2009	6d

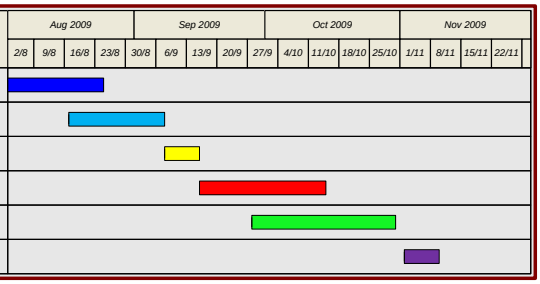

Figure 1 Project Plan

The actual project followed the original plan to the end of the design phase, after the design phase the plan fell considerable behind schedule.

While the project was completed on time, not all of the original objectives were met.

There were delays in acquiring parts and there were considerably more difficulties in the construction phase than expected. The construction phase ended up absorbing the testing phase and the testing and analysis phases were reduced to 1.5 weeks.

This project would have been better suited to a longer time period, of either 6 months at full load or over 12 months at half load.

The practicalities of obtaining parts on short notice and the construction and testing of a working practical system was challenging in the 14 weeks available for the project.

4 Literature Review

This project uses supercapacitors, regenerative braking theory and DC to DC converters. The background, theory and interconnections will be explained in this section.

4.1 Capacitors

Supercapacitors, also known as ultracapacitors, electric double layer capacitors and electrochemical double layer capacitors, are capacitors with high capacitance and high power density, with commercially available capacitances up to 5000 F and power densities up to 20kW/Kg.[1]

Supercapacitors are not new technology, as the first patent was issued in 1957 to General Electric for a low voltage electrolytic capacitor. [2] They are now in thousands of consumer electronics, mainly to provide backup power for memory in electronic devices such as PDAs, mobile phones and DVDs players. They are also used to supplement battery power for power intensive applications as a means to extend battery life.[3] A study by Maxwell technologies has shown that the cycle life of a battery can be drastically increased by the addition of a supercapacitor from around 180 cycles of a regular AA to about 580 cycles.[4]

Improvements in design and material technology are allowing supercapacitors to be used in much higher power applications such as UPS and hybrid cars.

Modern supercapacitors have many advantages over traditional capacitors and secondary batteries such as lithium ion batteries such as:

- They can provide high amount of power in a short period of time.
- As no chemical reactions take place the cycle life is over 500,000 cycles. The manufacture Panasonic states an unlimited number of cycles for their gold cap series [5]. On the other hand rechargeable batteries usually degrade in a few thousand cycles.[3] This results in a device that can out last the product it was designed for and requires lower maintenance.
- They have very good temperature operational characteristics and can operate as low as -40C°, where batteries have poor performances at low temperatures. This makes them suitable to assist batteries in low temperatures as the batteries can trickle

charge the capacitors and the capacitors can then provide enough current to start a motor in a car.

- No special charging equipment is necessary. As long as the capacitor's voltage and current ratings are not exceeded, the capacitors cannot overcharge.
- They have high efficiencies of up to 95% [6]

While supercapacitors have much higher power densities than batteries they have much lower energy densities.

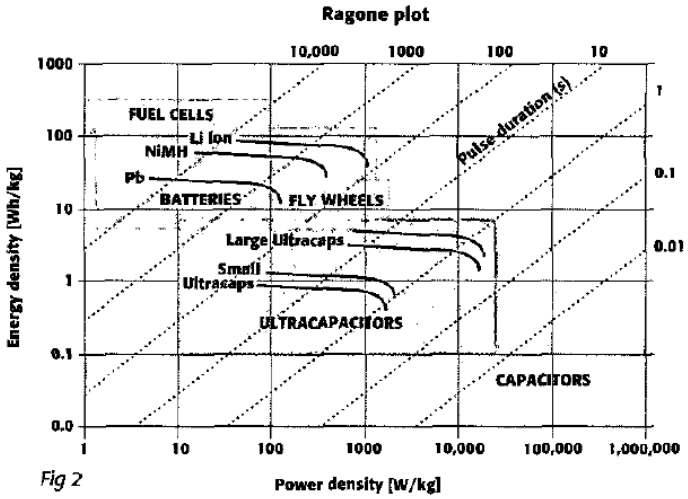

Figure 2 Ragone Plot[1]

As can be seen in Figure 2; supercapacitors have much higher power densities so their energy can be released in a fraction of the time taken by secondary batteries. But an supercapacitor has about 5% the energy density of a lithium ion battery. However studies are being undertaken at MIT to try increase this value to 50% with the introduction of bonded carbon nanotubes. [3]

At the moment supercapacitors cannot replace most battery applications but they can assist batteries where high currents over short periods and large number of cycles are needed.

Supercapacitors are fundamentally different to normal capacitors. They were first discovered by General Electric in the 1950s and then developed by the Standard Oil Company Ohio in 1966.[7] Capacitors store energy in an electric field which is created by applying a voltage across two plates. The two plates are separated by a thin insulator to stop

the plates from shorting out. This process stores energy without the need for a chemical reaction, but as a consequence, the energy is stored on the plates of the device, not in the bulk of the material. This lack of a chemical process infers that a capacitor has a nearly unlimited cycle life.[3]

Supercapacitors address two of the three features that affect capacitance in a capacitor, which are the surface area of the plates, the distance between plates and the dielectric of the material separating them. While the supercapacitor has basically the same structure as a capacitor i.e. two plates separated by a thin insulator, the construction of the plates and the electrolyte that fills them is vastly different. The two plates or electrodes are covered in a thin layer of activated carbon, giving them an effective surface area 100,000 times larger than a traditional capacitor. The insulator is a porous insulator that allows the flow of ions in the electrolyte. As the electrolyte can flow in the capacitor the positive and negative ions flow to the respective electrodes. [8] At the interface between two dissimilar materials or phases an array of charged particles is formed and this is known as the electric double layer. [9] As ions cling to the electrodes of opposite charge, this electrical chemical double layer forms a capacitor between the electrode and the electrolyte ions on the electrode, giving an effective plate separation of the size of a few molecules. [8]

The basic equation for capacitors is:

$$C = \varepsilon \frac{A}{d} \tag{1}$$

Where C is capacitance, ε is the product of the permeability of free space and the dielectric constant, A is the area of the plates and d is the distance between the plates. Supercapacitors increase the area A by using activated carbon and reduce d by using the electric double layer; this combines to give supercapacitors a high capacitance.[8] This is illustrated in Figure 3.

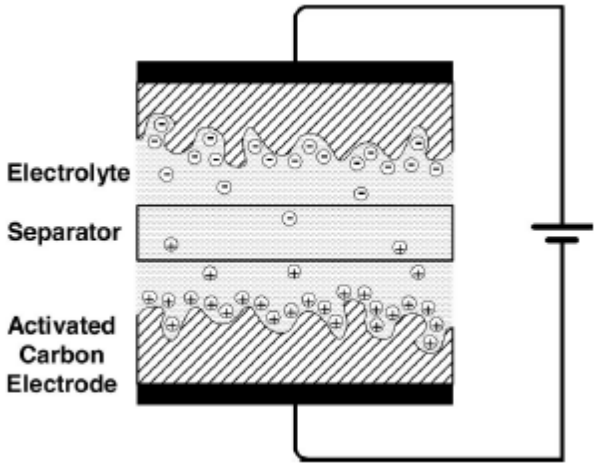

Figure 3 Cross sectional view of a supercapacitor[8]

There are numerous works being conducted to reduce the internal resistance, increase the current carrying capacity and capacitance. Some of the work being undertaken to increase the capacitance are through the use of carbon nanotubes to increase the electrode area and coating the electrode in a dielectric to increase ε.

The voltage of these capacitors needs to be low to stop reduction and oxidation from taking place at the electrodes. The voltage differs depending on the electrolyte in the capacitor. For aqueous capacitors the voltage has to be around 1V, while for organic electrolytes they can be as high as 3V, with 2.5V being typical. [1]

These low voltages are a weakness of supercapacitors. To get a reasonable voltage drop, many supercapacitors have to be placed in series. As capacitance is reduced when capacitors are placed in series, placing them in series results in both a loss of capacitance and a higher loss of power due to the increasing equivalent series resistance (ESR). Placing capacitors in parallel increases the overall capacitance and lowers ESR but then a DC to DC converter is needed which adds weight, cost, and introduces its own losses.

4.2 Regenerative braking

Hybrid electric vehicles aim to combine the best parts of combustion engine design and electrical technology (electric motors and storage devices) to make a car more efficient. This allows a car engine to be sized to handle cruising loads and uses the energy storage components to provide peak load power such as acceleration. Currently, most hybrids use batteries as the secondary energy source.

The disadvantages with using only batteries are:[6]

- Batteries don't function well at low temperatures.
- Sophisticated charging equipment is needed.
- Low life cycles mean that batteries need to be replaced often in the life of a single vehicle.
- Poor ability to retrieve and provide short bursts of high power.

The aim of regenerative braking in hybrid electric vehicles is to recover as much of the kinetic energy as possible when braking the vehicle. Most systems use a combination of friction brakes and a generator to achieve this, with the energy being put back in the electrical storage device of the vehicle.[10]

Regenerative breaking provides high current over a short period with a high number of cycles. Supercapacitors have the ability to absorb all of this energy at a high efficiency, while batteries on the other hand can not readily absorb high current. The supercapacitor can then be used to provide high current during acceleration. In addition, it can provide trickle charge for the batteries and can be used for other electrical loads, such as power steering. This increases the life of the batteries as there may be tens of thousands of regenerative cycles per year while a battery can only accept a few thousand cycles. Another factor which reduces the life of a battery is deep current draw, which can be avoided if the capacitors are used for high current loads. Therefore, using capacitors increases battery life and allows a smaller and lighter battery pack to be installed, and also helps the batteries operate at low temperatures. They also don't need sophisticated charging equipment and are low maintenance.

4.3 DC to DC converter

Supercapacitors operate on extra low voltages, while most hybrid electric vehicles, such as the Toyota Prius 2 operate their batteries at voltages of 202VDC, and the motor and generator runs off 500VAC. [10] To get 202 VDC from a supercapacitor bank requires 80 supercapacitors to be placed in series.

This may be impractical or increases the weight and cost by having a larger bank than required. Also, unlike batteries, capacitors lose their voltage quickly with the discharge of energy. For example, if a bank was reduced to half of its voltage it would have discharged 75% of its energy. Thus to allow better sizing of banks and allow for a higher discharge of energy a DC to DC converter is needed.

There are a vast number of different DC to DC converter topologies available, but in the regenerative braking application the converter will need to be able to increase the voltage for discharge, decrease the voltage of charging and be able to operate over a large voltage range. Two converters which satisfy this condition are the buck boost and full/half bridge converters.

Buck boost converters are able to increase or decrease the output voltage relative to the input voltage depending on how they are set up. While they have many advantages, such as having commercially available control chips, they are only unidirectional. This would result in a need for either two converters, one for charging one for discharging, or a switching arrangement that changes the input and output connections when charging/discharging is needed.

Full bridge dc-dc converters allow for bidirectional flow but the switching and control is more complicated. There are many topologies for full bridge and half bridge converters designed for supercapacitors and fuel cells which are highly efficient. [11, 12]

A dc to dc converter fits in to the hybrid electric power train as shown in Figure 4.

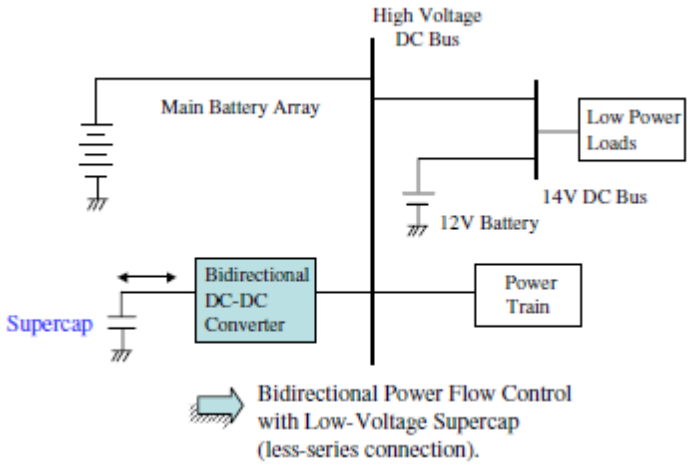

Figure 4 DC to DC converter [11]

5 Design

The design stage was completed in a methodical way to ensure both an accurate and efficient outcome. The process involved 3 phases:

- Selection of capacitor bank size
- Assessment of driving cycles to determine charging times and power
- Design of the DC to DC converter

5.1 Capacitor bank selection

The first stage in the design process was to determine the size of the supercapacitor bank. There were a number of considerations to take into account, such as voltage range, cost, flexibility, current and energy limitations, and lead time. It was decided that in order to lower lead time and cost, the parts would be sourced from local suppliers such as Altronics and Jaycar. Altronics had a number of super capacitors ranging from 5 F to 100F which appeared to be suitable.

The number of cells was selected to be 10 as it offered the most flexible bank configuration. By selecting 10 cells 4 different parallel/series arrangements could be made.

The capacitor size was selected as 25F. This value was chosen because when parts were sourced, it was the largest size available in the quantities required. It also meant that new power supplies and large MOSFETs were not required. The power supplies available could

provide enough power for the experiments and large MOSFETS were not required, as the current output was within tolerance of locally available MOSFETs.

The specifications of the different bank configurations are shown in table 1.

Table 1 Bank Specifications

Configuration	Series	Parallel	Capacitance (F)	ESR (Ohms)	Voltage (V)
1	10	1	2.5	0.4	27
2	5	2	10	0.1	13.5
3	2	5	62.5	0.016	5.4
4	1	10	250	0.004	2.7

5.2 Driving cycles

The second stage was to assess driving cycles to obtain braking times and velocities that could be used to determine the power and the times used in the experiments

The braking profile selected for the experiments and for the sizing of the capacitor banks was the US06 driving cycle[13] as seen in Figure 5.

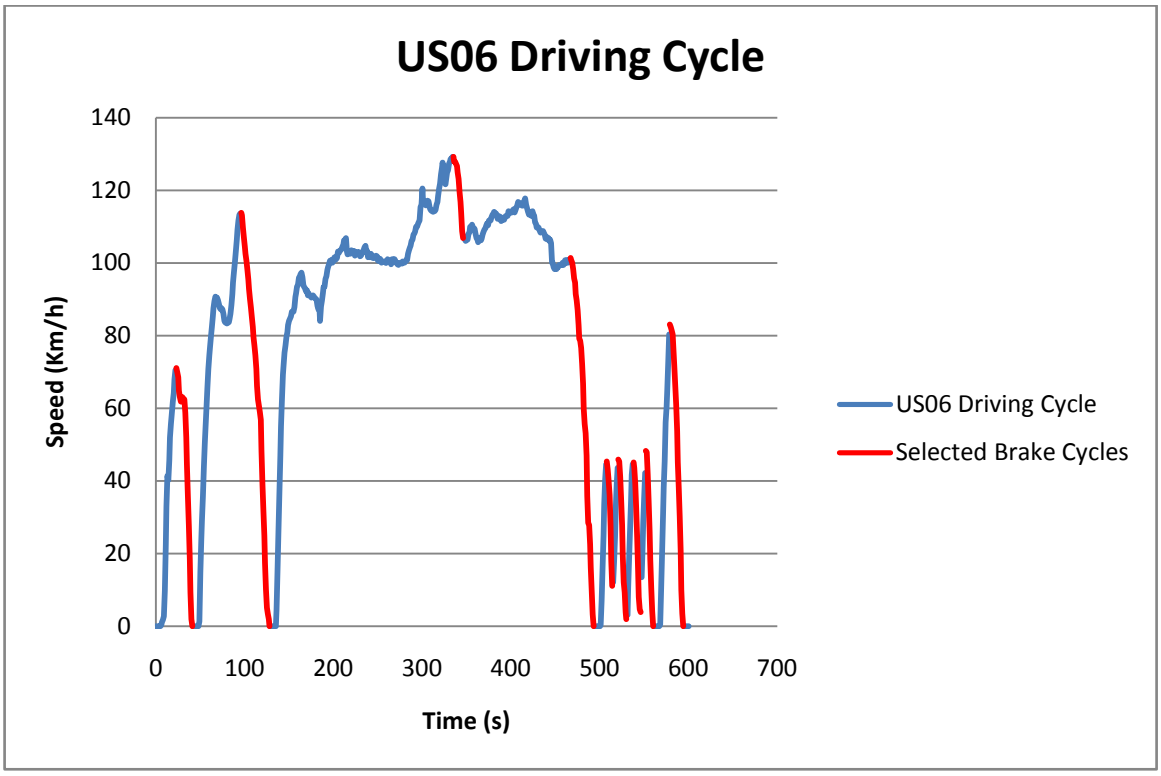

Figure 5 US06 Driving Cycle [13]

As a part of the design process this driving cycle was evaluated for a Toyota Prius 2. Each of the braking sections in Figure 5 was evaluated for the amount of power and energy that could be produced by the 47.6 kW engine of the 1254 Kg vehicle. While a number of assumptions were made, such as all of the kinetic energy during the braking could be converted to electrical energy (i.e. frictional and air resistance effects were ignored and the motor generator was assumed to be 100% efficient), it still provides insight into the amount of energy produced by regenerative braking. By using basic physics equations from [10, 14], Table 2 was produced.

Table 2 Braking Profiles

Braking Section	Change in Velocity (m/s)	Time (s)	Force Produced by Braking (N)	Power generated (kW)	Energy(kWh)
1	19.75	18	1376.14	27.18	0.136
2	31.6	32	1238.52	39.14	0.348
3	6.21	13	599.12	3.72	0.013
4	28.16	26	1358.4	38.25	0.276
5	9.42	6	1968.26	18.53	0.031
6	12.17	9	1695.96	20.64	0.052
7	11.44	8	1793.51	20.52	0.046
8	13.41	8	2102.54	28.2	0.063
9	23.06	15	1928.12	44.46	0.185

It was also found that if the air effects were ignored and the generator was 100% efficient that frictional brakes would not be needed to supplement the braking as the regenerative braking had enough force to stop the vehicle in the required time.

A number of these sections were chosen for the experiments.

From this table the braking section which produces the largest amount of energy was identified (no. 2) and used to size the power to be used in the experiments.

5.3 Charging characteristics

Using the process found in Douglas's Sizing Ultracapacitors for Hybrid Electric Vehicles[14], a scaled down charging power was selected for braking section 2 taken from Table 2.

The equations used were:

$$\frac{dE(t)}{dt} = \frac{-CE(t) \pm \sqrt{C^2E(t)^2 - 4R_{ESR}C^2p}}{2RC^2} \quad (2)$$

$$\frac{di(t)}{dt} = -\frac{i(t)}{C\left(R - \frac{p}{i(t)^2}\right)} \quad (3)$$

Where E is the terminal voltage, C is the cell capacitance, R and R_{ESR} is the capacitors equivalent series resistance (ESR) and p is the charging power.

These equations were placed into a MATLAB script which takes the specifications of a capacitor such as current rating and voltage. A minimum bank voltage is calculated from the constant discharge power and current rating. Then using equation 2 in a while loop the equation is resloved until the number of cells is high enough so the finial discharge voltage of the cell is greater than the minimum voltage. The MATLAB script is located in the appendices.

This process was then used to asses using a bank of Maxwell technologies 3000F cells is for the powers calculated in Table 2, using equations 2 and 3 it is found that due to the maximum current of 150A per cell[15] 208 cells needs to be added in series in order to absorb the highest power calculated in Table 2 of 39.14kW for the 32s braking time. This result in a maximum peak power of 84240 kW. Using data from [14], this equates to a DC converter weight of 16.84kg and a bank weight of 114kg giving a total weight of 130.84kg for the system. The weight could easily be reduced by using cells with a higher current rating. The cells used in this simulation evaluation only had a continuous current rating of 150A, resulting in a high minimum voltage.

As the system used in the project is based around a scaled system this process was used again but instead of the number of cells being the unknown the power was the unknown. Solving using an iterative process for a bank of 10 25F cells in the four configurations stated in the previous section, it was found that 25W was the recommended rated power. The results for the selected power of 25W for 32 seconds for the four configurations are shown in the charging profiles of Figure 6.

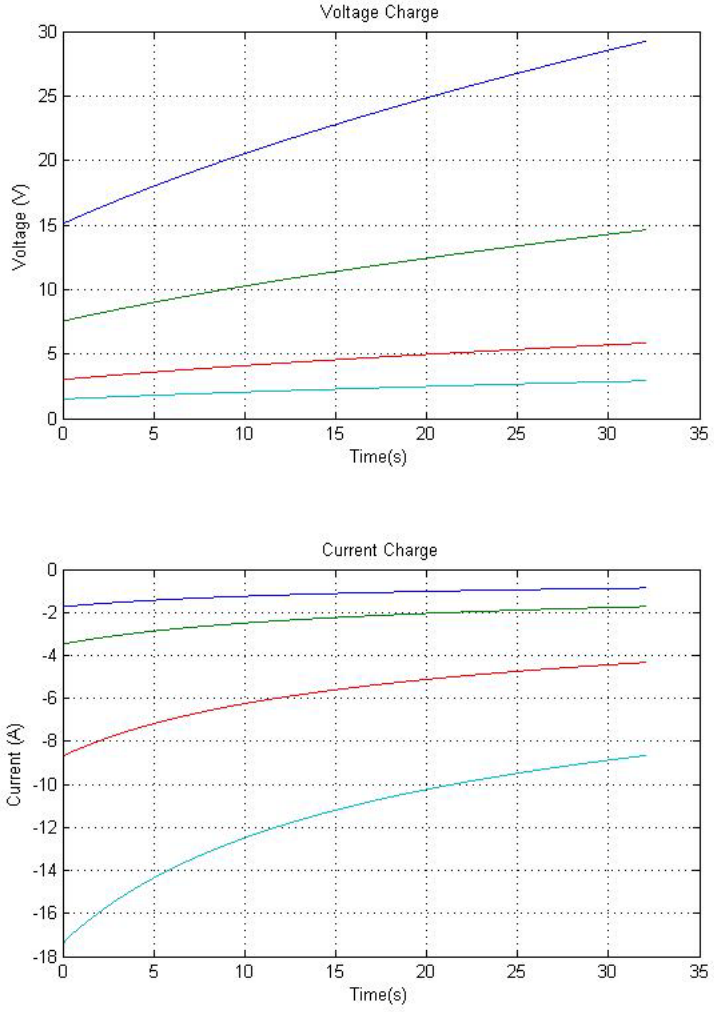

Figure 6 Charging Profile

25W for 32 seconds was a representation of the largest amount of energy in the braking profiles so for the experiments the other braking sections power was a ratio of 25W.

For the experiments three braking sections have been identified to be used and are summarised in Table 3.

Table 3 Selected Braking Profiles

no.	ΔV (m/s)	Time (s)	Charging Power (W)	Charging Energy (Wh)
8	13.4	8	18.01	0.0400
2	12.2	9	13.18	0.0330
2	31.6	32	25.00	0.2222

As can be seen in comparison with Table 2, the charging powers are all ratios of those calculated previously from the US06 driving cycle. The chosen experiments provide a range in both time and energy to give a good indication of the characteristics of the supercapacitors.

The capacitors will be discharged into a load bank of resistors, discharging at a rate of 25W to simulate acceleration of the vehicle after the braking section.

5.4 DC to DC converter design

The DC to DC converter was designed around the maximum currents and voltages calculated in the previous section.

While realistically the high voltage bus of a hybrid vehicle is around 200 VDC, due to safety concerns the high voltage bus for these experiments will be kept at 45 VDC to stay below the extra low voltage limit of 50 VDC. As was shown in the previous sections, the voltage of the supercapacitor bank will vary from 2.7 VDC to 27 VDC, meaning that the DC to DC converter will need to be able to switch from 45 VDC to a minimum voltage of 2.7 VDC.

There are a number of complexities when designing a converter for this kind of unique application, which means that an off-the-shelf device is not suitable.

Firstly, the device needs to be a bidirectional two quadrant converter, meaning that the converter needs to be able to switch current in both positive and negative directions of

flow. The output voltage varies over a large range and considerations in inductor selection need to be made carefully.
As the aim of the system is to simulate a regenerative braking system, constant power needs to be delivered to the load, which makes voltage regulation inappropriate and a new controller needs to be developed.

While there are a few topologies designed for supercapacitors in hybrid vehicles (see [11, 12]) these topologies are too complex to build in the limited time frame available for this project. Most of these topologies are full or half bridge arrangements that use zero voltage switching (ZVS) resonant circuits to reduce switching losses and increase the system frequency thus decreasing the size of the inductive components. They also include an isolation transformer which acts not only as isolation, but also as the inductor for the resonant circuit and assists in switching between large voltages.
With the currents involved with this design there are no off the shelf transformers suitable for the task, so that a transformer would need to be designed and wound for the converter.
To stay within the limited time frame, and to reduce circuit complexity a half bridge non-isolated topology was used. The circuit is shown in Figure 7.

Figure 7 DC to DC converter design

The operation of the converter is relatively simple and is essentially a buck converter stacked on top of a boost converter.

When operated in buck mode the MOSFET X2 switches with a duty cycle which is directly proportional to the output voltage, when the switch is in the off mode the energy stored in the inductor is discharged through D2, and when the switch is on energy is transferred from the input to the output.

When operated in boost mode the bottom switch is used: when switched on the energy is stored in the inductor and when switched off the inductor energy flows to the input thus transferring negative current.

5.4.1 Driver circuits

Switch mode power supply chips SG3524 were chosen to produce the pulse width modulation (PWM) to drive the MOSFETS. Though during testing it was discovered that the chips used did not provide enough current to quickly switch on the MOSFETs, to overcome this, for the low side n channel MOSFET, a transistor totem pole was implemented. The signal from the PWM chip goes through an inverter that provides 0 to 12 VDC signal to Q3. When the input is high Q1 switches on causing the MOSFET to turn on.

When the input is low Q2 turns on causing the MOSFET to turn off. The advantage of this system is that it provides the required current with low resistance to charge and discharge the gate of the MOSFET reducing the time required to turn on.

The high side MOSFET is a p channel MOSFET which required a more sophisticated design. To turn on the high side switch, the gate voltage needs to be 10 to 15 VDC below the source voltage which is the 45V rail. The driver circuit is similar to the low side switch but uses Q6 as a current source and selects the value for R1 so the voltage drop across the resistor becomes 15V when the input is high. When the input is low Q4 switches on bringing the gate voltage to 45V switching off the MOSFET.

5.4.2 Control Method

Due to the need for constant power delivery to the load, the control method for the switching of the MOSFETs cannot be the standard voltage mode control. Originally it was proposed to use proportional integral derivative control (PID) in a feedback loop, but due to the quick high order response of the system the control was unstable causing erratic unstable behaviour.

The difficulty with constant power control in this application is a step change in voltage does not result in a response that can be modelled by a first order circuit. It results in a large rapid positive change in power quickly followed by a rapid negative change in power. This is due to the rising capacitor bank voltage, as the bank voltage reaches the step input level the power returns to zero as there is no voltage difference.

The controller that was used is a model based controller with a proportional integral controller making minor adjustments. The concept behind the controller is that to obtain constant power with a capacitor bank the input voltage needs to be rising at the same speed as the capacitor bank voltage creating a voltage difference which is proportional to the required power.

This was achieved by sampling the capacitor bank voltage and then feeding it into equation 4.

$$V_{PWM} = P_{set}(K_1 - K_2 e^{-K_3 V_{out}}) \quad (4)$$

Where V_{PWM} is the voltage output of the converter, P_{set} the power setpoint, K_1, K_2 and K_3 tunning parameters and V_{out} the capacitor bank voltage.

This creates a reference trajectory for the control input voltage where the voltage difference starts off large as the capacitor bank voltage is low and gets smaller as the capacitor bank voltage increases thus keeping constant power.

The output from the above equation is then fed into a 4^{th} order polynomial which is a linearization of the PWM chip to produce the PWM chip's input voltage.

The buck converter was much simpler, as the load bank was resistive it was essentially a voltage controller not a power controller. The controller read in the capacitor bank voltage and calculated the duty cycle required to reach 45V and outputted that value. There was a small PI loop performing minor corrections on the power.

5.5 Data acquisition

A labVIEW program with a National Instruments USB-6008 data acquisition card was used for the data acquisition. The program has four analog inputs

- Voltage input
- Voltage output
- Current input
- Current output

The voltage signals are dropped down to a 0-10V input through a voltage divider and the current inputs are read in from two LEM LTS 15-NP Hall Effect sensors.

The software records all the data into a .csv file which is time stamped.

The front panel of the labVIEW program is displayed in Figure 8.

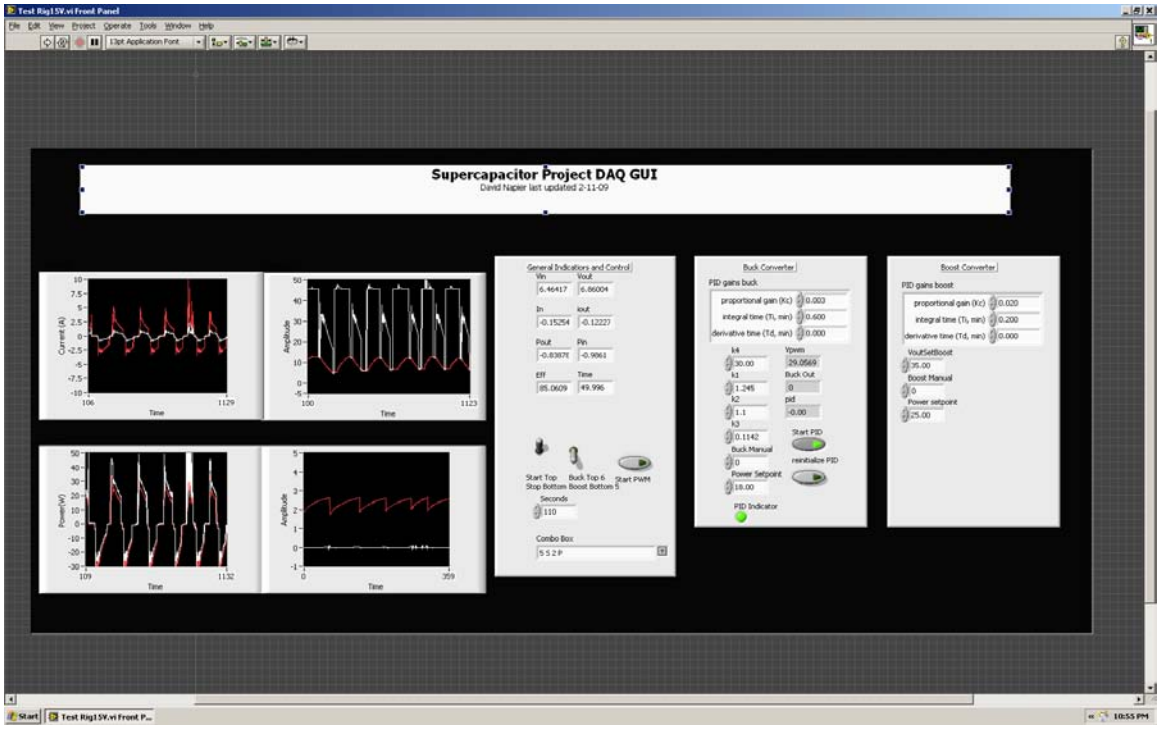

Figure 8 DAQ front page

The labVIEW program also has the controller onboard and outputs a 0-5VDC signal to the PWM chips to produce the PWM of the appropriate duty cycle.

From the front panel all of the major measurements are displayed along with all of the controller parameters and switches for the converter.

5.6 Integration

Figure 9 shows a system overview.

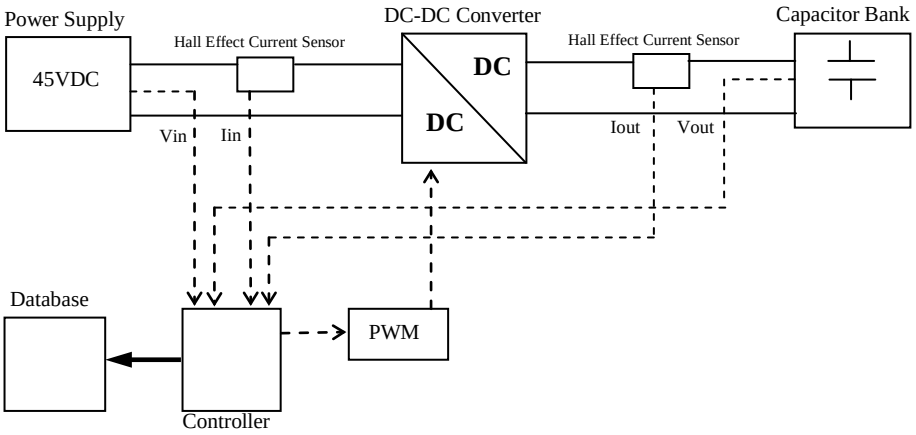

Figure 9 System overview

As can be seen in the figure the controller takes in all of the process information and outputs the PWM command to the PWM controller and passes the information to the database.

6 Construction and testing

The DC to DC converter and data acquisition system needed considerable testing and debugging to achieve satisfactory operation.

6.1 DC to DC converter

The DC to DC converter worked as expected after some modifications to the original design.

Originally the design did not include MOSFET driving circuits, which caused the MOSFETs to switch on very slowly which was causing them to burn out. Once driver circuits were added the boost converter was successfully operated at 133 kHz. The gate switching voltage contained a significant oscilliatiorycomponents as seen in Figure 10.

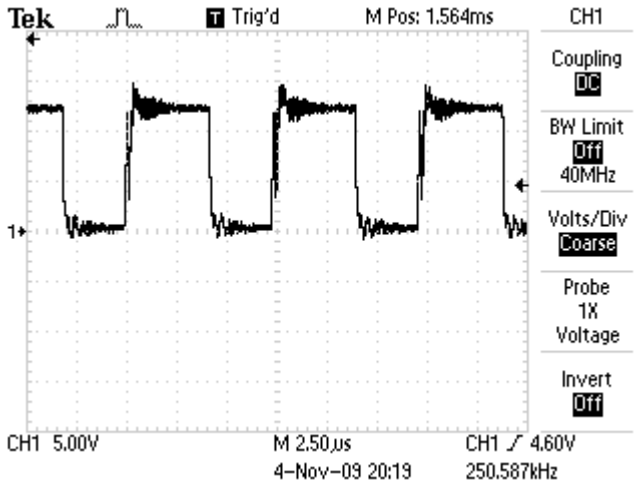

Figure 10 Boost mode gate switching

The boost converter was tested with an 8VDC input across its full range of duty cycles with a 28.4Ohm resistive load. The efficiency is shown in Figure 11.

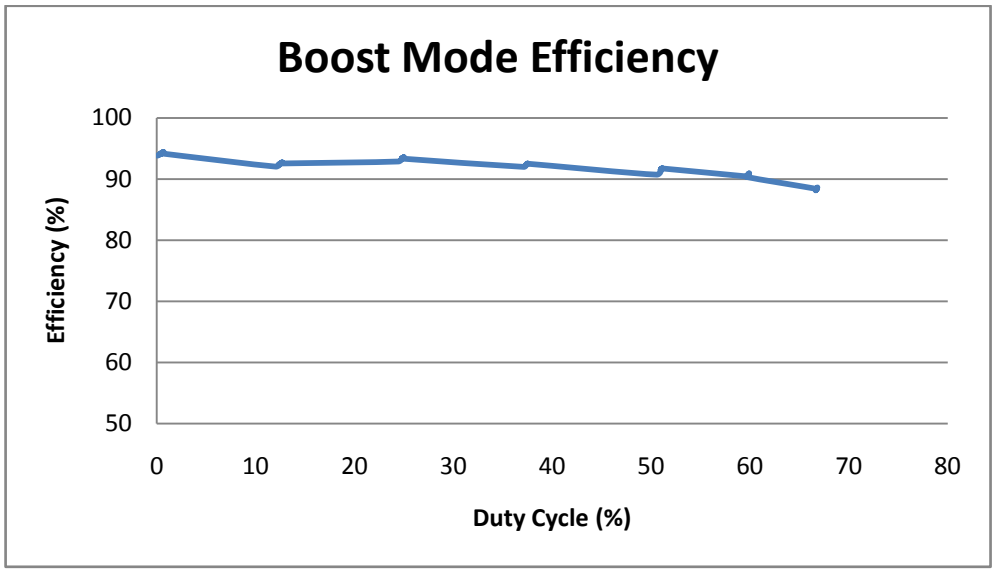

Figure 11 Boost mode efficiency

For this test, it became obvious that the converter would not be able to boost the voltage up from the lower voltages to 45 VDC which was the original intention.

The converter was able to step the voltage by a factor of three with a duty cycle of 66%.

This will have an effect on the subsequent experiments later.

The efficiency will be different for the experiments as they will be operating at higher currents, but it gives an indication of the characteristics of the converter.

During testing in boost mode with the capacitor bank as the input voltage source it was noticed that, as expected, the converter was operating in continuous conduction mode as indicated in Figure 12, which is a differential measurement of the inductor voltage.

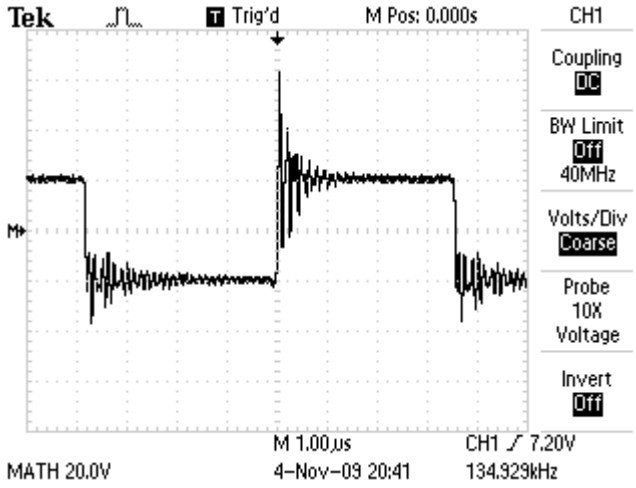

Figure 12 Boost mode inductor voltage

The buck converter had significantly more problems than the boost converter which was the result of using a p-channel MOSFET. When trying to switch the MOSFET at 133 kHz it was found that at lower duty cycles the MOSFET did not properly switch on as seen in Figure 13 which shows the MOSFETS gate to ground voltage.

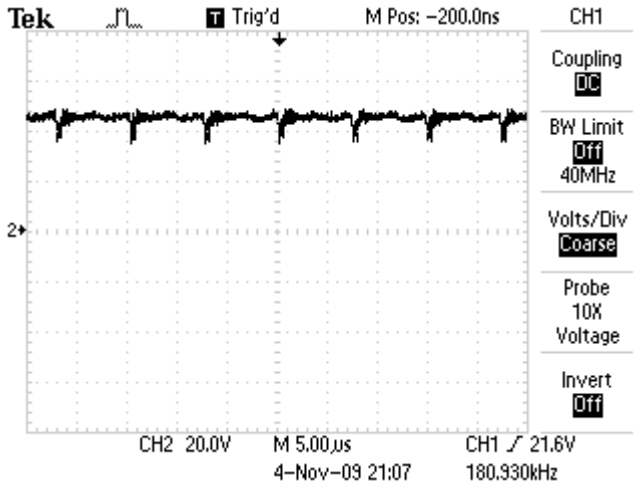

Figure 13 133 kHz switching

This resulted in an unstable controller as the converter had bad resolution at low duty cycles and didn't start operating correctly till the output voltage was around 15V.

To solve this problem the switching frequency was dropped down to 16 kHz. If more time was available the driver circuitry would have been improved to allow faster switching.

An example of the low duty cycle switching is shown in Figure 14 as can be seen the gate signal is much sharper and drops the required 10V to switch on the MOSFET.

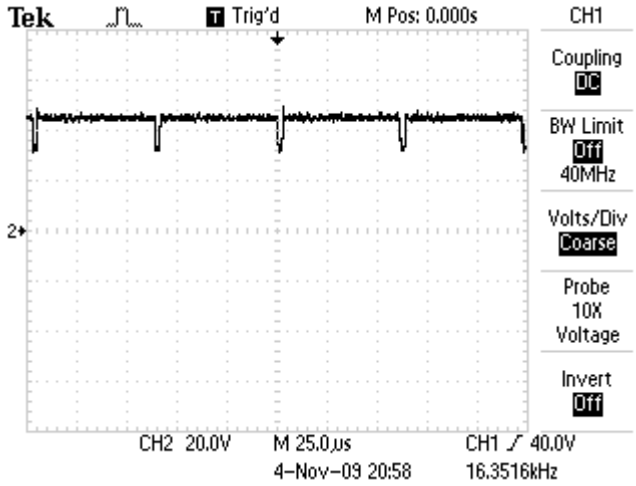

Figure 14 Low duty cycle 16Hz switching

While lowering the frequency increased the controller's stability it had some negative effects. Lowering the frequency meant that the inductor which was sized for 100kHz switching was much too small, making the converter operate in discontinuous mode which means that the inductor current falls to zero during the off state. While the converter will still work it complicates the characteristics of the converter. The output frequency was no longer just dependant on the duty cycle and input voltage but also on the output current. The discontinuous conduction operation is shown in Figure 15.

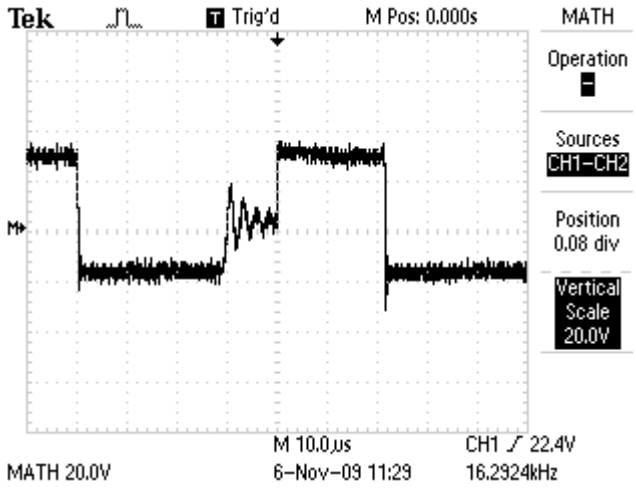

Figure 15 discontinuous operation

The buck converter was tested with a 45VDC input for all duty cycles from 8% to 60% with a 28.4Ohm resistive load. The efficiency is shown in Figure 16

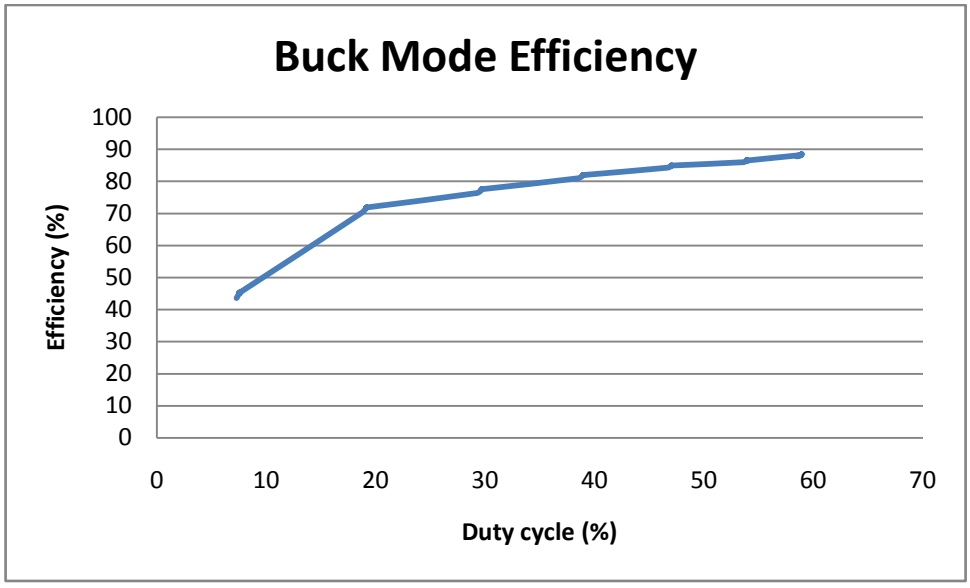

Figure 16 Buck Mode Efficiency measurements

The efficiency varies considerable across its range with higher efficiency at higher duty cycles. This will have repercussion on the experiments as the capacitor banks with a lower voltage are likely to have greater losses due to converter inefficiencies at low duty cycles.

6.2 Data acquisition system

The data acquisition system was relatively simple due to the programming nature of labVIEW. The major configuration that needed to be performed on the system was calibrating the voltage and current inputs. The voltage inputs were simple to calibrate using a simple calculation based on the input impedance of the analog input and the resistive divider values. However the current inputs were not as simple.

The original design used 20A 50 mV current shunts in conjunction with a -100 to 100mV to -5 to 5VDC signal conditioners. This was found to be unsuitable for a number of reasons. Most of the currents used in the experiments were low values for this size of current shunt, resulting in low values being passed to the signal conditioner.

The second problem is that there was considerable noise circulating in the circuit due to the high frequency switching. This noise impressed onto the current shunt was larger than the voltage output of the current shunt. This caused errors in the output which could not be filtered out in the software.

While a number of solutions were tried such as using shielded cables and shielding the inductors, this did not solve the problem. As the problem was enhanced by the low output value of the current shunt a different approach was taken.

The next approach was to use Hall Effect sensors. It was believed that as the problem was with noise over laid on a voltage signal, if current could be sensed directly and then amplified, a lot of the noise problems could be avoided.

This solved many of the problems but there was still noise overlaid on the Hall Effect sensor outputs. After some investigation it appeared that there was a ground loop in the system once the ground system was simplified and a two-stage second-order RLC filter was added prior to the DAQ card.

The two stage second order filter is shown in Figure 17 and its frequency response is shown in Figure 18. The high frequency noise is expected to output at 133kHz and 16kHz in line with the switching frequencies.

Figure 17 filter

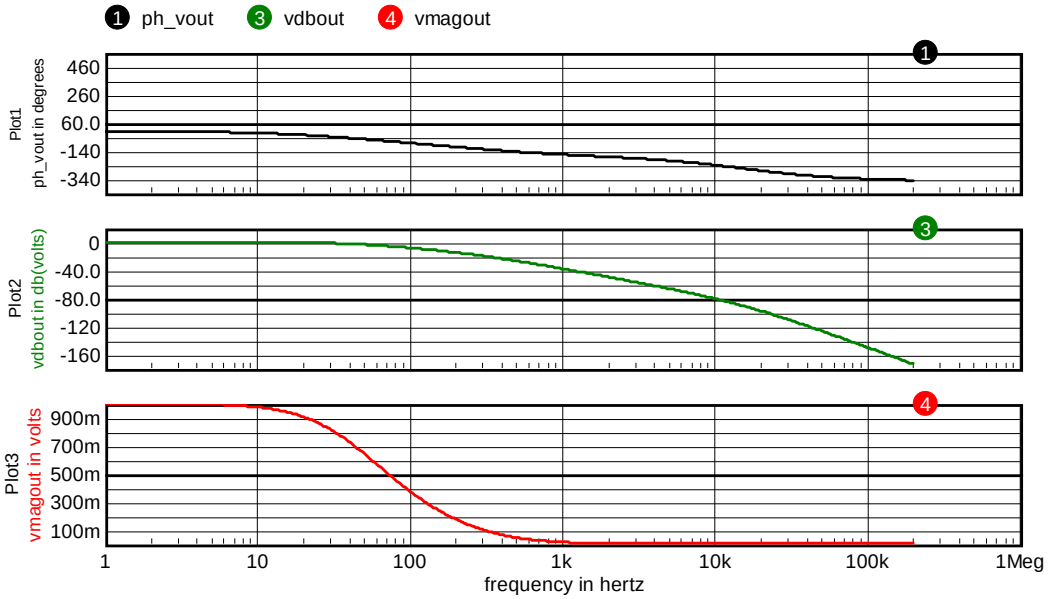

Figure 18 filter bode plots

6.3 Control loop

The control loop worked well once it was tuned, but needed retuning for different power set points. This was due partially to the model and to the converter operating in discontinuous conduction mode. A few examples of the controllers operation are shown in Figure 19 and Figure 20.

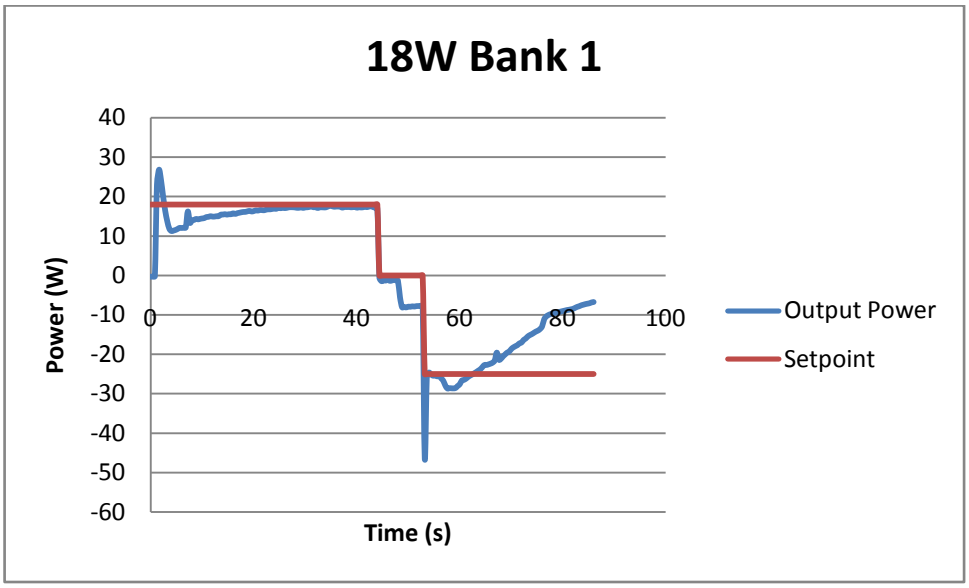

Figure 19 Controller response

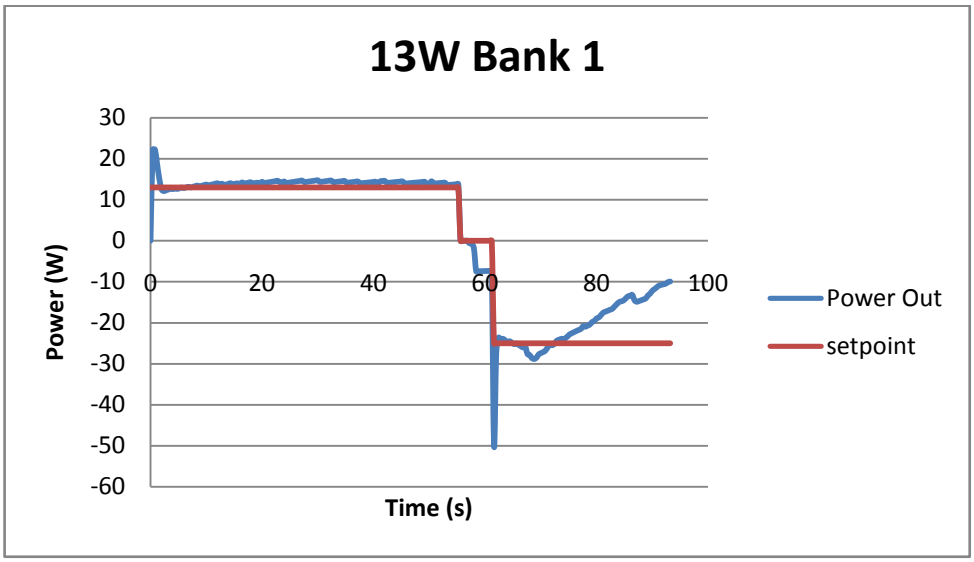

Figure 20 Controller response 2

These are examples of the tuned controllers, which as can be seen from the figures the buck operation has a very fast response and then settles on the set point for the duration of the test.

The controller worked best for lower powers; 25W appeared to be near its stability point. The controller was more likely to be unstable at higher set points if the tuning parameters were not quite right than at the lower set points.

The boost controller was much simpler due to the load being resistive and relied more heavily on the PI loop.

This controller was a linear controller that worked well for higher bank voltages. Once the voltage of the bank dropped below 15VDC the converter could no longer switch it up to the 45volts required to produce 25W, which explains the power drop off.

6.4 Capacitors

As supercapacitors, like electrolytic capacitors, have a tolerance of ± 20%, the capacitance needs to be verified for validation of experimental results.

As the capacitors were too large to be measured by multi meters that have an upper range in the order of micro Farads, a voltage step was performed on the capacitor bank to determine the capacitance.

Performed on the 27V capacitor bank over a 15V change the calculated capacitance was 2.495F where the expected nominal capacitance was 2.5F.

One of the practical factors in the construction of the capacitor banks was the inclusion of passive voltage balancing and over voltage protection. As supercapacitors have a large tolerance when they are placed in series there is the potential for some capacitors to have an unequal voltage drop across each cell, where a cell could have a voltage drop of over 2.7VDC, thereby damaging that capacitor. The passive voltage balancing was achieved by using high value low tolerance resistances across each capacitor cell to ensure the voltage was the same across each resistor.

The over voltage protection was a zener diode equal to the maximum voltage of the bank, This diode would discharge the bank to ground if the voltage exceeded the zener breakdown voltage.

7 Experimental method

The aims of the experiments are to measure the efficiency of charging and discharging a supercapacitor bank to/from a DC bus.

While the original intention was to do experiments for all four possible bank configurations, it became apparent that for the DC to DC converter testing it would not be possible to perform the required experiments on bank configurations 3 and 4 due to the low bank voltage.

7.1 Setup

Firstly the test rig, DC to DC converter and supercapacitor bank need to be set up using the following equipment or equivalents.

Equipment:

- 2 ESCORT 303TD power supplies
- 10 Vina 2.7V-25F Supercapacitors
- 2 LEM LTS 15-NP hall effect current sensors
- 1 NI USB-6008 DAQMX card
- Computer installed with labVIEW
- DC to DC converter in accordance with. schematic
- 2 low pass filters in accordance with schematic
- 2 SG3524 SMP control IC
- 4 270ohm 10W resistors
- 1 100uF capacitor
- Electronic consumables

The equipment is to be set up in accordance with the description given in section 5.6.

7.2 Method

The experiments to be performed are detailed in Table 4.

Table 4 Experiments

Test	Series Capacitors	Parallel Capacitors	Time (s)	Power (W)	Max Capacitor Voltage (V)
1.1	10	1	32	25.00	27
1.2	5	2	32	25.00	13.5
2.1	10	1	8	18.01	27
2.2	5	2	8	18.01	13.5
3.1	10	1	9	13.18	27
3.2	5	2	9	13.18	13.5

Tests are to be carried out in accordance with the above table with each test repeated 3 times or until the results are consistent.

The basic procedure for the experiments is as follows:

1. Connect the test rig as described in section 5.
2. Set up the labVIEW program for the test including setting time limits and voltage limits in the program
3. Set up the capacitor bank in the required configuration
4. Run the converter in buck mode at the appropriate power set point.
5. Disconnect the power supply and replace with a load bank
6. Run the converter in boost mode onto the load bank
7. Complete for all tests.

The general philosophy for each test is to charge the capacitor bank with constant power from the power supply through the DC to DC converter until the capacitor bank nears its maximum voltage rating and then to remove the power supply replace it with a load bank

and the converter then operates in boost mode to discharge the capacitor bank at a constant 25W.

8 Theoretical experiments

8.1 Theoretical results

A MATLAB script was created to assess the system's efficiency using the equations in section 5.3 as the capacitor model and using the following equations from Mohan[16] to model the losses in the DC to DC converter.

$$P_s = \frac{1}{2} V_d I_o f_s (t_{c(on)} + t_{c(off)}) \tag{5}$$

$$P_{on} = V_{on} I_o \frac{t_{on}}{T_s} \tag{6}$$

In the equation, V_d is the voltage seen by the MOSFET in the off position, I_o is the on state current. f_s is the switching frequency, and $t_{c(on)}$ and $t_{c(off)}$ are the MOSFET's switching delays times.

When capacitor internal loss due to ESR and inductor resistance are included, the total losses are given by:

$$P_{Loss} = P_s + P_{on} + I_o^2 \times (R_{ESR} + R_{LDC}) \tag{7}$$

This approach gives an indication of the losses of the converter but is not highly representative of the actual system as the calculations assumed a true square wave gate signal into the MOSFETs but in reality the system input waveforms are warped by the input capacitance of the MOSFET gate and the waveforms are rather noisy.

The MATLAB script uses the following equation and can be found in the appendices

$$\frac{dE(t)}{dt} = \frac{-CE(t) \pm \sqrt{C^2E(t)^2 - 4R_{ESR}C^2p}}{2RC^2} \quad (8)$$

Equation 8 is designed to obtain voltage discharge curves.

A script is first run to measure the discharge curve for the selected power and the final voltages are recorded.

These values are then placed into another script as the capacitor banks initial voltage. The equation is then run with a negative power to simulate charging. Once the time reaches its prescribed limit, the script feeds the equation a positive 25W, until the voltage of the bank is equal to or lower than the initial voltage. The script then outputs voltage, current and efficiency curves as well as calculations of energy.

The outputted graphs display voltage, current and efficiency. The curves have a positive gradient while the capacitor bank is being charged, and a negative gradient while the bank is being discharged.

8.2 Test 1

The first test applies 25W for 32 seconds. The results for all bank configurations are shown in Figure 21 and Table 5 and then discharged at a constant 25W.

Table 5 Test 1 Results

Bank	Input energy (Wh)	Capacitor energy (Wh)	Input efficiency (%)	Output energy (Wh)	Output efficiency (%)	Overall efficiency (%)
1	0.2222	0.2160	97.20	0.2054	95.09	92.44
2	0.2222	0.2147	96.62	0.2035	94.78	91.57
3	0.2222	0.2061	92.75	0.1871	90.78	84.21
4	0.2222	0.1793	80.69	0.1274	71.05	57.31

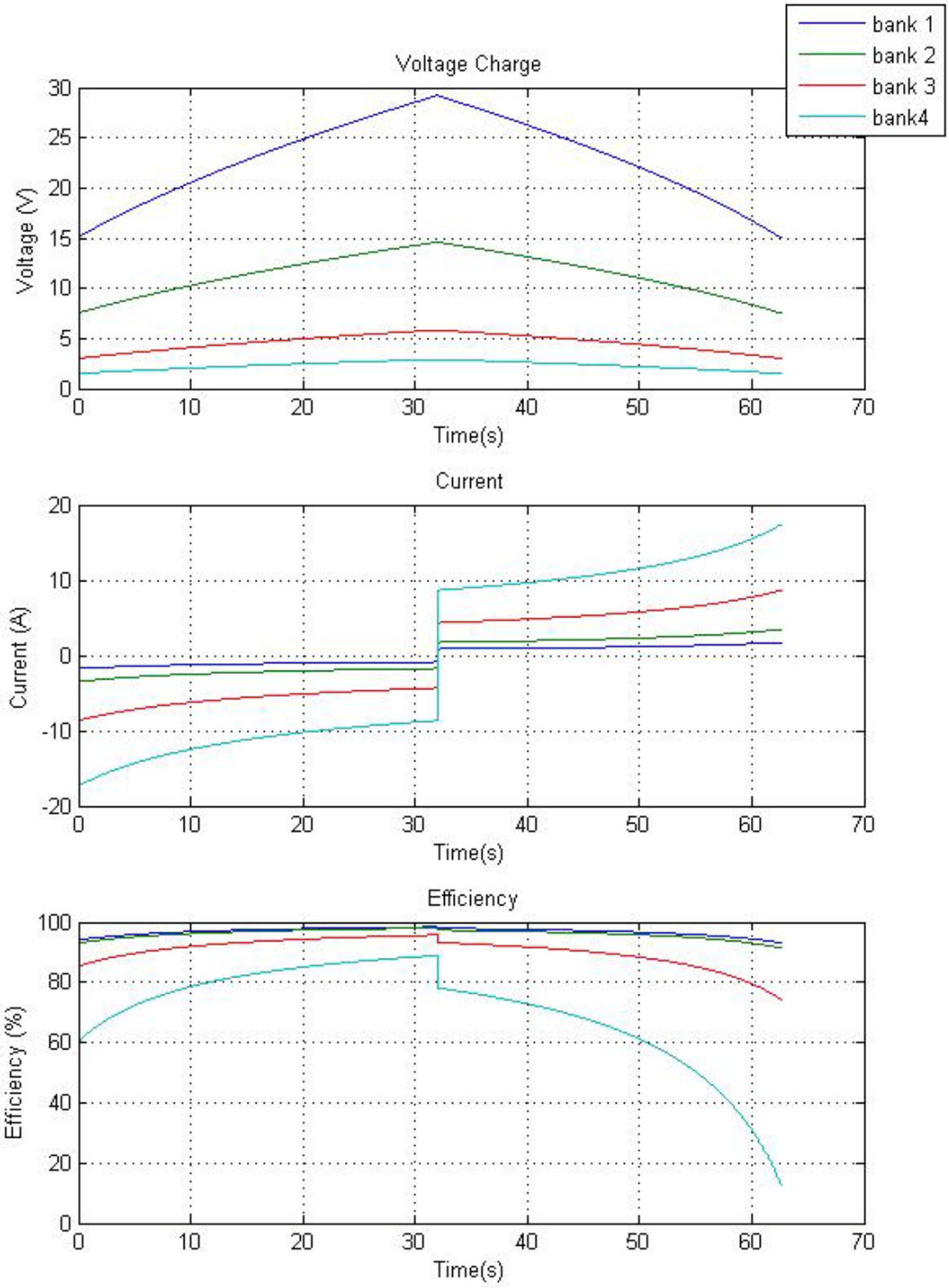

Figure 21 Test 1

8.3 Test 2

The second applies 18.01W for 8 seconds. The results for all bank configurations are shown in Figure 22 and Table 6 and then discharged at a constant 25W.

Table 6 Test 2 Results

Bank	Input energy (Wh)	Capacitor energy (Wh)	Input efficiency (%)	Output energy (Wh)	Output efficiency (%)	Overall efficiency (%)
1	0.0400	0.0395	98.70	0.0381	96.46	95.25
2	0.0400	0.0394	98.45	0.0378	95.94	94.55
3	0.0400	0.0386	96.45	0.0358	92.75	89.42
4	0.0400	0.0361	90.20	0.0282	78.12	70.54

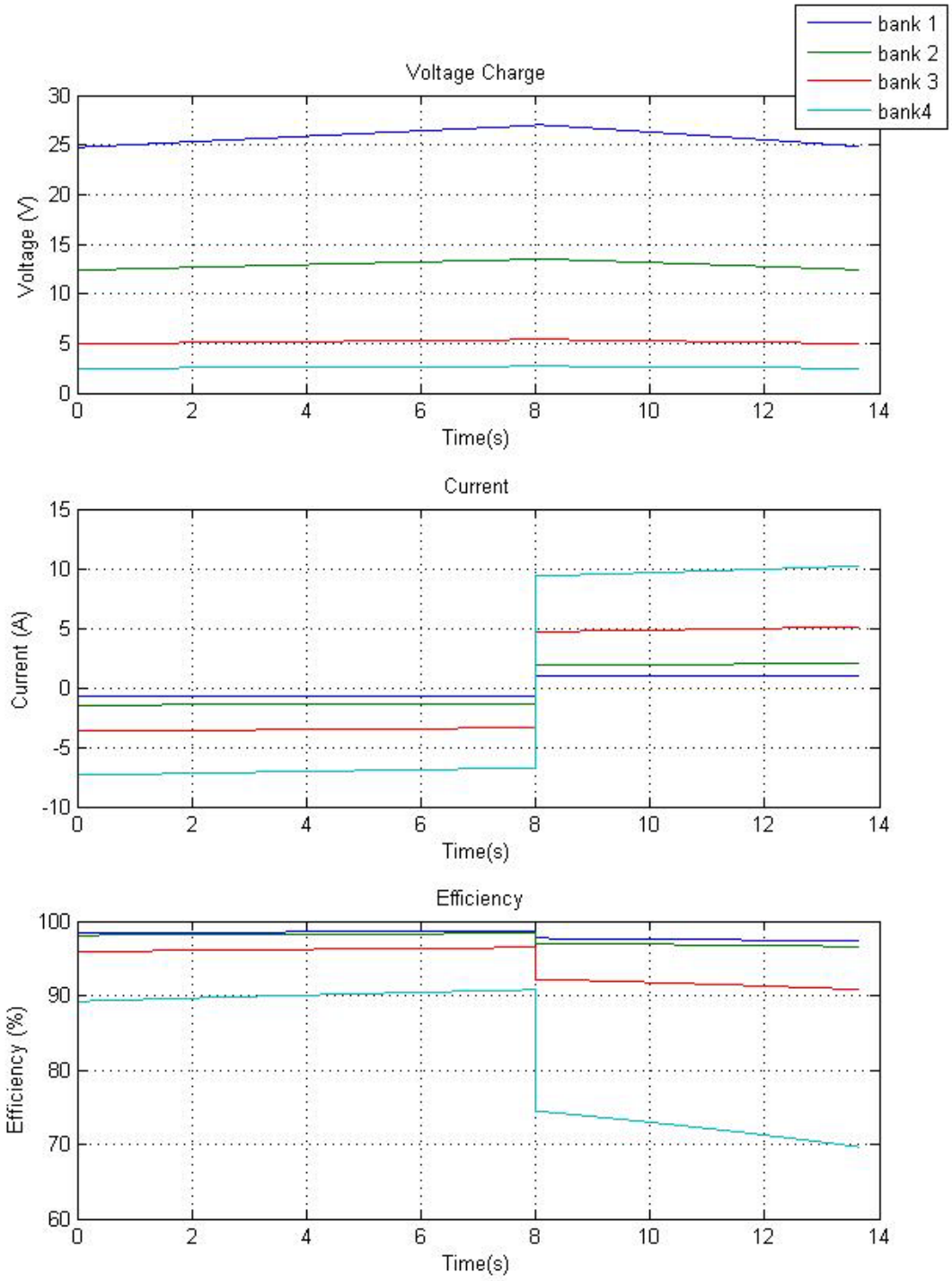

Figure 22 Test 2

8.4 Test 3

The third test applies 13.18W for 9 seconds. The results for all bank configurations are shown in Figure 23 and Table 7 and then discharged at a constant 25W.

Table 7 Test 3 Results

Bank	Input energy (Wh)	Capacitor energy (Wh)	Input efficiency (%)	Output energy (Wh)	Output efficiency (%)	Overall efficiency (%)
1	0.0330	0.0326	98.94	0.0315	96.63	95.61
2	0.0330	0.0326	98.94	0.0313	96.01	94.91
3	0.0330	0.0321	97.42	0.0296	92.21	89.88
4	0.0330	0.0306	92.87	0.0235	76.80	71.39

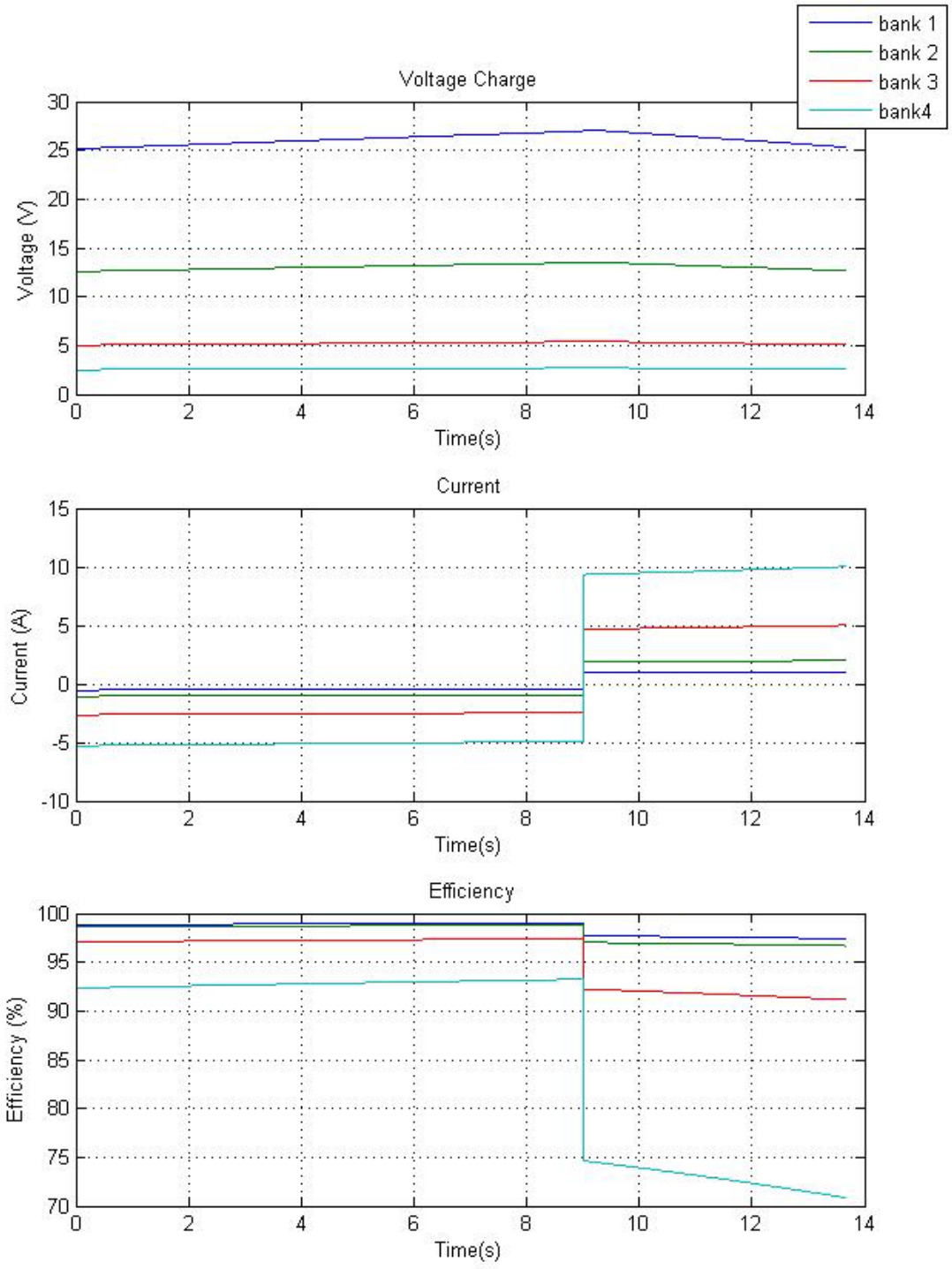

Figure 23 Test 3

8.5 Discussion

The four tests show a discernable pattern, the charging of the capacitor bank is highly efficient with low losses.

The major losses occur when the capacitors are being discharged, with the banks with a higher voltage being more efficient. This is the expected result due to the fact that the major losses are i^2R losses.

When the converter is operating in buck mode the switch only sees the higher currents of the lower banks for small time periods. The higher voltage configurations have the switch on for longer but at a much lower current. This results in lower losses in the buck mode then the boost mode.

When the converter is operating in boost mode the switch sees the output current from the capacitor bank which varies greatly with capacitor bank configuration. The lower voltage configurations have a higher capacitance, higher current output, and higher on switch time than the smaller capacitance higher voltage configurations. This results in larger switching losses and i^2R losses for these bank configurations.

Capacitors also have an internal equivalent series resistance (ESR), which as more capacitors are in parallel the resistance gets smaller due to the resistances being in parallel; the opposite occurs for series arrangements. While the ESR gets lower with more capacitors in parallel the current gets higher resulting in all the configurations having the same energy and same i^2R losses due to the ESR.

From the theoretical results it is clear that a capacitor bank with a higher voltage, while having less capacitance and a higher ESR ,is more efficient, as it will result in lower losses due to the lower current, while the configurations have the same losses due to ESR the MOSFET on state resistance and inductor resistance stay the same. As these configurations have lower current it will also result in a converter that is smaller, lighter and cooler, all of which are important factors in automotive applications.

9 Practical experimental results

The original intention was to test the four bank configurations but due to the operational characteristics of the converter it was decided to only test banks 1 and 2. A modification was also made to bank 2. Rather than switching to 45VDC and discharging at 25W (this was impractical as the highest gain possible out of the converter is roughly 3) it was switched to 30VDC and discharged at 25W.

Three tests were performed as outlined in the methods section, for each test tables were prepared with the following information.

- Buck
    - Ein, the energy delivered by the supply
    - Eout, the energy after the buck converter stage
    - Mean Pout, the power at the capacitor bank after the buck converter
    - ΔT which is the time period over which energy transfer was recorded over
- Boost
    - Eout, the energy out of the bank
    - Ein the energy into the load bank after the boost converter
    - Mean Pout, the mean power into the load bank after the converter
- Efficiency buck, the efficiency of the buck converter
- Efficiency capacitor is the efficiency of the capacitor bank
- Efficiency boost, the efficiency of the boost converter
- Efficiency total, the overall efficiency of the system

Bank 1 refers to the 27V arrangement and bank 2 to the 13.7V arrangement

9.1 Test 1 25W for 32s

The results for test 2 are depicted in Table 8, Table 9, Figure 24, Figure 25, Figure 26 and Figure 27.

Table 8 Test 1 energy

		Buck				***Boost***		
Bank	**Test**	**Ein (Wh)**	**Eout (Wh)**	**Mean Pout (W)**	**ΔT (s)**	**Eout (Wh)**	**Ein (Wh)**	**Mean Pout (W)**
1	**1**	0.2558	0.2054	23.3936	31.60	-0.1884	-0.1563	-14.8060
	2	0.2797	0.2277	25.6134	32.00	-0.2035	-0.1706	-14.6198
	3	0.2530	0.2085	25.3619	29.60	-0.1904	-0.1599	-15.6483
	4	0.2724	0.2222	24.9955	32.00	-0.2097	-0.1741	-13.9930
	Mean	**0.2652**	**0.2159**	**24.8411**	**31.2998**	**-0.1980**	**-0.1652**	**-14.7668**
2	1	0.2841	0.2183	24.56	32.00	-0.1946	-0.1598	-10.421
	2	0.2942	0.2188	25.91	30.40	-0.1929	-0.1604	-11.021
	3	0.2938	0.2265	25.49	32.00	-0.2022	-0.1683	-12.021
	4	0.2902	0.2238	25.17	32.00	-0.1993	-0.1660	-12.250
	Mean	**0.2927**	**0.2230**	**25.52**	**31.47**	**-0.1982**	**-0.1649**	**-11.76**

Table 9 Test 1 efficiency

Bank	Test	Efficiency buck (%)	Efficiency capacitor (%)	Efficiency boost (%)	Efficiency total (%)
1	**1**	80.28	91.74	82.96	61.10
	2	81.39	89.40	83.79	60.98
	3	82.43	91.32	84.00	63.23
	4	81.57	94.37	83.04	63.93
	mean	**81.42**	**91.71**	**83.45**	**62.31**
2	1	76.858	89.139	82.108	56.252
	2	74.375	88.178	83.143	54.527
	3	77.111	89.273	83.219	57.287
	4	77.104	89.064	83.314	57.213
	mean	**76.20**	**88.84**	**83.23**	**56.34**

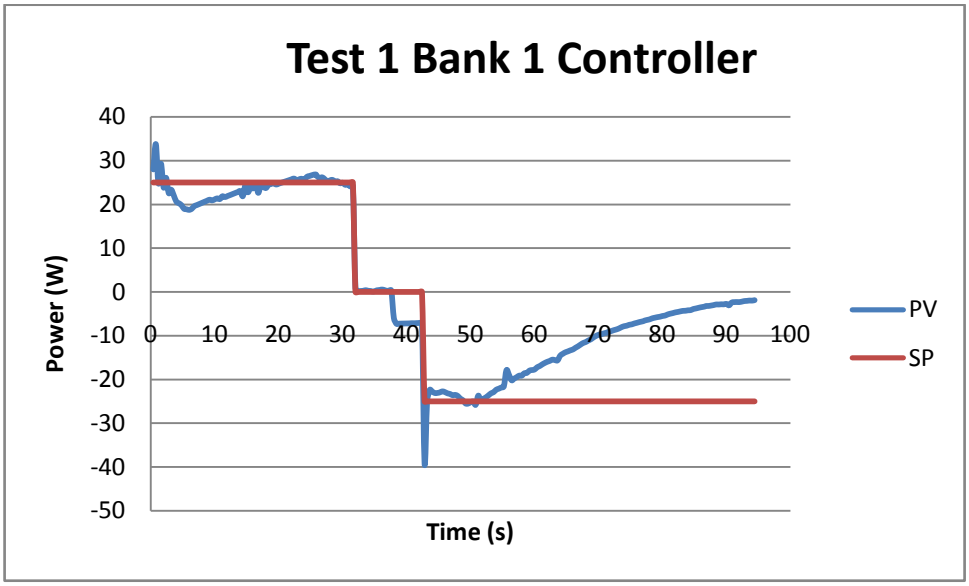

Figure 24 Test 1 bank 1 controller

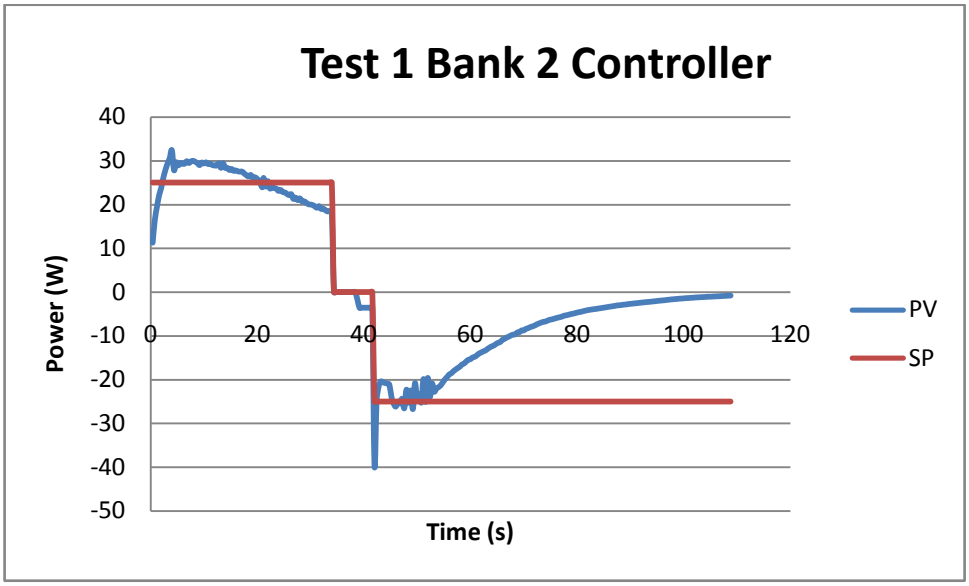

Figure 25 Test 1 bank 2 controller

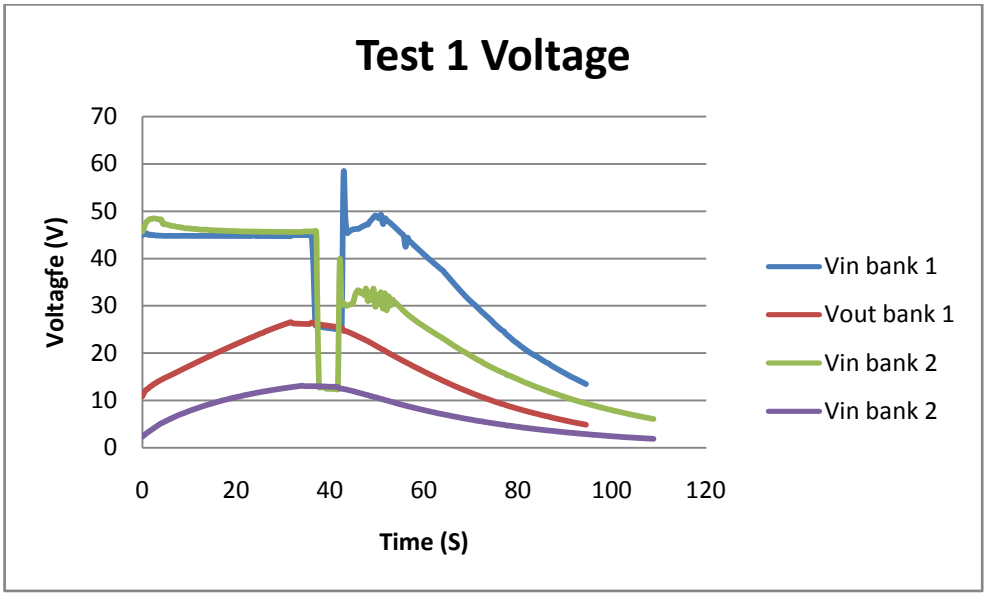

Figure 26 Test 1 voltage

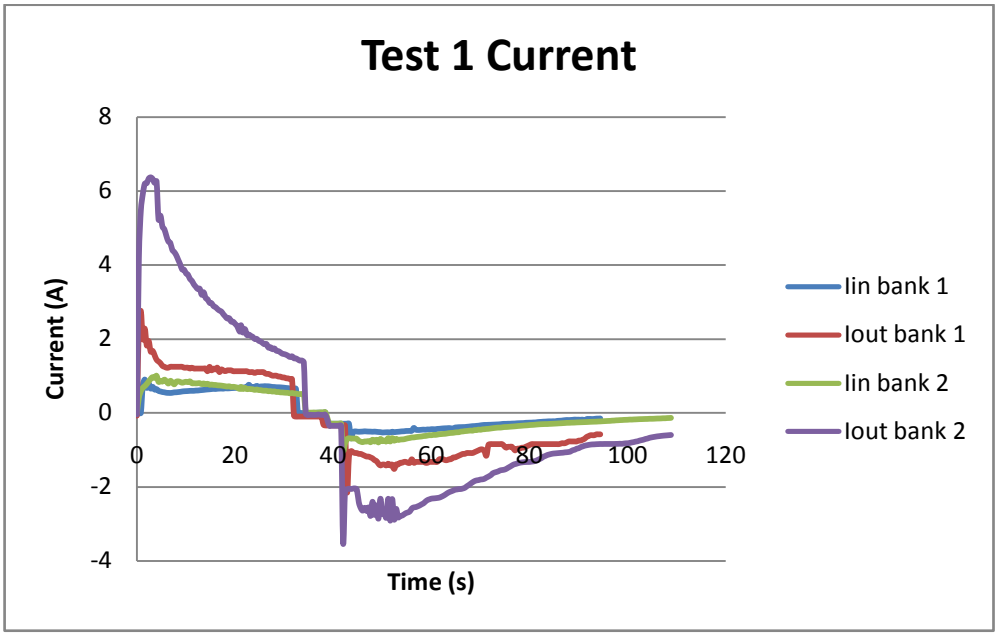

Figure 27 Test 1 Current

A few explanations are in order for the graphs. The start of the graphs display the buck mode with constant power of 25 watts in reference to the output power.

The next section, where the values go to zero in the controller/current graphs, is when the test was stopped due to the capacitor bank voltage reaching maximum bank voltage. Where the power drops down to a few watts the power supply has been disconnected and the load bank connected.

Finally the last section is when the converter is operating in boost mode.

One important aspect of this test is noticing that the converter does not boost the voltage up to 45V (for bank 1) and 30V (for bank 2) for the entire discharge period. This is because the bank voltage drops too low to be switched that high. This explains why the mean boost output power is -12W and -14W for bank 1 and bank 2 respectively rather then -25W as it should be.

9.2 Test 2 18W for 8s

The results for test 2 are depicted in Table 10, Table 11, Figure 28, Figure 29, Figure 30 and Figure 31

Table 10 Test 2 energy

		Buck				***Boost***		
Bank	**Test**	**Ein (Wh)**	**Eout (Wh)**	**Mean Pout (W)**	**ΔT (s)**	**Eout (Wh)**	**Ein (Wh)**	**Mean Pout (W)**
1	**1**	0.0452	0.0380	17.10	8.00	-0.0318	-0.0284	-23.213
	2	0.0509	0.0424	17.36	8.80	-0.0355	-0.0315	-23.592
	3	0.0460	0.0387	17.41	8.00	-0.0322	-0.0290	-23.692
	4	0.0437	0.0369	17.49	7.60	-0.0310	-0.0279	-22.800
	mean	**0.0464**	**0.0390**	**17.3395**	**8.1013**	**-0.0326**	**-0.0292**	**-23.3244**
2	1	0.0460	0.0359	16.55	7.80	-0.0307	-0.0258	-24.312
	2	0.0499	0.0393	17.68	8.00	-0.0323	-0.0268	-21.931
	3	0.0472	0.0368	16.55	8.00	-0.0315	-0.0264	-23.728
	4	0.0474	0.0373	17.66	7.60	-0.0318	-0.0269	-21.971
	mean	**0.0482**	**0.0378**	**17.29**	**7.87**	**-0.0319**	**-0.0267**	**-22.54**

Table 11 Test 2 efficiency

Bank	Test	Efficiency buck (%)	Efficiency capacitor (%)	Efficiency boost (%)	Efficiency total (%)
1	**1**	84.06	83.71	89.13	62.72
	2	83.34	83.68	88.57	61.77
	3	84.11	83.20	89.94	62.94
	4	84.58	83.99	89.84	63.82
	mean	**84.02**	**83.65**	**89.37**	**62.81**
2	1	77.987	85.685	83.793	55.993
	2	78.790	82.269	82.978	53.786
	3	77.814	85.608	83.835	55.847
	4	78.644	85.428	84.400	56.704
	mean	**78.42**	**84.44**	**83.74**	**55.45**

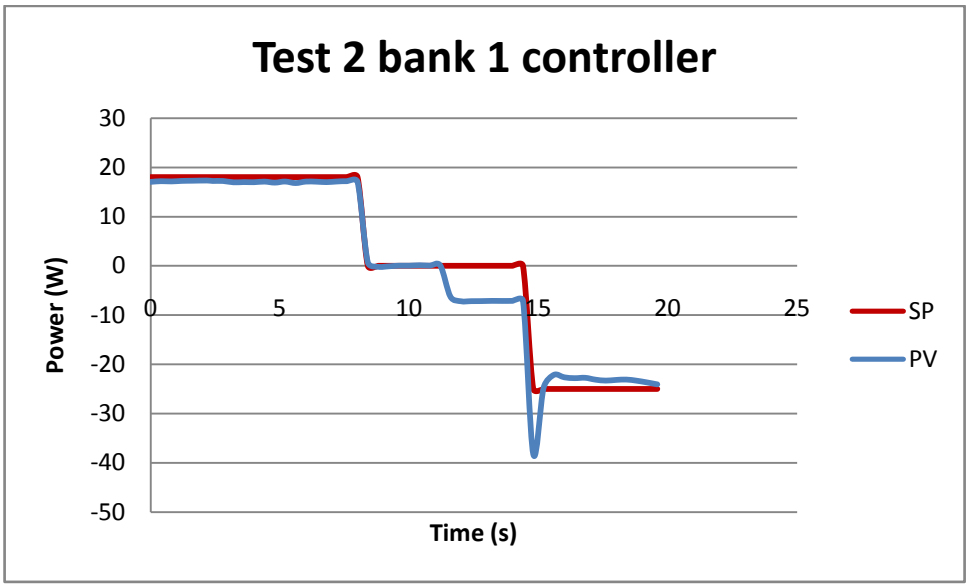

Figure 28 Test 2 bank 1 controller

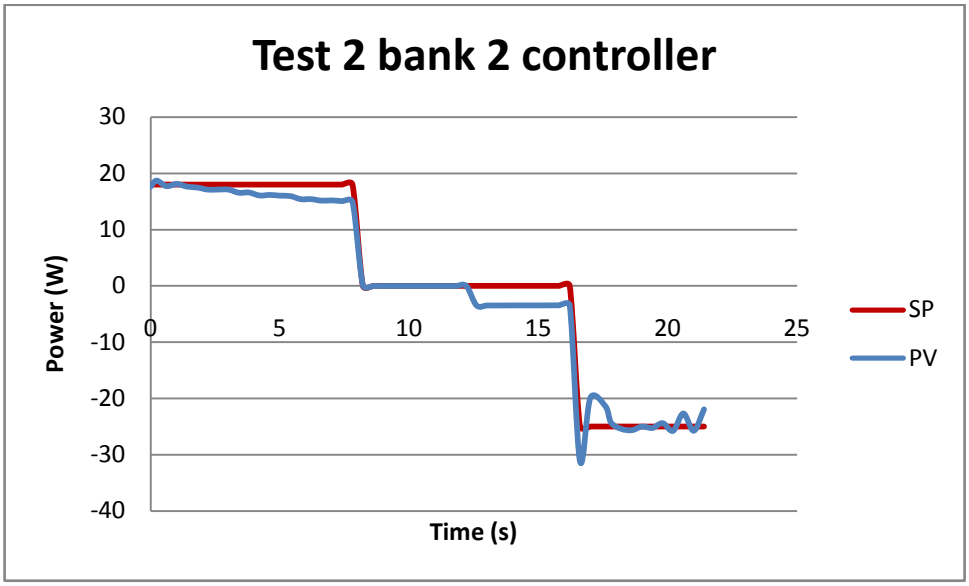

Figure 29 Test 2 bank 2 controller

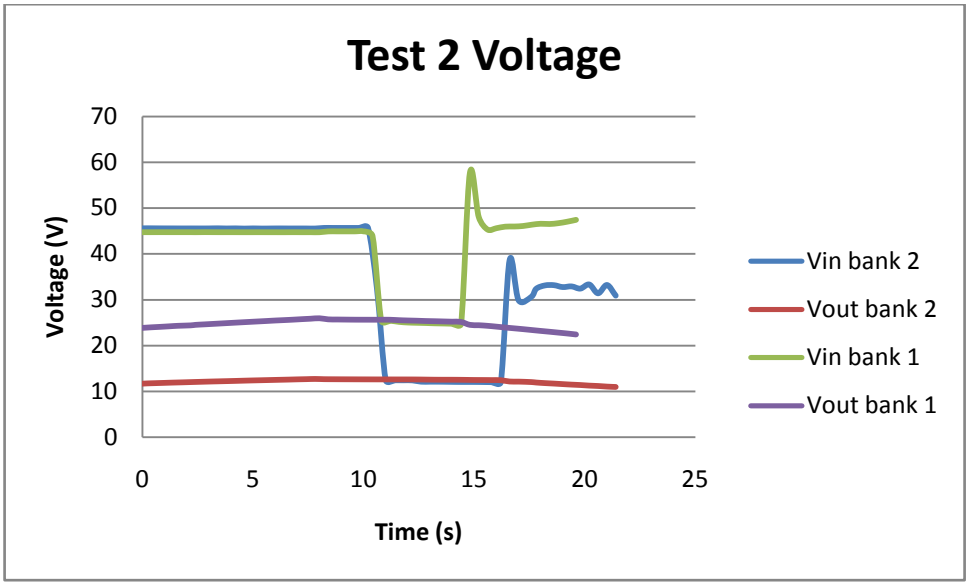

Figure 30 Test 2 voltage

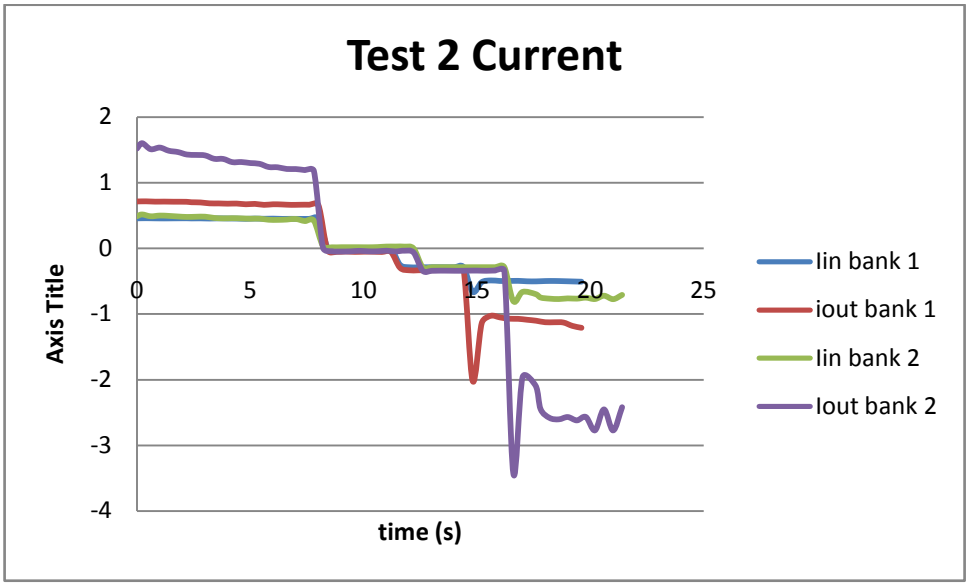

Figure 31 Test 2 current

The average powers are very close to the SP which means that the controller and converter operated as expected.

The way the data was analysed was that the experiment was started with the capacitor bank at a low voltage, when the voltage reached the maximum voltage of the bank it was switched from supply to load and then operated in boost mode till the capacitor bank was at a low voltage.

As the data only needed to be analysed for a constant power for 8 seconds, the analysed data was the data for the 8 seconds preceding the end of the buck mode. For the discharge, as there was some voltage drop due to the time taken to switch from buck to boost mode, the discharge data was taken by measuring the change in voltage during the buck mode and taking the data for the same voltage difference once the boost controller had started.

9.3 Test 3 13W for 9s

The results for test 3 are depicted in Table 12, Table 13, Figure 32, Figure 33, Figure 34 and Figure 35.

Table 12 Test 3 energy

		Buck				***Boost***		
Bank	**Test**	**Ein (Wh)**	**Eout (Wh)**	**Mean Pout (W)**	**ΔT (s)**	**Eout (Wh)**	**Ein (Wh)**	**Mean Pout (W)**
1	**1**	0.0387	0.0343	14.03	8.80	-0.0276	-0.0253	-22.79
	2	0.0371	0.0316	12.94	8.80	-0.0254	-0.0228	-22.85
	mean	**0.0379**	**0.0330**	**13.4860**	**8.8005**	**-0.0265**	**-0.0241**	**-22.8208**
2	1	0.0377	0.0295	12.63	8.40	-0.0219	-0.0190	-34.34
	2	0.0419	0.0319	13.05	8.80	-0.0266	-0.0226	-33.19
	3	0.0424	0.0309	12.10	9.20	-0.0268	-0.0226	-22.54
	4	0.0417	0.0317	12.96	8.80	-0.0260	-0.0218	-28.05
	mean	**0.0420**	**0.0315**	**12.70**	**8.93**	**-0.0265**	**-0.0223**	**-27.92**

Table 13 test 3 efficiency

Bank	**Test**	**Efficiency buck (%)**	**Efficiency capacitor (%)**	**Efficiency boost (%)**	**Efficiency total (%)**
1	**1**	88.65	80.41	91.80	65.44
	2	85.28	80.35	89.89	61.59
	mean	**86.96**	**80.38**	**90.85**	**63.51**
2	1	78.08	74.19	87.12	50.47
	2	76.04	83.35	84.98	53.86
	3	72.91	86.78	84.02	53.16
	4	76.04	81.94	84.05	52.37
	mean	**75.00**	**84.02**	**84.35**	**53.13**

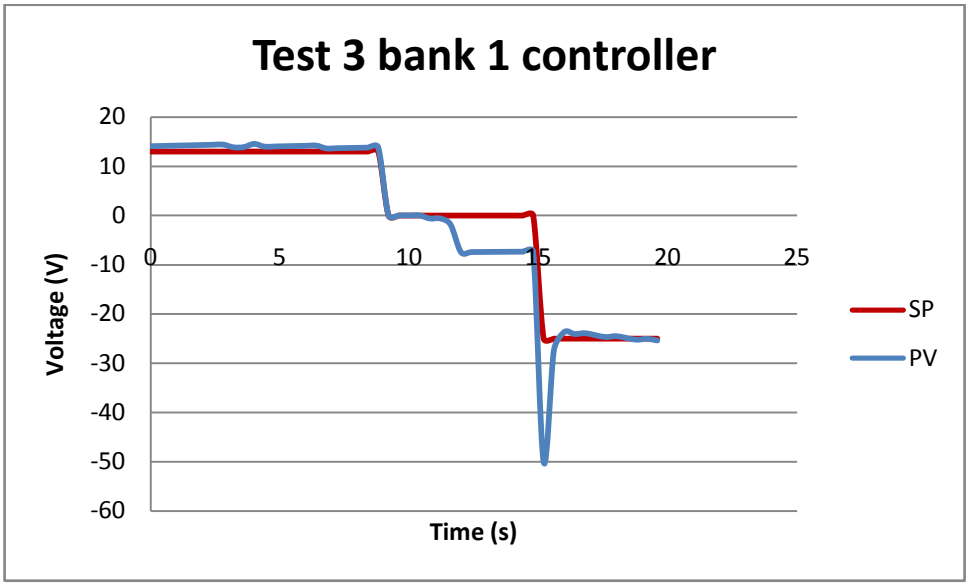

Figure 32 Test 3 bank 1 controller

Figure 33 Test 3 bank 2 controller

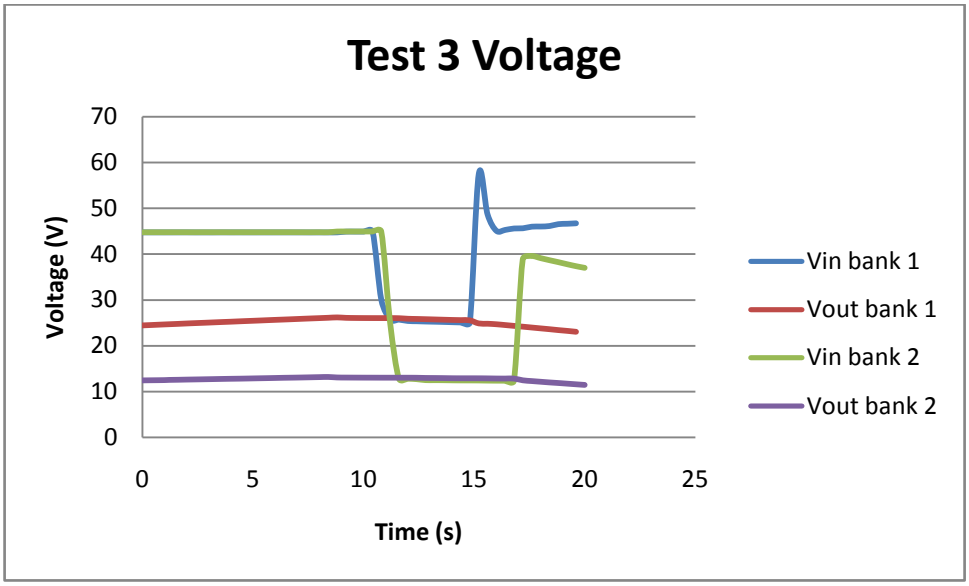

Figure 34 Test 3 voltage

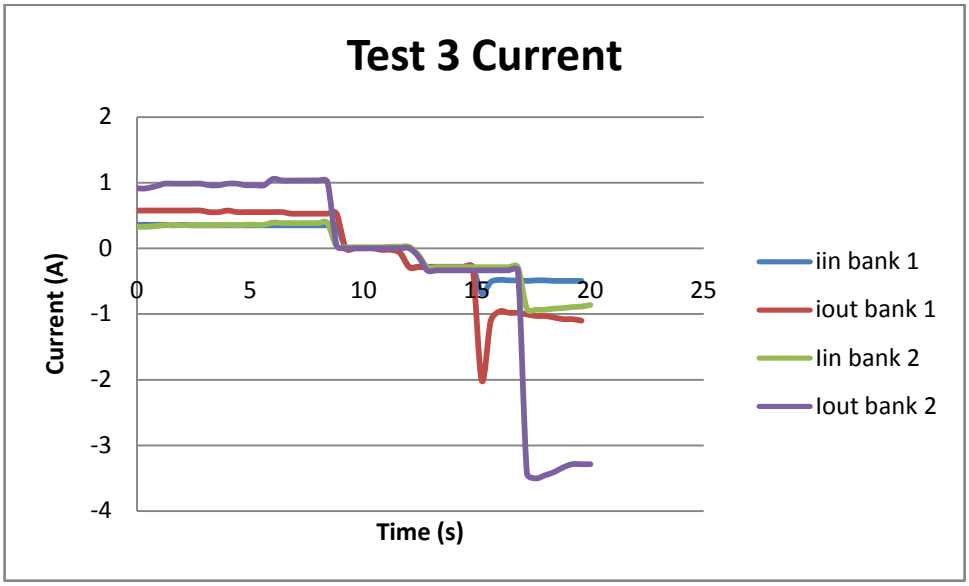

Figure 35 Test 3 current

The converter was not operating correctly in boost mode. For bank 2 the output voltage was too high, which explained the larger mean boost input powers. There were only two bank 1 measurements as the other measurements taken had erroneous current measurements.

9.4 Discussion

The results confirm the theoretical results and show that bank 1 is more efficient than bank 2. Looking at Table 14 and Table 15 some interesting trends have emerged.

Table 14 Bank 1 summary

Power	Efficiency buck (%)	Efficiency capacitor (%)	Efficiency boost (%)	Efficiency total (%)
13	86.96	80.38	90.85	63.51
18	84.02	83.65	89.37	62.81
25	81.42	91.71	83.45	62.31

For bank 1 the buck converter was more efficient at the lower powers with the capacitor more efficient at higher powers. The buck converter efficiency stayed relatively stable except for the 25W case and this decreased efficiency may be due to the large switching range.

The buck converter is more efficient at the lower powers. This was unexpected as the testing of the converter showed higher efficiencies with higher duty cycles. This can be explained, as the experiments had higher currents then the testing resulting in i^2R losses to dominate.

Interestingly enough, more energy was retrieved from the capacitor when charged at higher power levels. This was unexpected as the capacitors losses were modelled as i^2R losses due to the capacitors ESR and as such was expected that the larger powers would lose more power.

The results for the boost converter are as expected as each test has the same power flowing as it is being discharged at a constant 25W. The exception with the 25W test can be explained as the 25W test was run over 32 seconds for the buck mode causing the discharge to have to run for considerably longer than the other tests. This resulted in the converter having to operate over a much larger voltage range thereby decreasing the efficiency by increasing currents running through the MOSFET.

Table 15 Bank 2 summary

Power	Efficiency buck (%)	Efficiency capacitor (%)	Efficiency boost (%)	Efficiency total (%)
13	75.00	84.02	84.35	53.13
18	78.42	84.44	83.74	55.45
25	76.20	88.84	83.23	56.34

For bank 2 the results were much more consistent then for bank 1. It shows no discernable pattern for the buck mode and is relatively consistent for the capacitor and boost mode with a few variations. Similar to bank 1 the capacitor was more efficient at the higher powers and the buck converter was relatively constant.

Table 16 Bank 1 and 2 summary

Bank	Efficiency buck (%)	Efficiency capacitor (%)	Efficiency boost (%)	Efficiency total (%)
1	84.13	85.25	87.89	62.88
2	76.54	85.77	83.77	54.97

Table 16 displays the means of the efficiencies across all of the tests for each bank. This gives a clear indication into the performance difference between the bank configurations. As can be seen in the table, the capacitor efficiency is the same on average for both configurations where bank 1 has a more efficient buck and boost conversion.
The end to end efficiency of both bank 1 and bank 2 did not vary significantly over the different powers but there is a marked difference in efficiency between the two banks.

The difference in efficiency is in line with the theoretical results. Although the theoretical results were highly optimistic about the converters efficiency.

9.5 Measurement uncertainties

As with all physical measurement devices the devices used to obtain the results do have errors. While the hall effect current sensors had a very low error of .2%, the national instruments DAQ card has an absolute error of .0147 V. taking the error of the current measurements to.

$$I_{inerror} = \left(\left(I_{in}\frac{.625}{5} + 2.5\right)\frac{.2}{100} + .0147 - 2.5\right)\frac{5}{.625} \quad (8)$$

$$I_{outerror} = \left(\left(I_{out}\frac{.625}{15} + 2.5\right)\frac{.2}{100} + .0147 - 2.5\right)\frac{15}{.625} \quad (9)$$

As the hall effect outputs a voltage signal the current measurement needs to be converted back to volts where it is times against its error, then the DAQ card error is added, then converted back into amps.

The voltage was calibrated against a fluke 73 digital multimeters and thus the measured voltage errors are the same as the fluke device, which is 2%.

This creates an power error equation of

$$P_{inerror} = I_{inerror}\, V_{in}\, \frac{2}{100} \tag{10}$$

$$P_{outerror} = I_{outerror}\, V_{out}\, \frac{2}{100} \tag{11}$$

While this gives the theoretical uncertainties, in reality uncertainties will be higher due to noise on the system. While most of the noise for the current measurements was filtered out, some remained to add to the measurement error.

10 Results discussion

The efficiencies of the practical system were much lower than the theoretical results. This discrepancy is due mainly to the model not accurately representing the losses of the converter.

Both tests showed that the bank configuration with more cells in series is the more efficient due to the major losses of the system being in the converter and the efficiencies of the capacitor were similar for the different bank configurations when subjected to the same power test. This was expected, as while the ESR goes down with more cells in parallel the current goes up, causing the losses to theoretically be the same for different configurations.

While the converter could be redesigned to be more efficient for the lower bank configurations (i.e. more MOSFETs in parallel to reduce the on state resistance) this would increase the overall weight of the system, which is not desirable in an automotive application.

It is expected in practice there would be a point of equilibrium where the advantages of the decreased output current is out weighed by the large voltage that the converter has to operate over. For example if there was a maximum 500VDC rating on a bank the converter would have to be able to switch over at least a 250VDC range.

11 Improvement, complications and possible further work

As the project did not meet all of its original objectives due to time constraits, the major improvements are in line with the completion of the DC to DC converter design to get it to operate within the original expected behaviour.

This involves:

- Improvements of the driver circuits to get a higher boost duty cycle
- Improvements in the driver circuits to allow the buck switching frequency to be increased to 133kHz
- c
- Implementation of the controller onto a microcontroller such as the 68HC11 to increase controller speed and controller performance.
- Place circuits onto a PCB
- Improve test rig to include relays to switch the load bank and power supply in and out

With more time a more advanced DC to DC converter could be implemented such as an isolated ZVS resonant circuit. This would increase the operating efficiency.

A real world application which takes the project to the next level such as using a generator as the power supply at high voltage to charge a much larger capacitor bank would be ideal. This would allow more realistic testing and is the next step to introducing it into an electric vehicle.

As this experiment was originally designed to test a number of bank configurations, the DC to DC converter was designed with a broad operational range. This resulted in a converter that in practice could not perform experiments on the two lower bank configurations.

If a converter was designed for a particular configuration, an isolated topology would be ideal. This would allow the transformer to perform the majority of the voltage step-up and step-down. Coupled with zero voltage switching, which uses a resonant circuit to reduce switching losses, the converter would be more efficient and would be a more realistic real world solution, similar to [11, 12].

12 Summary

The aims of this project were to build a supercapacitor bank, a DC to DC converter, and a testing rig to perform efficiency testing for various configurations of the super capacitor bank against various hybrid electric vehicle regenerative braking profiles .

Most of the aims of the project were met. A DC to DC converter was designed, built and tested, a test rig was constructed and efficiency was tested for two bank configurations under three different braking profiles.

While improvements in the operation of the converter would have been ideal to allow for more testing of the capacitor bank in different configurations, most of the aims of the project were still met.

Both theoretical testing and practical experiments agreed that the configurations with higher maximum voltages, i.e. more cells in series were more efficient as they had lower output and input currents, which meant lower i^2R losses in the circuit.

In the practical apparatus, average efficiencies of around 63%were typical for the 27V bank arrangement and 55% for the 13.7V arrangement, showing a clear improvement in having more cells in series.

13 References

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14 Appendices

The Appendices are located on the attached CD under the following headings:

- Data sheets
- Programs
    - Matlab
    - Test rig
- Reports
- Results
    - Converter pictures
    - Processed
        - 15V
        - 27V
    - Raw data
    - Report data

Data sheets contains the relevant data sheets i.e. MOSFETs, Transistors, DAQ cards.

Programs contains the labVIEW test rig program and the MATLAB scripts used to create the theoretical results.

Reports contains the project plan, presentation and progress report.

Result contains all if the experimental data. Converter pictures contain the oscilloscope screen shots. Processed data includes the data that was used in the results sections. Raw data contains the unprocessed data and report data contains the tables for the report.