MOSFET short channel effects

overview

Five different short-channel effects can be distinguished:

- velocity saturation
- drain-induced barrier lowering (DIBL)
- impact ionization
- surface scattering
- hot electrons

MOSFET standard equations

1 $$I_{DS} = WC_{OX}(V_{GS} - V - V_{TH})\mu_n \, dV/dx$$

2 $$I_{DS}dx = WC_{OX}(V_{GS} - V - V_{TH})\mu_n dV$$

MOSFET standard equations

3

$$I_{DS}\int_0^L dx = WC_{OX}\mu_n \int_0^{V_{DS}} (V_{GS} - V - V_{TH})dV$$

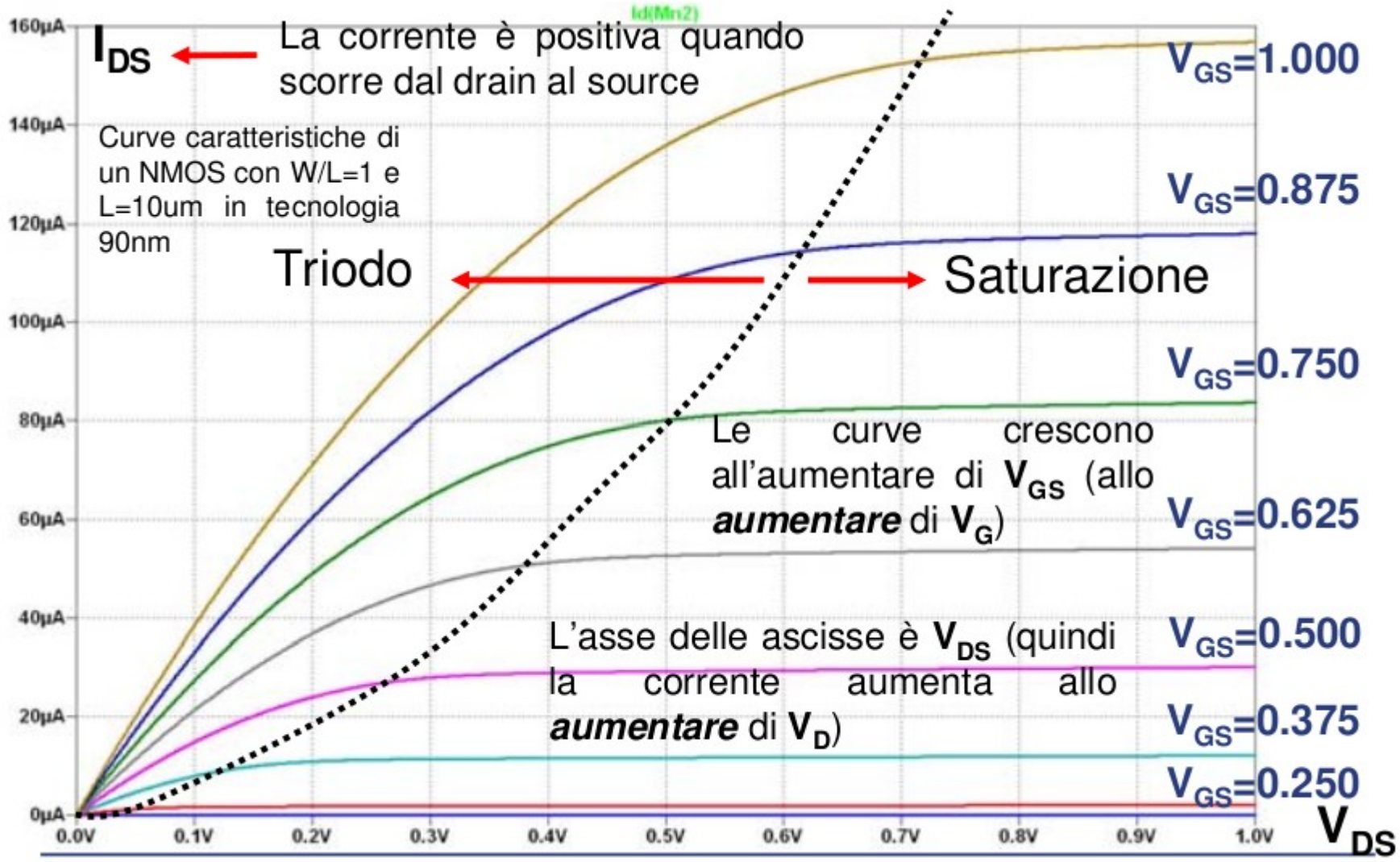
4

$$I_{DS}L = WC_{OX}\mu_n\left[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

5

$$I_{DS} = \mu_n C_{OX}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

MOSFET standard equations



Short channel effects

$$v_n = \mu_n E$$

$$v_p = \mu_p E$$

- Le equazioni classiche si basano sull'assunzione che la velocità dei portatori di carica (elettroni o lacune) sia proporzionale al campo elettrico orizzontale fra drain e source, attraverso una costante di proporzionalità denominata **mobilità**.

- In realtà la velocità dei portatori, per campi elettrici elevati, non aumenta linearmente ma viene limitata dagli effetti di scattering (collisioni) col reticolo del semiconduttore.
- La conseguenza è che la mobilità non è una costante ma varia col campo elettrico orizzontale (*E*).
- Esiste un valore critico del campo elettrico (E_C) oltre il quale la velocità satura e non aumenta più per ulteriori aumenti del campo elettrico.
- Quindi la dipendenza della velocità dal campo è **non lineare**
- Questo effetto è presente anche nei transistor a canale lungo, solo che in tale caso il campo elettrico orizzontale risulta più piccolo e non raggiunge il valore critico

$$v_n = \frac{\mu_n E}{1 + \frac{E}{E_C}}$$

MOSFET equation with SCE

1 $$I_{DS} = WC_{OX}(V_{GS} - V - V_{TH}) \frac{\mu_n \, dV/dx}{1 + \frac{dV/dx}{E_C}}$$

2 $$I_{DS}\left(1 + \frac{dV/dx}{E_C}\right) = WC_{OX}(V_{GS} - V - V_{TH})\mu_n \, dV/dx$$

MOSFET equation with SCE

3 $$I_{DS}\int_0^L dx + \frac{I_{DS}}{E_C}\int_0^{V_{DS}} dV = WC_{OX}\mu_n \int_0^{V_{DS}} (V_{GS} - V - V_{TH})dV$$

4 $$I_{DS}L + \frac{I_{DS}}{E_C}V_{DS} = WC_{OX}\mu_n\left[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

5 $$I_{DS} = \frac{\mu_n C_{OX}}{1 + \frac{V_{DS}}{LE_C}}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

MOSFET equation with SCE

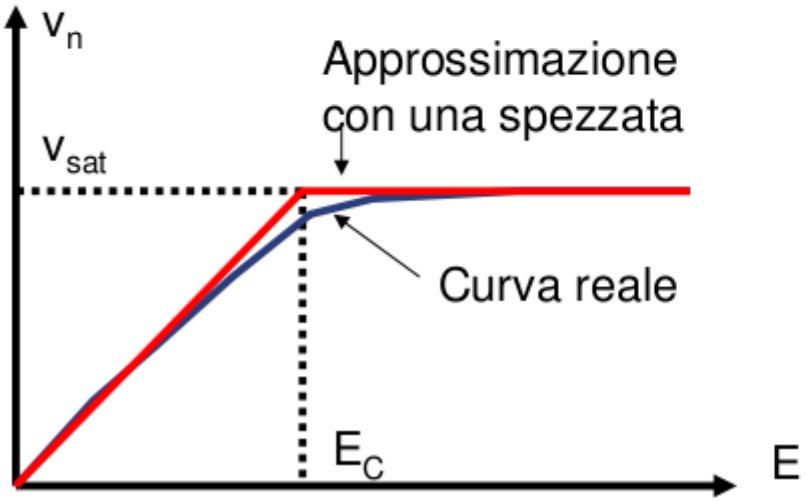
- L'espressione è uguale a quella classica con, in più, un termine al denominatore
- La corrente effettiva è dunque più piccola di quanto atteso, tanto più piccola quanto più è grande il termine V_{DS}/L, che fornisce una sorta di misura del "campo medio" nel canale
- Tanto più tale valore si avvicina al valore critico (quindi maggiore è V_{DS} o minore è L) tanto più il transistor è affetto dal fenomeno di saturazione della velocità

MOSFET equation with SCE

Le equazioni reali sono di difficile utilizzo, quindi useremo una semplificazione del primo ordine che si rileva però molto utile ed efficace per l'analisi dei circuiti digitali:

supponiamo che la saturazione della velocità avvenga bruscamente per un certo campo critico e che prima del valore critico abbia il valore costante normalmente utilizzato.

In questo modo l'equazione del transistor ***in triodo*** rimane quella classica e cambia solo l'espressione per la ***corrente di saturazione***, che ricaviamo dall'equazione classica sostituendo il nuovo valore della tensione di saturazione (che è la tensione per cui il campo raggiunge il valore critico)



$$v_{sat} = \mu_n E_C = \mu_n \frac{V_{DSAT}}{L}$$

$$V_{DSAT} = \frac{L v_{sat}}{\mu_n}$$

MOSFET equation with SCE

La corrente di saturazione risulta quindi pari a:

$$I_{DS} = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DSAT} - \frac{V_{DSAT}^{\ 2}}{2}\right]$$

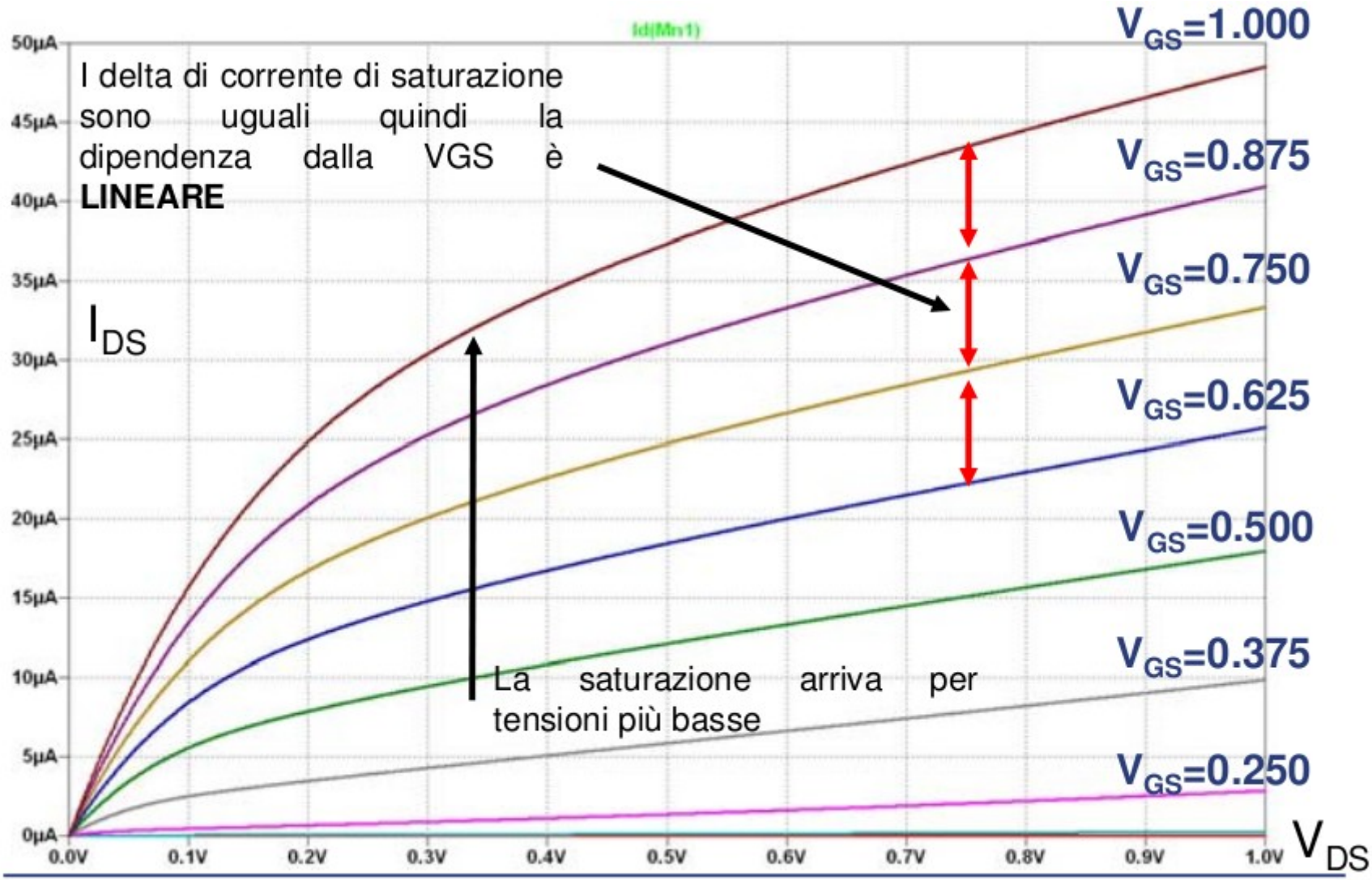
$$I_{DS} = \mu_n C_{OX} \frac{W}{L} V_{DSAT}\left[(V_{GS} - V_{TH}) - \frac{V_{DSAT}}{2}\right]$$

$$I_{DS} = k_n V_{DSAT}\left[(V_{GS} - V_{TH}) - \frac{V_{DSAT}}{2}\right]$$

Costanti di processo e progetto

La dipendenza dalla V_{GS} è **LINEARE** anzi che **QUADRATICA**

MOSFET equation with SCE



introduction

- In order to realize higher-speed and higher-packing density MOS integrated circuits, the dimensions of MOSFET's have continued to shrink

- The power consumption of modern VLSI's has become rather significant as a result of extremely large integration

- Choosing a lower power supply voltage is an effective method. However, it leads to the degradation of MOSFET current driving capability

- Scaling of MOS dimensions is important in order to improve the drivability, and to achieve higher-performance and higher-functional VLSI's

overview

- "The story of MOSFET scaling is the history of how to prevent short-channel effects (SCE)"

- SCE causes the dependence of device characteristics, such as threshold voltage, upon channel length

- This leads to the scatter of device characteristics because of the scatter of gate length produced during the fabrication process

- Moreover, SCE degrades the controllability of the gate voltage to drain current, which leads to the degradation of the subthreshold slope and the increase in drain off-current

- Thinning gate oxide and using shallow source/drain junctions are known to be effective ways of preventing SCE

overview

- The detrimental short-channel effects occur when the gate length is reduced to the same order as the channel depth

- When the channel length shrinks, the absolute value of threshold voltage becomes smaller due to the reduced controllability of the gate over the channel depletion region by the increased charge sharing from source/drain

- The predominating features of SCE are a lack of pinchoff and a shift in threshold voltage with decreasing channel length as well as drain induced barrier lowering (DIBL) and hot-carrier effect at increasing drain voltage

- Increased charge sharing from source/drain degrades the controllability of gate voltage over channel current

overview

• Short-channel effects (SCE) can be physically explained by the so-called drain-induced barrier lowering (DIBL) effect which causes a reduction in the threshold voltage as the channel length decreases

• In an SOI device, SCE is also influenced by thin-film thickness, thin-film doping density, substrate biasing, buried oxide thickness and processing technology

Drain-induced barrier lowering (DIBL)

- In the weak inversion regime there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions

- The barrier height for channel carriers should ideally be controlled by the gate voltage to maximize transconductance

- DIBL effect occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, upon application of a high drain voltage

- This increases the number of carriers injected into the channel from the source leading to an increased drain off-current

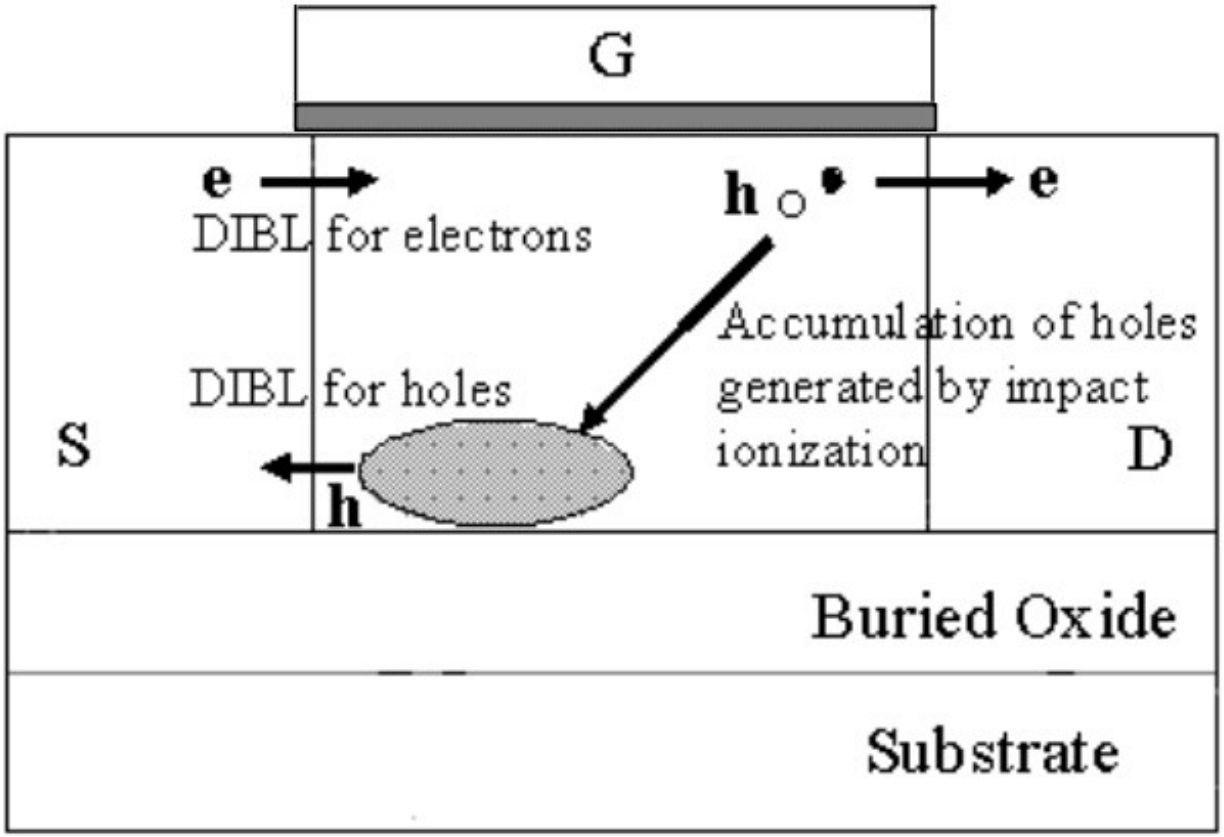
- **Thus the drain current is controlled not only by the gate voltage, but also by the drain voltage!**

Drain-induced barrier lowering (DIBL)

- In addition to the surface DIBL, there are two unique features determining SCEs in thin-film SOI devices

- Positive bias effect to the body due to the accumulation of holes generated by impact ionization near the drain

- The DIBL effect on the barrier height for holes at the edge of the source near the bottom



Drain-induced barrier lowering (DIBL)

- Holes generated near the drain due to impact ionization accumulate in the body region, and then positively bias the body, reducing VT

- This positive bias effect leads to VT lowering for all gate lengths, including rather long gates such as 2 μm

- The hole generation rate due to impact ionization increases as gate length decreases under a fixed value of VD

- This effect is predominant in PD SOI nMOSFETs and results in so-called floating body effects (FBE)

Drain-induced barrier lowering (DIBL)

- The DIBL effect on the barrier height for holes reduces the positive bias effect to the body because the accumulated holes in the body can more easily surmount the barrier and flow to the source

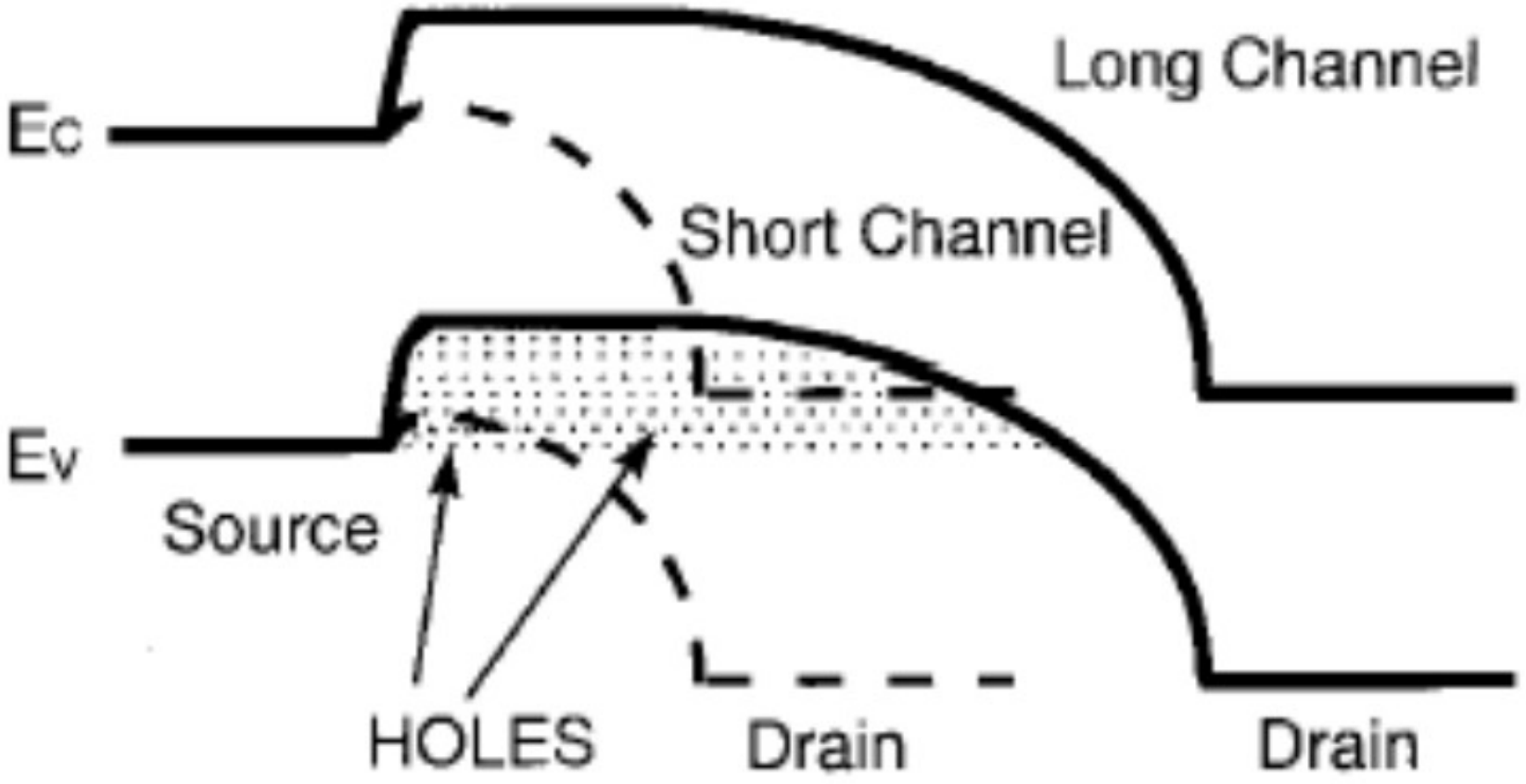
- As a result fewer number of accumulated holes remain which weakens the VT lowering

- The potential near the bottom in the thin-film increases as gate length decreases due to the drain electric field

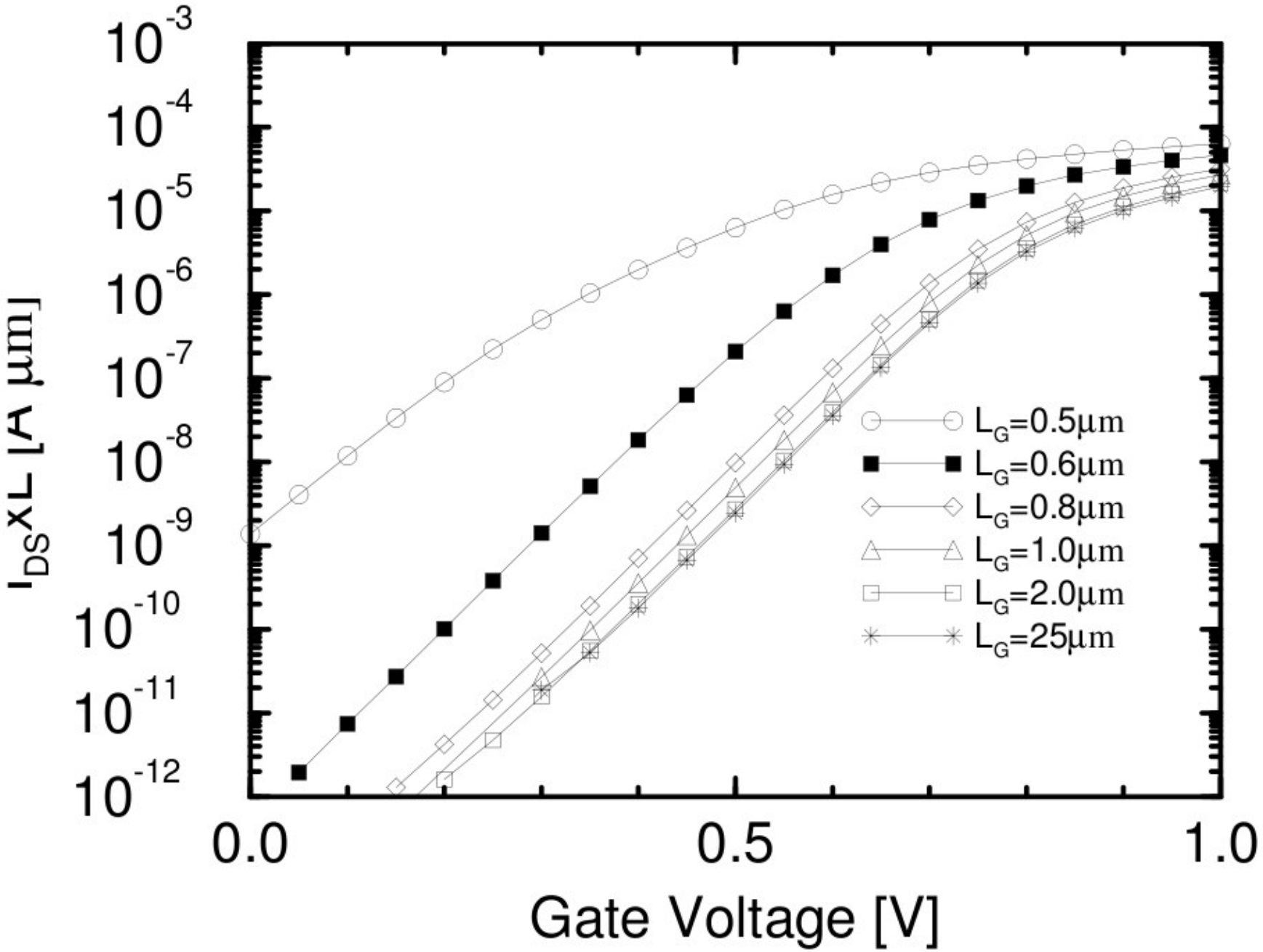
- This leads to the lowering of the barrier height for holes at the source edge near the bottom with shorter gate lengths

Drain-induced barrier lowering (DIBL)

• With shorter gate lengths, the barrier height for holes near the bottom is lowered by the influence of the drain electric field, and holes accumulated in the body region can more easily flow into the source



Drain-induced barrier lowering (DIBL)



Impact ionization

- Impact ionization is the process in a material by which one energetic charge carrier can lose energy by the creation of other charge carriers

- In semiconductors, an electron (or hole) with enough kinetic energy can knock a bound electron out of its bound state (in the valence band) and promote it to a state in the conduction band, creating an electron-hole pair

- If this occurs in a region of high electrical field then it can result in avalanche breakdown. This process is exploited in avalanche diodes, by which a small optical signal is amplified before entering an external electronic circuit. In an avalanche photodiode the original charge carrier is created by the absorption of a photon.

Impact ionization