# Comparator Design in Sensors for Environmental Monitoring

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**Abstract.** This paper presents circuit design considerations of comparator in analog-to-digital converters (ADC) applied for a portable, low-cost and high performance nano-sensor chip which can be applied to detect the airborne magnetite pollution nano particulate matter (PM) for environmental monitoring. High-resolution ADC plays a vital important role in high performance nano-sensor, while high-resolution comparator is a key component in ADC. In this work, some important design issues related to comparators in analog-to-digital converters (ADCs) are discussed, simulation results show that the resolution of the comparator proposed can achieve 5 μV, and it is appropriate for high-resolution application.

## 1. Introduction

In the real world, all signals in the nature environment are essentially analog signal. Once, almost all of the signal processing was carried out in the analog domain, which lasted until very large scale integrated circuits have appeared, because noise suppression capacity of digital circuit is much better than that of the analog circuit, various signal processing functions can be performed with higher resolution, higher stability, and much lower price in the digital domain than analog domain.

In modern electronic system, including environmental monitoring, telecommunications, voice, video, computer and many other electronic systems, in order to make full use of these advantages of digital signal processing, analog signals are often converted into digital signals by analog to digital converters (Analog-to-digital, converter, ADC), which are essential components for analog and digital domains.

ADC is mainly divided into Over-sampling ADC and Nyquist-Rate ADC. The basic principle of Over-sampling ADC is over-sampling and noise shaping. Band quantization noise is eliminated by digital decimation filter, as a result, the quantization noise can be reduced dramatically. By altering the number of order sampling rate and transfer function, its precision can reach 30 bits or more [1], but analog components in Over-sampling ADC called modulators and digital components in Over-sampling ADC used to implement decimation and digital filtering lead to a lot of hardware consumption. Typical Nyquist ADC can be divided into many types according to their operating principles, for example, Flash, Pipelined, Sub-arrangement, successive approximation, etc. They are able to work at a fast rate with very large bandwidth. The standard CMOS process allows the ADC to achieve GHz levels of bandwidth. However, with the rapid development of digital signal process

technology, the requirement of the accuracy of an analog to digital data converter becomes more and more critical especially on environmental monitoring applications, the disadvantage of Nyquist ADC lies in the fact that their accuracy cannot be very high. This is due to the limited process matching of analog components. If no correction or trimming technology is applied, it is difficult for the Nyquist ADC to achieve an accuracy more than 12~14 bits. Another drawback of Nyquist ADC is its complex hardware structure. For example, flash ADC, mainly due to the large number of comparators, additional bit will lead to the hardware consumption increases exponentially. Although the use of interpolation structure can reduce the number of comparators, it is still very large. High performance Pipelined ADC exploits multi stages of operational amplifiers to realize high sampling rate and high resolution, it is not appropriate for the low power sensor design. SAR ADC, which makes a trade-off between speed and accuracy, can achieve an ideal power efficiency by its simple architecture.

**Table 1**. Comparison of ADC with different architectures.

| Type | Resolution | Speed | Power | Area |
|---|---|---|---|---|
| SAR | Medium to high | Medium | Ultra-low | Small |
| Flash | Low | Ultra-high | High | Big |
| Pipeline | Medium to high | High | High | Big |
| ΣΔ | Ultra-high | Ultra-low | medium | medium |

Table 1 concludes the performance of Nyquist-Rate ADC with different architectures. It is worth to mention that the ADC with the lowest FOM is SAR ADC [2]-[11]. Figure 1 shows a simplified representation of a SAR ADC, whose main components are a Sample/Hold stage, a SAR logic stage, a N-bit DAC, and a comparator. It converts an analog value into its digital counterpart via a binary search algorithm. Nowadays, SAR ADC has become a practical solution for high efficient ADC design. In the process of designing a SAR ADC, comparator is the main functional part in it, in this paper, one novel time-domain comparator is designed. The remainder of this paper is organized as follows. Section II concludes some important progress of comparator in recent years, and section III describes design considerations, circuit architecture and simulation results. The conclusions are finally drawn in section IV.

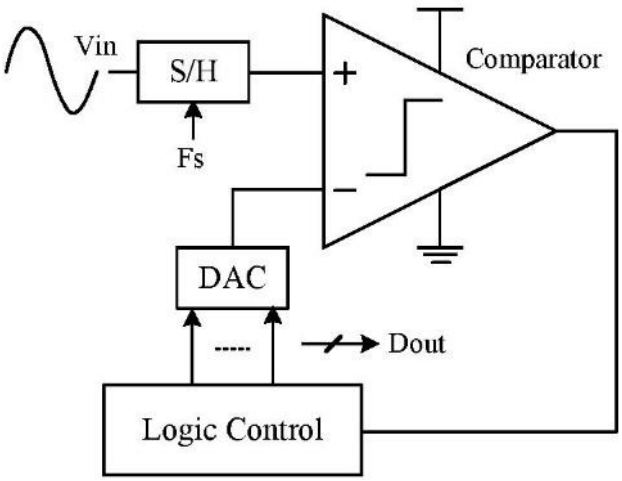


**Figure 1.** Typical architecture of SAR ADC.

## 2. Overview of Progress in Comparators in Analog-to-Digital Converters

Generally speaking, comparator can be classified into two classes: voltage comparator and current comparator; voltage comparator is more commonly used, basic function of voltage comparator is to

compare two voltage signals, output 1 or 0 according to the comparison result. For conventional voltage comparator, the most commonly used structures can be roughly divided into two types: the open-loop comparator and latch, as shown in figure 2. In figure 2(a), essentially, open-loop comparator is an operational amplifier which works in saturation region. Because the high gain of open-loop operational amplifier, the output reaches saturation even if there is only small difference exists between the two inputs, the advantage of open-loop comparator is high resolution, but limited by response time and power consumption; Latch in figure 2(b) does not consume static power and the speed of latch reaches GHz, but limited by the resolution and noise, the latch is usually cascaded by two or three pre-amplifiers to decrease the kickback noise influence of positive feedback latch, as shown in figure 3, but preamplifiers still consume non-ignorable power consumption.

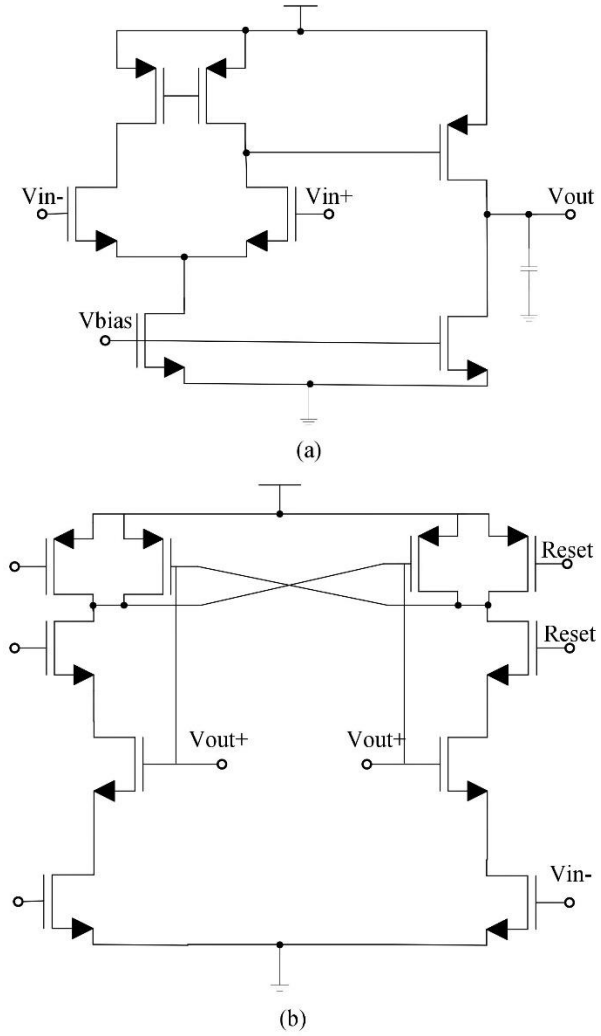


**Figure 2.** Typical voltage comparators: (a) open-loop comparator; (b) latch .

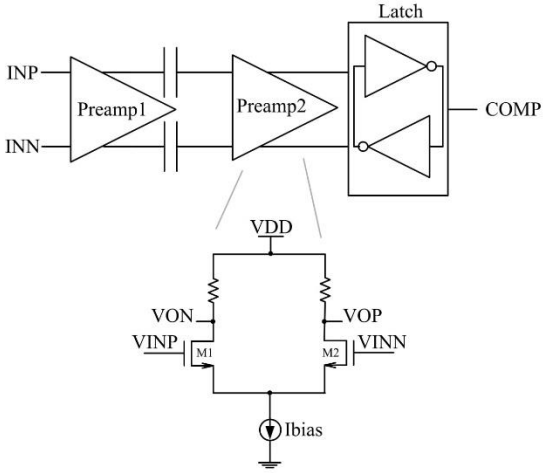


**Figure 3.** Two stages of preamplifiers with latch.

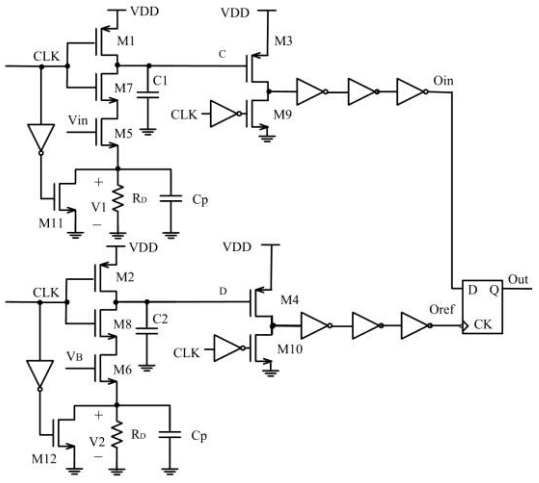


**Figure 4.** Time-domain comparator proposed in [12].

The time-domain comparator proposed in [12] obviates the need of preamplifier that dissipates static power, but it can only be applied to single-ended SAR ADC, because one of the inputs of the time-domain comparator in figure 4 is connected to a fixed voltage, VB, which must be large enough to provide the reference pulse, as a result, differential signal cannot be applied to VB. The operation of the time-domain comparator is as follows: when the signal CLK is low, transistors M1 and M2 charge the nominally equal capacitors C1 and C2 to VDD, when CLK rises, transistors M5 and M6 begin to

discharge capacitors C1 and C2, producing two pulses with different durations T1 and T2. The flip-flop reflects the pulse that ends first and provides the comparator output.

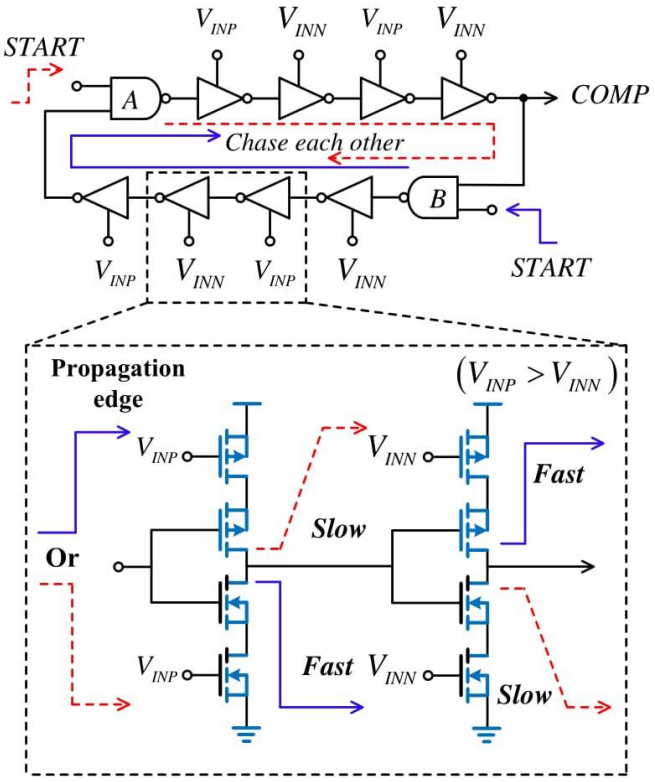


**Figure 5.** Structure of the Edge-Pursuit Comparator in [13].

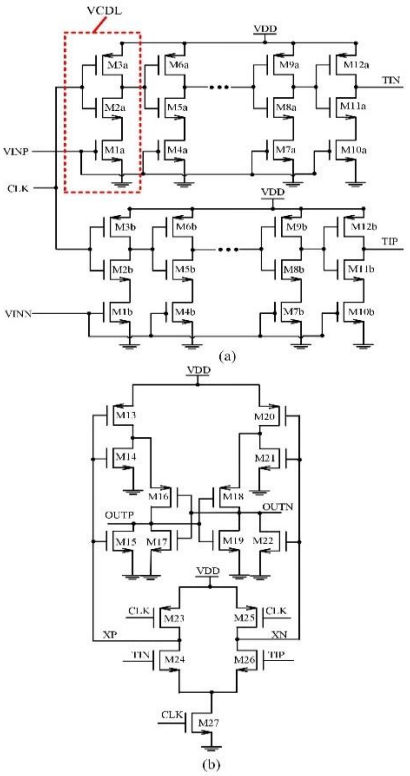


**Figure 6.** Time-domain comparator proposed.

Inverter based comparator was invented in [13] to further decrease power consumption. As shown in figure 5, it is composed of two NAND gates and inverter delay cells, automatically scales comparison energy according to its input voltage difference without external control, eliminating unnecessary energy. Initially, as the signal START is low, the comparator is in the reset state, the comparator begins to compare when the signal START goes high, which injects two propagating edges into the oscillator. The drawback of the comparator proposed in [13] lies in the fact that the propagation path of rising edge is different from that of falling edge, and positive terminal voltage $V_{INP}$ and negative terminal $V_{INN}$ appear alternately, leads to cross coupling of signals and layout between $V_{INP}$ and $V_{INN}$.

## 3. Design and Realization of Time-Domain Comparators in SAR ADC

Figure 6 shows the structure of the high-resolution time domain comparator proposed, which improves the conventional time domain comparator proposed in [12] and [14], and it can be applied to both single-ended SAR ADC and full differential SAR ADC. As shown in figure 6, it is composed of a voltage-time converter and a time-digital converter, and the voltage-time converter is composed of a series of inverters which are current limited [14]. In reset mode, CLK is high, the output voltage TIP and TIN of the voltage-time converter reset to low level. In comparison mode, CLK becomes high, then TIP and TIN transfer to high, too. The speed of TIP and TIN go from low to high is related to the magnitude of input voltage VINP and VINN. The greater the input voltage, the shorter the time for TIP and TIN transfer from low to high. The outputs (OUTP and OUTN) of time-digital converter [15] are determined by the time difference between TIP and TIN change from low to high. If VINP is greater than VINN, OUTP is high and OUTN is low. On the contrary, if VINP is lower than VINN, OUTN goes high and OUTP goes low.

Time-domain Comparator proposed in this work is simulated in 0.18$\mu m$ technology, simulation results show that the resolution is 5$\mu V$, the highest speed of comparator reaches 200 MHz, while the time-

domain proposed in [14] is simulated with the same technology and same simulation conditions. As shown in table 2, simulation results show that the comparator proposed achieves higher speed, higher resolution and wider input range, and the time-domain comparator proposed can be applied to both single-ended and differential SAR ADC while the comparator proposed in [14] can only be applied in single-ended SAR ADC.

**Table 2.** Simulation summary of comparator.

| | [14] | Proposed |
|---|---|---|
| Technology($\mu m$) | 0.18 | 0.18 |
| Single-ended/Differential | Single-ended | Both Single-ended and Differential |
| Highest Speed(MHz) | 166 | 200 |
| Resolution($\mu V$) | 122 | 5 |
| Input voltage Range | 0~ 1 | -1~ 1 |
| Simulation/Measure | Simulation | Simulation |

## 4. Conclusion

This paper presents circuit design considerations of time-domain comparators in data converters applied for SAR ADC, some important progress related to comparators in analog-to-digital converters (ADCs) are introduced. One practical design of high resolution time-domain comparator design is given in this work and the design considerations mentioned in this paper are useful for the practice and high resolution data converters applications in environmental monitoring fields.

## 5. References

[1] ADI, "32-bit, 10 ksps, sigma-delta adc with 100 μs settling and true rail-to-rail buffers," *ANALOG DEVICES DATASHEET*

[2] Tai H-Y, Hu Y-S, Chen H-W and Chen H-S 2014 A 0.85 fj/conversion-step 10b 200ks/s subranging sar adc in 40nm cmos *Digest of Technical Papers of IEEE International Solid-State Circuits Conference(ISSCC)* pp 196–7

[3] Liu M, van Roermund A and Harpe P 2016 A 7.1 fj/conv.-step 88db sfdr 12b sar adc with energy-efficient swap-to-reset *European Solid-State Circuits Conference 42nd* pp 409–12

[4] Kim M, Ha U, Lee Y, Lee K and Yoo H-J 2016 A 82nw chaotic-map true random number generator based on sub-ranging sar adc *European Solid-State Circuits Conference* 42nd pp 157–60.

[5] Lin J-Y and Hsieh C-C 2015 A 0.3 v 10-bit 1.17 f sar adc with merge and split switching in 90 nm cmos *IEEE Transactions on Circuits and Systems I: Regular Papers* vol 62 no 1 pp 70–9

[6] Chung Y-H, Wu M-H and Li H-S 2015 A 12-bit 8.47-fj/conversion-step capacitor-swapping sar adc in 110-nm cmos *IEEE Transactions on Circuits and Systems I: Regular Papers* vol 62 no 1 pp 10–8

[7] Sanyal A and Sun N 2014 An energy-efficient low frequency-dependence switching technique for sar adcs *IEEE Transactions on Circuits and Systems II: Express Briefs* vol 61 no 5 pp 294–8

[8] Harpe P, Dolmans G, Philips K and de Groot H 2012 A 0.7v 7-to-10bit 0-to-2ms/s flexible sar adc for ultra low-power wireless sensor nodes *European Solid-State Circuits Conference(ESSCIRC)* pp 373–6

[9] H. Fan, H. Hadi, F. Maloberti, D. Li, D. Hu, and Y. Cen, "High Resolution and Linearity Enhanced SAR ADC for Wearable Sensing Systems," in *IEEE International Symposium on Circuits and Systems(ISCAS)*, 2017, pp. 180–3.

[10] van Elzakker M, van Tuijl E, Geraedts P, Schinkel D, Klumperink E and Nauta B 2010 A 10-bit charge-redistribution adc consuming 1.9μw at 1ms/s *IEEE Journal of Solid-State Circuits* vol 45 no 5 pp 1007–15

[11] H. Fan and F. Maloberti, "High-Resolution SAR ADC with Enhanced Linearity," IEEE Transactions on Circuits and Systems II: Express Briefs, vol 64, no 10 pp 1142–6, 2017.
[12] Agnes A, Bonizzoni E, Malcovati P and Maloberti F 2008 A 9.4-enob 1v 3.8μw 100ks/s sar adc with time-domain comparator *Digest of Technical Papers of IEEE International Solid-State Circuits Conference(ISSCC)* pp 246–610
[13] Shim M, Jeong S, Myers P D, Bang S, Shen J, Kim C, Sylvester D, Blaauw D and Jung W 2017 Edge-pursuit comparator: an energy-scalable oscillator collapse-based comparator with application in a 74.1 db sndr and 20 ks/s 15 b sar adc *IEEE Journal of Solid-State Circuits*
[14] Kobenge S B and Yang H 2008 Ultra-low-power high-speed vcdl based time domain comparator *Chinese Patent* ZL200810114514.4 pp 1–10
[15] Schinkel D, Mensink E, Kiumperink E, Van Tuijl E and Nauta B 2007 A double-tail latch-type voltage sense amplifier with 18ps setup+ hold time *Digest of Technical Papers of IEEE International Solid-State Circuits Conference(ISSCC)* pp 314–605

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