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Circuit elements for quantum phase-slip devices

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Abstract

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Circuit elements for quantum phase-slip devices

by Christopher Robert Nash

If proved to exist, the phenomenon of quantum phase slips (QPS) allows us to provide a new standard for current. In order to investigate this effect a QPS circuit needs to be constructed with a superconducting nanowire connected in series with an inductor and two thin film resistors.

It was found that it was possible to control the low temperature resistance of chromium oxide films by increasing the oxygen pressure at the time of deposition, meaning chromium oxide films could be fabricated for a large resistance range of thin film resistors, from values in the hundreds of ohms to megaohms. These films were found to be amorphous when measured with XRD and displayed extremely low magnetoresistance (with a peak magnetic moment of $5{\times}10^{-3}$ μ_B per atom, compared to 2 μ_B per atom in bulk ferromagnetic Cr_2O_3). The contact resistance of joining these chromium oxide resistors to gold or niobium-silicon was measured using a transmission-line model and this revealed that a gold interlayer provided a much lower contact resistance than direct contact of the circuit components (a contact resistivity of $0.15\,\mathrm{m\Omega cm^2}$ for chromium oxide to gold compared to $65\,\mathrm{m\Omega cm^2}$ for chromium oxide to niobium silicon).

Several methods were used to restrict nanowire dimensions. It was found that combining a HSQ fabrication method with a neon mill resulted in the creation of wires below the coherence length of niobium nitride (30 nm), which made these wires suitable for QPS measurements.

For my beautiful wife Steph.

Thank you for all of your love and support, without which this would not exist.

To my wonderful daughter Elizabeth.

Thank you for all the smiles.

Declaration

I, Christopher Robert Nash confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

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Chapter 1

Theoretical Background

The following section provides a brief introduction to the current understanding of low temperature conduction of electrons in thin films and nanowires. Firstly the conduction properties of thin metal films are discussed, followed by a discussion of superconductivity. A description of the Josephson junction is provided, as it is the analogous relationship between Josephson junctions and quantum phase-slips in nanowires that motivates the current experiment. Finally a description of superconductivity in one dimension is provided, including the prediction of quantum phase-slips, and how this could lead to a new standard for current. This would offer an improved accuracy over the existing standard which exploits Coulomb blockade effects in a single electron pump[1].

1.1 Properties of thin metal films and nanostructures

1.1.1 Conduction in limited dimensions

Bulk conductors show characteristics that are largely predictable by application of the free and nearly free electron models. However when dimensions are restricted to a 2-D thin film or 1-D nanowire, new models are needed to predict the impact these dimension restrictions might have. For example, imagine a metal with impurity sites in the lattice. In a bulk conductor the current channels can find a path around these impurities. However, in a nanowire, any impurities will have a dominant effect on the conductance as there are very few current paths available [2]. Other effects, such as quantised conductance, can also become apparent. A description of the effects of restricted dimensions on a 1-D superconducting wire will be presented in section 1.4.

1.1.2 Matheissen Rule

The electron scattering of a film can be expressed as a sum of three parts as given by the Matheissen rule [3].

$$R_f = R_b(T) + R_{df}(n_d) + R_s(h) \tag{1.1}$$

The first term is the contribution based on collisions of electrons with phonons. This is dependent on temperature (T) as phonons are a representation for vibrations in the crystal lattice, which are greater at higher temperature. The second term is the contribution due to collision of electrons with defects in the lattice. This is dependent on the number of impurities in the crystal lattice (n_d). The third term is due to collisions with the surface of the film and is dependent on the thickness of the film.

As the thickness of a film is decreased it becomes more resistive. This is due to the fact that the total resistance is no longer that of the bulk material, but a combination of the bulk resistance and the resistance due to surface effects. Resistance will be higher at the surface as the lattice is deformed from the bulk, impeding the path of electrons through the material. As the film decreases in thickness this contribution becomes more important and so the resistance will increase. If the thickness is on the order of the mean free path of electrons in the film then collisions with the surface will be as frequent as collisions with the rest of the material. This term can become dominant in a 2-D film.

1.1.3 Sheet Resistance

When describing a thin film it is usual to express its conduction properties using the sheet resistance, this is derived as follows

$$R_s = R\frac{L}{b} \tag{1.2}$$

where b is the width of the film, L is the length of the film and R is the bulk resistance due to scattering in the film. This is an expression for the resistance of the film without having to know the film thickness. This is useful for making thin film resistors on integrated devices as if we know the resistance per square, then we can increase resistor value by simply stacking squares of the resistor material next to each other.

1.1.4 Temperature Co-efficient of Resistivity

The temperature coefficient of resistivity (TCR) gives information on how the resistivity will change with temperature. It is expressed as

$$\alpha = (\frac{1}{\rho_0})(\frac{d\rho}{dT}) \tag{1.3}$$

where ρ_0 is the initial resistivity and ρ is the resistivity at temperature T. It has units of K^{-1} and if it is positive then resistivity increases with temperature, if negative then resistivity decreases with increasing temperature. For pure bulk metals α is always positive, however for some metals such as chromium, the inclusion of defects such as oxygen can send α negative. This is due to the formation of thin dielectric (insulating) layers at grain boundaries, which will become electrically isolated from each other. In the case of all metals, when the resistivity is almost entirely due to phonon scattering the temperature coefficient will be positive, as resistivity contributions due to defects and surface effects are introduced the temperature coefficient is reduced or becomes negative.

1.1.5 Variable Range Hopping

A film fabricated by sputter deposition will always have an element of granularity. If the film is mostly metallic then the grains will be in contact with each other and conduction will be metallic. However, if elements such as oxygen are introduced then metallic grains can become isolated from each other and electrons will have to tunnel through an energy barrier to conduct through the film. When the film is at high temperature the phonon energy will be sufficient to allow electrons to tunnel through the barriers. When the temperature is lowered phonon energy will decrease and the conduction will transition from metallic to insulating. This behaviour can be predicted by the variable range hopping (VRH) model, first described by Mott [4], and takes the form

$$R = R_0 \exp(T_0/T)^n \tag{1.4}$$

where T is the film temperature and T_0 is the localisation temperature. For Mott (VRH) $n = (d+1)$ in d dimensions; for Efros–Shklovskii VRH, appropriate for stronger electron-electron interactions, $n = 1/2$ [5]. From T_0 the localisation length ξ can be calculated using the equation

$$T_0 = e^2\beta/k_B k\xi \tag{1.5}$$

where β is a numerical constant, k_B is the Boltzman constant and k is the electrical permittivity of the material. This characterises the distance an electron can tunnel from the grain boundary it is isolated in.

1.1.6 Contact Resistance

When two interfaces meet, there will inevitably be imperfect contact between them. Unevenness in each surface and the mismatch of lattice structures will cause gaps and defects at the surface of the two materials. This will be a component of any resistance measurement we make. Minimising this contact resistance is one of the main challenges in fabricating multi-layered on-chip circuits.

One way to calculate contact resistance is to use the transmission line model (TLM) [6]. Originally designed to give the contact resistance between a component and an underlying semiconductor, the transmission line model is based on a circuit test pattern consisting of identical contacts separated by a range of distances. Overlaying the contacts with a strip of the second material and plotting a graph of measured resistance against distance between contacts will give the contact resistance at the intercept of the graph.

This is because as the distance between the pads decreases, there are less squares of the strip material. At the intercept the number of squares is zero. This means the intercept resistance is a combination of the pad material resistance and the contact resistance of the two pads. By subtracting the pad resistance and dividing the result by two, we can obtain the contact resistance of the two materials. Once this is known steps can be taken to reduce it.

Many such steps can be taken. The choice of materials can be crucial; a gold interlayer can significantly improve contact resistance but will introduce more steps into the fabrication process. Plasma ashing between stages can remove unwanted organics or resist residue, baking can remove residual water vapour from the surface. The crucial consideration is whether the extra time involved implementing each of these steps contributes to a significantly better contact resistance on the end device.

1.2 Superconductivity

1.2.1 History of Superconductivity

Superconductivity is the sudden drop in resistivity to zero when a sample is cooled to a sufficiently low temperature, the critical temperature Tc. Originally discovered by Onnes

in 1911, soon after successfully producing liquid helium, research in the field quickly expanded. In 1935 the London brothers described the interaction of superconducting current with electric and magnetic fields through a series of equations.

$$\Lambda(\Delta \times J_s) + B = 0 \tag{1.6}$$

$$\Lambda \frac{\partial J_s}{\partial t} = E \tag{1.7}$$

where J is the current density and

$$\Lambda = m^*/n^* e^{*2} \tag{1.8}$$

where e is the charge of an electron, m^* is the mass of a pair of electrons and n^* is the density of paired electrons in the superconductor. These equations describe the relation in the presence of a magnetic field between effective mass of a pair of bound electrons (known as a Cooper pair) and the density of Cooper pairs times the pair charge. These equations describe how the magnetic field (B) controls current flow for Cooper pairs, not electric field (E). It also shows that there is no electric field for stationary currents. These equations lead to the description of the Meissner effect; when the temperature drops below Tc where magnetic flux is almost completely excluded from the superconductor, and only resides in a thin layer on the surface known as the penetration depth. This is caused by screening currents flowing across the surface in a way that cancels out the applied magnetic field.

The most widely accepted theory for low temperature superconductors to date is that proposed by Bardeen, Cooper and Schrieffer in 1957 [7], this is known as BCS theory. The basis of the theory is that there is an attractive interaction between electrons when the difference in energy between the electron states is less than the phonon energy. This will be described in more detail below.

1.2.2 Cooper Pairs

When a superconductor is cooled to sufficiently low temperatures, electrons will occupy states in pairs. If one electron has to occupy a different state, say due to a scattering event, then the second electron must also occupy the same state with opposite spin. If an electron in state k_1 moves into state k_2, then its pair must move from state ψ_1 to state ψ_2. This is caused by an attractive interaction between pairs of electrons; if an electron movement distorts the surrounding lattice this will create a slightly more positive region that remains after the electron has moved by. As ions move more slowly

than electrons this will draw the second electron towards the newly created positive region. In the superconducting ground state all of the electrons are paired and there is a certain amount of energy required to break the pairing, known as the energy gap.

The reason for this pairing was shown by Cooper. He found that the system has its lowest energy if the paired electrons have opposite spins. We consider two electrons occupying a pair of plane wave states; ψ_1 and ψ_2. The electron occupying state k_1 vibrates the lattice, which is represented as the electron emitting a phonon, this is then absorbed by the electron in state k_2. The phonon exchange takes place in a short time Δt, this means that by the Heisenberg uncertainty principle

$$\Delta t \Delta \varepsilon \geq \hbar \tag{1.9}$$

the uncertainty in the energy is very high. This means that energy does not necessarily have to be conserved and the phonon is known as a virtual phonon. It is assumed however that the total momentum K is conserved during the interaction.

The Cooper model consists of a system in which all states are occupied up to the Fermi energy, $k \leq k_F$. If another two electrons are added then they must occupy states with energy greater than the Fermi energy, $k > k_F$. It is assumed that there is an interaction between the electrons that can be expressed as an interaction potential energy $V_{r_1 - r_2}$. If this interaction potential is negative then this is taken as a bound state representing a bound pair of electrons, a Cooper pair. As system energy is lowered by pairing we find that a system that consists of single electrons is unstable, as any perturbation that moves electrons above the Fermi energy will result in electron pairs and so provide a lower energy state for the system to be in.

1.2.3 Pair Phase Coherence

The fundamental reason for superconductivity at low temperatures is the long-range coherence of Cooper pairs. It is energetically favourable for overlapping Cooper pairs to lock phases. This will occur over the whole length of the material. The whole superconducting fluid can be thought of as overlapping spheres of phase locked Cooper pairs. The phases of all the pairs are locked together in the absence of any net pair momentum and so they all oscillate together. As all of these electrons are oscillating together, to break the phase of one means breaking the phase of all other electrons in the system.

This means that the pair current can only be altered by something that alters all pairs simultaneously, such as a magnetic field. In this case the magnetic field the pairs generate

in the interior of the sample is equal and opposite to the applied magnetic field. At low temperatures the lattice vibrations do not have enough energy to break the phase of all of the pairs and so the system experiences zero resistance.

1.3 Josephson Junctions

1.3.1 The Josephson Effect

Discovered by B. Josephson in 1962 [8], the Josephson junction consists of two superconductors separated by a thin insulating film. Under suitable conditions superconducting electron pairs can tunnel from a superconductor, through a layer of insulator, into another superconductor.

Let Ψ_1 be the probability amplitude of electrons on one side of the junction, region 1, and Ψ_2 be the amplitude on the other side of the junction, region 2. It is assumed that the superconductors are identical and they are both at zero potential. The time-dependent Schrödinger equation

$$i\hbar\frac{\partial\Psi}{\partial t} = H\Psi \tag{1.10}$$

applied to the two amplitudes gives

$$i\hbar\frac{\partial\Psi_1}{\partial t} = \hbar T\Psi_2 \tag{1.11}$$

$$i\hbar\frac{\partial\Psi_2}{\partial t} = \hbar T\Psi_1 \tag{1.12}$$

where $\hbar T$ represents the effect of the electron pair coupling or transfer operation across the insulator. T has the form of a rate or frequency; it is a measure of leakage of Ψ_1 into region 2, and Ψ_2 into region 1. If the insulator is very thick then T is zero and there is no pair tunnelling. As the thickness is lessened the wavefunctions can penetrate the barrier and couple, locking their phases together, at which point Cooper pairs can pass through the barrier without energy losses.

The two wave functions are defined in the following way

$$\Psi_1 = n_1^{1/2}\exp^{i\theta_1} \tag{1.13}$$

$$\Psi_2 = n_2^{1/2}\exp^{i\theta_2} \tag{1.14}$$

$$\phi = \theta_2 - \theta_1 \tag{1.15}$$

where θ is the phase of the electron and ϕ is the phase difference. If equations (1.13) and (1.14) are expanded out, assuming the superconductors are identical, $n_1 = n_2$, then

$$\frac{\partial n_2}{\partial t} = -\frac{\partial n_1}{\partial t} \tag{1.16}$$

The current flow from regions 1 to 2 is given by either side of this equation. The current density J flowing across the junction is then dependent on the phase difference

$$J = J_0 \sin\phi = J_0 \sin(\theta_2 - \theta_1) \tag{1.17}$$

where J_0 is proportional to the transfer interaction T. The current density J_0 is the maximum zero voltage current density that can pass through the junction and is known as the critical current density. With no applied voltage a dc current will flow through the junction with a value between J_0 and $-J_0$ depending on the value of the phase difference. This is the dc Josephson effect.

If a voltage is applied across the junction then the phases of the electron pairs can slip relative to each other in a way that is proportional to the voltage. This is expressed by the relation

$$\frac{\partial \phi}{\partial t} = \frac{2e}{\hbar} V \tag{1.18}$$

This is known as the ac Josephson effect. It states that under constant voltage the phase will alternate with a frequency of $2e/\hbar$. This will lead to current oscillations at that frequency due to Eq. 1.17.

1.3.2 Josephson Washboard Potential

The Josephson effect can be described by a second order non-linear differential equation

$$\frac{\hbar C}{2e} \cdot \frac{d^2\phi}{dt^2} + \frac{\hbar}{2eR} \cdot \frac{d\psi}{dt} + i_1 \sin(\phi) = i \tag{1.19}$$

for a critical current i, resistance R and capacitance C. This is directly analogous to a mechanical system of a ball bearing rolling down a washboard shaped slope.

Imagine a ball bearing sitting in a groove on a washboard. If the washboard is slightly tilted the ball bearing will remain in the groove but will settle on a rest position slightly off the centre of the grove, adjusting the position to a new minimum.

Once a critical slope is reached the bearing will move to the next depression and continue to move down the slope at an accelerating rate, escaping each local minima once the tilt

has reached the local critical point. The distance the ball has moved is analogous to the phase difference ϕ across the junction, with the minima (groves) spaced by 2π.

The critical slope corresponds to the critical current across the junction. The angle of inclination corresponds to the current being driven by an external source across the junction.

For small currents the phase is independent of the time (small oscillations in the grove). Once the critical current is reached the phase difference starts to increase with time, rapidly reaching a constant rate of increase (ball rolling and then reaching terminal velocity due to friction with the washboard). Reducing the current may not stop the phase difference increasing with time due to the capacitance of the junction (inertia of the ball).

The change in phase will lead to a voltage across the junction given by the relation

$$V = \frac{\hbar}{2e} \cdot \frac{d\phi}{dt}. \tag{1.20}$$

The voltage is analogous to the velocity of the ball travelling down the slope.

The friction on the ball is a work done against the gravitational force of the ball moving down the slope, given by

$$F\frac{d\phi}{dt} = kv^2 \tag{1.21}$$

where k is the dissipation constant. The voltage is analogous to phase velocity $d\phi/dt$, so power dissipated is given by V^2/R, where R is the resistance of the junction when biased in the finite voltage state.

The kinetic energy of the junction $CV^2/2$, where C is the junction capacitance, is analogous to supplying the ball with kinetic energy to overcome the potential energy of the local minima, tilting the washboard then reducing the slope to less than the critical value to allow the ball to continue rolling.

1.3.3 Josephson Junction Voltage Standard

One of the uses of Josephson junctions is to provide a standard for voltage. These have been the principle devices for defining the Volt since 1985 [9]. A Volt is defined in SI units as the electromotive force between two points on a wire that allows a one ampere current to dissipate one watt between the two points. When a microwave signal is coupled to a current-biased Josephson junction with dc voltage, the total potential difference is found to be a combination of the dc voltage and a voltage related to the

frequency (f) of the microwaves. This results in quantised steps in voltage, observed by Shapiro in 1963 [10], given by the relation

$$V_n = n\frac{\hbar}{2e}f \tag{1.22}$$

where (n = 0, 1, 2).

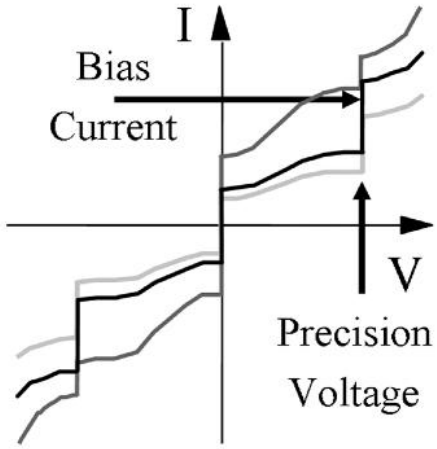

FIGURE 1.1: Current-Voltage diagram by Benz et al [11] showing identical steps in $n = 1$ voltage for three different junctions with the same microwave frequency used for each.

This means the ability to measure the volt is now largely determined by the knowledge of the value of a couple of fundamental constants and the ability to accurately measure the frequency of the microwaves being used.

1.4 Superconductivity in reduced dimensions

The following section describes the current state of the field of superconductivity in restricted dimensions, with a particular focus on materials and devices that can exploit the affect of quantum phase slips. Finally the quantum current standard circuit proposed by Mooij et. al. [12] is described.

1.4.1 Superconductivity in thin films

When the dimensions of a superconductor are restricted, the material can display a dramatic change of properties from those of the bulk. A thin superconducting film has a thickness small enough to enter this new regime. Films of this type can display a

prominent insulating phase at temperatures just above the transition, or even have the transition entirely suppressed.

Recently Ivry et. al. [57] reviewed the state of the field of thin superconducting films. They took data from forty six papers in a wide variety of materials to compare how superconductivity is affected by the thickness of the material. The motivation behind this work was the fact that above T_c the relationship between film thickness d and sheet resistance R_s can be described by the Matheissen rule. However, as these films approach T_c this rule breaks down.

By comparing the transition of different materials at various thicknesses they found that there is a scaleable relationship between d, R_s and T_c that is common across all of the materials assessed. This relationship is described by the power law

$$dT_c = AR_s^{-B} \tag{1.23}$$

where A and B are fitting parameters.

1.4.2 Destruction of Superconductivity in 1-D

In 2008 Arutyunov et. al. [58] presented a comprehensive review of the superconducting state in one dimension. Although the field has moved on since then the descriptions provided are useful to understanding the nature of phase slips. A superconducting transition is not necessarily a spontaneous drop at Tc, but can be broadened by inhomogeneity in the sample causing different parts of the sample to go superconducting at different temperatures. However, even if all inhomogeneity is removed, some samples can still have a broad transition.

This is due to phase slips in the material of which it is proposed there are two varieties. Thermally activated phase-slips (TAPS) and quantum phase-slips (QPS) become prominent when the diameter of the wire is reduced to the nanometer scale. However; when the sample is cooled to very low temperatures it is possible for quantum phase-slips (QPS) to become dominant and destroy superconductivity altogether.

According to Ginzburg-Landau theory, a superconducting nanowire can be described by a complex order parameter

$$\Psi(x) = |\Psi(x)| \exp i\theta x \tag{1.24}$$

where θ is the phase and $|\Psi(x)|$ is the amplitude. Thermal fluctuations in the nanowire can cause disruption of the phase and modulus of the order parameter; if the modulus of

the order parameter drops to zero then the phase can jump to any value of $2\pi n$, where n is any integer. This is a thermally activated phase slip. After the phase slip the modulus is restored and the system returns to its initial state with a new phase of $2\pi n$. These events are rare so the model can be restricted to fluctuations of $n = \pm 1$.

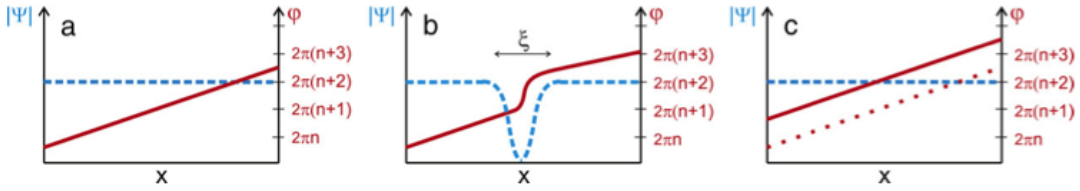

FIGURE 1.2: Diagram by Arutyunov et al [58] showing the relationship between the modulus of the order parameter and the phase of a nanowire a) before, b) during and c) after the phase slip.

A thermally activated phase slip can cause a non-zero drop in voltage across a superconducting wire, described by the ac Josephson effect (1.18), this can be rewritten as

$$V = \frac{\hbar \dot{\phi}}{2e} \tag{1.25}$$

If there is no bias current across the wire then the average number of positive and negative phase slips will be equal and so there will be no net voltage drop. However; if there is a bias current applied then it is more likely to find positive phase slips and so a voltage drop. This means that TAPS can cause a sudden jump in resistance in the superconducting state, i.e. below Tc. The likelihood of TAPS decreases with decreasing temperature as the system has less energy to overcome the potential barrier to an adjacent energy minimum.

As the temperature decreases further below T_c, thermally activated phase slips become less likely and so quantum phase slips dominate. This means that even close to $T = 0K$ resistance in nanowires can still be seen due to quantum phase slips and in some cases blocking all conduction turning the material into an insulator. The QPS effect should be more pronounced in long wires than short wires [59] , but it will play a significant role in any length of nanowire with a width of 10 nm or less.

1.4.3 Coherent quantum phase-slips

Since quantum phase-slips were first postulated numerous groups have attempted to prove their existence. Evidence for incoherent quantum phase-slips has been reported [30, 60, 61], however for a working QPS device coherent quantum phase-slips are desirable.

The first successful report of coherent quantum phase-slips was made by Astafiev in 2012 [62]. This effect was observed first in a superconducting loop of disordered indium oxide, and later repeated in niobium nitride [63]. This was achieved through the fabrication of a resonator with a 40 nm wide constriction in a superconducting loop.

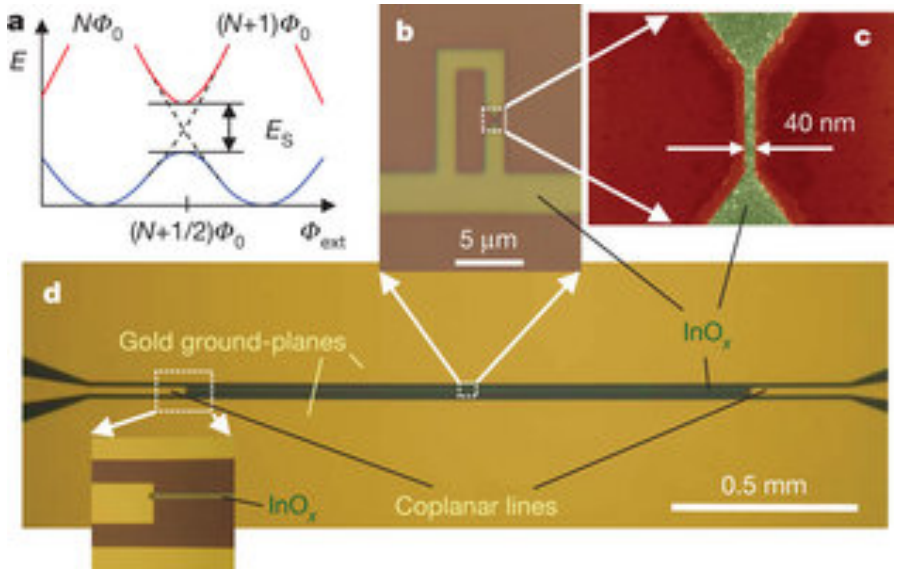

FIGURE 1.3: Device fabricated by Astafiev et. al [62] featuring a resonating superconducting loop with a 40 nm constriction.

The use of a superconducting loop is to reduce the dissipative effects of attempting to observe CQPS by other means, such as a chain of Josephson junctions. By creating a superconducting loop with a constriction, phase slips in this constriction will cause a change in the number of quantized fluxes. This change was successfully measured by Astafiev et. al to provide the first direct observation of these coherent phase-slips.

1.4.4 Phase-slip Centres

It is possible to find non-perfect conductance in wires of higher dimensions. One effect that superconducting wires can exhibit when near the critical current is that of phase-slip centres. First described by Skocpol, Beasley and Tinkham [64] the theory states that there will be a section of the nanowire where the critical current will be less than the sections on either side, a weak spot.

This means that as the current increases there will be parts of the wire that will transition from superconducting to normal resistance. As the current is increased more areas of the nanowire will return to normal resistance until there are no remaining areas of the wire which are superconducting. If an I-V is plotted for a wire exhibiting phase-slip

centres then a series of lines of increasing resistance will be seen, each of these lines can be extrapolated through the origin.

1.4.5 QPS and Josephson Junction Duality

Recently A. J. Kerman [65] has published a theory attempting to show that the flux-charge duality holds at the microscopic level. This illustrated in a conceptual way how Josephson junctions and QPS circuits can be shown to be linked.

According to London's first equation (Eq. 1.8), free charge will move ballistically in a superconductor. Similarly Maxwell's equations (Eq. 1.25) show that a free fluxoid moves ballistically through an insulator.

$$Superconductor : \mathbf{\Lambda}\frac{d\mathbf{J}_Q^f}{dt} = \mathbf{J}_\Phi^b \tag{1.26}$$

$$Insulator : \epsilon\frac{d\mathbf{J}_\Phi^f}{dt} = \mathbf{J}_Q^b \tag{1.27}$$

If we think of a Josephson junction as an insulating barrier separating two superconductors, and a QPS producing nanowire as two insulating regions of flux quanta separated by a superconducting barrier, we can see how the duality between the two can arise.

1.4.6 QPS Current Standard

It has been shown by Mooij et. al. [12] that the quantum phase slip in a superconducting nanowire can be the dual of Cooper pair tunnelling in the Josephson junction, as long as the successive quantum phase slips are coherent. This duality can be shown in two circuit set ups, shown in Fig. 1.4.

One application of this duality is the possibility of finding a new standard for measurement of current. The standard for current, measured by Coulomb blockade effects in a single electron pump only has an accuracy of $9{:}10^7$ [13]. By using the dual circuit of a Josephson junction for QPS effects we can use the method of the voltage standard to find the current standard. This could be achieved by coupling microwaves with a superconducting nanowire circuit, causing steps to appear in the current proportional to the frequency of the microwave. This is given by Eq. 1.28.

$$I = n2ev \tag{1.28}$$

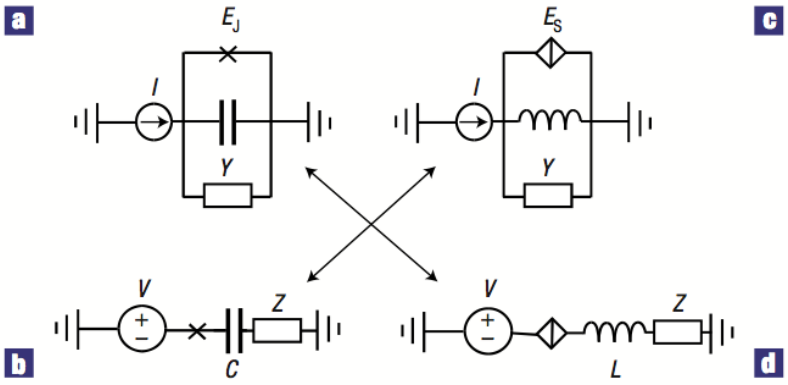

FIGURE 1.4: Diagram by Mooij et al [12] showing the duality of Josephson junction and QPS circuits, a) is a current biased Josephson junction, b) is a voltage biased Josephson junction, c) is a current biased QPS junction and d) is a voltage biased QPS junction. Circuit a) is the dual of d), and b) is the dual of c).

This shows that the accuracy in measuring the current is largely dependent on our accuracy in measuring the frequency of the microwaves used, which will be the same as for the Josephson junction, 1:10^{16}. In order to replicate the Josephson circuit the nanowire should be coupled to an inductor and a high value resistor. The inductor can be made of a wider region of Nb-Si connected to the nanowire. The resistor will then be connected to this setup, as shown in Fig. 1.5.

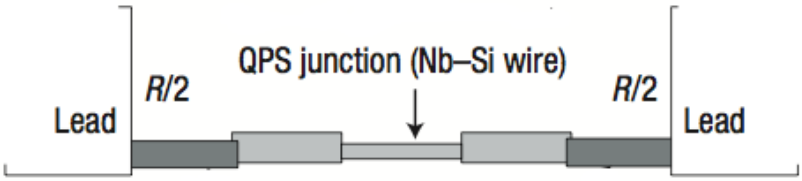

FIGURE 1.5: Diagram by Mooij et. al [12] showing the experimental set up of circuit d from Fig. 1.4.

Mooij et. al. postulate that these resistors should have a resistance of a least 60 kΩ to guarantee that charge is well defined. This is because high value series resistors will reduce hysteretic current-voltage relationships. It is the attempt to grow thin film resistors, of sufficiently high resistance for use in this circuit, that is one of the focuses of this project.

1.4.7 Thin Film resistors for use in a QPS Circuit

Since the 1960s, on-chip thin-film resistors have found applications in integrated circuits [14, 15]. Materials such as NiCr [16, 17], SiCr [18, 19], TaN [20, 21], and TiO [22] have all been used, fabricated by evaporation or sputter deposition. They provide room-temperature sheet resistances ranging from $10\,\Omega/\square$ to $2000\,\Omega/\square$, but materials to provide higher sheet resistances are less commonly used, with W and Bi [61] being reported for this use. In nanoscale electronic circuits, there is frequently a need for resistive elements which are smaller than the wavelength associated with the frequency of interest. In particular, in coherent quantum circuits there is a need for compact resistors to isolate devices from the environment at frequencies in the GHz range [23]. Such resistors have found applications in the fields of Josephson junctions and nanoscale circuits [24–26, 28, 29]. In order to provide a high-value resistor using standard materials, it is necessary to pattern long (often meandering) paths, thereby leading to an undesirably high shunt capacitance.

On-chip resistors play an important role in the current-standard QPS circuit, providing a shunt resistance to ensure the overdamped behaviour in which microwave-induced step features are best observed. Work on investigating quantum phase-slips in superconducting nanowires has ensued, including recent microwave spectroscopy measurements, which showed features of coherent QPS origin [62]. The QPS current-standard circuit described by Mooij and Nazarov comprises two resistors on either side of a niobium-silicon nanowire, with a combined series resistance which should exceed a certain value in order to minimise hysteresis in the current-voltage characteristics of this particular circuit. For typical parameters, the series resistance should exceed $60\,\mathrm{k}\Omega$.

Chromium oxide is a potential candidate for use as a high-resistance thin-film component [29]. Chromium oxide has a resistance that is tunable through oxygen doping, as well as showing good adhesion to silicon substrates; it is also easy to pattern by chemical etching or lift-off. The electrical and mechanical characteristics of chromium [31–33], Cr_2O_3 [34], and CrO_2 [35] are all well-documented, due to the numerous applications of these materials in microcoating and magnetic tape manufacture. Less work has focused on amorphous chromium oxide films. Recent studies [37, 38, 48] have looked into the mechanical properties of amorphous films and found good hardness and resistance to wear, but the electrical properties of the films are less well-documented. While groups which utilise pure Chromium resistors can use shadow evaporation to deposit a thin file ([28]), other groups ([36–38]) have used magnetron sputtering while introducing an oxygen gas to achieve an oxide film. These studies have also noted that when annealed below 400^0C, CrO_x films are primarily amorphous, which is desirable for high frequency circuits ([39]). The films are non-magnetic and therefore suitable for use in a circuit

with superconducting elements in close proximity. In the past, thin, weakly oxidised Cr resistors with a sheet resistance up to 800 Ω/□ have been employed successfully to provide high resistance [29]; however, the small widths and large length scales necessary to create higher-value resistors in materials such as weakly oxidised chromium or NiCr can be more difficult to fabricate, in addition to the issue of parasitic capacitances. Strongly oxidised chromium oxide films have the advantage of a larger sheet resistance, meaning a high-resistance structure can be more compact.

Parasitic capacitances between the resistor and the substrate can become a substantial issue for high frequency circuits. In an ac circuit this can result in an unwanted coupling to the circuit components, or delayed circuit response at high frequencies [46, 47]. This effect is minimal in low frequency circuits, but in a high frequency circuit this current can be very large as the extra current needed is governed by the equation

$$i_{PC} = C_{PC}\frac{dv}{dt} \tag{1.29}$$

where C_{PC} is the parasitic capacitance. This means the impedance is no longer constant, but dependant on the frequency applied to the circuit.

$$Z = R - \frac{j}{wC} \tag{1.30}$$

This is because the on-chip resistors and the parasitic capacitance is forming a low-pass RC filter. Above a certain frequency, the cut-off frequency, the passage of current through this circuit will be halted entirely as the filter provides a short circuit at high frequencies. An estimate of the value of the resistor capacitance, and the cut-off frequency this corresponds to, has been outlined in calculations by Zorin [29] et al. Their method allows us to calculate the capacitance for a resistor by using the area of the resistor in contact with the substrate

$$C = C_0 \cdot A \tag{1.31}$$

where A is the resistor area given by the length (L) times the width (b) and C_0 is the capacitance per unit area. The cut-off frequency is given by the relation

$$f_c = \frac{1}{2\pi \cdot R \cdot C_0 \cdot L \cdot b} \tag{1.32}$$

where R is the resistance of the resistor. This shows that if a low resistance film is used, such as NiCr, then making a high value resistor out of a long narrow section of this material can result in significant effects in a high frequency circuit. Even the high value (26 KΩ) resistors used in the Zorin paper resulted in a cut off frequency of 7.5 MHz, too low for a QPS circuit. This effect can be minimised by using a high resistance material to create a more compact resistor, as investigated in this thesis.

Another capacitance related issue for thin film resistors is Coulomb blockade. In non-continuous thin films, where the film is made up of isolated grains of material, the barrier between two grains can act as a tunnel junction that electrons will have to pass for conduction to continue [39]. This can be thought of as a capacitor with a dielectric material between the two terminals. This is primarily an issue in low-temperature circuits where tunnelling electrons will charge the capacitor with a characteristic voltage of

$$U_{CB} = e/C_{CB} \tag{1.33}$$

where C_{CB} is the blockade capacitance. Coulomb blockade effects become dominant for voltages below the value of U for which electrons will not have the energy to pass across the barrier, causing an increase in the resistance of the thin film resistor.

Chapter 2

Experimental Method

The aim of the project was the fabrication of thin film resistors of value sufficient for use in the QPS circuit in figure 1.5, and then to integrate these into the on-chip circuit, with nanowires of low enough dimensions to observe quantum phase slips. To achieve this goal films were grown by physical vapour deposition onto a silicon substrate. Once the low temperature resistance characteristics were found patterning by photolithography was investigated in order to find a viable process to make an integrated device. The following section describes the materials used during the investigation, a brief outline of the techniques of physical vapour deposition and photolithography, which were used to fabricate the samples, and a description of the equipment used to characterise the samples.

2.1 Fabrication

2.1.1 Evaporation

Evaporation is a method of creating thin films of material. The material is contained in a crucible which will be heated (by passing a current through the crucible in the case of thermal evaporation) to allow the evaporation of the material onto a substrate. In this way nanometer or millimetre thick films can be created.

The are several advantages to evaporation over other means of deposition. It is relatively quick to deposit large thickness films (compared to sputter deposition for example) and so it is favourable for films in the 100's of nanometer to micrometre range. The evaporated material also has a strong directionality so if it is important to the film design for material to be deposited from one direction then evaporation is preferable to sputtering, which deposits from a wide area.

2.1.2 Sputter Deposition

Sputter deposition, is a process in which material is ejected from one or several sources, known as targets, and projected onto a target substrate. In dc sputtering the particles that emerge from the targets are extracted (sputtered) from a bulk material by firing particles of an inert gas, usually argon (Ar), at the material, which then releases the particles as a plasma which is accelerated from the target to the substrate by applying an electric field. For rf sputtering the sign of the target and substrate are reversed at high frequency. Combinations of different materials, e.g. a niobium-silicon structure, can be obtained by having each element emerge from a different target to combine on the substrate. By mixing oxygen with the argon gas it is possible to incorporate oxygen into the plasma beam and so grow oxide films. It is using this method that oxygen defects were introduced to thin chromium films to increase the resistance of the films. All films produced for this thesis were produced using magnetron plasma sputtering, with differences in voltage and whether dc or rf sputtering highlighted in each section.

There are several parameters set before deposition that must be taken into consideration when growing films in this way, as the eventual structure can be affected by argon gas pressure, amount of oxygen included with the argon gas and the temperature of the substrate. For example, low temperature deposition on a randomly arranged substrate will lead to nucleation; the formation of randomly distributed isolated islands of our material. Thornton described the relationship between gas pressure and substrate temperature for sputtered films [76] through the use of the structure zone model.

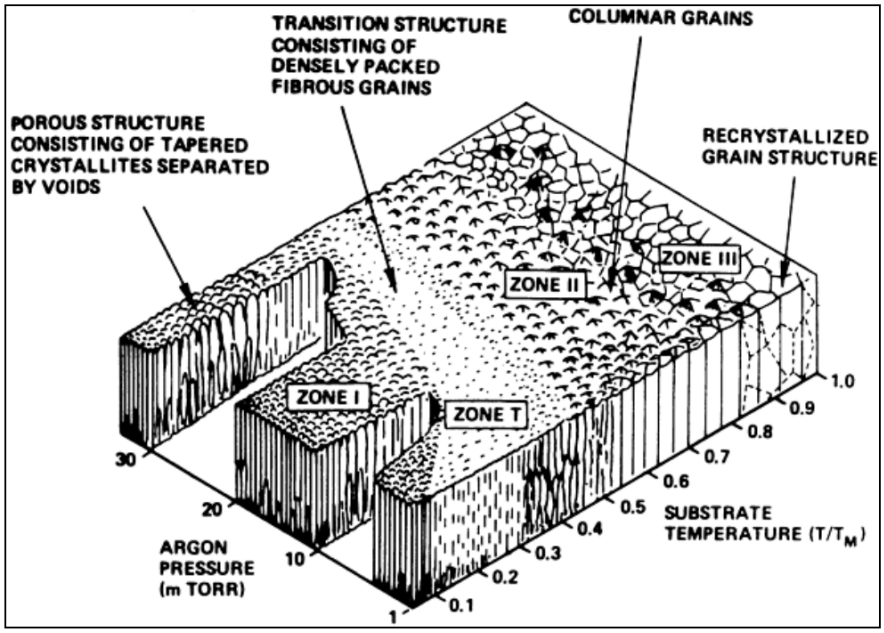

FIGURE 2.1: Diagram of the structure zone model by Thornton [76]

The resistivity of a film formed by sputter deposition will usually increase for increasing gas pressure. This is because as pressure is increased the film is likely to take on the structure of columns of material with voids in between. The number of voids increases as pressure is increased, inhibiting electron flow and so increasing the resistivity. Mahieu et. al. [78] found that this is due to the fact that at higher pressures the particles in the beam will have more collisions with each other, removing some of their energy before they reach the film, meaning they have less energy to move around and produce a dense, uniform arrangement, and instead form columns and voids. Conversely, as substrate temperature is increased particles will have more energy to diffuse on the surface and arrange denser structures and crystalline forms which will in turn affect resistivity [77].

2.1.3 Photolithography

Photolithography is a microfabrication process that can be used to pattern features on a micron scale. In this project, wet etching and lift off were both used to fabricate test patterns. In both methods a resist is applied to a film and then exposed to UV through a mask of the desired pattern. The resist is then developed; for a positive resist where the UV is not exposed will be protected from the etching process and the pattern will be left after a chemical wet etch. In lift off, regions of a negative resist exposed to UV are protected, after development these areas will leave exposed substrate that can be sputtered onto. After deposition the resist is lifted off using a solvent, leaving just the pattern behind [45]. The two types of processes are illustrated in Fig. 2.2:

Lift-off can be advantageous when a wet etch could damage layers already deposited, or if the material being patterned is difficult to etch. However, it can be difficult to remove the entire resist following lift off, also a lilypadding effect can be observed, distorting the desired pattern. This is described in more detail in section 3.3.1.1. In contrast, the wet etch method can result in smoother features. The exact method, or combination of methods used depends on the number of layers and pattern of each layer.

Each step in this process can have a large impact on the final pattern produced. If the spin speed is too low then the resist layer will be too thick, leading to exposing problems. If the UV exposure time is too long then the pattern will lose its sharply defined edges. Likewise overdeveloping will cause sharp edges to disappear and degenerate the pattern. If the sample is etched for too long then too much metal will be removed and the pattern will be removed.

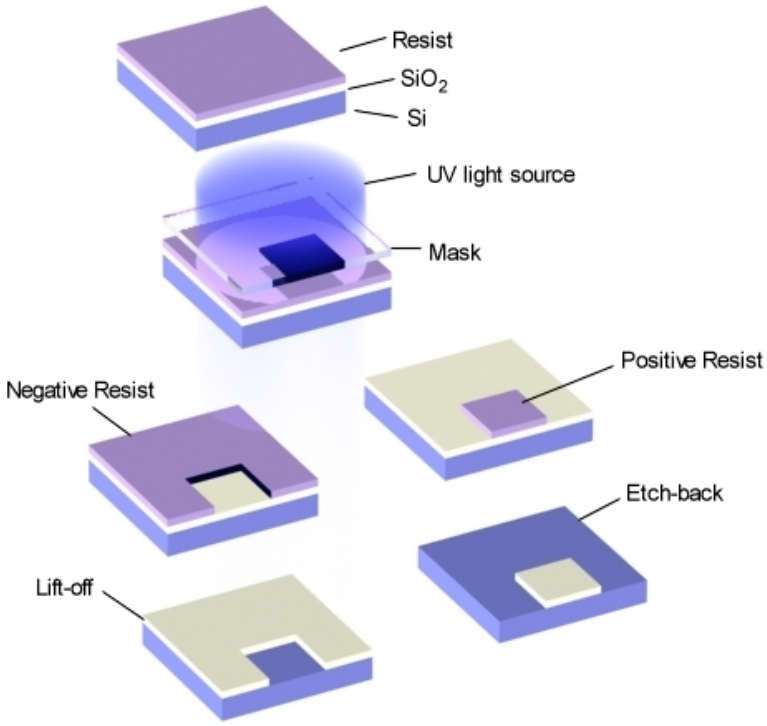

FIGURE 2.2: Breakdown of the photolithography process [79]

2.1.4 Electron Beam Lithography

Although photolithography is ideal for features down to one micron once the wavelength of the light used for exposure is reached it is impossible to achieve better resolution. If we wish to expose features smaller than this we must switch to a new type of exposure. Electron-beam lithography (EBL) utilises electron sensitive resists and a focused electron beam to reach a resolution of tens of nanometers. An EBL system usually consists of an electron beam source, several sets of electrostatic or magnetic lenses used for focusing, a movable stage that wafers are placed onto and a scanning electron microscope (SEM) used to image the surface.

To make a pattern using EBL an electron sensitive polymer in solvent, such as polymethyl methacrylate (PPMA) or hydrogen silsequioxane (HSQ), is first spun onto a wafer and baked to remove some of the solvent from the surface. This resist is then exposed using a small focused electron beam at a single spot, this spot will correspond o a single pixel on an imported pattern. The beam will then move within a range of a few hundred microns to expose the whole designed pattern to the electron beam, if larger exposure areas are required the stage will move and the individual patterns stitched together. Exposing areas of the resist to an electron beam will cause long polymer chains to be broken up into smaller ones [40] (for a positive resist), making them soluble during

development in solvents such as methyl isobutyl ketone (MIBK) or isopropyl alchohol (IPA). These areas will be exposed substrate that material can be deposited into. Once material has been deposited the wafer can then be left in a suitable solvent, such as Acetone or 1165, this will remove the remaining resist and any deposited material not bonded to the substrate leaving just the desired structures.

2.1.5 Reactive ion etching

Reactive ion etching is a process typically used for substrate cleaning. A substrate is isolated in vacuum in the chamber, the chamber is then filled with a plasma for the desired time to etch the substrate. This will clean the surface of contaminants and can also remove an oxide layer that can build up on some substrates such as Silicon.

Using reactive ion etching before applying a thin film or a lithographic mask can help to improve the adhesiveness to the surface, allowing for sharper design features and less failure with lithographic techniques such as lift off.

2.1.6 Ion milling

A sputter system can be used for substrate cleaning as well as depositing materials. As described above a plasma (typically argon) is used to sputter material from the target. By allowing this argon plasma to generate around the substrate instead of the target, the substrate surface will instead be impacted by the argon ions which will remove material from the surface.

This process can be used as an in situ cleaning stage before deposition to remove any unwanted contaminants from the surface without having to release a sample from vacuum. This can help improve the purity of a thin film or improve the success of lithography.

2.1.7 Focused Ion Beams

Focused Ion Beams (FIB) are a tool that can be used for the fabrication of nanoscale structures as an alternative to lithography. In FIB ions are generated in a source, such as gallium, and then accelerated to the target substrate using an ion gun. The ions are focused on route using electrostatic lenses. By focusing ions in this way extreme precision can be achieved in milling, allowing the creation of nanometer scale features.

This has several advantages over standard lithographic techniques. The first is that the pattern can be imaged as it is created, using an SEM camera. This means that

adjustments can be made while the sample is in situ, rather than having to complete the whole process and see the results. The second advantage is that the patterning stage is entirely completed in vacuum, reducing contaminants. By selecting an inert material as the ion source, such as neon, contaminants can be even further reduced. Initial mills for this thesis were completed using Gallium ions. However, upon the purchase of a new FIB system the mill ion was switched to Neon as this was hoped to reduce implantation of impurities in the sample. This is discussed further in section 3.4.2.3.

2.2 Measurement

2.2.1 Energy / Wavelength Dispersive X-Ray Spectroscopy

Energy dispersive x-ray spectroscopy (EDS) is a technique used to find the individual elements that make up a sample. It works by analysing the x-rays emitted after shining a focused beam of electrons, protons or x-rays at a sample, with electrons used for these experiments. This causes an electron in an inner shell of one of the atoms to become excited, leaving a hole. This hole is then filled by an electron from an outer shell, causing the emission of an x-ray in the process. By analysing the energy of x-rays emitted we can work out which element they came from.

There are several factors that will affect the accuracy of the EDS measurements. The system cannot detect the x-rays produced by elements with an atomic number less than four (H, He, Li). It is also important to select the correct energy for the incoming x-rays. The x-rays should have an energy roughly double that of the largest element that you are trying to observe. However; if the energy of incoming x-rays is too high then for a thin film they can penetrate all the way through and provide more information about the substrate than the film. The key is to use the lowest energy possible that can detect all of the elements expected to be found in the sample. Some elements also have overlapping energies such as chromium and oxygen, as this had a bearing on measurements described later wavelength dispersive spectroscopy (WDS) was also used.

In a WDS system the sample is exposed to x-rays as in EDS, however on the return they are diffracted through a crystal in front of a detector. In this way the x-rays are separated on their way to the detector as described by Braggs Law

$$N\lambda = 2d\sin\theta \tag{2.1}$$

The separated x-Rays are then collected by the detector and assigned to each element. A series of crystals is used to cover most of the periodic table in this way. The advantages

of WDS are an increased accuracy for the lower order elements such as oxygen and no overlap of peaks of chromium and oxygen, which is crucial in later measurements. Whereas if there is no overlap of energy peaks then EDS can be advantageous as it is less sensitive to the position of the sample, allowing rougher samples to be analysed where WDS would require flat surfaces [41].

2.2.2 X-Ray Diffraction

X-ray diffraction is a technique which enables us to examine the chemical structure of a material. X-rays are emitted from a source, which will then interact with the electrons of atoms in the crystal structure we are interested in. The electron will be excited and emit an x-ray of the same frequency as the incident wave.

The intensity of the returning x-rays will be at a maximum when the emitted and returning x-rays have the same angle of incidence. This will be at different angles for different structures. Using Bragg's law (2.1), by analysing the angle at which peaks in intensity occur for x-rays of known wavelength, we can deduce the spacing of crystal layers and so deduce the structure of the crystal [42].

2.2.3 Four Point Measurements

All sheet resistance measurements were completed using the principle of the four-point measurement. This type of measurement has an advantage over two point measurements as the contact resistance contribution to the measurement is zero. The principle involves having two contact leads supplying the current and two separate leads to measure the resultant voltage, this results in a negligible voltage drop as the voltmeter carries an extremely small current. As current is the same at all points in the circuit we can measure the sheet resistance using ohms law so that

$$R_s = K \cdot \frac{V_m}{I_s} \tag{2.2}$$

where I_s is the current supplied, V_m is the voltage measured and the multiplication factor $K = \pi/ln2 = 4.53$ is used if the film is large compared to the probe geometry and the probe spacing is large compared to the film thickness [80]. A linear geometry (all four leads placed in a straight line) was used for these measurements, alternatively the leads can be placed in a square configuration. A Veeco FPP5000 was used for all sheet resistance measurements in the cleanroom. This has an accuracy of within 1% as long as the sample is significantly larger than the distance between the end probe points, ideally 5 times the distance between the probes. For this reason a glass slide

was sputtered along with a Si wafer in each run so an accurate sheet resistance of the film could be measured. The probe had a limit of measurement of $1x10^5\Omega$ which proved to be a limiting factor for chromium oxide films with a significant oxygen content, as described later.

2.2.4 Liquid Helium Measurements

Measurements of the resistance as a function of temperature were conducted using liquid helium. A sample was placed on a mount with a series of contacts. Four aluminium wires were bonded from the sample to the mount in a line to create a four-point probe set up. This was then attached to a long dip probe for insertion into the liquid helium. The dip probe allowed a maximum voltage source for measurement of $\pm$ 5V. The key to accurate measurement is as large a voltage range as possible. However as the resistance of some samples increased with decreasing temperature it was important not to set the voltage to the maximum at room temperature. The current range was not set higher than $\pm$ 200mA to avoid heating in the sample and connecting wires. Once the current and voltage were set to appropriate ranges the dip probe was inserted into the dip probe. In this way the resistance could be measured as a function of temperature from room temperature (292 K) to 4.2K.

2.2.5 Physical Properties Measurement System

The Quantum Design Physical Properties Measurement System (PPMS) is an instrument designed for use with a variety of probes. In basic operation the system can cool a sample down to 2K, expose the sample to a magnetic field of up 14T in magnitude perpendicular to the sample. In these conditions a variety of resistive and thermal measurements can be programmed and automatically performed by the system. Different probes can be used to hold the sample to open up the system to more versatility.

The horizontal rotator allows the rotation of a sample around its axis perpendicular to the magnetic field applied by the physical properties measurement system (PPMS). The horizontal rotator can be exposed to all temperatures in the range of the PPMS down to 2K. A sample can be exposed to a magnetic field in this temperature range of -14 to 14T, through an arc of rotation of -10^0 to 370^0 in a direction perpendicular to the field.

The ^{3}He probe can be used to cool a sample further than the normal system limit of 2K using a reservoir of liquid ^{3}He. With this addition it is possible to keep a sample at a minimum constant temperature of 500mK, and cool a sample to 300mK in a 90 minute burst of measurement.

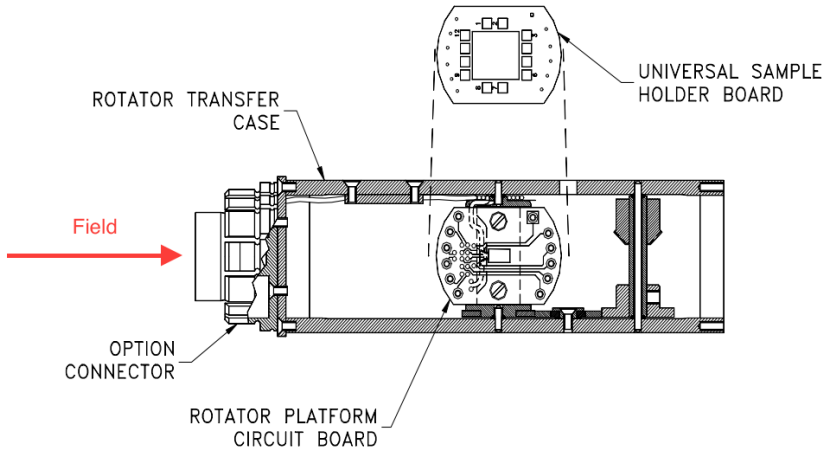

FIGURE 2.3: Diagram of field orientation of the PPMS horizontal rotator [43]

Chapter 3

Results

In order to fabricate the QPS circuit described by Mooij [12], a nanowire exhibiting QPS effects needs to be connected in series to an inductor and a resistor of value over 60 kΩ. The first section of this chapter describes the investigation of thin chromium oxide films for use as resistors in this circuit. In order to maximise the QPS rate, narrow, homogeneous nanowires with a low value of Tc are desirable [58]. The next two sections describe the growth of nanowire materials and attempts to fabricate nanowires of these materials and minimise their dimensions. The final section describes recent attempts to fabricate a QPS circuit, and some of the considerations that need to be taken into account.

3.1 Growth of thin film chromium oxide resistors

A particular example of an application requiring high-value resistors is circuits for exploiting quantum phase-slips. In 2006, Mooij and Nazarov [12] showed a duality between Josephson junctions and a coherent quantum phase-slip (QPS) circuit element — a superconducting nanowire — which implies the potential for a new quantum standard for current.

A series of CrO_x films was created, using a broad range of oxygen dopant levels. The CrO_x films were deposited on p-doped silicon by dc-magnetron sputtering in an argon and oxygen atmosphere, using a 3" Cr target with a 500 W sputter power for ten minutes with a three-minute pre-sputter. The target-to-substrate distance was 18 cm and deposition took place at room temperature. The total gas pressure was 5 mTorr. The film thicknesses, measured by a DektakXT surface profiler, were all in the range 179 nm for growth in pure argon to 246 nm for growth with an oxygen partial pressure of 0.7 mTorr,

implying deposition rates from 17.9 nm/min to 24.6 nm/min. We report below on the characterisation of these films.

3.1.1 Wavelength dispersive spectroscopy measurements

Wavelength-dispersive spectroscopy (WDS) in a scanning electron microscope was used to determine the composition of the films grown. Fig. 3.1 shows the variation of the oxygen-to-chromium mass ratio in the film with the O_2 partial pressure used during sputter deposition. There is a gradual increase in the proportion of oxygen in the film as the pressure of oxygen introduced into the argon gas is increased. Oxygen is detected in the film by WDS even if no oxygen is added whilst sputtering. Since the silicon WDS signal is small, the contribution to the oxygen WDS signal from the surface of the substrate is expected to be unimportant. Instead, the oxygen detected is likely to arise from oxidation of the surface of the film after removal from the chamber and the influence of residual oxygen in the chamber during growth.

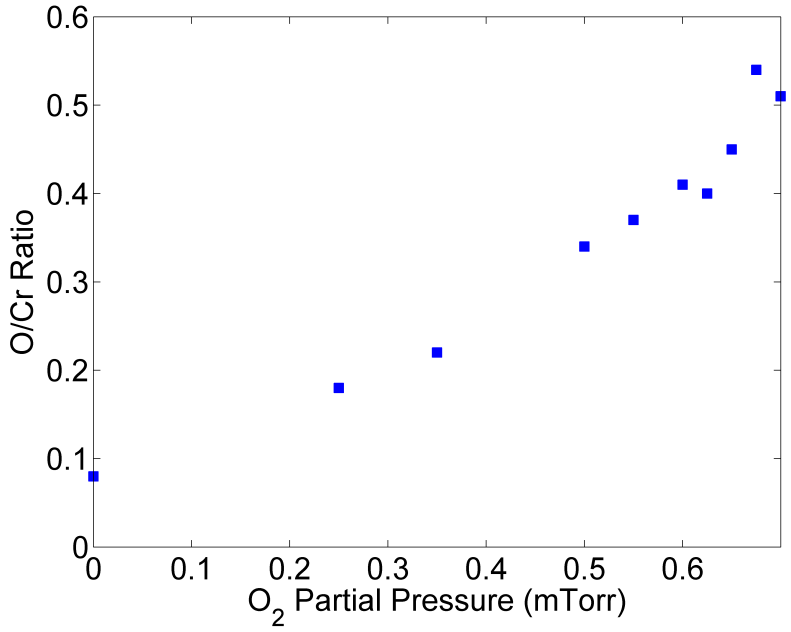

FIGURE 3.1: Dependence of the oxygen-to-chromium mass ratio in the film (as measured by WDS) on the O_2 partial pressure during growth. An argon gas partial pressure of 5 m torr was used for all samples.

Fig. 3.1 shows that there is a gradual increase in the proportion of oxygen in the film as the pressure of oxygen introduced to the argon gas in the sputterer was increased. The next section details the use of X-ray diffraction to investigate the structure of the films.

3.1.2 Structural measurements using XRD

X-ray diffraction was used to investigate the structure of the films. Fig. 3.1 shows the measured trace for bare substrate as well as the 0.34 and 0.37 O/Cr mass ratio films, the other films have been removed and the data offset for clarity. All of the films from Fig. 3.1 were measured and only substrate peaks were visible above experimental noise, consistent with the conclusion that the films are amorphous. Fig. 3.2 shows the trace for two of these films compared to the silicon substrate. The traces have been displaced for clarity.

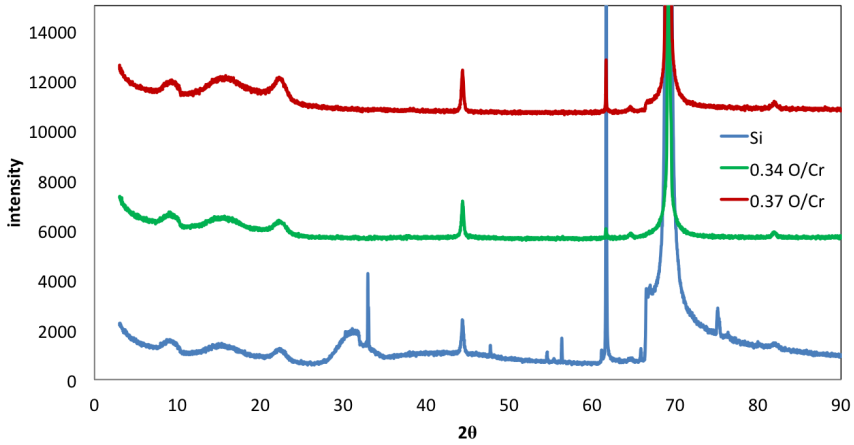

FIGURE 3.2: Graph showing the XRD trace for the bare silicon and two of the chromium oxide films.

This is to be expected for thin sputtered films that have not been annealed such as the results from Pang et. al. [38] who reported that chromium oxide films annealed below 400^0C were primarily amorphous.

3.1.3 Variation in sheet resistance with Oxygen concentration

Four-point electrical transport measurements were performed at room temperature to determine the sheet resistance of the films. A linear contact configuration was used and the measurement was made immediately after removing the sample from the sputterer vacuum chamber.

Fig. 3.3 shows the variation of room-temperature sheet resistance of the chromium oxide films (the same samples as shown in Fig. 3.1) with the oxygen-to-chromium mass ratio. It is worth noting that some conduction through the semiconducting substrate is likely in such measurements. Fig. 3.3 shows a steep increase in room-temperature sheet resistance as the oxygen incorporation increases, corresponding to a departure from standard metallic conduction. The samples with O/Cr mass ratios of greater than 0.45, which

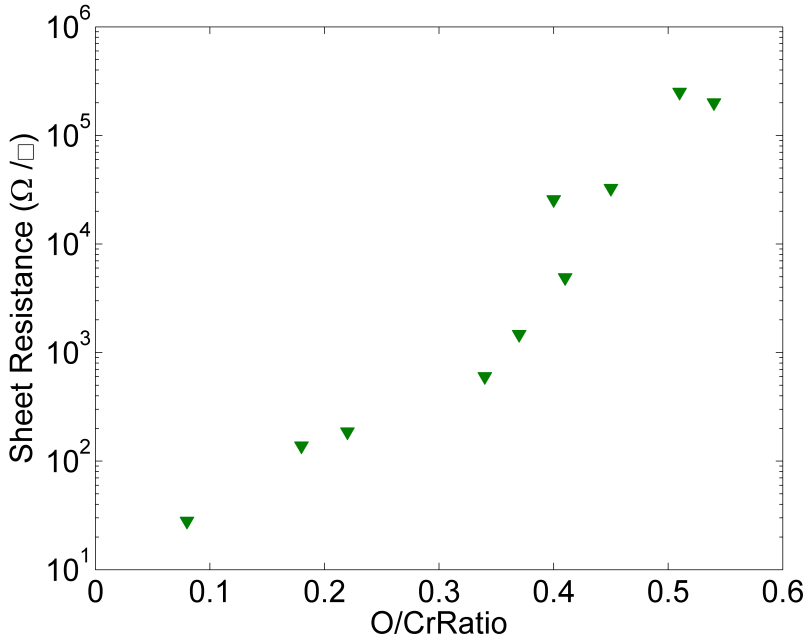

FIGURE 3.3: Variation of room-temperature sheet resistance of chromium oxide films with the oxygen-to-chromium mass ratio for the same samples as shown in Fig. 3.1.

had higher resistance, were measured later using equipment with a larger measurable resistance range.

3.1.4 Variation in conductance with thickness

Another factor that can have a significant effect on the conduction properties of a thin film resistor is the thickness of the film. A series of films were grown with a constant O_2 pressure (0.5 mTorr) and constant base pressure ($3x10^{-5}$ mTorr). It is important to maintain a constant base pressure as residual water vapour in the system can form monolayers on the surface. If this interacts with the plasma it can split into atomic hydrogen and oxygen, which will contaminate the film and lead to inconsistant oxygen incorporation [44]. The time the substrate was exposed to material from the target (run time) was decreased for each run. The thickness was measured using the Dektak 8 for all results to ensure consistency down to thicknesses below 50 nm.

As the thickness of the sputtered films decrease they become less conductive. This is due to the fact that the total resistance is no longer that of the bulk material, but a combination of the bulk resistance and the resistance due to surface effects (see section 1.1.2). The results seem to indicate that there is low dependence of thickness on conductance until the thickness approaches 50 nm, at which point there is a dramatic decrease in conductance as the thickness is reduced further, suggesting that surface effects have

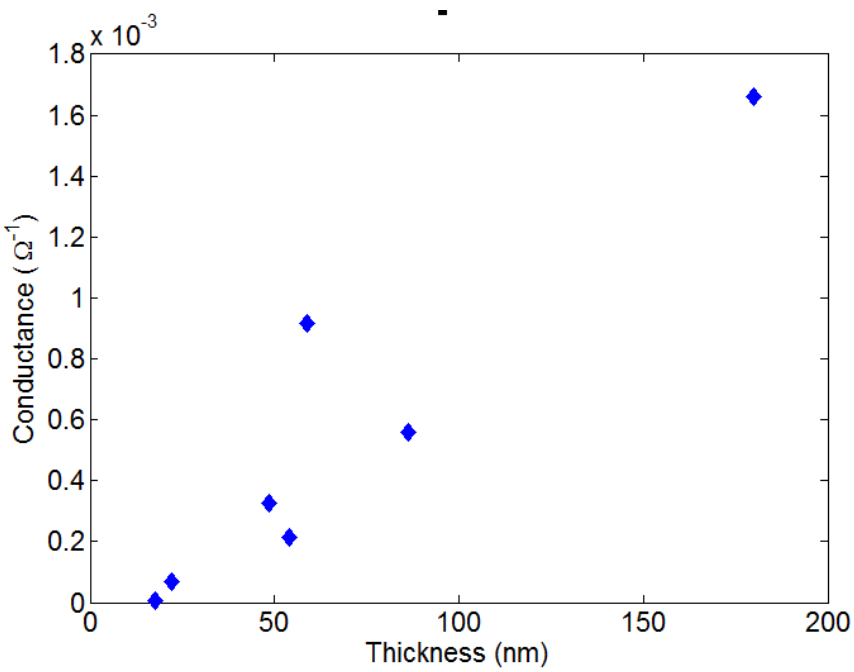

FIGURE 3.4: Variation of room temperature sheet conductance with film thickness.

now become dominant. Gould [31] found similar results for the resistivity of thin pure chromium films compared to bulk.

3.1.5 Variation of resistance with temperature

In order to measure the resistance of the films as a function of temperature, bonded aluminium wires were used to make contact to the films at four points, spaced by approximately 1 mm, in a linear configuration and the resistance was measured by means of a four-point technique. At room temperature, conduction was ohmic in the measured range of currents, up to 200 μA. The samples were cooled, by manual insertion of a probe into liquid helium, to 4.2 K, and the changes in the resistance of the films with temperature during cooling was measured, using a dc bias current of 10 μA for all films. Conduction remained ohmic at 4.2 K for all measured films in the whole measured range (to 500 nA for the high-resistance 0.41 O/Cr mass-ratio film and to 200 μA or all other films). The inset of Fig. 3.5 shows an example of this, for the 0.34 O/Cr mass-ratio film.

Fig. 3.5 shows the measured variation of four-point resistance with temperature for CrO_x films of varying composition. The data has been normalised with respect to the resistance at 100 K; in the temperature range shown, conduction through the substrate is negligible. The graph shows that oxygen incorporation has a significant effect on the variation of resistance of the films with temperature, and there is a large variation between the films in the value of low-temperature resistance. The films become more resistive for

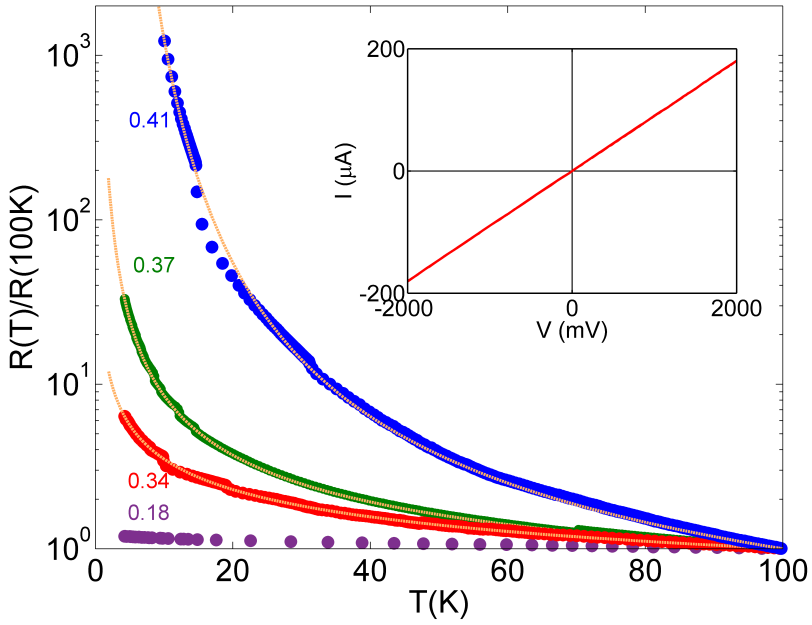

FIGURE 3.5: Variation with temperature of measured four-point resistance, normalised to the value at 100 K, for CrO_x films of varying composition. Labels denote the oxygen-to-chromium mass-ratio of the film, as determined by WDS. Lines in gold denote fits to a variable-range hopping model. Films were biased at 10 μA and cooled to 4.2 K. The rate of temperature change was 20 K/min below 150K and 6 K/min below 20K. Slight discontinuities in the data points are associated with thermal lag as the probe was raised from the dewar in stages. (Inset): Current-voltage characteristics up to 200 μA of 0.34 O/Cr mass-ratio film at 4.2 K, demonstrating ohmic behaviour.

increasing oxygen concentration. Initially phonon scattering will dominate the resistance of the films, as the films are cooled further this effect will minimise as phonon scattering is dependant on temperature (see section 1.1.2) and impurities in the film start to dominate, which causes the curves to deviate from each other. The sheet resistance at 4.2 K was obtained from the measured resistance by means of a standard transformation for the films [52] and is shown in Table 1. The 0.41 mass-ratio film reaches a resistance at 4.2 K much greater than 20 GΩ at 4.2 K, the input impedance of the measurement equipment, corresponding to a sheet resistance well above 80 GΩ.

Since oxygen incorporation over time is a known issue for amorphous films, we re-measured the films with 0.34 and 0.37 O/Cr mass-ratio composition 18 months after deposition (the measurements shown in Fig. 3.5 were carried out within 2 weeks of deposition). For both films the room-temperature resistance was unchanged, while the resistance at 4.2 K increased by a factor of two. This provides an indication of the level of stability of the resistance value of our CrO_x films. Since the properties of the film vary strongly with changing oxygen content (Fig. 3.5), we are able to conclude that the further oxygen incorporation which has occurred over time is small.

The data shown in Fig. 3.5 have been fitted to a variable-range hopping form, $R = R_0 \exp(T_0/T)^n$, where T_0 is the localisation temperature. For Mott variable-range hopping (VRH), $n = (d + 1)$ in d dimensions; for Efros–Shklovskii VRH, appropriate for stronger electron-electron interactions, $n = 1/2$ [5]. This functional form provides a good fit to the data for the films with higher oxygen content, as shown in Table 1. The fitted value of n varies with the oxygen concentration; it is consistent with 3-D Mott VRH for the 0.37 O/Cr film and Efros–Shklovskii VRH for the 0.41 O/Cr film. The crossover from Mott VRH to Efros–Shklovskii VRH with increasing oxygen content is in line with expectations that electron-electron interactions become increasingly important in the most resistive films. The values of T_0 were found to be of the order of those found in other materials that exhibit Efros–Shklovskii VRH [53, 55]. T_0 is related to the localisation length ξ via the equation $T_0 = e^2\beta/k_B k\xi$ where β is a numerical constant, k_B is the Boltzman constant and $k = \epsilon_r\epsilon_0$ is the electrical permittivity of the material [4, 51]. Dielectric constants for disordered metals have not generally been reliably determined, only estimated [53, 54]; independent of such estimates $\epsilon_r\xi$ can be calculated from T_0. Taking $\beta = 2.8$ [54], we obtain $\epsilon_r\xi = 1240\,\text{nm}$ for the 0.37 mass-ratio film and $\epsilon_r\xi = 737\,\text{nm}$ for the 0.41 mass-ratio film. If we assume ξ=10 nm, this gives an estimate of $\epsilon_r = 124$ for the 0.37 mass-ratio film and $\epsilon_r = 74$ for the 0.41 mass-ratio film. The high value of T_0 for the 0.34 mass-ratio film may indicate that this film is at the border of applicability of this model. Poor fits for the lower oxygen-content films indicate that conduction in those films is too metallic to be accurately predicted by the VRH model.

O/Cr Mass Ratio	$R_{(4.2\,K)}$ ($\Omega/\square$)	n	T_0 (K)	Fit $\mathcal{R}^2$
0.18	65	-	-	-
0.22	317	-	-	-
0.34	1.1×10^4	0.185 ($\pm$ 0.006)	41490	0.9996
0.37	9.5×10^4	0.351 ($\pm$ 0.004)	474	0.9998
0.41	$>2.0\times10^{10}$	0.530 ($\pm$ 0.014)	796	0.9988

TABLE 3.1: Variation of the measured sheet resistance at 4.2 K for chromium oxide films of varying oxygen concentrations. $R_{(4.2\,K)}$ is the measured sheet resistance at 4.2 K. Coefficients of a fit to the equation $\ln R = \ln R_0 + (T_0/T)^n$ are also shown. $\mathcal{R}^2$ is the coefficient of determination and indicates the goodness of fit. Fits for the 0.18 and 0.22 mass-ratio films to this model were poor, associated with little change in resistance across the temperature range.

3.1.6 Magnetoresistance

In order to check whether nano crystals of magnetic chromium oxide phases, which could suppress superconductivity, an Oxford Instruments Physical Properties Measurement system was used to investigate the magnetoresistance of the chromium oxide films. A

film with an mass ratio of 0.34 O/Cr was cooled to 2 K and then exposed to magnetic fields up to 14 T.

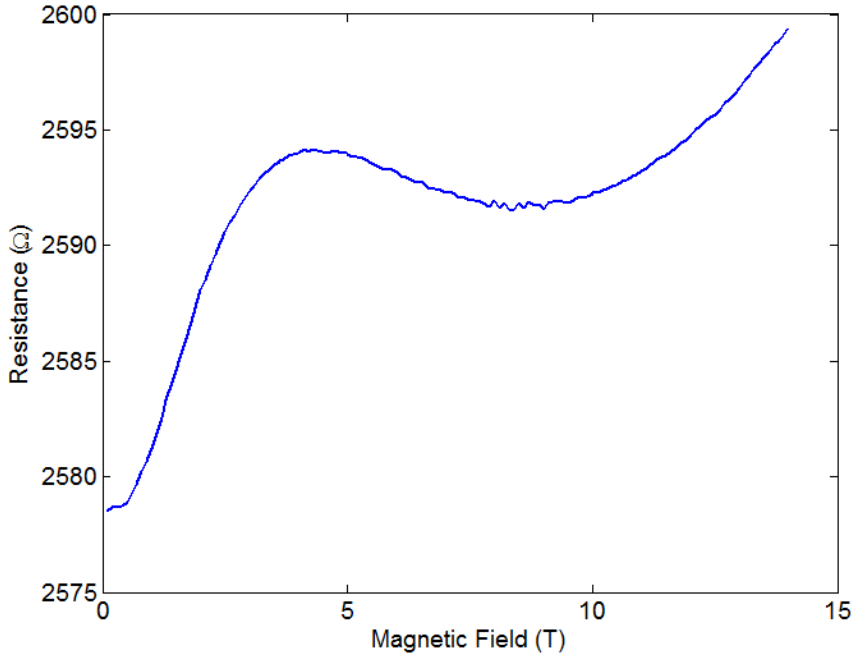

FIGURE 3.6: Variation of resistance of chromium oxide with applied field perpendicular to the surface at 2 K.

Fig. 3.6 shows the measured four point resistance with a DC bias of 10 μA as the applied field perpendicular to the direction of current was varied from 0 T to 14 T. The resistance of the 0.34 O/Cr film was found to vary by only 0.01 % of the total resistance.

Fig. 3.7 shows the change in resistance as the sample was rotated through a field of 14 T from perpendicular to the surface through 180^0, so that the field is parallel to the surface at 90^0 . There is again very little variance in resistance which implied the Lorentz force contribution to the resistance is also minimal. This shows that the potentially disruptive magnetic chromium oxide phases were not present in this film to any significant degree.

As well as checking for magnetoresistance the film was measured in an MPMS to check for nano crystals of ferromagnetic chromium oxide which could affect superconductivity measurements. The sample was cooled to 2 K and a field applied to the sample. As field was swept the sample was moved up and down inside a SQUID to measure the magnetic moment. The background from the sample holder is subtracted for all measurements.

Fig. 3.8 shows that there is a trace amount of magnetic hysteresis, which would be expected if magnetic domains in the film are being aligned by the initial magnetic field and then requiring energy to reorientate if the field direction is reversed. At the peak field strength there is an estimated magnetic moment of 5×10^{-3} μ_B per atom. By

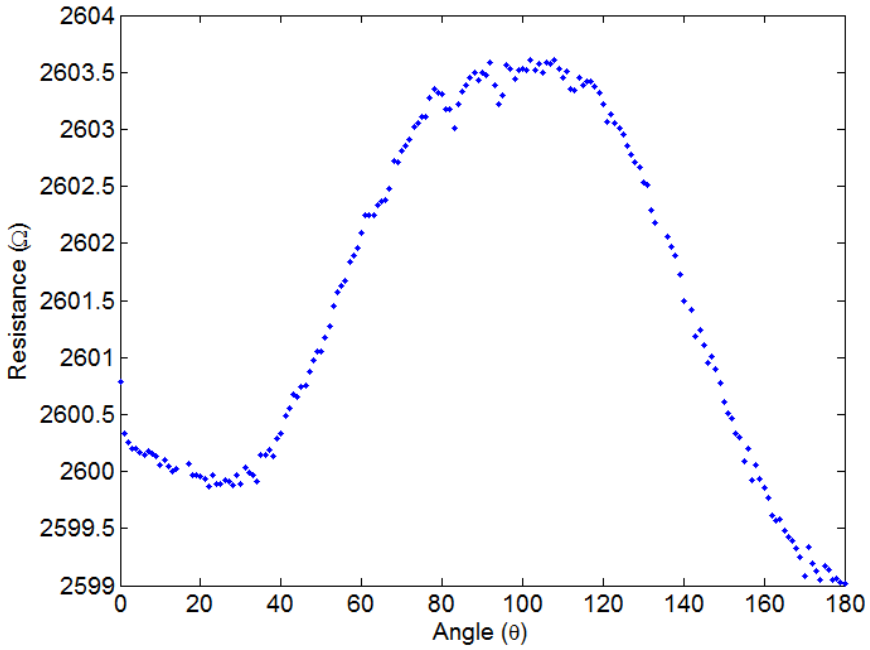

FIGURE 3.7: Variation of resistance of chromium oxide with applied rotating 14 T field at 2 K.

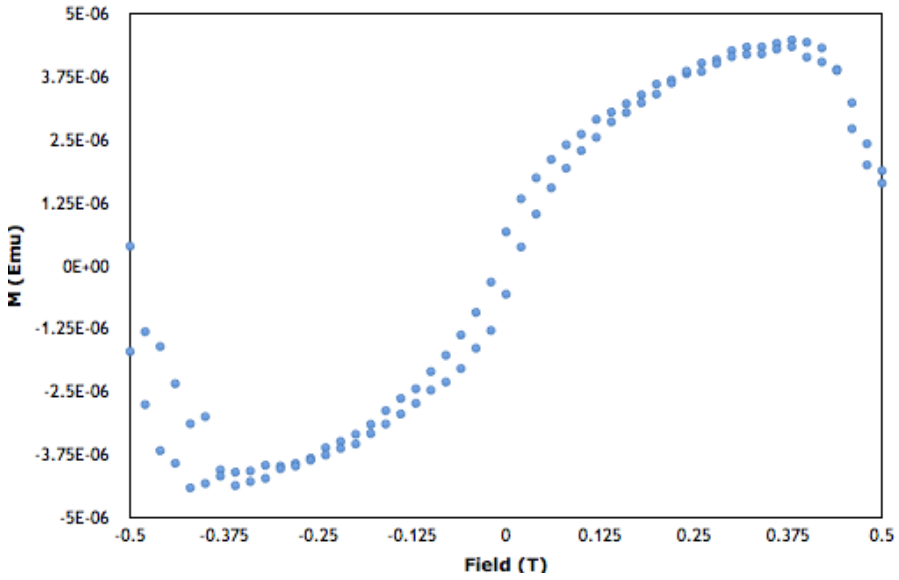

FIGURE 3.8: Variation of magnetic moment with applied field at 2 K.

comparison, a ferromagnetic Cr_2O_3 film has a magnetic moment of 2 μ_B per atom. This small proportion of ferromagnetic phase is unlikely to cause significant suppression of superconductivity in adjacent nanowires and suggests these ferromagnetic nanocrystals are not present to any significant degree in this film.

3.2 Growth of nanowire materials

Several materials were grown to test their suitability for nanowire fabrication. First, pure niobium was grown to test the ability of a new sputter system to produce pure superconductors.

Niobium-silicon was initially the material of choice for use in fabricating the nanowires for a QPS circuit. It is created by two target sputtering to produce an alloy of the two metals. It was chosen as it has a low Tc and a large coherence length, both necessary for maximising the rate of QPS. However, experiments elsewhere in the group concluded that there were issues with the granularity of niobium-silicon films produced, which was suppressing the T_c.

Indium oxide was investigated later in the project as an alternative to niobium-silicon after these difficulties in producing superconducting nanowires were found. It has been shown [71] [72] that it is possible to fabricate amorphous indium oxide films with Tc of between 2-3K. Though films made by sputter deposition tend to be polycrystalline, it is possible to favour amorphous films by altering the oxygen pressure, deposition rate and substrate temperature [73].

Finally niobium nitride was investigated after issues highlighted below with fabrication in niobium silicon and indium oxide. It has been show to exhibit quantum phase-slips [63] while also exhibiting a large enough T_c to be measured using liquid helium.

3.2.1 Growth of high purity niobium films

In parallel to the investigation of thin film chromium resistors, a separate investigation took place on a new magnetron plasma sputter system (SVS 6000). The aim was to investigate the initial parameters needed to grow high purity niobium films. This would then provide a standard recipe for niobium films that could be used as a reference when growing niobium-silicon films of varying compositions to fabricate into nanowires.

3.2.1.1 Variation of Tc with presputter time

The main aim of the initial tests of the new sputter system was to try to grow films of relatively pure niobium. A straightforward test of the purity of a niobium film is to measure the temperature of the transition to superconductivity (Tc), as this is a known quantity for pure niobium (9.2 K). Initially all films were sputtered onto a Si wafer in a base pressure less than 5x10-7 mBar, with a gas pressure of 3x10-3 mBar, a presputter time of five minutes. Beam powers were varied up to the maximum achievable at the time (160 W). However this was not sufficient to grow a film that showed a superconducting transition within the measurable range (4.2 K). The beam power was then kept at a constant 160W and the presputter time varied to try and increase the Tc. Presputtering is important to achieve a pure film as it will remove the oxide layer which can build up on the target as well as having a gettering effect whereby impurities in the sputter system will be coated with a layer of the presputter material onto the chamber walls, avoiding contamination with the resulting film. The films were cooled to a temperature of 4.2 K in liquid helium and a four-point measurement was carried out to find the transition to zero resistance.

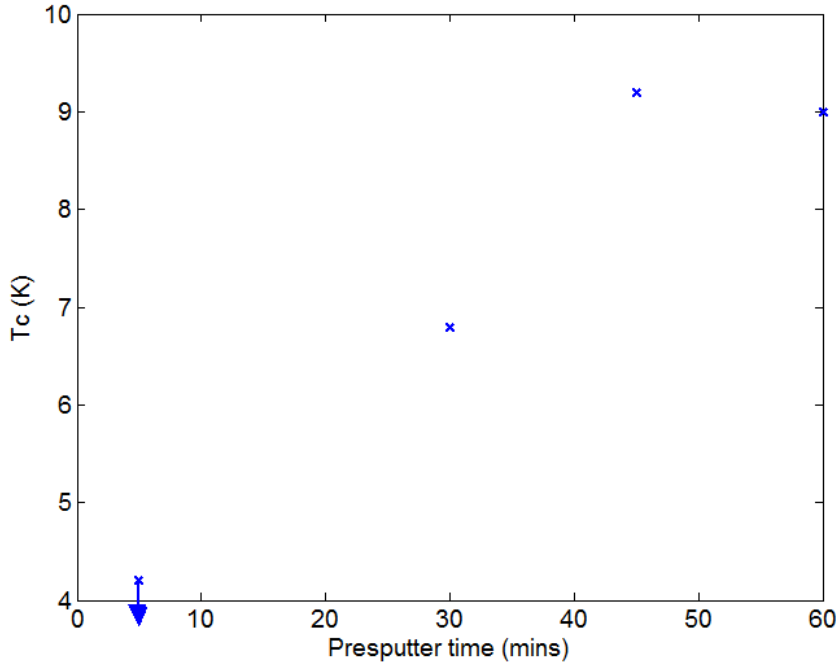

FIGURE 3.9: Tc against presputter time for niobium films sputtered at 160 W.

Fig. 3.9 shows that a presputter time of five minutes results in a film with a Tc less than the measurable limit of 4.2 K. The Tc increases with presputter time with a Tc of 9.2 K for a time of 45 minutes, which is the same as that for pure niobium. It has been shown

that the Tc of Niobium will decrease by 0.93^0K per at. % Oxygen [74], meaning the films grown with a presputter time of 45 mins have minimal impurities.

3.2.1.2 Variation of RRR with presputter time

Another way to parameterise the purity of the film produced is by using the residual resistance ratio (RRR). The resistance against temperature profile for a metal will show a steady decrease in resistance with temperature, due to the reduced contribution of lattice vibrations to the resistance of the film, with an eventual plateau at low temperatures as resistance due to lattice defects dominates, followed by the drop to zero resistance as the temperature drops below Tc. This effect can be seen in the profile for a superconducting Nb film shown in Fig. 3.10.

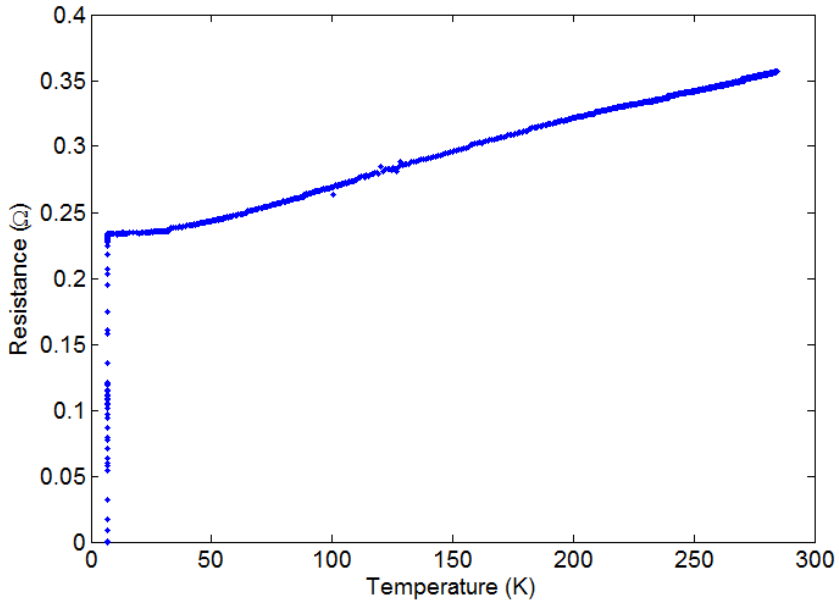

FIGURE 3.10: Resistance against temperature for a niobium film, showing a superconducting transition and residual resistance.

Fig. 3.11 shows that there is an increase in film purity with presputter time. The superconducting transition is strongly correlated to the residual resistance ratio. This is due to the fact that a more metallic film (in this case a purer Nb film) will have a steeper drop in resistance as the total resistance is due more to lattice vibrations than defects. A purer film will also have a higher Tc. The residual resistance ratio is low in the films measured compared to a high-purity film (300 [75]), suggesting there are still impurities in the film, however the high Tc in the previous section suggests these are not oxygen impurities.

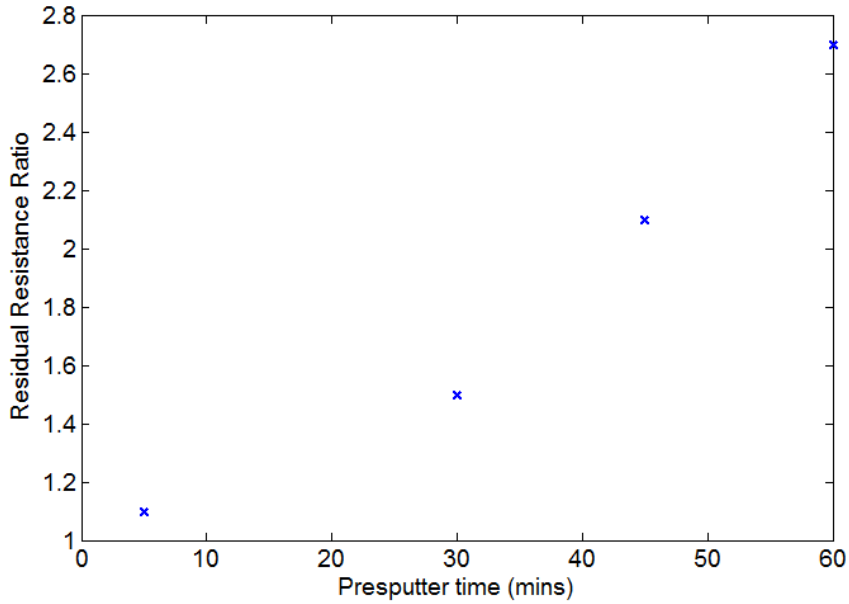

FIGURE 3.11: Residual resistance ratio against presputter time in niobium films.

3.2.2 Growth of thin indium oxide films

Growth of thin films of amorphous indium oxide was investigated as an alternative to niobium-silicon for use in superconducting nanowires. This is due to the reporting of observed QPS effects in a recent Nature paper [62] as well as possible granularity issues in niobium-silicon films grown so far.

Films were grown using a three inch indium oxide sputter target. Films were initially sputtered at 300 W with a five minute presputter and five minute sputter time. Partial oxygen pressures of zero, five and ten percent were used to investigate the effect of oxygen incorporation on the amorphous nature of the film and Tc. Ramping issues caused cracking of the target after three runs, so future films were sputtered at a lower power with a slower ramp rate to preserve the target for longer.

3.2.2.1 Structural analysis of indium oxide films

XRD analysis was used to determine the structure of the films grown. Figs. 3.12, 3.13 and 3.14 shows that for the 300 W sputtering recipes used, the films remain polycrystalline and not amorphous. It appears that the films are more amorphous with oxygen incorporation, an oxygen partial pressure of five percent producing the lowest peaks.

Further films were not measured with XRD as the other properties of the films were found to be unsuitable for QPS applications as described in the next section.

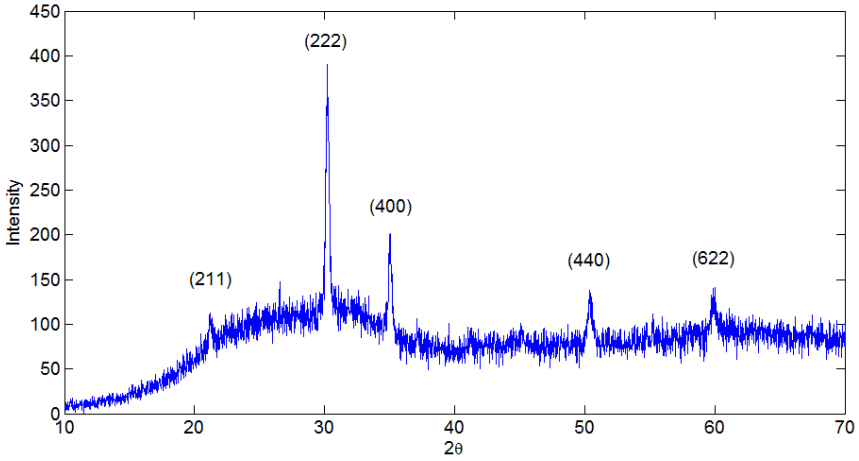

FIGURE 3.12: XRD for In_2O_3 with no oxygen partial pressure.

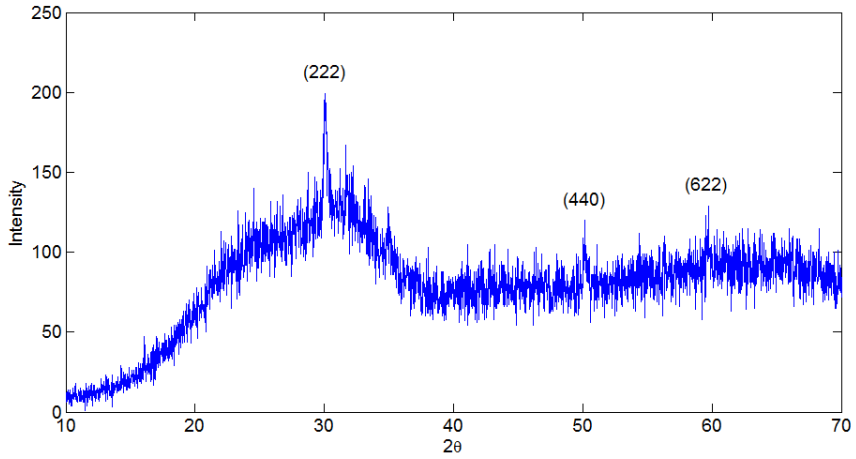

FIGURE 3.13: XRD for In_2O_3 with 5% oxygen partial pressure.

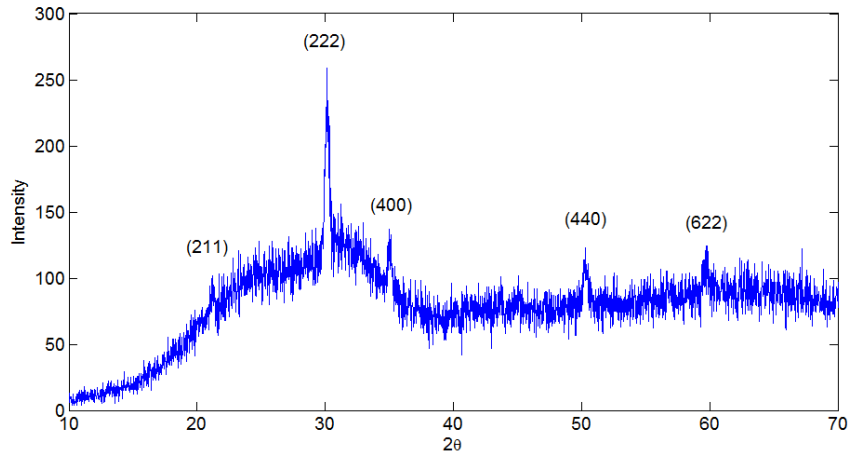

FIGURE 3.14: XRD for In_2O_3 with 10% oxygen partial pressure.

3.2.2.2 Variation of resistance with temperature

Amorphous indium oxide films are expected to have a T_c in the range of 2-3 K. The above films and several further generations were cooled in a physical properties measurement system (PPMS) to see if a superconducting transition could be observed. It was found that for films with below a 5% oxygen pressure the films were largely invariant to temperature and showed no sign of a superconducting or insulating transition. Films grown with a higher oxygen partial pressure, or with a lower sputter power to increase granularity, were found to be extremely insulating and quickly became too resistive for measurement. They were again showed no superconducting transition.

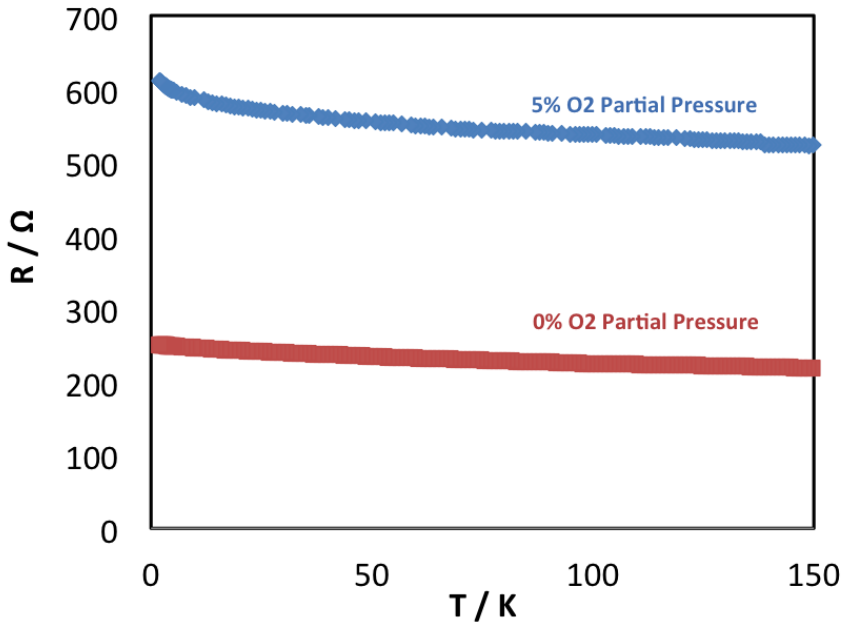

FIGURE 3.15: Resistance against temperature for indium oxide films grown with a sputter power of 300 W and 0 % and 5 % O_2 partial pressure.

It was concluded that it was not feasible to grow indium oxide in the sputter system as an amorphous film with a measurable T_c could not be produced. As the most common growth system used in the literature (e-beam evaporation) was not available it was decided that alternative materials should be used.

3.2.3 Growth of niobium nitride films

As the indium oxide films were found to be too insulating for use in QPS circuits, a different material was required. Niobium nitride was chosen due to its high T_c, enabling circuit characterisation in liquid helium as opposed to a dilution fridge, and its proven

demonstration of QPS effects in the literature [63]. Niobium nitride films were created by sputtering a niobium target with a 50:50 mix of Ar and N_2 gas. This produced a material with a high T_c in bulk (13.5 K) and high sheet resistance, this made it an ideal candidate for the development of QPS nanowires.

3.3 Fabricating minimum width nanowires

For use in a QPS circuit, nanowires of as small dimensions as possible were required. This is due to the need of the cross sectional area of the wire to be smaller than the coherence length of the material. If the cross section was larger than this then when a phase-slip event occurs there would still be a preferable current path around the area with a now finite resistance.

A variety of methods were tried over the course of the project to push the wire dimensions down further, the successes and failures of each of these is highlighted below.

3.3.1 Fabricating nanowires using lift-off method

Lift-off was the first method attempted for the fabrication of nanowires. A positive e-beam resist (PMMA 950 A2) was spun onto a substrate, then an EBL is used to pattern the surface. The resist will be removed from wherever it is exposed during development. The sample then has the chosen material deposited onto it. After this the remaining resist is lifted off in a solvent (1165 was used for all lift-off processing) to leave just the exposed pattern. See also section 2.1.3 for more detail on the photolithography process.

3.3.1.1 Lilypadding of niobium-silicon nanowires

Once fabricated, the nanowires were examined using an SEM to determined if the structure was uniform. It was found that a lilypadding effect was seen as shown in Figs. 3.16 and 3.17. This is where sputtered or evaporated material on the resist walls, deposited after the lithography stage, remains attached to the design. This is due to insufficient undercut in the resist layer, meaning there is no break between material deposited on the substrate and the resist. When the resist is removed this material will fold over the edges of the design, causing the lilypad effect.

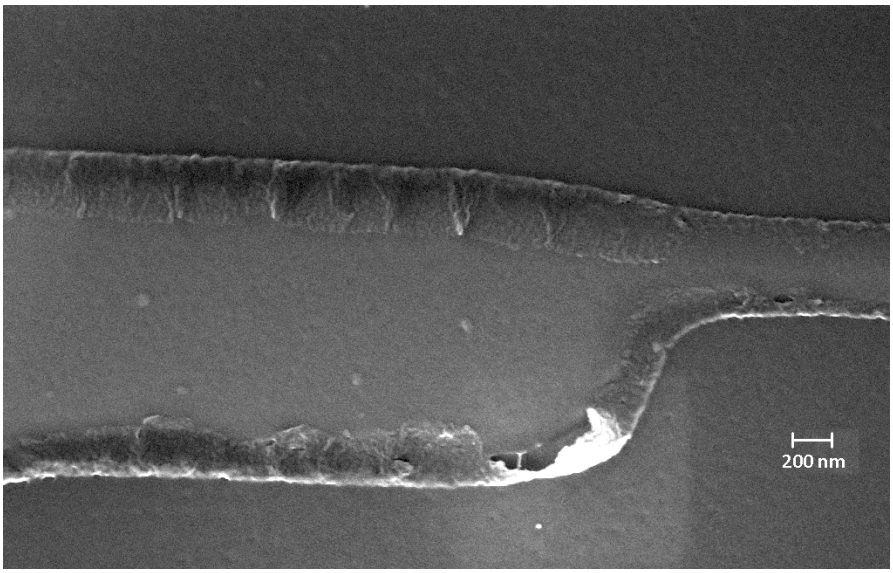

FIGURE 3.16: Lily padding effect on fabricated niobium-silicon inductor.

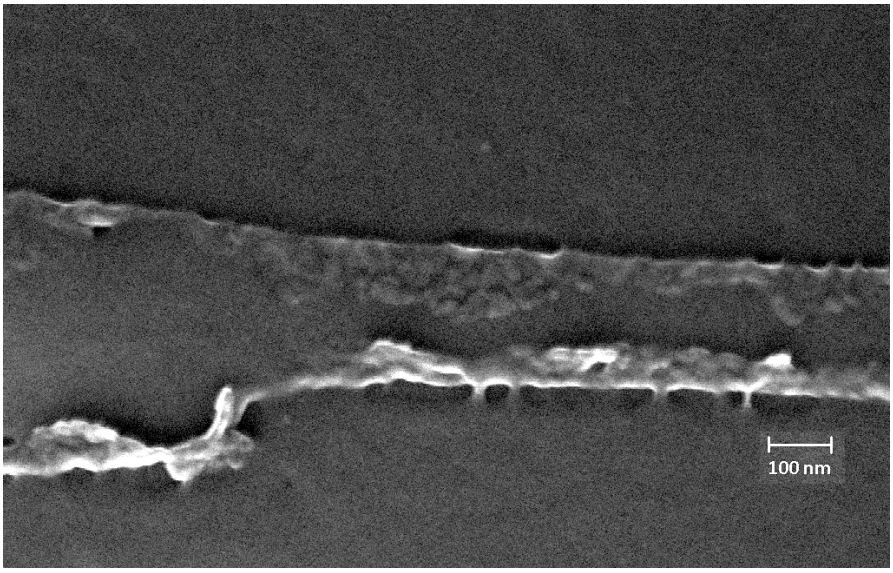

FIGURE 3.17: Lily padding effect on fabricated niobium-silicon nanowire.

By reducing the thickness of the resist from 300 nm to 100 nm it is possible to reduce the size of these lilypads from near 100 nm to around 20 nm (Fig. 3.18).

One way to try and eliminate lilypadding altogether is by using a bilayer resist. This consist of a thin layer of low density PPMA, with a thin layer of high density PMMA on top. When the PPMA is developed, the low density layer will be eroded more than the high density layer. This will create a larger undercut than a single layer of PMMA, stopping the lilypadding altogether.

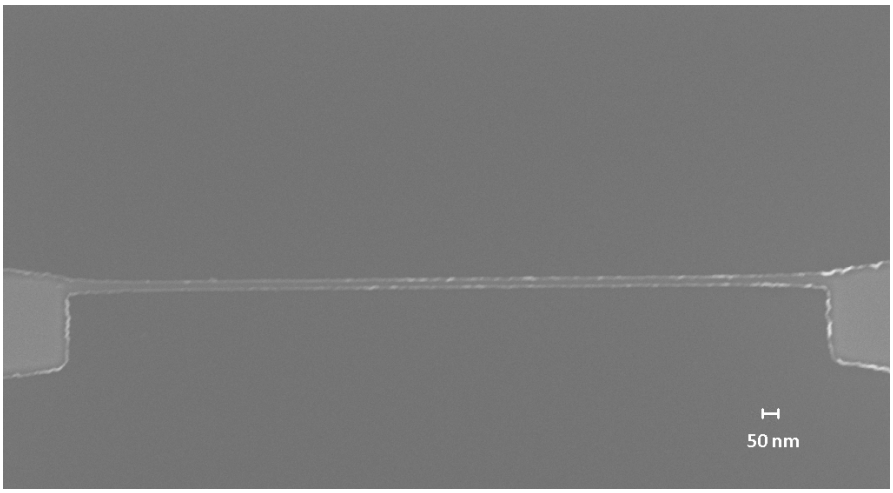

FIGURE 3.18: Reduced lilypadding on a 60 nm nanowire created with a resist layer 100 nm thick.

To create a bilayer 450 PMMA A2 was deposited with a spin speed of 4000 rpm, after baking a second resist layer of 950 PMMA A2 was added at a spin speed of 4000 RMP. This created a bilayer with low and high density resist layers of 50 nm each. First attempts at using a bilayer produced a lilypad effect similar to that for 100 nm single layer PPMA. It is possible that the lack of directionality of the sputtering technique is still causing the PMMA side walls to be coated, despite the undercut. To solve this a thicker low density layer was tried. However, resulting nanowires were considerably wider as the resolution achievable is decreased as the resist is thickened. As the end goal was for nanowires of 20 nm or less it was impractical to continue using a thick resist layer.

Next the acceleration voltage was increased from 10 KeV to 30 KeV as this should give the incident electrons enough energy to pass through the resist to the substrate, this means exposure is caused by backscattered electrons instead of electrons scattered inside the resist. This should increase the resolution and ensure the underlayer is exposed more than the top layer. A range of development times and doses were used to see if any improvement could be made.

Fig. 3.19 and Fig. 3.20 show that it is hard to achieve nanowires with widths of less than 40 nm using the dual layer resist. The lilypads were still consitantly around 20 nm in width, with only the 60 second development creating lilypads of less than this. Unfortunately, the 60 second development corresponded with some of the broadest nanowires. The reason for such large nanowires is likely to be because the acceleration voltage is still quite low at 30keV. This means electrons are still being scattered in the resist, meaning a broadening of features. This will also cause a less significant undercut meaning the side walls will still be coated during sputtering. Typically acceleration voltages of

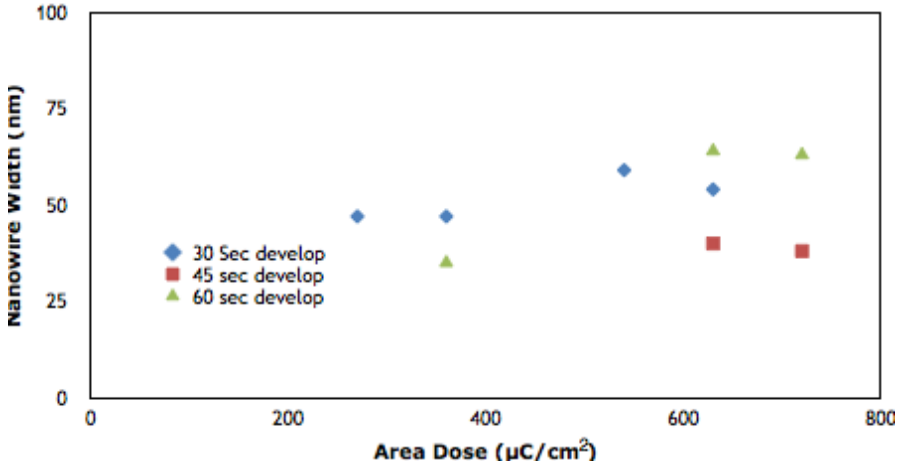

FIGURE 3.19: Nanowire width against area dose with different development times. All wires were linewidth exposures at 30 keV with a 20 μm aperture and a 2 minute ash prior to sputtering.

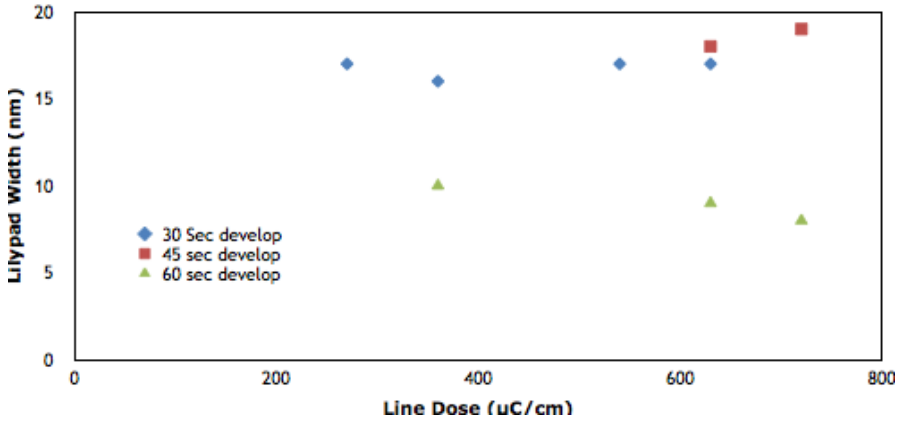

FIGURE 3.20: Lilypad width against area dose with different development times. All wires were linewidth exposures at 30 keV with a 20 μm aperture and a 2 minute ash prior to sputtering.

50-100 keV are used for resists of this thickness. Unfortunately the Raith-150 system cannot produce acceleration voltages this high, meaning a dual-layer resist is impractical for this machine.

3.3.1.2 Reducing nanowire dimensions

As well as trying to reduce the effect of lilypadding during lift-off, a parallel investigation tried to determine the optimum parameters for reducing the dimension of niobium-silicon nanowires made with this method. There are many factors that can affect the minimum dimension achievable using EBL. Acceleration voltage can play a key role. If a high acceleration voltage is used (50 to 100 eV) the electrons will have high energy

and pass straight through the resist, with backscattering from the substrate only. If lower acceleration voltages are used (2 to 20 eV) the electrons will tend to scatter in the resist material, increasing sensitivity during development and decreasing resolution [40]. For small features a thin resist layer (ideally less than 50nm) should be used for any acceleration voltage to prevent scattering causing a broadening of the pattern.

Electron dose can also have a large impact on the eventual feature size. If a pattern is underexposed then it could have irregularities or be resistant to the development process. This can cause resist material to remain after development causing poor adhesion during deposition. Overexposure can result in features being broader than designed. Ideally dose tests will be carried out for each new recipe to find the optimum dose (minimum dose that results in consistent pattern generation).

Line edge roughness can be a limiting factor in very small features (< 50 nm). In a resist such as PMMA aggregates of polymers can form, leading to areas of high and low polymer density. When developing, areas of high density in the sidewalls will be resistant to the development process as the dose is lower at the exposure edge. This leads to an unevenness at the edge of a pattern. This roughness can vary from a few nanometers to tens of nanometers depending on the resist used, causing an unacceptable deviation from design for narrow nanowires. Using a low molecular size resist such as Hydrogen silsequioxane (HSQ) should result in smaller aggregates and so smaller line edge roughness.

In all cases the sample was moved as close to the column chamber as possible (21.8 mm) to improve focus. This allowed a spot size of 15 nm or under to be achievable for all samples. In the first set of samples, the acceleration voltage was kept at a standard 10 kV, the resist layer was kept at a constant 100 nm for a single layer of 950 PMMA A2, and 50 nm each for a bilayer of 495 PMMA A2 and 950 PMMA A2. The aperture size was varied from 20 μm to 7.5 μm. It was found the a linewidth nanowire exposed with these parameters had a width after lift-off of 70 nm for a 20 μm aperture, and 60 nm for a 7.5 μm aperture. This is due to the fact that the electron beam width has been reduced. In traditional optics, a narrower aperture leads to a spreading of the light waves leaving it. However, in an electron beam, a magnetic field is used to focus the electrons, so a narrower aperture means a narrower beam profile. This means the beam will be less diffuse when it hits the sample, meaning backscattering of electrons is reduce. This will reduce the final width of the device.

3.3.2 Fabrication of nanowires by etch method

To avoid the issue associated with lift off described in the previous chapter, a new technique was used to try and reduce the nanowire dimensions further. Unlike the lift off method, where patterning is done before deposition in a positive resist, a film was first deposited and then patterned using a negative resist (HSQ). A subsequent etch phase is then used to create the nanowire pattern. This eliminates all defects caused by lilypadding as well as reducing the dimension of the wires further than the achievable HSQ exposure as the etch will occur across the entire surface of the wire, meaning width and thickness will be reduced the longer the wire is etched for.

3.3.2.1 Fabrication with HSQ and EBL exposure

HSQ was the resist chosen for fabricating nanowires with an etch method as it has a small line edge roughness and small molecular size, which can limit the minimum achievable width at these scales [40]. It is also proven to achieve the desired dimensions in the nanowire material of choice with a comparable EBL system [81].

HSQ 004 was used to create nanowire patterns on a niobium nitride surface. It was possible to spin a coating of this resist 40 nm thick, which when combined with a 30 kV electron beam allowed much narrower wires to be produced.

After development in MF26-A only the exposed HSQ pattern remains. This was then etched using a reactive ion etcher with CHF_3 and SF_6 the active gases used to strip material from the substrate. This left only the nanowire pattern in niobium nitride, onto which other circuit components could be added.

3.3.2.2 Fabrication with neon FIB mill

In order to reduce nanowire dimensions further still a neon focussed ion beam was used to trim the wires after fabrication. The reason was that circuit fabrication could be completed without risking damage to a fragile nanowire, while trimming with neon as opposed to gallium would minimise contaminants to the material which could potentially destroy superconductivity.

Using a neon beam it was possible to reduce nano wires of several hundred nanometers width to below 30 nm width in under one minute. This meant it was possible to process several nanowire samples in under one hour, making this technique very time effective for creating nanowires as well as increasing the yield of successful devices compared to a normal etch method.

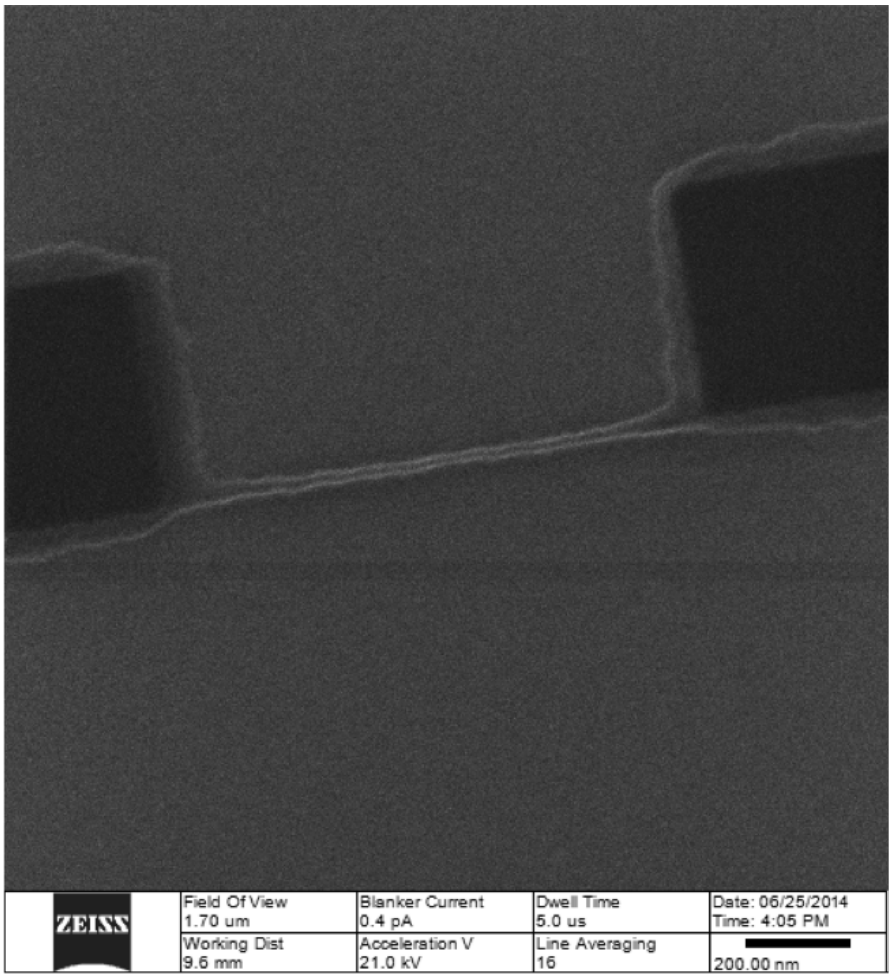

FIGURE 3.21: An example of a nanowire pattern in 40 nm thick HSQ after exposure to an electron beam and development.

3.4 Measurement of nanowires of varying width

Due to the various materials used during the project, as well as the different methods of fabrication, there were several attempts to characterise candidate nanowires for use in a quantum phase-slip circuit. Each of these produced different characteristics and different observed phenomena, as described below.

3.4.1 Measurement of niobium-silicon nanowires

The first material from which nanowires were fabricated was niobium silicon. Nanowires of this material were fabricated using lift-off from a pattern created by electron beam lithography. Gold contact patterns were then added using photolithography and the samples first characterised in liquid helium to check connectivity, and then measured to below T_c using a PPMS.

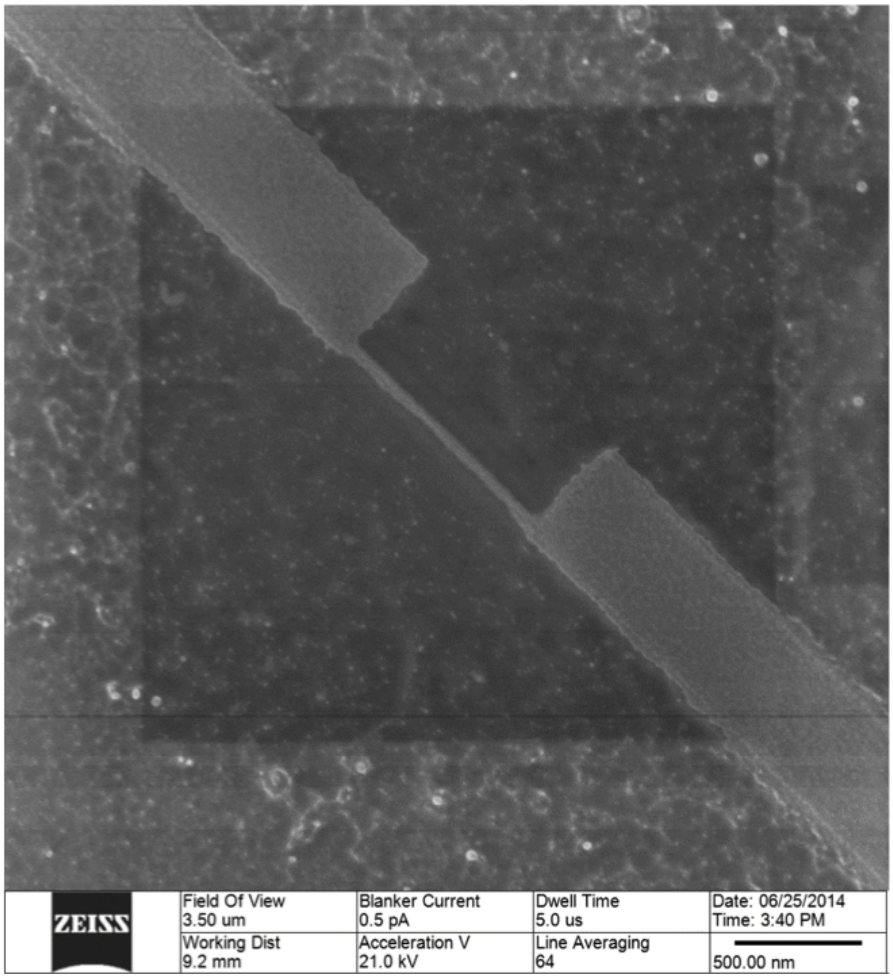

FIGURE 3.22: An example of a nanowire trimmed with a focussed neon beam after fabrication had been completed.

There were several issues that prevented a large scale fabrication of niobium-silicon wires. Firstly a large contact resistance was observed in early attempts to fabricate these wires. The details of how this issue was solved are in section 3.5.1. Once this problem was solved there were also large delays in the availability of the electron-beam lithography system needed to manufacture the wires, and the availability of a low temperature system to measure them below the transition temperature. These delays meant that by the time niobium-silicon wires could be manufactured reliably the focus of the research had moved to niobium nitride wires.

Although this means that data for niobium silicon wires is limited, there are still interesting conclusions to be drawn that helped to inform the decision to switch to niobium nitride wires.

3.4.1.1 Variation of resistance with temperature

Niobium silicon nanowires were fabricated using a lift-off method with electron-beam lithography. This enabled nanowires of a variety of widths to be fabricated from a 70 nm thick layer of niobium silicon. Fig. 3.23 shows the profile of a wire of width 2 μm and length 5 μm. This wire will have properties similar to that of the bulk material.

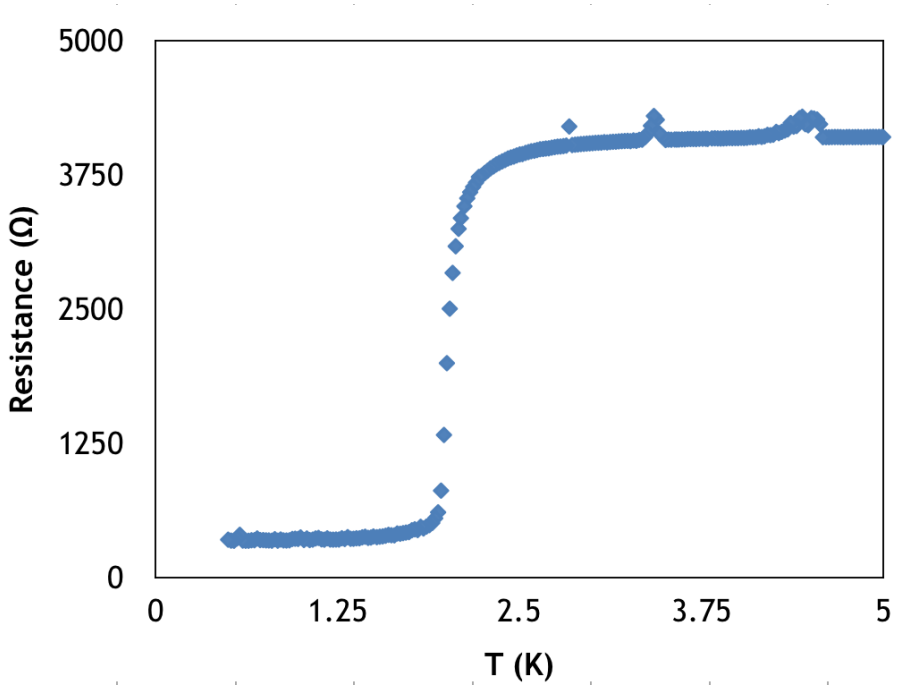

FIGURE 3.23: Variation of resistance against temperature for a NbSi nanowire of thickness 70 nm and 2 μm width.

The wire shows a T_c of 2 K, which is expected for this material. There is a residual resistance, but this can be entirely accounted for by the contact resistance between the niobium-silicon and gold contact layers and the resistance of the connecting pads. In bulk the material appears suitable for QPS applications. However, when the dimensions start to be constricted further as in Fig. 3.24 the material starts to appear less desirable.

Fig. 3.24 shows a nanowire with a width of 850 nm, length 5 μm and thickness 70 nm. Both wires have a breadth of transition of 0.3 K, however steps in the transition start to appear when the wire is narrowed. These are examined in more detail in the next section. Also, when dimensions were restricted further to measure wires in the range of 200 - 50 nm it was found that the wires rapidly became insulating, rapidly increasing outside of the range of the measurement equipment. This prevented study of the material in the range needed for QPS experiments and so other fabrication methods and material were studied to try and push down into the dimensions needed for a QPS circuit.

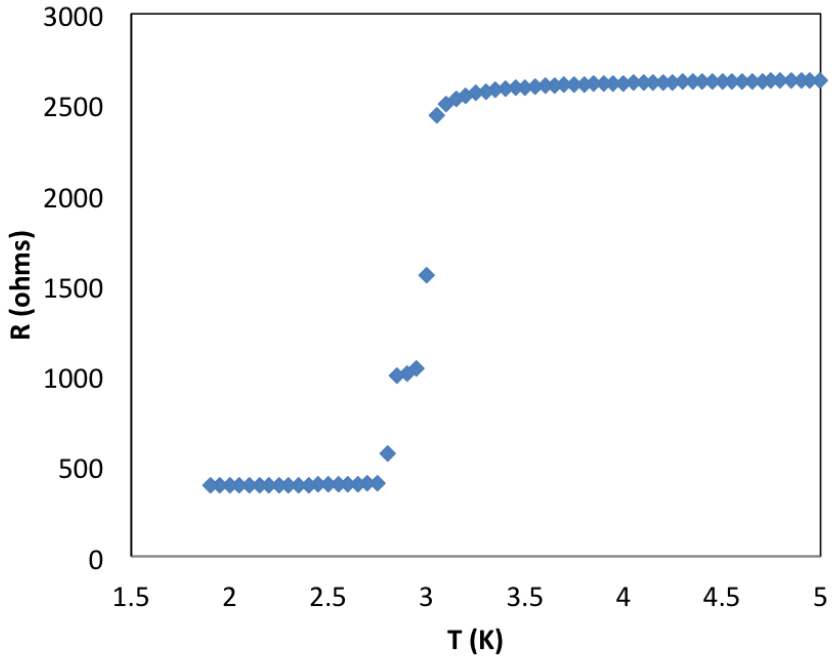

FIGURE 3.24: Variation of resistance against temperature for a NbSi nanowire of thickness 70 nm and 850 nm width.

3.4.1.2 Evidence of phase-slip centres

The wire from the above section that showed the most promising characteristics was investigated further to see what further conclusions could be drawn. The wire was cooled to just above the transition temperature and then subjected to current sweeps as the temperature was incrementally cooled to below the transition. This resulted in the steps visible in Fig. 3.25. It is worth noting that there is residual resistance visible for the nanowire, though this is entirely due to contributions from the contact resistance between niobium silicon and gold as well as the resistance of the gold connection pads.

The steps shown in the above figures can be attributed to a phenomenon known as phase-slip centers. This was first observed by Mayer [49] in tin whiskers and then described by Skocpol, Beasley and Tinkham [64]. This effect is linked to imhomogeinities in the superconducting wire. One section of the wire will have a lower critical current than the rest of the wire. As the current is raised to this critical current that section of the wire will enter the normal state. As the current is raised further more of these normal states will emerge, until the critical current for the pure superconductor is reached, at which point the whole wire enters the normal state. As the temperature is lowered further below T_c the critical current will be raised for more of the inhomogeneous areas, so the effect will become less pronounced.

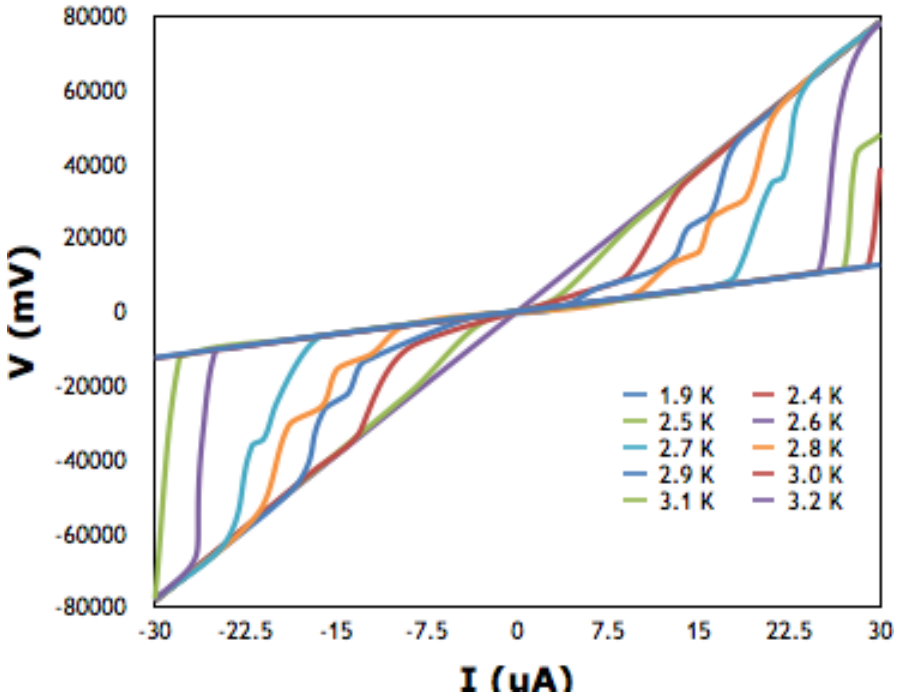

FIGURE 3.25: Variation of voltage with current for a NbSi nanowire of thickness 70 nm and 850 nm width.

The presence of these phase slip centres in the nanowire indicate that the wire is non-homogeneous. This, along with the low T_c of niobium silicon which makes characterisation difficult, was an instigator of the decision to move towards niobium nitride as the material to use for a QPS nanowire.

3.4.2 Measurement of niobium nitride nanowires

After measurement of niobium-silicon wires it was decided that the nanowire material should be switched to niobium nitride. This was due to the impracticality of waiting for time on a low temperature system to measure each device iteration, when measurements could be done immediately in liquid helium for a material with a higher Tc. It was found that niobium nitride could be easily grown in the SVS sputterer with an argon and nitrogen gas mix and a niobium target.

Several generations of niobium nitride nano wires were created with a HSQ and reactive ion etch fabrication method. Gold contacts were then added to the wires using photolithography and sputtered gold.

3.4.2.1 Variation of resistance with temperature

After the nano wires had been prepared for measurement four point resistance measurements were made as the wires were cooled in liquid helium. A dc bias of 500 nA was used for all measurements.

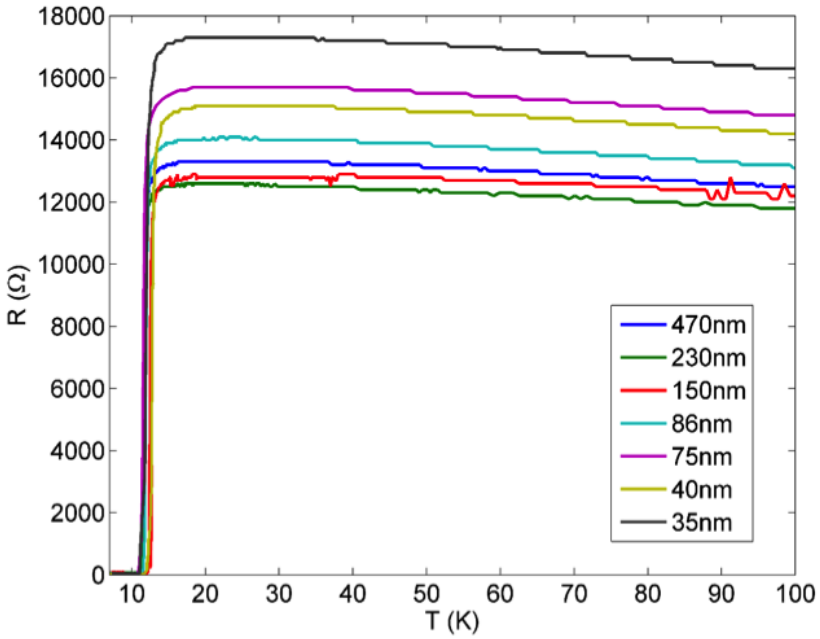

FIGURE 3.26: Variation in resistance with width for niobium nitride nanowires of 20 nm thickness, measured with a 500 nA dc current.

Fig. 3.26 shows the results for wires of various widths. All wires had a critical length of 1μm and a total length of 55μm. After the critical length, for which the widths are recorded on the graph, the wires had 4μm at 500 nm width and 50μm of 1μm width. The results show that there is generally an increase in the measured resistance as the critical width decreases. However, there are some wires that go against this trend. It is possible that they have been formed on areas of the chip with a higher than expected nitrogen concentration, suggesting non uniformity in the deposition. It is also possible that there is variation in the contact made during fabrication, or during measurement, to explain these discrepancies.

3.4.2.2 Current-Voltage Relationship

As well as measuring the resistance as a function of temperature, the critical current of the wires below the superconducting transition was also measured. Fig. 3.27 shows the

transitions of NbN wires of various widths. These wires were cooled to 4.2 K in liquid helium and then a series of current and voltage sweeps were preformed on each wire.

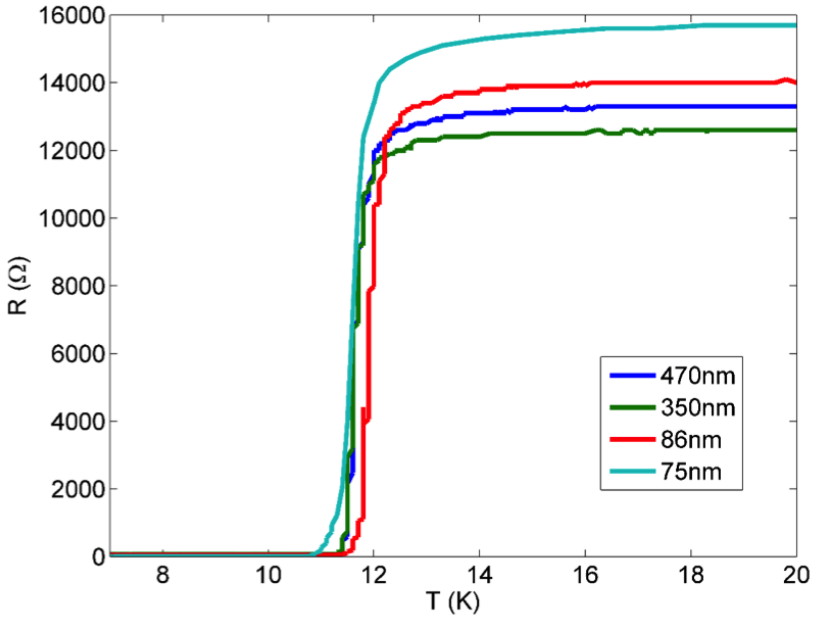

FIGURE 3.27: Variation in resistance with width for niobium nitride nanowires of 20 nm thickness, measured with a 500 nA dc current.

Fig. 3.28 shows the current against voltage relationship for each of these wires at low gain, allowing a maximum range of current to be measured. It shows that there are several stages of retrapping that occur as the current is cycled through the full positive and negative range. This could be due to the formation of phase-slip centres in areas of inhomogeity in the sample [56]. It was found that these curves were traced each time the current cycled, showing a lack of hysteresis in the wires.

Fig. 3.29 shows the high gain current sweeps. This allows the critical current to be estimated. It shows that while the normal state resistance did not follow a predictable trend across all wires, the critical current was higher for wires with larger widths.

3.4.2.3 Effect of neon mill

The effect of milling the wires with a neon beam was investigated as this was expected to be the means of fabricating a wire of dimensions sufficiently small so that quantum phase slips would be observable.

Fig. 3.30 shows the variation of resistance with temperature around the critical temperature for a wire before and after milling with a neon focussed ion beam. It shows

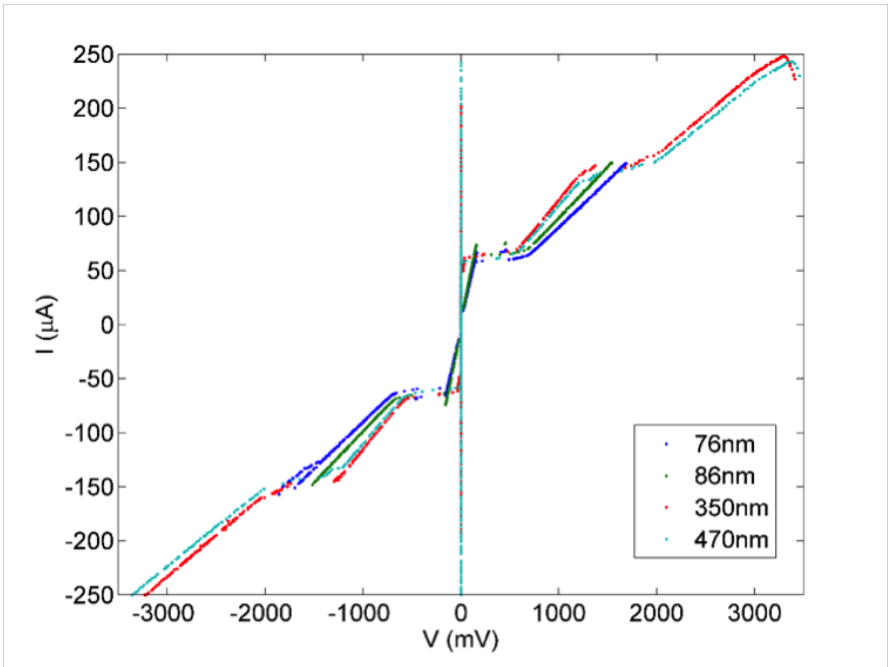

FIGURE 3.28: Variation in voltage with current for niobium nitride nanowires of 20 nm thickness at low gain.

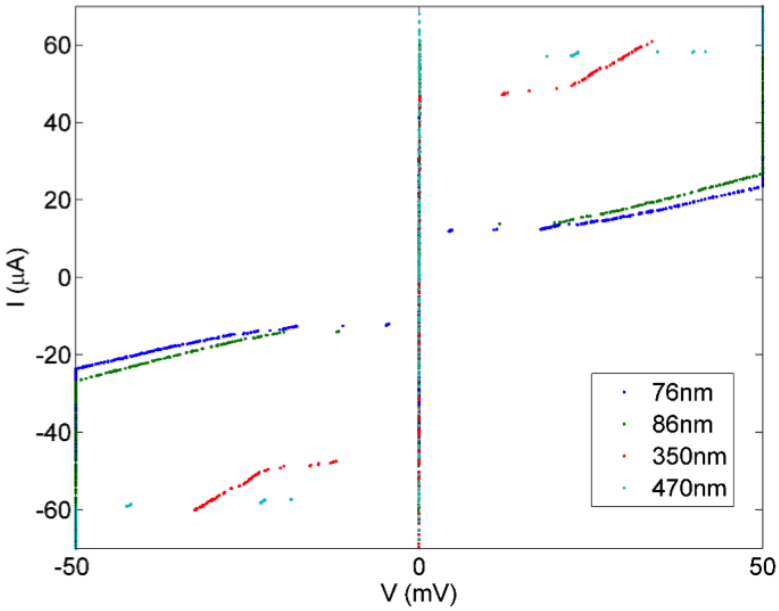

FIGURE 3.29: Variation in voltage with current for niobium nitride nanowires of 20 nm thickness at high gain.

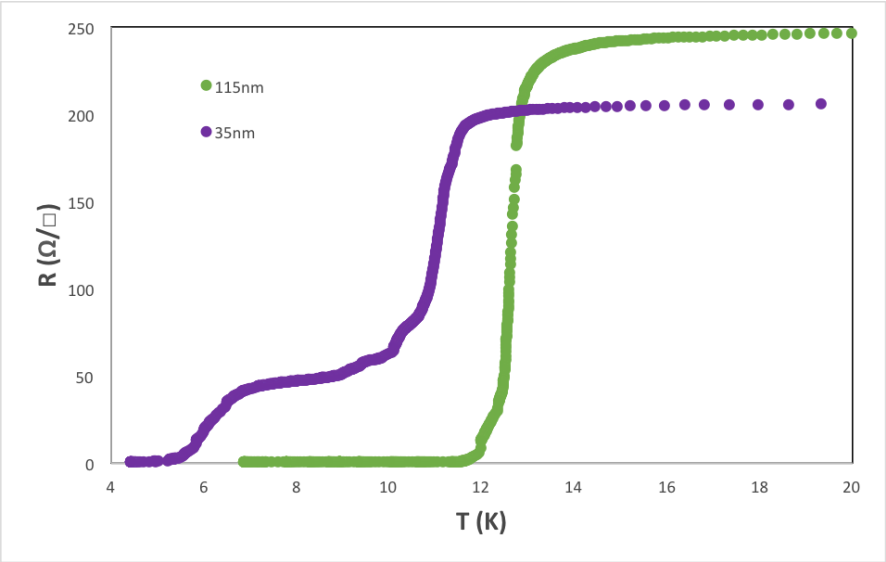

FIGURE 3.30: Variation in resistance with width for a niobium nitride nanowire of 20 nm thickness before and after mill with a neon beam, measured with a 500 nA dc current.

that although the wire is still superconducting there are consequences to the mill. The transition has been significantly broadened and shows evidence of impurities in the material. This could be due to implantation of carbon or even neon during the mill process. Although it was hoped that there would be significantly less impurities added than by a gallium beam, it appears that contamination is still occurring.

3.5 Fabrication of a QPS circuit

In order to construct the quantum phase-slip circuit proposed by Mooij [12] a thin nanowire must be connected to an inductor and series resistors. The following chapter is a description of current attempts to fabricate such a circuit.

3.5.1 Contact resistance of QPS components

When two materials meet, band-structure incompatibility and Fermi-velocity mismatch lead to an electrical contact resistance even for a perfect interface. Impurities, unevenness in each surface and mismatch between the lattice structures will cause voids and defects at the interface, and these will also contribute to the electrical contact resistance [50]. Minimising this contact resistance is one of the main practical challenges in fabricating multi-layered on-chip circuits. We have therefore investigated interfaces

between chromium oxide and other materials. We report on tests of niobium-silicon-to-chromium-oxide interfaces; these are relevant in the preparation of these resistors for use in a quantum phase-slip circuit in which the thin-film resistors must be electrically connected to niobium-silicon nanowires fabricated by multi-stage electron-beam lithography. We also present results of tests of chromium oxide-to-gold interfaces.

When connecting chromium oxide resistors to niobium-silicon nanowires in a QPS circuit, there are several possible methods to use. Direct connection of the components may be used by overlapping the components during deposition; this has the advantage of minimising the number of fabrication steps necessary. An alternative is to use an inert non-oxidising interlayer, such as gold, to connect the two. This might be appropriate if direct contact would result in too high a contact resistance.

In order to determine whether QPS nanowires could be connected in series to chromium oxide resistors without a large contact resistance, the contact resistance of the interface between chromium oxide and niobium-silicon was investigated. A transmission-line model test pattern was used to determine the contact resistance [6]. This model pattern consists of a series of pads of one material spaced apart by varying distances overlaid by a strip of another material (Fig. 3.31). The resistance between any two of these pads is $R \simeq 2R_{contact} + R_{strip}$, where $R_{contact}$ is the contact resistance between the pad and the strip $R_{strip} = r_{strip}\,D$ is the resistance of the strip material, r_{strip} is the resistance per unit length of the strip material and D is the length of strip between the two pads. Two-point measurements are performed for each pad combination and the known resistance of the pads is subtracted from this value in order to determine R. The resistance of the pads was determined by calculating the number of squares of material on the pad and multiplying this by the measured low temperature sheet resistance. On a plot of R against D, the $D = 0$ intercept conveniently gives the contact resistance.

The transmission-line model test patterns were fabricated using photolithography. Initially niobium-silicon was used as the pad material and chromium oxide was used as the strip material. First, a pattern of niobium-silicon pads was created using lift-off. Niobium-silicon pads were co-deposited using a 2" Nb target and a 2" Si target. Silicon was sputtered at 150 W while niobium was simultaneously deposited at 75 W, using a sputter time of five minutes, leading to a film with a composition of $Nb_{0.2}Si_{0.8}$, as measured using wavelength-dispersive spectroscopy, and a thickness of 70 nm, confirmed with a Dektak thickness profiler.

After lift-off, a second lift-off mask and chromium oxide sputter deposition were used to produce, after a second lift-off, a chromium oxide strip with a mass ratio of around 0.37 O/Cr by using the same oxygen partial pressure as for the 0.37 O/Cr chromium oxide film produced in section 3.1. The area of each niobium-silicon-to-chromium-oxide contact

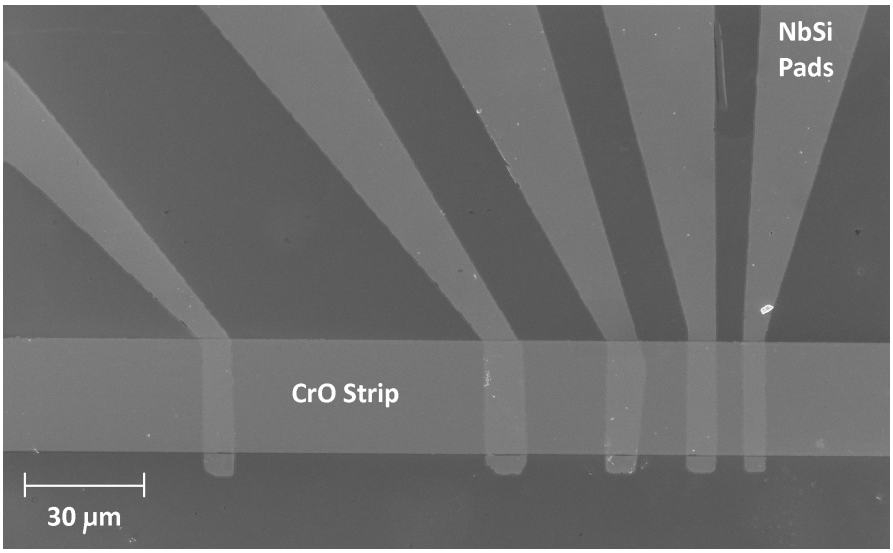

FIGURE 3.31: Optical image of a contact-resistance test pattern fabricated with photolithography. Niobium-silicon pads of width 5 μm ($\pm$1 μm) are in contact with a chromium oxide strip of width 30 μm.

was $5\times30\,\mu\mathrm{m}^2$. Aluminium bond wires were connected from the sample pads to copper pads that led to the measurement equipment. Two-terminal resistance measurements were made in the range $\pm10\mu$A between every pad combination at 4.2 K. The measured resistance is dominated by the contact resistance and resistance of the strip.

Fig. 3.32(a) shows the variation of the two-terminal resistance as a function of the distance between the pads for the niobium-silicon-to-chromium-oxide interfaces. $R_{contact}$ is 22 kΩ, implying a large specific contact resistivity of 65 mΩcm^2 (6.5 M$\Omega\mu$m^2). This contact resistance is around the same value as the chromium-oxide resistance for a contact area of a few square microns, and therefore would be too high for use in fabrication of a circuit for QPS current-standard experiments.

Utilising a gold interlayer is a potential solution to this problem; we therefore investigated the contact resistance between chromium oxide and gold. To produce gold contact pads, a 10 nm chromium adhesion layer, and afterwards a 40 nm gold layer, were thermally evaporated and then patterned using a positive resist and wet-etch method. The chromium oxide strip was then added, as before, using sputtering and a lift-off process. Fig. 3.32 (b) shows that the contact resistance of gold to chromium oxide was 48 Ω, implying a specific contact resistivity of 0.15 mΩcm^2 (15 k$\Omega\mu$m^2). This is several orders of magnitude less than the contact resistance between niobium-silicon and chromium oxide. By using gold as a intermediate layer, the contact resistance at interfaces between different materials can therefore be significantly reduced.

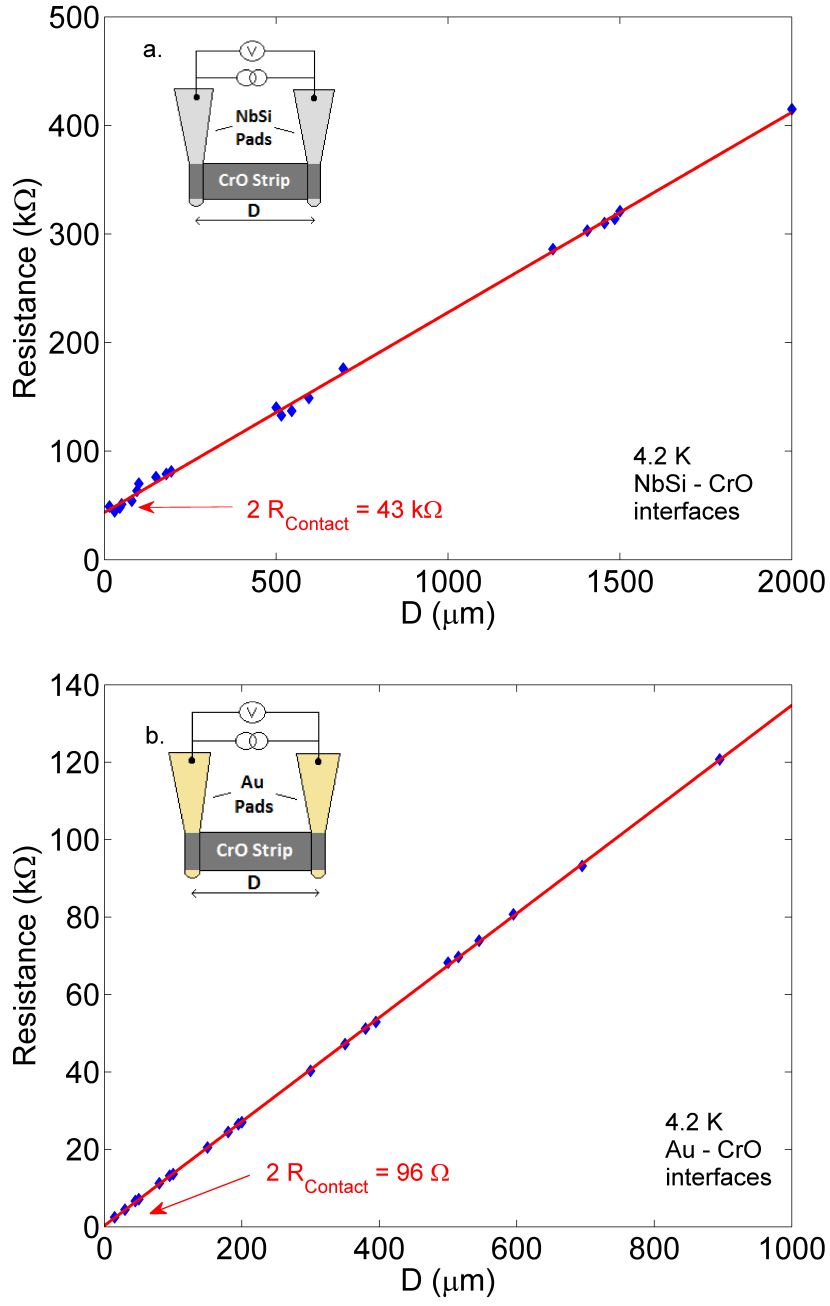

FIGURE 3.32: (a). Variation of two-terminal contact resistance at 4.2 K with distance between contacts for a contact test pattern of NbSi (pads) and chromium oxide (strip). (b). Variation of two-terminal contact resistance with distance between contacts for a contact test pattern of gold (pads) and chromium oxide (strip). (Inset). Experimental set-up for the two-terminal measurements of each pair of pads.

3.5.2 Step coverage in circuit fabrication

There were several issues that arose during fabrication that caused a rethink of the design process. The first of these was step coverage between different components, first noticed during experiments to determine the contact resistance between chromium oxide and niobium-silicon. If the two materials are of comparable thickness, then a break can appear when one layer is stacked on top of the other, as shown in Figs. 3.33 and 3.34. This can in turn cause a dramatic increase in contact resistance between the two layers as the existing current channels are disrupted.

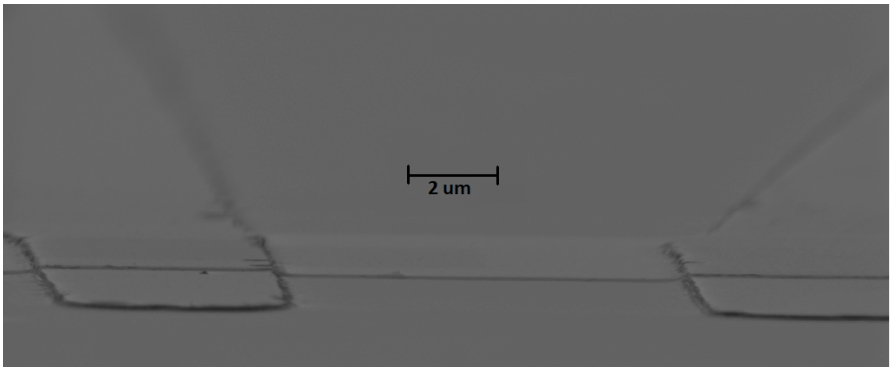

FIGURE 3.33: Step issues arrising between niobium-silicon and chromium oxide layers.

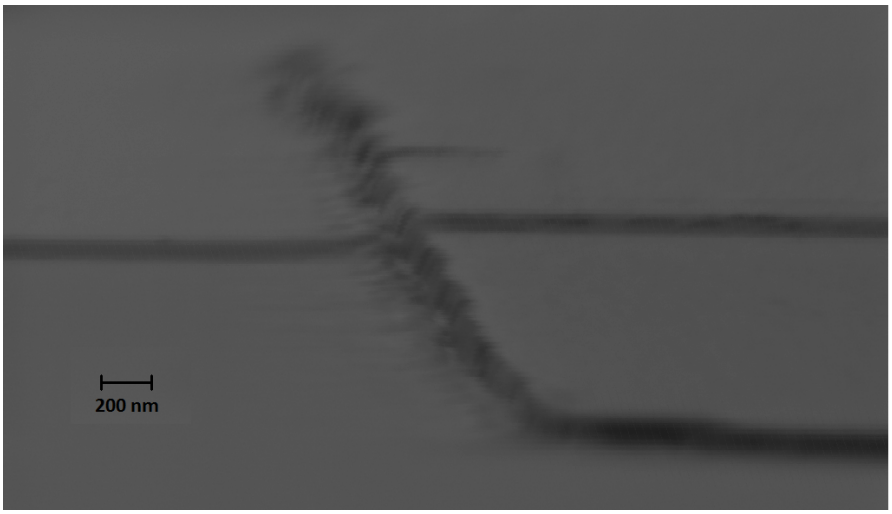

FIGURE 3.34: Close up of step issues.

This problem was solved by creating a thin layer of gold (12 -15 nm) to which the other components, which are thicker, can connect to without making direct contact to each other. This allows a continuous film without a break, as well as reducing the contact resistance through gold contacts.

For the gold and chromium oxide layers sputter deposition was used to produce the components as this minimises the chance of step coverage problems. As each of these layers required a resist layer it was important to ensure a clean surface to sputter onto. Ashing before sputtering is an option; however the layers are quite thin and so could be destroyed. It is also possible to recontaminate the surface before sputtering as oxidation can occur shortly after the layer is removed from vacuum.

A preferable option was to mill the surface in situ before sputtering as the layer will not leave vacuum between the mill and sputtering stages, reducing the risk of contamination. This was achieved by sputtering the surface of the sample with argon plasma while rotating, without exposure to the material targets. This created a suitable milling rate for all the materials used, with the advantage of taking place under vacuum, which reduces the risk of surface oxidation between the cleaning and sputtering phases. Table 3.2 shows the mill rates for the materials used for circuit fabrication. Measurements made by creating a film of each material and then masking off a section during sputtering. A Dektak surface profiler was then used to measure the amount of each material removed by the argon mill.

Material	Mill Rate (nm/min)
S1805	30
LOR3A	22
Exposed HSQ	2.5
Nb	1
CrO	1
NbN	3.5

TABLE 3.2: Mill rates for various materials used in the QPS circuit fabrication. Materials were exposed to a argon plasma with 100W RF power for five minutes and the mill rates measured and averaged.

3.5.3 Circuit Design

The large contact resistance of niobium-silicon to chromium oxide means a gold interlayer must be used to connect the circuit elements together. In order to achieve an interlayer, a series of gold contacts of 5x30 μm were created, linking to wire bonding pads of 200x300 μm. Two patterns were created with connections to all four contact pads to allow for characterisation of each individual component, with the remaining patterns with only external connections on the two outer pads, to prevent parasitic capacitances caused by these links (section 3.5.5).

Fig. 3.35 shows a close up of one of the circuit designs. The nanowire (cyan) widens to larger areas which act as the inductor. This is connected in series to two thin film resistors (green). Also shown are the EBL representation of the gold contacts (blue).

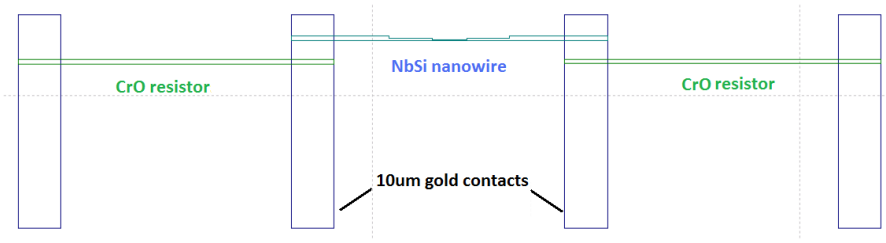

FIGURE 3.35: View of one of the QPS circuits to be fabricated, showing a nanowire leading to thicker inductor sections, connected to two series resistors.

3.5.4 Capacitance issues in thin film resistors

The results in the section 3.1 above have shown that chromium oxide is a good potential resistor candidate. There are, however, other factors that have to be considered when designing and fabricating these component. One such factor, contact resistance to other components, has already been described (section 3.5.1); another factor, capacitance from the resistor to ground via the substrate, will be dealt with in this section.

Parasitic capacitances between the resistor and the substrate can become a substantial issue for high frequency circuits. In an ac circuit this can result in an unwanted coupling to the circuit components, or delayed circuit response at high frequencies [46, 47]. This effect is minimal in low frequency circuits, but in a high frequency circuit this current can be very large as the extra current needed is governed by the equation

$$i_{PC} = C_{PC}\frac{dv}{dt} \tag{3.1}$$

where C_{PC} is the parasitic capacitance. This means the impedance is no longer constant, but dependant on the frequency applied to the circuit.

$$Z = R - \frac{j}{wc} \tag{3.2}$$

Moreover, above a certain frequency, the cut-off frequency, the passage of current through the resistor will be halted entirely. An estimate of the value of the resistor capacitance, and the cut-off frequency this corresponds to, can be made for our resistors by comparing to similar resistors designed by Zorin [29] et al. Their measured value for the

capacitance per unit length of weakly oxidised chromium oxide resistors is $62\,\mathrm{aF}\mu\mathrm{m}^{-1}$. From the resistor dimensions we can then work out a capacitance per unit area $C_0 = 7.75\,\mathrm{fF}\mu\mathrm{m}^{-2}$. The capacitance for our chromium oxide resistors can be estimated by using the area of the resistor in contact with the substrate

$$C = C_0 \cdot A \tag{3.3}$$

where A is the resistor area given by the length (L) times the width (b). The cut-off frequency is given by the relation

$$f_c = \frac{1}{2\pi \cdot R \cdot C_0 \cdot L \cdot b} \tag{3.4}$$

where R is the resistance of the resistor. Using this equation the cut-off frequency of the original design of series resistors (L=55 μm, b=2 μm, R=25 kΩ at 4.2 K) was calculated to be 7.5 MHz. This is too low for QPS applications, where GHz frequency RF lines will be coupled to the circuit causing inductance to be unacceptably high. This means a redesign is needed to increase the cut-off frequency.

It was found that if a cut-off frequency of 10 GHz and a resistance value of 50 KΩ is required, then for a 100 nm wide wire the maximum length of the resistor material is 0.41 μm. Though this length can be slightly increased if the resistor width is reduced further, it still required a rethink on the original design of this circuit element to accommodate the reduced dimensions.

Another capacitance related issue for thin film resistors is Coulomb blockade. In non-continuous thin films, where the film is made up of isolated grains of material, the barrier between two grains can act as a tunnel junction that electrons will have to pass for conduction to continue [39]. This can be thought of as a capacitor with a dielectric material between the two terminals. This is primarily an issue in low-temperature circuits where tunnelling electrons will charge the capacitor with a characteristic voltage of

$$U_{CB} = e/C_{CB} \tag{3.5}$$

where C_{CB} is the blockade capacitance. Coulomb blockade effects become dominant for voltages below the value of U for which electrons will not have the energy to pass across the barrier, causing an increase in the resistance of the thin film resistor.

3.5.5 High Resistor values in QPS Devices

Fully integrated devices were fabricated with resistors made of 0.34 O/Cr mass ratio chromium oxide. It was found when these devices were measured at 30 mK that the resistor values were multiple GΩs. This meant that a very long wait time was needed between measurements to ensure equilibrium voltages were reached [82]. It had been expected that there would not be such a significant increase in resistance between the previously measured values at 4.2 K and the dilution fridge base temperature of 30 mK.

To predict what choice of material would be needed to create ideal resistor value at 30 mK the variable range hopping model was applied to films measured to 4.2 K to extrapolate the resistance at base temperature (section 3.1.5). Table 3.3 shows the calculated values for varying oxygen content films. The oxygen content has been expressed as a percentage of the argon gas used at time of deposition as the WDS data had not been obtained for all films.

Oxygen Content	R(4.2 K) (Ω)	R(30 mK) (Ω)
8%	219	340
9%	4.6×10^{4}	6.9×10^{4}
10%	9.9×10^{3}	3.2×10^{6}
11%	9.7×10^{4}	3.8×10^{15}
12%	7.6×10^{8}	6.6×10^{101}

TABLE 3.3: Calculated resistance values at 4.2 K and 30 mK for CrO films with varying oxygen content. Oxygen content is expressed as the percentage of oxygen gas, as a fraction of argon gas, introduced during deposition.

As the percentage increase in resistance for the lower oxygen content films was not enough to apply the variable range hopping model a simpler power law model was employed ($R = R_0 T^N$ where R_0 and N are constants determined by the fit). The data shows that although the resistance at 4.2 K was reasonable at room temperature for the 10% O_2 film (equivalent to 0.34 O/Cr mass ratio), at 30 mK it had reached too high a range for QPS measurements. Depending on the exact resistor dimensions a 8% or 9% film would be more appropriate.

Chapter 4

Conclusion

The research for this thesis looked at the steps needed to fabricate a quantum phase-slip circuit for use as a new current standard. In particular there were several areas explored; the fabrication of compact chromium oxide resistors and a detailed investigation of their properties, exploration of the design of a QPS circuit and how components should interact, investigation of the choice of material for a superconducting nanowire and investigation of the fabrication method needed to minimise the dimensions of a nanowire.

It was found that it was possible to control the low temperature resistance of chromium oxide films by increasing the oxygen pressure at the time of deposition, meaning chromium oxide films could be fabricated for a large resistance range of thin film resistors, from values in the hundreds of ohms to megaohms. These films were found to be amorphous when measured with XRD and displayed extremely low magnetoresistance (with a peak magnetic moment of $5{\times}10^{-3}$ μ_B per atom, compared to 2 μ_B per atom in bulk ferromagnetic Cr_2O_3).

The resistance values have been found to be tuneable and repeatable. It was possible to model the behaviour of the higher oxygen content films films using a variable range hopping model, allowing the low temperature resistance of these films to be predicted.

It was found that for fabrication of an on-chip circuit, gold, or a similarly low resistivity interlayer is needed to ensure a low contact resistance. The contact resistance of joining the chromium oxide resistors to gold or niobium-silicon could be measured using a transmission-line model and this revealed that a gold interlayer provided a much lower contact resistance than direct contact of the circuit components (a contact resistivity of $0.15\,\mathrm{m\Omega cm^2}$ for chromium oxide to gold compared to $65\,\mathrm{m\Omega cm^2}$ for chromium oxide to niobium silicon).

Quick oxidisation of the surface of the films also means careful consideration of the method of device manufacture and order of layers is needed. However results have indicated that after oxidisation, resistance values stay stable for many months after fabrication. It was also found that careful choice of oxygen content and resistor dimensions was needed to ensure a resistor in the right range could be created without causing shorting by parasitic capacitance when the circuit was coupled at high frequency. It was found that if a cut-off frequency of 10 GHz and a resistance value of 50 kΩ is required, then for a 100 nm wide wire the maximum length of the resistor material is 0.41 μm.

Several materials were investigated to test their suitability as a QPS nanowire. The initial candidate was niobium-silicon and while low temperature transitions were attained for this material the critical temperature was deemed too low for continued experimentation. Indium Oxide was investigated as a potential replacement due too its higher T_c and successful observation of coherent QPS by Astafiev et. al. Unfortunately attempts to recreate these films using a sputter system resulted in films that were too crystalline, with none of the insulator-superconductor transitions observed by other groups. Finally niobium nitride was investigated, this resulted in films with transitions observable in liquid helium which allowed for further development of a QPS circuit. This material was used for all later experiments.

Several methods were used to restrict nanowire dimensions. A lift-off method was first investigated. While this method was found to be effective for nanowires down to 100 nm, trying to restrict the dimensions further resulted in large defects in the wire, causing failure when measurements were attempted. Using HSQ and an RIE etch proved much more effective allowing restriction in width to tens of nanometers in niobium nitride. Finally, combining the HSQ fabrication with a neon mill resulted in the creation of wires below the coherence length of niobium nitride (30 nm), which made these wires suitable for QPS measurements.

This project concluded before full QPS circuits were created. However, the building blocks for these circuits have been fully investigated allowing for devices to be built following this research. Once test circuits have been successfully created using niobium-nitride nanowires, the devices should be cooled to 50 mK to look for signs of QPS action. Recently this work was taken a step further using the components optimised in this thesis resulting in 15 nm NbN nanowires being cooled to 350 mK with preservation of the superconducting transition and linear dc characteristics observed [83]. With the delivery of a new Helium-3 system to the group the lower temperature measurements to observe CQPS behaviour should be able to take place.

The final stage of the project is to couple the circuits to microwaves to look for signs of Shapiro steps in current. If these experiments are successful then it would be possible to

build a quantum current standard using the components investigated here. The results in this thesis have shown it is possible to grow novel thin film resistors that allow high resistance values to be reached, remain stable and operate at high frequency. This thesis has also shown that high quality NbN nanowires can be created and both components coupled in a device that remains stable a demonstrates desired characteristics at low temperature. The continuation of this work in the group as device characterisation moves into the QPS range will mean the work in this thesis will prove an important step in the move to a new quantum current standard.

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Appendix A

Published Article: Compact chromium oxide thin film resistors for use in nanoscale quantum circuits

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