Key Strategies for Safety-of-Life Receiver Development

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BIOGRAPHY

Manuel Cuntz received the diploma degree in electrical engineering in 2005 from the Technical University of Kaiserslautern. He joined the Institute of Communications and Navigation of DLR in 2006. His fields of research are satellite navigation receivers.

Holmer Denks received his diploma in electrical engineering and Communications from the University of Kiel, Germany, in 2002. He was involved in investigation and simulation of communications systems. In 2002 he joined the Institute of Communications and Navigation of the German Aerospace Center (DLR). Currently he works on simulations of Galileo signals.

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Achim Hornbostel received his engineer diploma and Ph.D. in electrical engineering from the University of Hannover in 1989 and 1995. He joined the German Aerospace Centre (DLR) in 1989, where he became member of staff at the Institute of Communications and Navigation in 2000 and is leading a research group on receivers and algorithms since 2005. He was involved in several projects for remote sensing, satellite communications and satellite navigation. His main activities are currently in signal propagation and receiver development. He is member of VDE/ITG and ION.

Andriy Konovaltsev received his engineer diploma and the Ph.D. degree in electrical engineering from Kharkov State Technical University of Radio Electronics, Ukraine in 1993 and 1996, correspondingly. He joined the Institute of Communications and Navigation of DLR in 2001. His research interests are in array processing for satellite navigation systems, signal processing algorithms for navigation receivers including synchronisation, multipath and radio interference mitigation.

Georg Buchner joined the Institute of Aeronautical Radio and Microwaves of the German Aerospace Center in 1976. Since then he is working as technician in the fields of antenna measurements and prototyping of antennas and electronic circuitry.

Achim Dreher received the Dipl.-Ing. (M.S.) degree from the Technische Universität Braunschweig, Germany, in 1983, and the Dr.-Ing. (Ph.D.) degree from the FernUniversität, Hagen, Germany, in 1992, both in electrical engineering. From 1983 to 1985, he was a Development Engineer with Rohde & Schwarz GmbH & Co. KG, München, Germany. From 1985 to 1992 he was a Research Assistant, and from 1992 to 1997, he was a Senior Research Engineer with the Department of electrical engineering, FernUniversität. Since 1997 he has been with the Institute of Communications and Navigation, German Aerospace Center (DLR), Oberpfaffenhofen, Germany, where he is currently Head of the Antenna Research Group. His current research interests include analytical and numerical techniques for conformal antennas and microwave structures, smart antennas for satellite communications and navigation, and antenna technology for radar applications. Dr. Dreher is Senior Member of IEEE.

Michael Meurer received the diploma and Ph.D. degrees in Electrical Engineering from the University of Kaiserslautern, Germany. After graduation in 1998, he joined the Research Group for Radio Communications at the University of Kaiserslautern, Germany, as a research engineer and, finally, senior key researcher and senior lecturer. Since 2005 Dr. Meurer has been an Associate Professor (Priv-Doz.) at the University of Kaiserslautern, Germany. Moreover, since 2006 Dr. Meurer is with the German Aerospace Center (DLR), Institute for Communications and Navigation, where he is the director of the Department for Navigation and responsible for performance issues concerning the satellite navigation system Galileo.

INTRODUCTION

It is well known from the open literature that interference is a serious threat for the new Galileo services especially in the E5 and E6 bands. In particular for the Safety-of–Life (SoL) applications like aviation high power pulsed radars and DMEs are a major concern.

To cope with such interference it is essential for the development of a SoL receiver to consider the impact of interference on each part of the receiving chain. For this reason a new project was launched by the Institute of Communications and Navigation of the German Aerospace Center (DLR). The aim of this project is to perform the necessary pre-development research as well as to develop, build and demonstrate an integrated SoL receiver system, which is robust against interference and multipath effects. Since array antennas with digital beamforming offer a very high potential for suppression of interference and multipath signals, the integration of an array antenna has been included in the receiver design from the early beginning of the project. Some of the most challenging tasks to achieve the project goal include:

- Development of antenna elements and arrays optimized for the reception of GPS and Galileo signals
- Design of robust front-ends suitable for multi-constellation multi-frequency reception with multiple antennas
- Robust and reliable calibration of the full analog receiving chain including antenna and front end
- Development and analysis of powerful interference detection and mitigation techniques enhanced for Galileo
- Development and analysis of algorithms for providing integrity for SoL applications by receiver autonomous or assisted strategies.

The proposed antenna array allows a polarization selective reception as well as adaptive nulling and sidelobe suppression. Through this, the impact of jamming and interference, as well as of multipath can be dramatically reduced.

The receiver demonstrator at the recent implementation stage consists of a planar 2x2 adaptive antenna array and a multichannel L1 GPS/Galileo navigation receiver. L1 was chosen here for demonstration purposes, in order to make use of GPS L1 signals, although interference is mainly expected at E5 and E6. In the further development the design will be extended to L1/E5 reception. The demonstrator is easily expandable to a 3x3 uniformly spaced rectangular array configuration, which is chosen as goal for the final implementation.

This paper gives an overview of the complete receiver architecture and the innovative key technologies utilized to ensure the high demands on robustness and reliability of SoL receivers. Especially sensitive but also highly robust multi-frequency reception requires novel innovative concepts which are presented in the paper.
The main parts of the demonstrator are shown in Fig. 1, where the user interface, the board containing the front-ends (left), and the 2x2 microstrip antenna array (right) are presented.

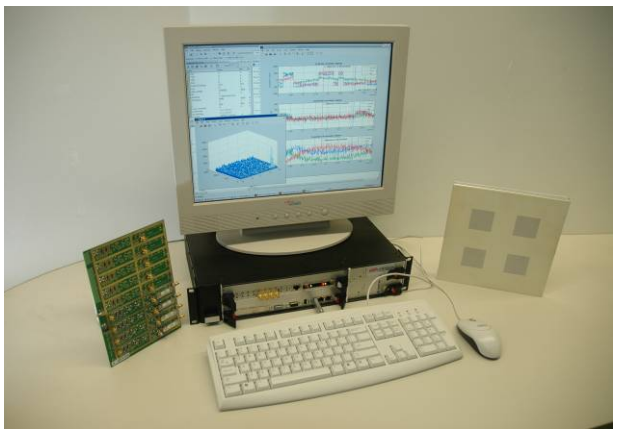

Fig. 1: main components of DLR's SoL receiver demonstrator

The first part of the paper describes the single antenna element and the design issues of the complete array. The second part is a discussion of the multi-channel front end utilized for the first implementation of the demonstrator. In the third part, the baseband digital receiver design, which is implemented in an FPGA in order to handle the high data rates of the ADCs, is discussed. After that, an overview of the software receiver, which processes the digital baseband signal records, is given. Subsequently the developed and implemented digital beam-forming as well as direction finding techniques are discussed.

1. ANTENNA ARRAY

I. SINGLE ANTENNA ELEMENT

Due to their low aerodynamic profile, ease of construction and low cost, the antennas of the microstrip type are very suitable for SoL applications, especially for the integration of the antenna in the bodyshell of aircrafts. Moreover, other passive circuits, such as 90°-hybrids and directional couplers can also be implemented in microstrip technology and directly integrated in the antenna, saving costs, weight and space.

In order to increase the beamwidth, the effective aperture of the antenna has to be reduced. For microstrip antennas, this can be achieved by using substrates with higher dielectric constants (ε_r), which is demonstrated in [1]. After that a compromise between broadening the radiation pattern and efficiency has been made, the stack-up of the proposed structure is presented in Fig. 2. The substrates composing the striplines have been selected to have different dielectric constants, so as to avoid the excitation of parallel-plate waves [2]. The square patch is protected by a radome located at the top of the multilayer structure, the slots are in the middle and the feeding system, which is composed of stubs and the 90°-hybrid, is at the bottom. The integration of the 90°-hybrid geometrically below the patch results in a compact design that is suitable for integration into arrays. The optimisation of the circular polarization purity of the antenna is an important strategy for the suppression of multipath signals. Several parameters are to consider for the optimization of this antenna in order to obtain a good matching inside the band of interest and a strong reflection outside of it. The lengths of the slots have been adjusted as a compromise between bandwidth and excitation of substrate waves (modes other than the parallel-plate mode) inside the stripline structure. The two stubs are used to match the input impedance of the antenna.

This antenna was fabricated with the dimensions given in Table II in [1]. The measured S-parameters of this antenna show that the impedance matching is good in the band of interest (see Fig. 3). Furthermore, the isolation between the two outputs is also good in this frequency region (1575.42 ± 7 MHz). The poor isolation for the other frequencies is the main factor governing the desired decrease in gain outside the band.

A curve showing the simulated behaviour of the gain with the frequency is presented in Fig. 4. One can see that the gain at the GSM region is approximately 15 dB below the level in the band of interest. The measured and computed gain patterns are shown in Fig. 5. During the electromagnetic analyses, which were done with Ansoft Designer [3], infinite ground planes and dielectric layers were considered. For this reason, the fields vanish for angles between 90° and 270° in the simulation results.

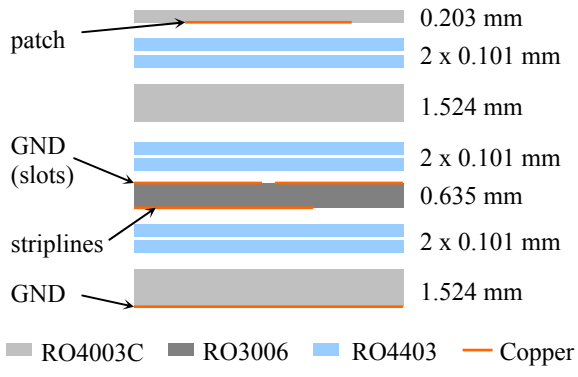

Fig. 2: Stack-up for the designed microstrip antenna

II. Antenna Array and the Integrated Calibration Network

Digital beamforming requires the received signals of each antenna element to be processed independently up to the analogue to digital conversion. Between the antenna and the analogue-to-digital converter (ADC), the signals are amplified, mixed and filtered using analogue devices. Since each analogue signal path does not present exactly the same characteristics in terms of total gain and phase, it is necessary to compensate for these unbalances. For this purpose, a directional coupler has been integrated at the outputs of each single antenna element and a power divider to distribute the calibration signal for the antennas has been developed. The calibration network and the directional couplers are integrated on the same layer, which is shown in Fig. 10. The locations of the SMD-resistors are indicated by red dashed circles. The four outputs of the single antennas are identified by black dashed circles. These are connected via SMP-connectors to the boards containing the low-noise amplifier (LNA), as sketched in Fig. 7. To minimize the possible cross-talking that could influence the accuracy of the calibration process, the calibration network is shielded with vias that are located along its lines. The amplitude and the phase at the four outputs of the calibration network have been measured and are shown in Fig. 7 and Fig. 8.

The receiver demonstrator at the recent implementation stage consists of a planar 2x2 adaptive antenna array and a multichannel L1 GPS/Galileo navigation receiver. It is easily expandable to a 3x3 uniformly spaced rectangular array configuration, which is chosen as goal for the current implementation.

A photo of the 2x2 array and a comparison between computed and measured radiation patterns are shown in and Fig. 11. Good agreement has been obtained between the measurements and the numerical predictions. The levels of the measured cross polarization component were much lower than the simulated ones. The computed far-fields have been obtained with Ansoft Designer under the assumption of infinite ground. The patterns shown in Fig. 11 have been obtained for the passive array only.

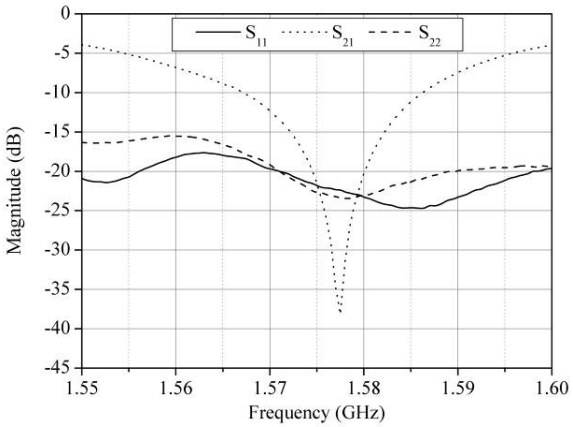

Fig. 3: Measured S-parameters

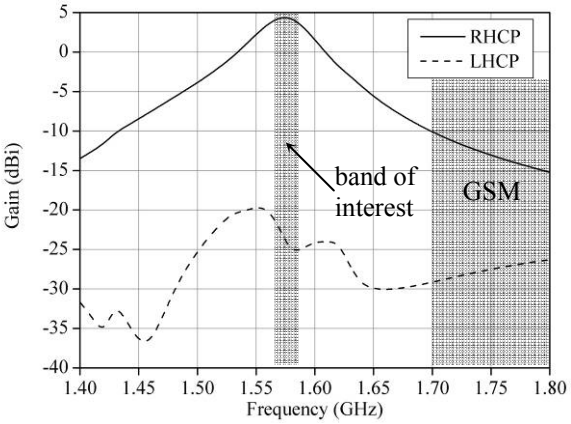

Fig. 4: Variation of the gain with the frequency with Port 2 terminated by a 50-Ω load (simulation)

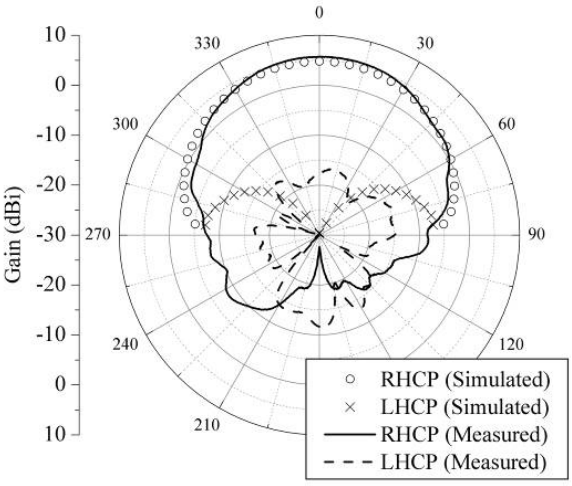

Fig. 5: Realized gain pattern at 1575 MHz

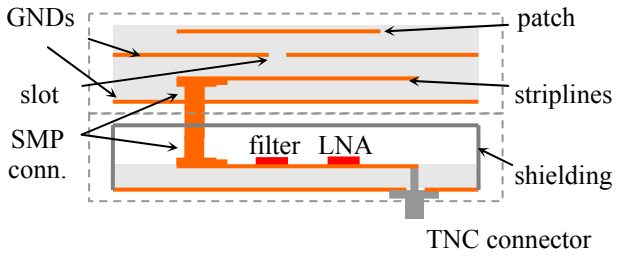

Fig. 6: Schematic cross-sectional view of the connection between the microstrip antennas and the microwave comp

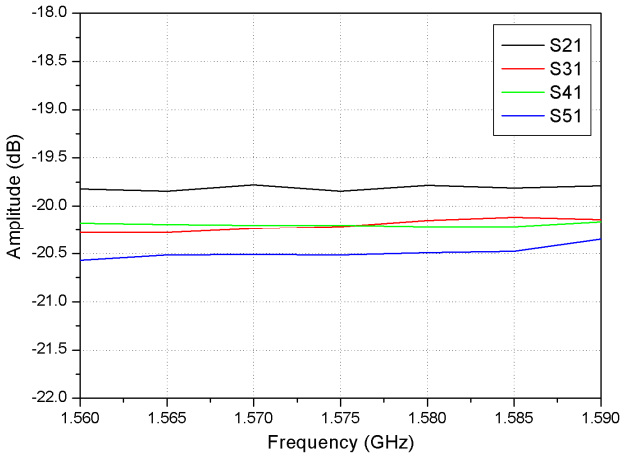

Fig. 7: Measured amplitude at the four individual outputs of the calibration network

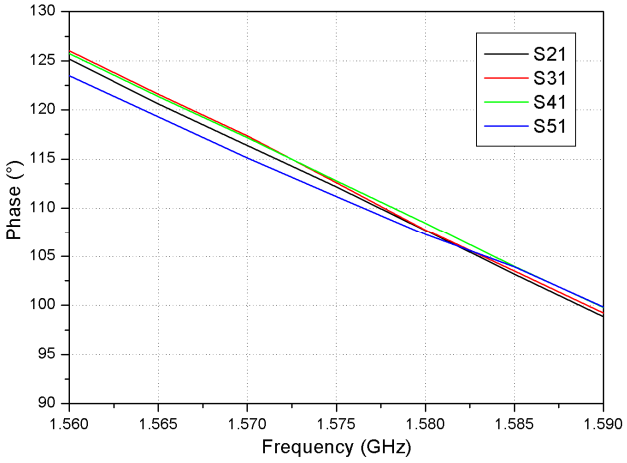

Fig. 8: Measured phase at the four individual outputs of the calibration network

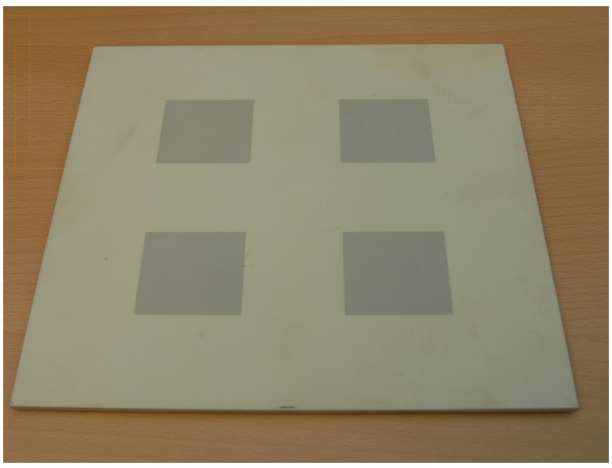

Fig. 9: 2x2 antenna array

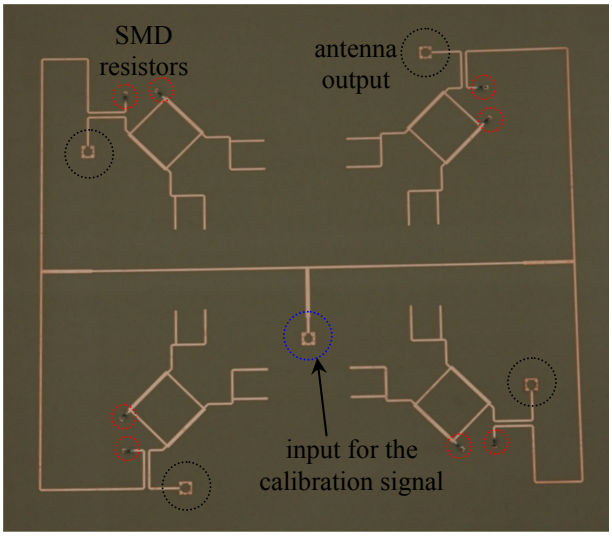

Fig. 10: Layer with the calibration network and directional couplers

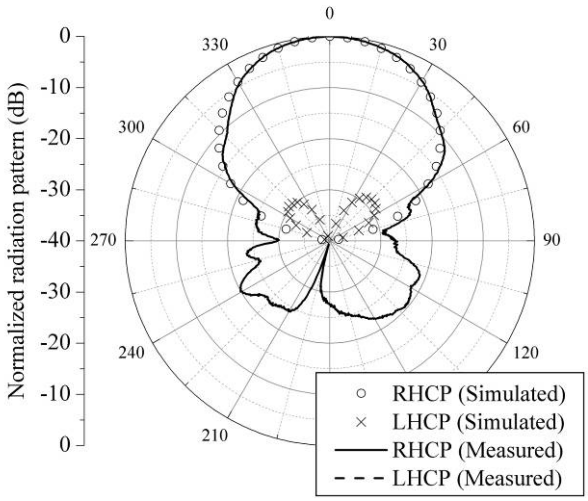

Fig. 11: Radiation pattern of the 2x2 array with the main beam pointed to broadside.

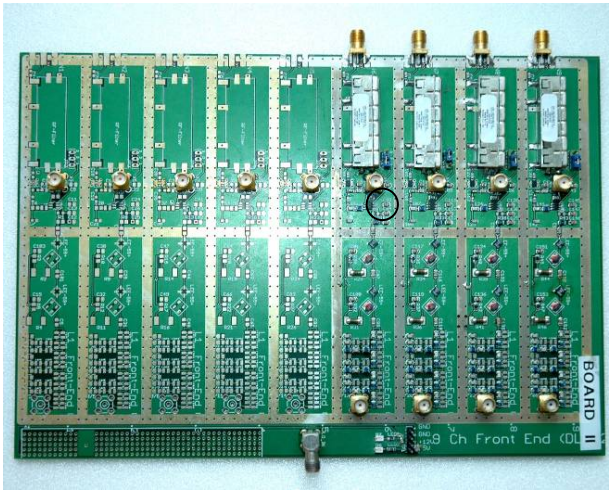

Fig. 12: Nine Channel L1 Front End

2. FRONT END

To ensure an interference robust reception of GNSS signals, an appropriate front end design is essential. In the following a description of the RF- and IF part of the front end will be given. For the first prototype a 9 channel L1 single frequency front end was developed, see Fig. 12. It is designed for the reception of the SoL signals in the L1 band with a bandwidth of 14 MHz. The first part of the front end was already discussed in the previous chapter. It has been integrated in the antenna array and consists of an LNA, an integrated directional coupler and a bandpass filter, c.f. Fig. 14Ⓐ–Ⓑ. This first filter together with the frequency selective properties of the antenna element does the first filtering of the signal. The LNA has relatively low gain of 13 dB, a high IP3 and is placed after this first bandpass filter to prevent its saturation by out of band interference. The low insertion loss of the bandpass filter together with the good noise property of the LNA result in a noise figure of approx. 1.6 dB for the whole system, which is quite reasonable despite the late allocation of the LNA.

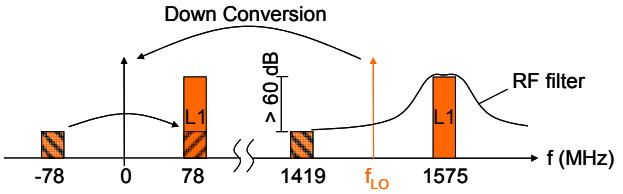

Fig. 13: Down Conversion Scheme

After this first conditioning the received signal enters the actual front end board. Here the signal is filtered again by a higher order ceramic filter. This filter has a 3 dB Bandwidth of 32 MHz to move the steep increase of the group delay outside of the band of interest. The high order of the filter provides a steep descend to the stopband.

The subsequent mixer down converts the incoming signal to an intermediate frequency of 78 MHz. The corresponding local oscillator frequency gives enough spectral separation between the RF signal and the unwanted alias, to sustain the needed suppression of the alias by the RF filters, see Fig. 13. Because of this a poly phase filtering at IF is obsolete.

For the distribution of the local oscillator (LO) signal to each mixer a 1:9 distribution network was developed. Fig. 15 shows the layout of this structure. Since the high LO power which is needed to be about 5 dBm, it is necessary to avoid unwanted radiation of the LO signal. To minimize this radiation the LO distribution network was designed in stripline technology and is integrated in the lower three layers of the front end board.

Due to the relatively high ε_r of the used substrate, the 50 Ω stripline has already a width of 0.24 mm. After dividing the power 1:3, the impedance of the connecting lines must be higher by a factor of $\sqrt{3}$ and for 50 Ω basic line width that would result in 87 Ω and unacceptable narrow lines. Therefore, the LO network is designed for 32 Ω impedance with a λ/4

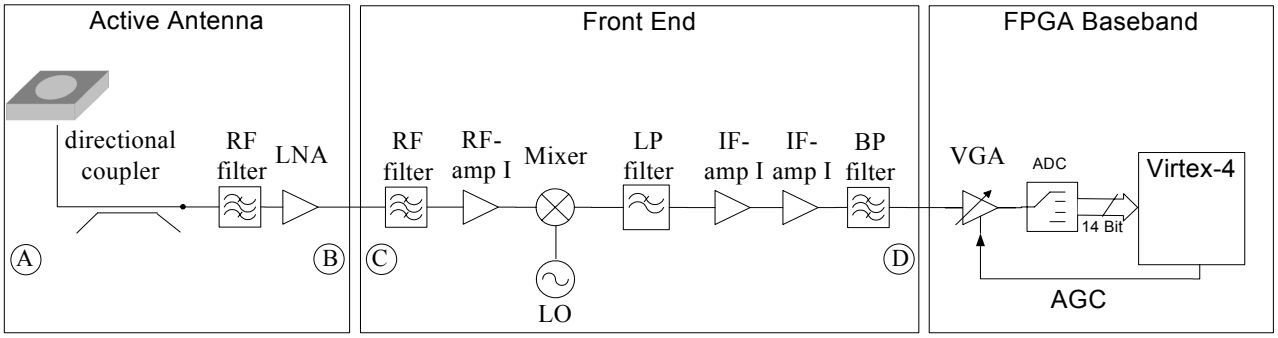

Fig. 14: Front End Architecture

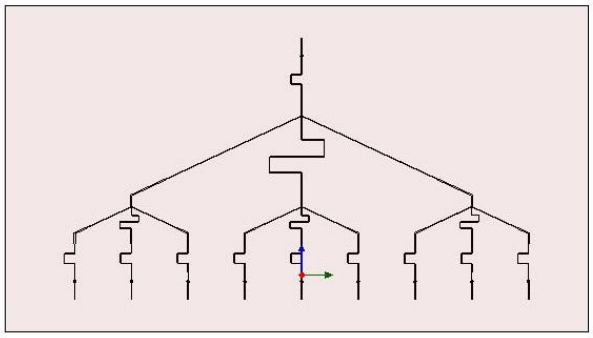

Fig. 15: LO Distribution Network

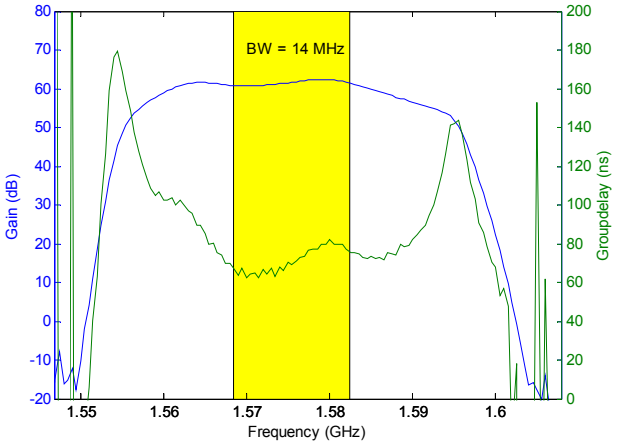

Fig. 16: Measured Gain and Group Delay of the Complete Front End Chain (c.f. Fig. 14Ⓒ – Ⓓ)

transformer inside the network of 55 Ω. A λ/4 transformer is used to match the network to the 50 Ω lines. After the down conversion to IF a third order Chebychev low pass filter is utilized to mitigate the RF breakthrough effects of the mixer. This is necessary to avoid a further amplification of the RF signal by the IF amplifiers, otherwise this would harm the crosstalk isolation. This crosstalk isolation determines the depth of the nulls in the steered beam pattern.
Subsequently the IF signal is amplified by another 40 dB in two stages before it enters the anti aliasing bandpass filter. This last filter is a 7^{th} order Type I Chebychev with a 1dB bandwidth of 14 MHz.

Finally the signal enters the FPGA Board. This board is populated with a powerful DSP-FPGA (Virtex-4 SX55) and 16 variable gain amplifiers as well as 16 ADCs which digitize the incoming IF with 104 MHz and a 14 bit resolution. Sampling the incoming IF signal with 104 MHz causes an intentional aliasing down to a new digital IF of 26 MHz.

The 14 bit resolution of the analogue to digital conversion together with the digital steerable variable gain amplifiers result in a very high dynamic range, which is ideally suited for the use of digital signal processing algorithms for interference detection and mitigation. Fig. 16 shows measured gain and group delay characteristics of the front end, c.f. Fig. 14 Ⓒ – Ⓓ . As can be seen the gain variation over the 14 MHz bandwidth is approx. 1 dB. The variation of the group delay is less than 14 ns.

3. FPGA – SIGNAL PROCESSING

The presented FPGA architecture comprises data reduction, i.e. bandwidth limitation, down conversion to baseband and data recording. The typical operations of a navigation receiver take place in software and are discussed later on. The FPGA used for this approach is as stated above a Virtex4 SX55 device. The main steps of the signal processing in the FPGA are:

1. Synchronization of the four independent digital data streams from the different antenna elements to the system clock. This is done by a simple FIFO construction. The output of the FIFO which contains the data from the four antenna elements will be used twofold: Without further processing for the gain control of the ADC and as input for the digital-down-converter block (DDC) for further processing.
2. Due to the high sampling rate and the limited data rate of the PCI bus which is used for data transfer to the processing unit, it is necessary to reduce the signal bandwidth and the data rate. After a baseband transformation and I/Q separation the signals are band limited by an FIR-filter architecture and down sampled by a factor of 42.
3. After the DDC block the data transferred via PCI to the PC and stored on hard disk. The maximal record length is currently almost 60 seconds.

4. SOFTWARE-BASED SIGNAL PROCESSING

Currently, the complete baseband receiver including acquisition, tracking, array processing, and navigation solution is realized as a software receiver in MATLAB for offline processing.
In the next steps of development the high data rate signal processing functions like correlators will be implemented in the FPGA, but low data rate functions will be still kept in software. The signal processing in software will then complement the processing in the FPGA part taking over less time

demanding processes at low data rates. It can be implemented either on an external PC or Notebook or in an integrated software or hardcore CPU on the FPGA chip. The remaining low data rate signal processing in software consists of array processing algorithms (direction finding, beamforming), navigation solution and, in future, additional integrity processing. It includes also some parts of the digital receiver, i.e., the correlators will be implemented directly in FPGA, but the loops will be closed in the software part. This option will be realized by the bi-directional PCI interface to the FPGA part, which offers higher flexibility and the possibility to implement the array signal processing in the software part of the platform.

The array processing options available in the software part include direction finding with ESPRIT and MUSIC algorithms as well as adaptive beamforming. The adaptive beamforming can be used in a blind manner (without *a priori* information) applying minimum variance (MV) algorithm for placing a spatial null in the radio interference direction of arrival. The assisted options include LMS beamforming using the local receiver PRN code replica as the reference signal or constrained MV algorithms with the corresponding constrains in the directions of GNSS satellites and interference. The direction finding can be optionally used to obtain the directional information about the desired and unwanted signals (radio interference, multipath), but also the GNSS almanac information can be used to calculate the line of sight directions to the satellites. Because the array processing is performed on digital signals, the beamforming can be done in every signal processing channel for each tracked satellite independently by parallel implementation.

As already mentioned, currently all the array processing options described above are realized on an external PC as a MATLAB program. Because of the limitations of the software or hardcore CPU on the FPGA board only a part of these algorithms and/or for reduced number of tracking channels can be transferred from the external PC to the CPU(s) on the FPGA board.

SUMMARY AND OUTLOOK

Interference and multipath robustness are key requirements in SoL applications. Array processing is a very powerful technique for the suppression of such disturbing signals and, therefore, a key technology for the development of robust SoL receivers with improved and reliable signal reception. For the implementation of array processing techniques in real hardware the design of the single antenna elements, of filtering, the calibration of hardware channel imbalances and sufficient bit resolution are key issues to be solved. The paper describes the architecture of a GNSS array processing prototype utilizing a 2x2 single frequency antenna array with enhanced capabilities for improved signal reception and interference mitigation at L1. Because SoL services are allocated in the L1 and E5 band and with respect to the expected availability of GPS L5 and Galileo E5a/E5b signals with a sufficient number of satellites in view in the near future, the L1 prototype will be extended to dual frequency signal reception with a 3x3 L1/E5 array antenna in the next steps of development. The final goal is a dual frequency array demonstrator with real time capability for demonstration of the high potential and performance of the array processing in laboratory tests and field experiments.

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