DESIGN AND OPTIMIZATION FOR INDUSTRIAL PRODUCTION OF A 4-8 GHz MONOLITHIC AMPLIFIER FOR HIGH-CAPACITY RADIO LINKS

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Abstract: A MMIC development philosophy for industrial production purpose is first described. The design is then reported for a laboratory prototype of a two stage 4-8 GHz MMIC amplifier to be used in high capacity radio links. Then, the paper describes the overall job (involving a number of design and testing cycles, back end simulations and measured data critical analyses) which was done to make the circuit up to a standard industrial production.

Introduction

The development of GaAs MMIC chips to be used in high volumes is, as well known [1,2,3], much more difficult than the construction of laboratory circuit prototypes. This is, unfortunatly, the reason [2] why a great quantity of the MMIC prototypes developed by international research do not reach the market. In fact, to satisfy such a condition, a very complex job has to be done, involving a number of design cycles, back end simulations and critical comparisons between measured results and simulated circuit behaviour.
In this paper we describe in detail the full work performed for the construction of a mass producibile 4-8 GHz MMIC amplifier for high-capacity radio links. The circuit provides a gain of 13±0.8 dB, +18 dBm output power at 1 dB gain compression and 6 dB noise figure. The amplifier is used in the amplification chain of a transmitter, where the incoming low power signal, after up conversion, need to be amplified to adequate level to drive the last power amplifier stage near the compression point.
To make more easy a full understanding of the relevant problems and of their mutual interactions, a description of the MMIC development philosophy and its flow chart is first given.
Then, the chosen basic circuit topology, the main reasons for its selection and the relevant trade-offs will be described.
Subsequently the first design cycle and the inherent parameter extraction and measurement problems will be described, outlining the features concerning the achievement of an accurate circuit diagnostic and back end simulation taking adequately into account a number of important parameters like the layout induced parasitics, the interelement coupling effect, and the chip grounding system.
The circuit redesign will be then described, where all the experimental measurements and back end simulation achievements are taken into account.
The end product simulated and measured performances as well as the used fabrication technology will be finally described.

MMIC's development philosophy for industrial production

A GaAs MMIC, up to date with the present world-wide status of the art, would seem, to the unexperienced people, a very simple circuit.

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However, its design, development and industrial engineering is much complex because one has to deal with a number of mutually interacting problems.
The designer starting point is, usually, the circuit target specifications on the basis of which a suitable circuit configuration has to be choosen. When faced with the circuit rerquirements, the designer must first decide about the opportunity and the real possibility of satisfying them with a MMIC chip. The knowledge of the capabilities of FETs and others standard components give the basic background to this statement.
The detailed design of the MMICs depends on the availability of computer aided circuit analysis and optimization programmes.
In fact the individual circuit elements cannot be described by their nominal value but need to be characterized by fairly complex equivalent circuits to take into account their parasitics. Moreover the comparison between the published single component theoretical models (such as those used in most commercial CAD routines) and the results of accurate r.f. measurements frequently shows the substantial unadequacy of the available routines [1].
The present lack of an adequate theoretical background is evidenced by the fact that most MMICs factories make use of empirical models based on a fitting of precision microwave measurements made on a great number of components of various values and forms.
When a first prototype electrical design of acceptable performance has been done, consideration must be given to the overall chip layout and to a first rough verification of the various production yields.
Since the circuit cost is strictly related to the chip area, particular attention must be dedicated to its minimization with the consequence of rising the intercomponent parasitics coupling effects.
The difficulty of handling sufficiently accurate theoretical single component models as well as the risk of undesired mutual coupling effects may require experimental measurements on particular "subnetworks" of the monolithic itself. Notice on this subject, that the proximity effects can be easily calculated only for very simple geometries.
The subnetworks may be included in special test patterns realized together with the chip first version or, if the quasi monolithic test approach is chosen [4], especially realized on low-cost S.I. GaAs substrates.
Some interaction and, sometimes, a specification review, can result necessary before a full satisfaction of performance and layout requirements. At this stage the previous rough yield analysis can be deepened taking into account the peculiarity of the synthesized layout and a circuit sensitivity analysis must be done which will be based on the knowledge of the tolerances of the employed fabrication process and the estimated value of the in-specification chip yield can be determined. If the results of the yield prediction are not satisfactory, a chip redesign which relaxes this effect, may be necessary. If the results are O.K., one can proceed to the design of the complete mask set and to the construction of the first circuit prototypes.
If these samples satisfy the revised specification the design can be considered sucessfull and the circuit may proceed to the last engineering stages (packaging and reliability tests); if not, the reasons for the unsatisfying performance must be identified. This is frequently a quite difficult job since the reason may reside in the material, processing, mask layout or manufacturing errors. The possibility of a fault diagnosis made with direct measurements on various circuit points is extremely limited by the circuit dimensions. Here a basic aid can be obtained by a proper use of the above mentioned test patterns. Fault correction will require full or partial reconsideration of the design process depending on the nature of the faults. An intelligent use of the circuit simulation programs may also be of some help in the fault diagnosis.

A flow chart of the overall development process for industrially producible MMICs is shown in Fig.1.

The MMIC development

The MMIC basic target requirements were: 4-8 GHz bandwidth, >10 dB gain, <-10 dB input/output reflections, ≥18 dBm power output at 1 dB gain compression, <6 dB noise figure, <500 mW d.c. power consumption. The use of one single +5 Vdc bias voltage was also requested.
In spite of the very broadband performances allowed, a single stage MMIC amplifier topology [4,5,6] was discarded for the inherent unability to reach the required gain level. So, a cascade of two inverters with shunt resistive feedback was chosen (see Fig.2) because it permits a better amplifier isolation and a separate adjustment of the input/output matching conditions (so making more easy the trade off between input VSWR and amplifier noise figure and between output VSWR and second stage gain). The device current rating was fixed at $I_{dss}/2$ and gate widths of 300 and 600 /um were chosen for FETs 1 and 2 respectively. Then, the Fig.2 circuit parameters optimizing the in band amplifier gain, were computer calculated under the condition that the circuit was using the standard Telettra A 1 /um gate process and that it was meeting the above reported gain and VSWR requirements. Table I reports the optimized circuit scattering parameters and its stability factor when all the single element parasitics are included. An overall gain reduction of about 1 dB with respect to the previous simulation neglecting parasitics, is obtained.
This prototype circuit was then implemented and constructed in a monolithic form on a 1x0.8x0.2 mm^3 chip. A photograph of the MMIC is shown in Fig.3.
A wide number of such circuits, for which an external hybrid bias circuitry was required, were mounted on chip carriers and tested as R.F. performances.
During the chip mount particular attention was paied to guarantee a low parasitic inductance ground connection of the source pad of each FET device. In fact the use of 6 bonding wires instead of 3 resulted on a ~1.5 dB gain increase. No better appreciable gain advantages were noticed for an higher wire number because of the effect of the on chip metallization parasitic inductance and of the mutual wire coupling. The experimental results showed ~1.5 dB gain deterioration between the measured and the simulated data.
By a proper back end simulation, this difference was ascribed both to modeling inaccuracies of the parasitics effects of the metallizations connecting the FET sources to the bonding wires and of the losses in the spiral inductors. Moreover an undesiderable effect on the gain of the external bias circuitry especially near the band edges, was demonstrated.
A full d.c. on wafer circuit testing, showed that the achieved MMIC functional yield [8] was ~65% of the expected one.
In order to remedy to the performance inadequacy the development of an improved circuit version using a ~0.5 /um gate length devices, with on chip bias netwroks and reduced source parasitics was decided.
For improving the circuit total yield to the expected values, more restrictive values on the wide number (>50) MMIC layouting rules [7] were introduced, following the recommendations of the reference [1] work.
In Fig.4 the circuit diagram of the complete amplifier is depicted.
Tab.II shows the predicted small signal performance where all the single element parasitics are included.
The fabricated chip with 1.2x1x0.2 mm^3 dimensions is shown in Fig.5.
Measured small signal gain and input/output return loss are reported in Fig.6.

Amplifier fabrication

The two versions of MMIC amplifier were fabricated using the standard foundry processes A e B employed in Telettra.
The A process, applied for the first generation of the amplifier, makes use of 1 micron gate technology on implanted layers with Si29 ions. The process A is done at an energy of 120 keV and a dose of $3.6.10^{12}/cm^{+2}$ to achieve typical 3.5 V pinch off and I_{dss} 250 mA/mm.
Air bridge interconnects and PECVD Si_3N_4 dielectric layers for passivation and MIM capacitors were employed.
The final thickness of metallization was 2 microns and it was obtained by selective electrolityc gold growth. Both active and Ti resistors were used.
The B process, adopted for the second generation of the amplifier, has the same characteristics of the process A for the metallizations and passive components, while for the active devices makes use of 0.5 micron gate technology on implanted layer with Si29 ions at energy of 70 keV and a dose of $4.6.10^{12}/cm^2$ to achieve typical 2.5 V pinch-off and I_{dss} 200 mA/mm. Fig.7 describes the various layers and the process steps used.

Conclusions

A general philosophy for the development of industrially producible MMICs has been described. Then the specific development work for a 4-8 GHz monolithic amplifier has been reported.
It was outlined the importance of an accurate characterization and modeling of each individual element of the circuit to achieve an accurate circuit diagnostic and back end simulation.
The final version performance demonstrate the propriety of the general MMIC development philosophy here described.

References

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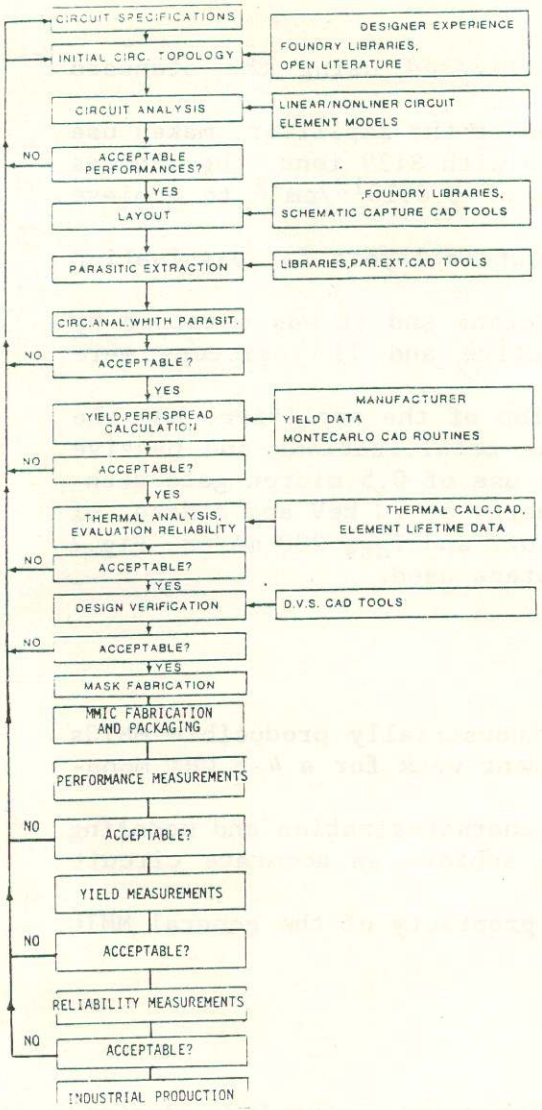

Fig.1 - Flow chart for the development of an industrially producible MMIC.

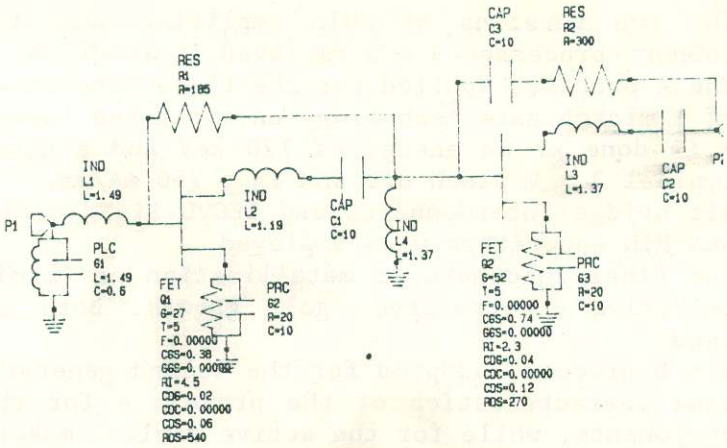

Fig.2 - Circuit configuration of the dual-stage MMIC 4-8 GHz MMIC amplifier.

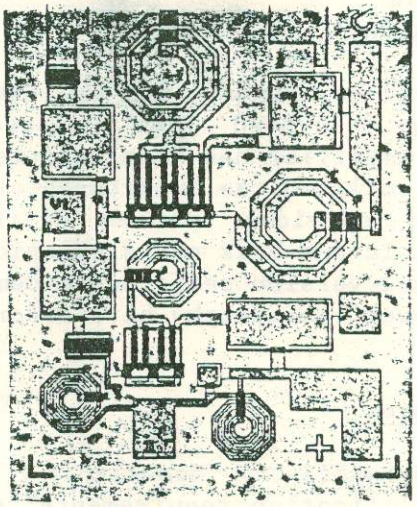

Fig.3 - Photograph of the fabricated chip.

FREQ-GHZ	DB[S11] X	DB[S21] X	DB[S12] X	DB[S22] X	K X
3.00000	-9.508	4.597	-28.084	-6.085	5.036
3.50000	-15.210	7.397	-25.737	-7.828	3.335
4.00000	-13.728	8.966	-24.573	-9.690	2.627
4.50000	-14.207	9.982	-23.937	-11.591	2.327
5.00000	-19.032	10.646	-23.639	-13.828	2.220
5.50000	-23.831	10.941	-23.701	-16.157	2.217
6.00000	-15.895	10.917	-24.069	-17.486	2.276
6.50000	-12.588	10.740	-24.575	-17.470	2.377
7.00000	-11.742	10.569	-25.055	-16.831	2.507
7.50000	-12.780	10.472	-25.435	-15.756	2.658
8.00000	-15.790	10.396	-25.764	-14.116	2.822
8.50000	-15.115	10.153	-26.223	-12.195	2.993
9.00000	-9.116	9.470	-27.083	-10.567	3.169
9.50000	-5.150	8.173	-28.515	-9.557	3.344
10.0000	-2.931	6.350	-30.431	-9.049	3.519

Table I - S-parameters of the optimized circuit.

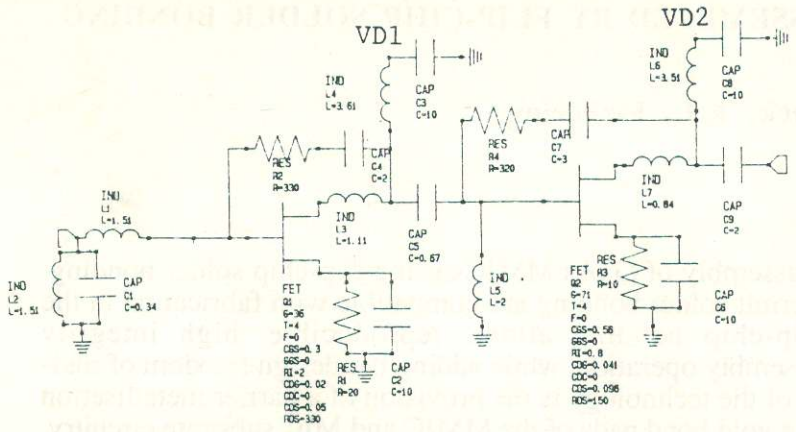

Fig.4 - Circuit configuration of 2nd version 4-8 GHz MMIC amplifier.

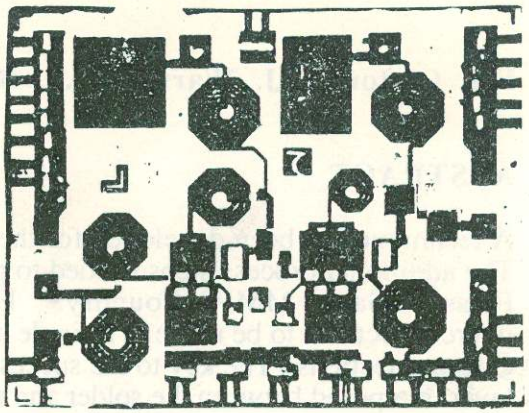

Fig.5 - Photograph of the fabricated chip.

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FREQ-GHZ	DB[S11] C	DB[S21] C	DB[S12] C	DB[S22] C	K C
4.00000	-13.947	13.828	-28.631	-13.610	2.652
4.50000	-12.315	13.865	-28.905	-12.057	2.635
5.00000	-12.138	13.823	-29.210	-12.129	2.713
5.50000	-13.724	13.841	-29.417	-12.588	2.818
6.00000	-17.057	13.878	-29.575	-12.940	2.923
6.50000	-21.571	13.879	-29.742	-13.015	3.019
7.00000	-20.531	13.823	-29.942	-12.875	3.105
7.50000	-16.547	13.718	-30.165	-12.644	3.181
8.00000	-13.699	13.579	-30.395	-12.371	3.247

Table II - Predicted small signal performance of 2nd version amplifier.

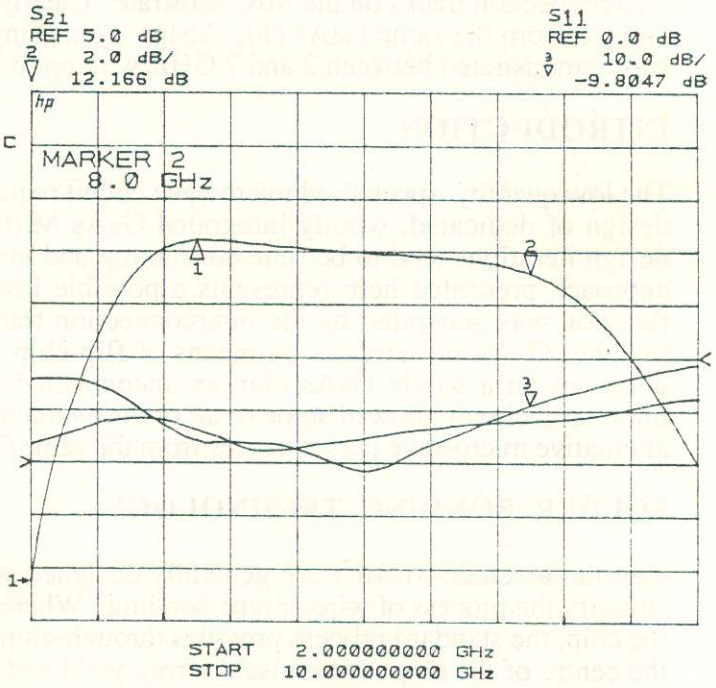

Fig.6 - Measured performance of 4-8 GHz MMIC amplifier with 0.5 gate length devices.

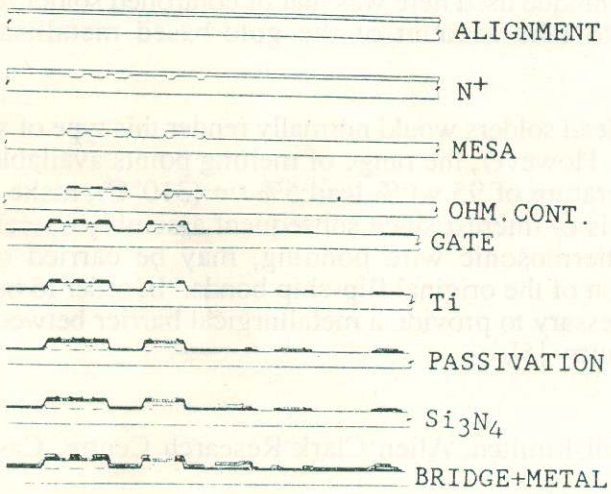

Fig.7 - Fabrication process steps.