COMPACT ECL GATE DESIGN FOR DOUBLE MESA HBT PROCESS

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ABSTRACT

Emitter Coupled Logic (ECL) gate is a good candidate for gigabit logic when one uses GaAs/GaAlAs Heterojunction Bipolar Transistor (HBT). With the double mesa process, interconnections between the 5 transistors of the elemental gate have to climb the emitter and base mesas, leading to lack of density. A more compact design of the ECL gate has been achieved, in which the transistors are directly connected on the top of the base mesa. The DC characteristics of this gate are similar to these obtained with conventional gate design and the surface is reduced by a factor 1.6.

I - INTRODUCTION

GaAs/GaAlAs Heterojunction Bipolar Transistor (HBT) has been proved to be a very efficient device for gigabit/s integrated circuits. It takes advantage of the bipolar structure, of the high mobility of GaAs material and of the possibility to realize *heterojunction* thanks to the good lattice matching between the high band-gap GaAlAs material and the lower band-gap GaAs. An emitter-base heterojunction allows a high injection efficiency [1], even with a very high base doping level ($<10^{20}$ cm^{-3} [2]). As a consequence, very impressive results (cutoff frequency higher than 120 GHz, maximum oscillation frequency higher than 200 GHz) have been obtained in many laboratories [3].

This device can be used for gigabit/s digital integrated circuits. Two major logic gates are available :

- saturated logic such as IIL, which allows the fabrication of LSI ICs (a 32-bit RISC CPU operating at 150 MHz [4] and 6k-gate arrays [5]),
- non saturated logic, whose speed is higher and the density lower. The most known is the Emitter Coupled Logic. The highest performance for divider circuits (34.8 GHz [6]) have been obtained with such a gate.

At present times these results have been obtained with a process which is based on a double mesa (self-aligned) device, where the interconnections are made outside the mesa structures. This kind of connection constitutes a major limitation for integration density, when compared to Silicon technologies.

In this paper, we present a ECL gate (figure 1) design improving the planarization and the internal interconnection of the structure without any performance degradation.

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II - CONVENTIONAL PROCESS

Two possibilities are available at CNET to contact the base layer of a HBT (figure 2). The first one uses a p-type diffusion or implantation through the emitter layer [7]. The collector layer is connected with use of an etch of the upper layers of the device (mesa). The second one, the so-called double mesa process [8], is based on successive etch of n-type GaAlAs emitter layer and p-type GaAs base layer. Ohmic contacts are then deposited directly on the convenient layers. In both cases, Boron-Proton implantation is used to delimitate the active area of the transistors and resistors, allowing the insulation of the devices in a circuit. A polyimide film is used to make the climbing of the mesa easier. It also allows the insulation between the two levels of metal interconnection. The transistors are connected through the polyimide film by vias, with the second level of metal.

Extensive study has been made to compare the potential performances of the two kinds of process for digital application [9]. The implanted process allows a better planarization of the circuits but, because of the thermal annealing of the p-type implanted area and of the high diffusivity of the Be which is used as a p-type impurity in the base layer, the base doping level cannot be so high as in the double-mesa process. As a consequence, the propagation time per gate of digital circuits is lower with the second kind of process.

To connect two devices, the TiPtAu metal must then climb two mesas in a standard way. It induces a lack of density and risks of cut interconnections.

III - COMPACT ECL GATE DESIGN

ECL/CML circuits are mostly based on series-gating of a elemental gate which has a fixed topology. Taking advantage of this fact, we propose, in order to compact the ECL gate area, to use an unique base mesa for the five transistors of the elemental gate (figure 1) and to make common the two emitter mesas of the differential pair. As the emitters (T1 & T2) and bases (T4 & T5) are at same potential in an ECL gate, the corresponding ohmic contacts can also be common. A drastic reduction of the via number results and the interconnection procedure is simplified. We have to remark that an efficient boron-proton insulation between the transistors is indispensable.

Such approach leads to the design of figure 3 where collector contacts are connected with vias through the base layer.

The area of such compact gate is $250 \times 250\ \mu m^2$ which is to compare with the $200 \times 410\ \mu m^2$ of a conventional one when the same design rules are used.

IV - PERFORMANCE

The transfer curves, relative to the compact gate, have a 1.33 slope for 3 mA operation current and a 1.63 slope for 6 mA operation current (figure 4). It shows regenerative signal capabilities between the input and output. These results are very similar to those obtained with ECL gates with conventional design, processed on the same wafer.

V - PERSPECTIVES, CONCLUSION

We have presented a compact ECL gate design where the five transistors are sharing the same base mesa, with internal interconnection optimization compatible with the double-mesa technology. We haven't observed any performance degradation when compared with a classical gate.

Our ECL compact gate design approach can be conveniently used in order to build sea of gates (or differential pairs) with application to LSI/MSI circuits, based on the gate array approach **[10] [11]**.

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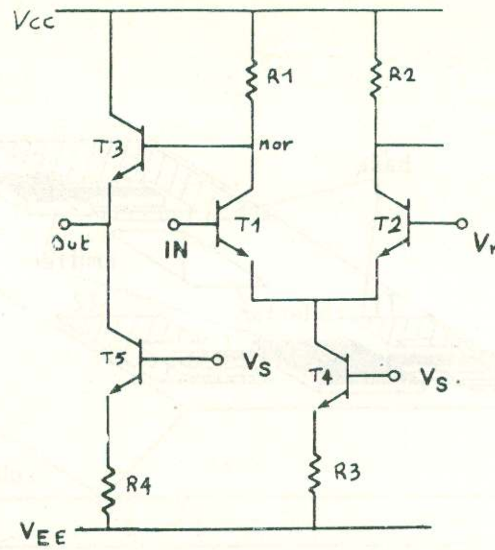
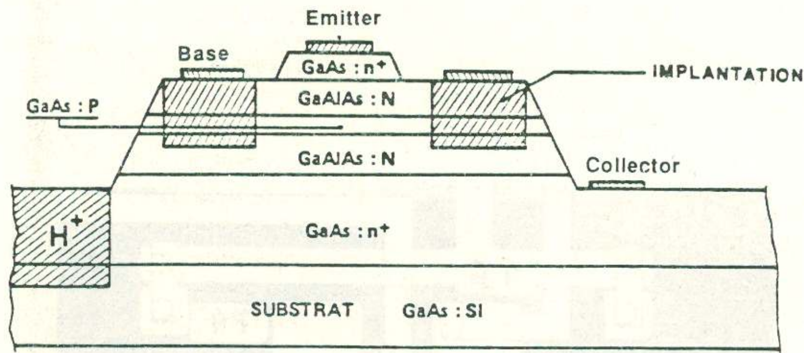
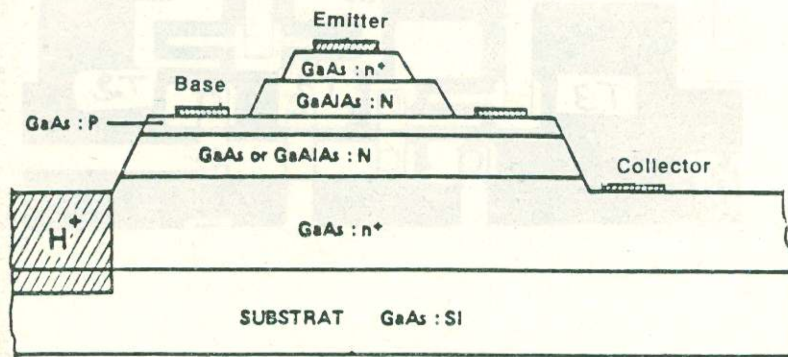


Figure 1 : Emitter Coupled Logic gate

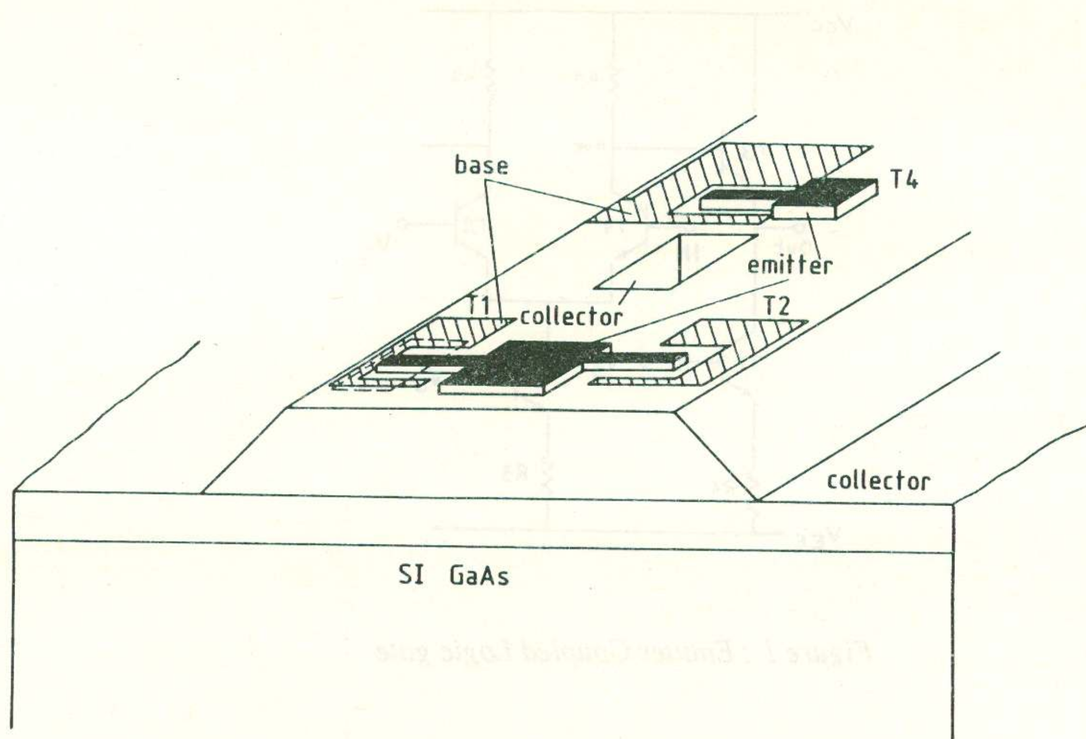


a) Implanted



b) Double Mesa

Figure 2 : Heterojunction Bipolar Processes



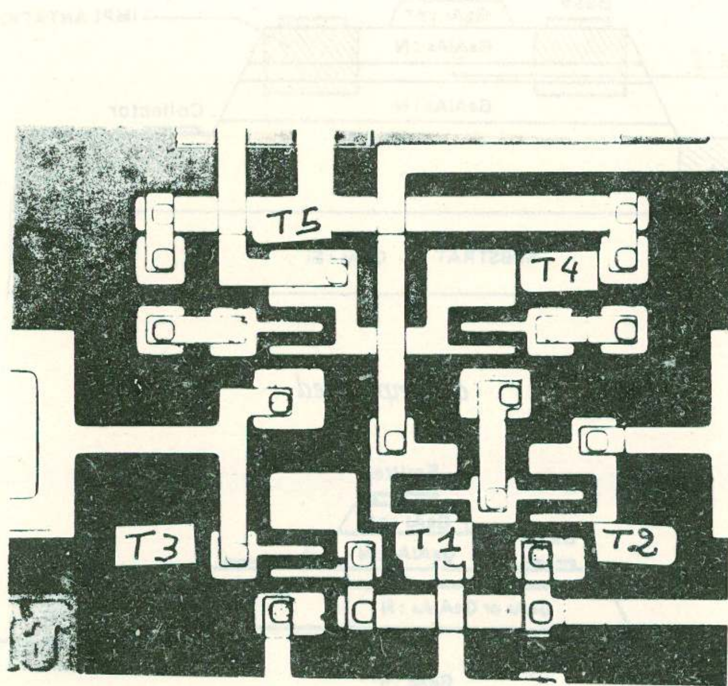
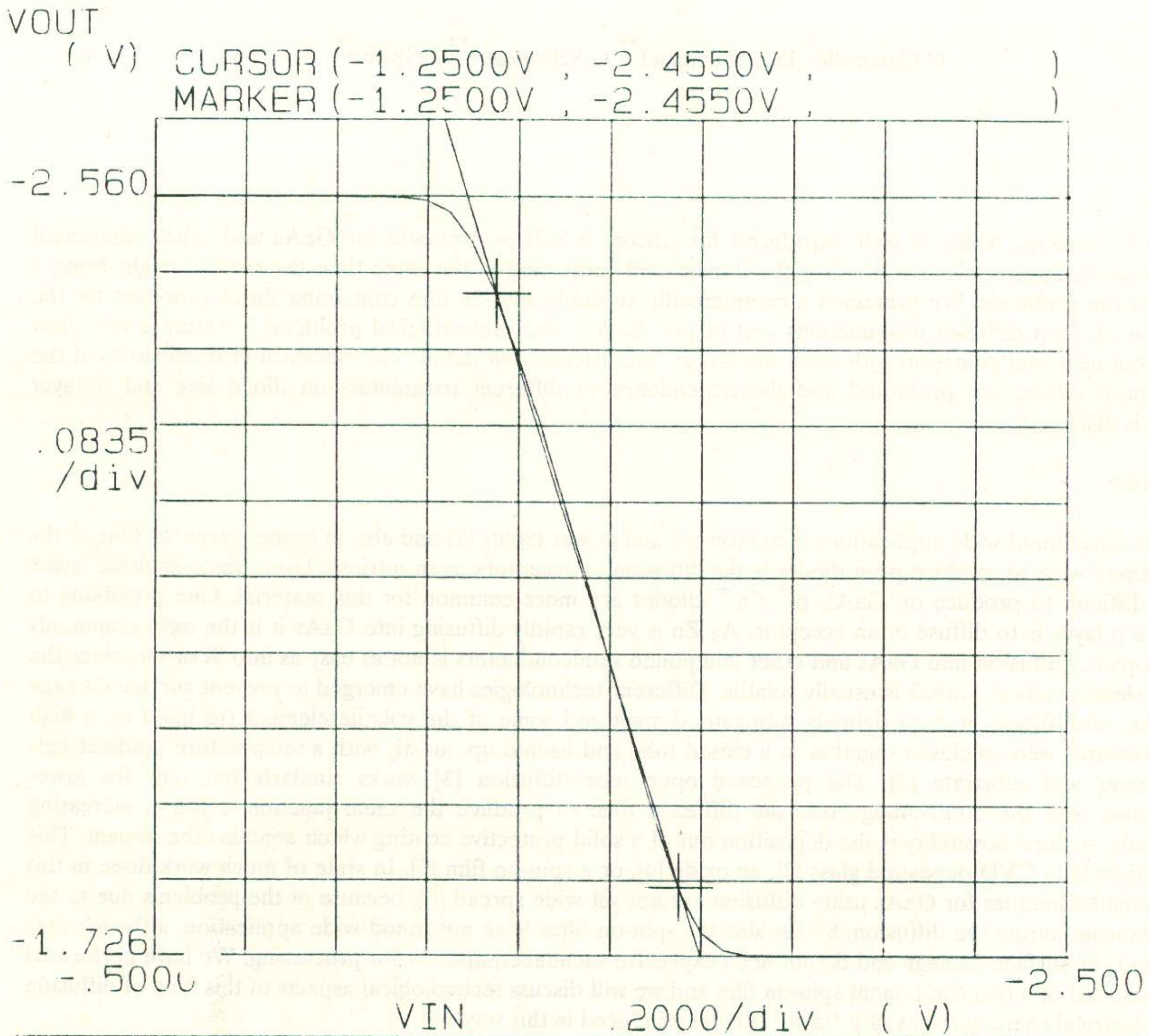


Figure 3 : Compact ECL gate : partial perspective view of the differential pair and photography of the whole circuit



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-1.63E+00	-613E-03	-2.75E+00	-4.50E+00
LINE2				

Figure 4 : Transfer curve of the ECL compact gate