# IMPROVED NOISE PERFORMANCE OF ION-IMPLANTED MESFET DEVICES BY OPTIMISED PRE AND POST IMPLANT WAFER ANNEALING.

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ABSTRACT

In this article we illustrate how the noise performance of ion-implanted MESFET devices can be appreciably improved by means of optimised pre and post implant annealing cycle. With this technique the 12 GHz noise figure of 0.5x300 $\mu$m devices is reduced from 2.7 dB to 1.8 dB.

## INTRODUCTION

Most of the work published to date to improve the on-wafer activation uniformity of ion-implanted semi-insulating GaAs substrates has concentrated primarily on substrate material characteristics (1-4) (such as for example residual stress, dislocation density and EL2 concentration) and related phenomenon induced by the capping or capless medium during annealing. Infact little importance has been given to the details of the heating cycle and the associated on-wafer radial and longitudinal thermal gradients which can play an important role in modifying said material characteristics to yield in optimised conditions improved on-wafer activation uniformity and device performance.

In this article we will illustrate how by optimising the radial and longitudinal thermal gradients generated on a GaAs wafer during the post-implant annealing cycle, appreciable improvement in on-wafer activation uniformity can be achieved and furthermore how a pre-implant annealing cycle under the same conditions can results in much improved performance of MESFET devices.

## EXPERIMENTAL

Pre and post implant annealing of the undoped semi-insulating GaAs wafers is carried out in a specially designed furnace (5-6) which eliminates all on-wafer thermal gradients during the anneal cycle. Prior to annealing at 820°C for 10 min. all wafers are capped on both faces with a reactively sputter deposited $Si_3N_4$ film. The on-wafer activation efficiency and uniformity is evaluated by measuring the corresponding saturation current ($I_{dss}$) of an array of 300 $\mu$m wide metal semiconductor field effect transistor (MESFET) ohmic contacts fabricated on the selectively doped substrates. In particular, approximately 400 devices, uniformity distributed on the 2-in. GaAs substrates, are measured for each wafer to ensure statistically significant evaluation of the on-wafer activation uniformity. From room temperature Hall measurements of appropriate reference wafers (i.e. undoped ingot annealed material) we extrapulate

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the activation efficiency $\eta$ of the ion implanted donor species and as such convert the $I_{dss}$ maps into activation efficiency maps. After this first characterisation we then proceed to complete the MESFET devices by conventional recessed gate technology and finally we evaluate their electrical performance by d.c. (including low-field mobility under the gate (7) ) and r.f. noise measurements.

RESULTS

In fig.1 we present typical activation efficiency maps of undoped (1a and 1b) and undoped ingot annealed (1c) semi-insulating GaAs substrates after ion-implantation with a $^{29}Si^{+}$ dose of $1x10^{13}$ at 40 keV plus $5x10^{12}$ at 120 keV and annealing in a conventional horizontal tube furnace (1a) and a low thermal gradient (LTG) furnace (1b and 1c). As illustrated in fig.1a, for undoped S.I. GaAs, conventional furnace annealing gives rise to a radial fourfold symmetry in activation (along the (110) axis), similar to the maps of residual stress, dislocations and EL2 concentration observed by near-infrared transmittance spectroscopy (1-2).

Infact for this condition the on-wafer activation efficiency

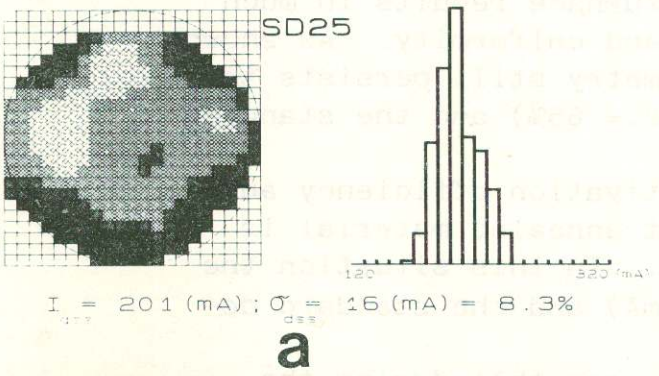


FIG.1 - Activation efficiency maps of undoped (a and b) and undoped ingot annealed (c). S.I. GaAs substrates after ion implantation with a $^{29}Si^{+}$ dose of $1x10^{13}$ at 40 keV plus $5x10^{12}$ at 120 keV and annealing in (a) conventional horizontal tube furnace, (b and c) low thermal gradient furnace.

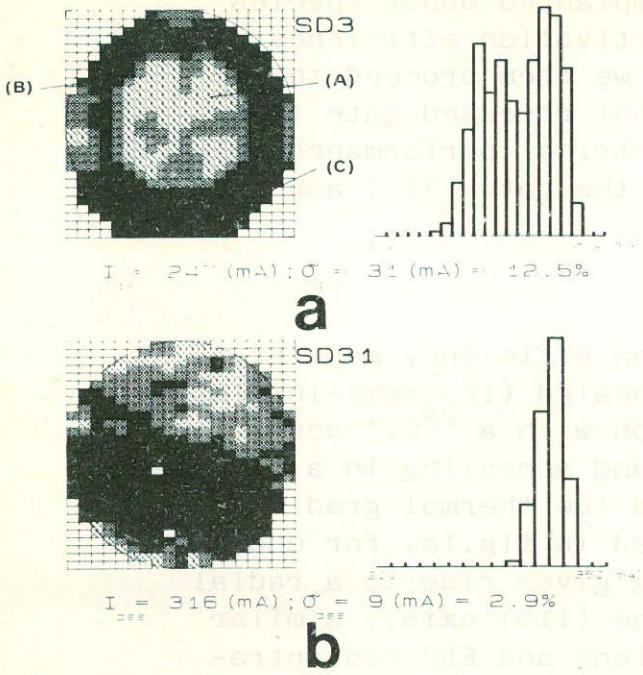


FIG.2 - Activation efficiency map of undoped S.I. GaAs after ion implantation and (a) conventional furnace annealing and (b) prolonged annealing with low thermal gradient furnace.

and uniformity are,poor with average $I_{dss}$= 201 mA (corresponding to 50% activation) and standard deviation $\pm$ 8.5%.

The same material annealed in a LTG furnace results in much improved on-wafer activation efficiency and uniformity. As shown in fig.1b, even thougth the fourfold symmetry still persists the average $I_{dss}$ has increased to 273 mA (i.e.= 65%) and the standard deviation reduced to $\pm$ 3.5%.

As illustrated in fig.1c the best activation efficiency and uniformity is achieved when undoped ingot annealed material is post implant annealed in the LTG furnace. In this situation the activation efficiency $\simeq$ 80% ($I_{dss}$ = 350 mA) and the standard deviation $\pm$ 1.5%.

From these preliminary results it appears that during the post-implant annealing cycle the LTG furnace appreciably modifies the physical properties of the material to yield improved activation efficiency and uniformity. To verify this hypothesis we have investigated the relationship between material properties and duration of the annealing cycle. Because prolonged post-implant annealing can result in donor species diffusion (8) and consequently deterioration of active device performance, pre-implant annealing is introduced as a means of extending the overall duration of the annealing cycle.

In fig.2 we present the activation efficiency map of an undoped S.I. GaAs wafer after a prolonged annealing cycle with the LTG furnace (fig.2b), together with a reference wafer annealed with a conventional horizontal tube furnace (fig.2a). The prolonged annealing cycle consists of a 15 min. pre and 10 min. post-implant anneal at 820°C in the presence of a $Si_3N_4$ cap. As shown, for this condition the fourfold symmetry in activation is no longer present and the corresponding on-wafer activation efficiency and uniformity (i.e. 75% and 2.9% respectively) are

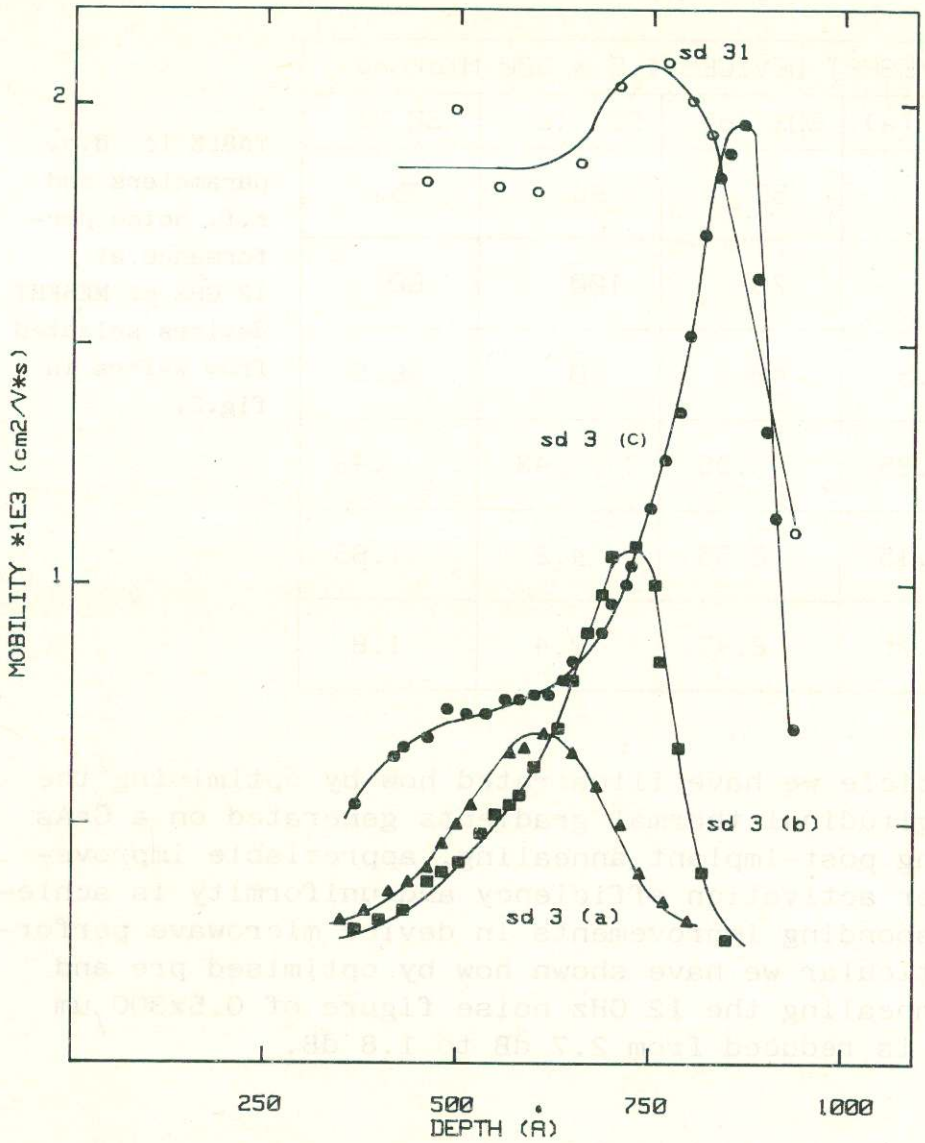


FIG.3 - Low-field mobility under the gate of 0.5x300 um MESFET devices selected from wafers in fig.2.

very similar to what is achievable with undoped ingot annealed material (fig.1c).

That the annealing cycle plays an important role in determining device performance is clearly illustrated by the results of low field mobility under the gate (7) and r.f. noise measurements presented in fig.3 and Table 1 respectively. Infact from MESFET devices selected from significant areas of the wafers shown in fig.2 we observe that:

- devices from low activation efficiency regions (i.e. $\eta \simeq 40\%$ as in A of fig.2a) have a very low mobility under the gate and as such a poor noise performance (typically 2.7 dB at 12 GHz);
- devices from medium-high activation efficiency regions (i.e. $\eta$ from 55 to 65% as in B and C of fig.2a) have increased mobility and improved noise performance (typically 2.4 dB at 12 GHz);
- devices from high activation efficiency regions, obtained by prolonged annealing with the LTG furnace (i.e. $\eta \simeq 75\%$ as in fig.2b) have an extended region of high mobility under the gate and good noise performance (typically 1.8 dB at 12 GHz).

| | MESFET DEVICES (.5 * 300 Micron) | | | |
|---|---|---|---|---|
| | SD 3 (a) | SD3 (b) | SD3 (c) | SD 31 |
| Act. Eff. $\eta$ (%) | 40 | 55 | 65 | 75 |
| Idss (mA) | 45 | 70 | 100 | 60 |
| gm (mS) | 37.5 | 40 | 40 | 46.5 |
| Cgs (pF) | .35 | .35 | .43 | .43 |
| Vth (V) | 2.15 | 2.55 | 4.2 | 1.85 |
| Nf (dB) | 2.7 | 2.45 | 2.4 | 1.8 |

TABLE 1: d.c. parameters and r.f. noise performance at 12 GHz of MESFET devices selected from wafers in fig.2.

## CONCLUSIONS

In this article we have illustrated how by optimising the radial and longitudinal thermal gradients generated on a GaAs substrate during post-implant annealing, appreciable improvement in on-wafer activation efficiency and uniformity is achieved with corresponding improvements in device microwave performance. In particular we have shown how by optimised pre and post-implant annealing the 12 GHz noise figure of 0.5x300 um MESFET devices is reduced from 2.7 dB to 1.8 dB.

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