SELF - CONSISTENT SIMULATION AND MANUFACTURING OF SPICE - DOPED GaAs FIELD EFFECT TRANSISTORS

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Abstract

The concept of a linear transistor, called δ-FET, was developed. The device conduction path is formed by a two-dimensional electron gas, and has a simpler construction in comparison to heterostructure devices, such as the High Electron Mobility Transistor (HEMT). A computer program was developed so as to self-consistently simulate the electrical and physical characteristics under the gate region. By using this simulations, the semiconductor film to be grown by MOCVD was optimized. The film showed a two-dimensional density of 1.10^{12} cm^{-2} *and FWHM of only 30 Å.*

The fabricated device characteristics were in good agreement with the simulated ones, with a transconductance of 130 mS/mm and cut-off frequency of 8 GHz. The promising features of this type of device are presented and analyzed.

Keywords: FET, delta doping, linear transistor

1. Introduction

High-speed field-effect transistors are largely used in high performance integrated circuits, manufactured with selectively doped heterostructures. In this type of device, the conduction channel is a two-dimensional electron gas, which shows a high electron mobility at low temperatures[1]. The purpose of this work is to study a device that features the good characteristics of a 2-DEG device, such as the HEMT, while being of simpler and less critical manufacturing. This transistor is called delta-FET (δ-FET).

2. Delta-FET

Delta doping[2,3] consists in confining doping atoms in a two-dimensional plane, instead of homogeneously doping the material.

The following features are expected from transistors manufactured with this kind of material:

-Easier construction, once it requires the growth of only one type of material, instead of a heterostructure such as the HEMT, thus avoiding the need for an excelent quality interface.

-High two-dimensional electron gas density, which leads to a low ohmic contact resistivity. In this way, a low noise figure is expected in comparison to a conventional MESFET.

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-High Schottky barrier breakdown voltage, once the barrier is made on undoped GaAs.

-Proximity of the 2-DEG to the gate, which implies in a high transconductance, improving the frequency performance of the device.

-High linearity of Ids current with Vgs, as will be shown next. This feature implies in low harmonic intermodulation, reducing noise and allowing for the design of more sensitive amplifiers.

By analysing the shown qualities of the δ-FET, it can be seen that this device will find direct applications in circuits requiring high sensitivity and low noise, such as low noise amplifiers for microwave and millimeter wave band.

2.1 Modelling and simulation

So as to study δ-FET physics, and aiming the optimization of the semiconductor film characteristics for further processing, a computer program was developed to simulate the transistor behaviour.

The program uses self-consistent routines for solving Poisson's equation in the region under the gate.

We show next some physics concepts used in the development of program DELTAFET:

In GaAs, electron drift velocity is a non-linear function of applied electric field[4].

Suppose a two-dimensional electron gas whose dimensions are width w and length L, under voltage V. One can calculate the flowing current, assuming the electric field along the gas has not reached the saturation value.

$$I = q.n_{2DEG}.w.\mu_o.\frac{V}{L} \qquad (1)$$

Where μ_o = low field electron mobility

With no voltage between drain and source a charge transfer between gate and electron gas occurs.

When applying voltage V_{ds} at drain terminal, a non-linear voltage distribution will occur along the channel, called $V_c(x)$, in the x-direction . Considering parasitics resistances as null, the voltage will vary from 0 V at the source to V_{ds} at drain.

Once the voltage along the channel is variable, so will be the electric field in the transverse direction. In this way, the free electron density will decay with x, given by

$$n_{2DEG}(x) = N_d^{2D} - \frac{\varepsilon\varepsilon_o}{q.d}.\left[V_{bi} - V_{gs} + V_c(x) \right] \qquad (2)$$

For I_{ds} computation, a linear first aproximation is assumed for the voltage $V_c(x)$ along the channel.

Using the vector $V_c(x)$, the charge density $n_{2DEG}(x)$ is computed, also showing a linear distribution.

The aproximate formula used for mobility was:

$$\mu(x) = \frac{\mu_o}{1 + \frac{E(x)}{E_{cr}}} \tag{3}$$

Where E_{cr} = critical field, where drift velocity begins to saturate

$E_{cr} \cong 3.2$ KV/cm

I_{ds} current, at each interval dx, is given by:

$$I_{ds} = q.n_{2DEG}(x).Z.\mu(x).\frac{\partial V_c(x)}{\partial x} \tag{4}$$

Where Z is the channel width.

Integrating both sides, we have:

$$\int_0^L \frac{I_{ds}}{q.n_{2DEG}(x).Z.\mu(x)} dx = \int_0^L dV_c(x) = V_{ds} \tag{5}$$

Isolating I_{ds},

$$I_{ds} = \left[\int_0^L \frac{1}{q.n_{2DEG}(x).Z.\mu(x)} dx \right]^{-1} . V_{ds} \tag{6}$$

With that value for I_{ds}, $n_{2DEG}(x)$ and $\mu(x)$, $V_c(x)$ is computed:

$$\int_0^x dV_c(\lambda) = V_c(x) = \int_0^x \frac{I_{ds}}{q.n_{2DEG}(x).Z.\mu(x)} d\lambda \tag{7}$$

One cycle of the iterative process is then finished. The complete sequence involves recalculating $n_{2DEG}(x)$, $\mu(x)$, I_{ds} and $V_c(x)$ until I_{ds} convergence occurs.

Until now, the modeling considered null parasitics. However, the real device has access resistances R_s and R_d and a leakage resistance that shunts the channel, R_{leak}.

In this way, the channel current is calculated by the iterative process shown above, known V_s' and V_d'. However, these voltages are dependent upon the channel current and the leakage current. The latter can be calculated analitycally:

$$I_{leak} = \frac{V_{ds} - (R_s + R_d).I_{chann}}{R_{leak} + R_s + R_d} \tag{8}$$

I_{ds} current will be:

$$I_{ds} = I_{leak} + I_{chann} \tag{9}$$

Voltages V_s' and V_d' will be:

$$V_s' = R_s.I_{ds} \tag{10}$$

$$V_d' = V_{ds} - R_d.I_{ds} \tag{11}$$

In this way the problem consists in iteratively solving for I_{ds}, finding voltages V_s' and V_d' that will result in channel and leakage current that added will result in I_{ds}.

For device simulation based on these equations, the computer program DELTAFET was written.

Program inputs are doping planar density, gate length and width, low field electron mobility, bias point, Schottky barrier built-in voltage, cap-layer thickness and resistances.

The program outputs are $I_{ds} \times V_{ds}$ curves and device parameters at a given bias such as transconductance, C_{gs} capacitance, pinch-off voltage, bias current and transition frequency.

The program also shows the voltage, mobility and density distributions along the channel, until the point where saturation starts to occur. Charge accumulation and domains formation where not considered in the program.

We show some simulation results done with DELTAFET program, where input and output data are shown, together with $I_{ds} \times V_{ds}$ curves in figure 1.

2.2 Semiconductor film characteristics and growth

By using DELTAFET, we were able to optimize the growth of the semiconductor film.

A high planar density of the electron gas was found to be needed, in the order of 5.10^{12} cm^{-3}, so that the gate metal to the delta layer distance can be reduced to a few hundred of angstrons without the electron gas being depleted. In this case, the δ-FET can shows high transconductances, in the order of 600 mS/mm, as computed by the program.

On the other hand, the device performance is tied directly to electron mobility, which decays with electron density. So, there must be a trade-off between electron density and mobility.

Simulations resulted in a linear I_{ds} behaviour in respect to gate voltages, thus there is a flat region in the device transconductance, phenomenon attributed to the two-dimensional gas properties. This linear characteristic is one of the advantages of such a device, making it of strategical importance to microwave circuits that need low noise figure and low harmonic intermodulation.

So, we suggested the growth of a GaAs semiconductor film with Silicon planar doping of 5.10^{18} cm^{-2}, with cap-layer thickness of 700 Å that should be recessed to 250 - 300 Å.

The GaAs film was grown by Metallorganic Chemical Vapour Deposition - MOCVD.

Trimethil Gallium and Arsine were used as sources of Gallium and Arsenium, respectively.

The growth temperature was 650°C for undoped layers and 750 °C for the delta layer, where Silane (SiH_4) where used as Silicon source.

Capacitance-voltage[5] characterization revealed the presence of a delta layer buried at 700 Å from surface, with a peak 3-D density of 4.10^{18} cm^{-3} and a residual density at the buffer of $\cong 10^{15}$ cm^{-3}. A

full width at half maximum found was 30 Å, showing the reached high degree of confination.

The planar density calculated corresponds to 1.10^{12} cm^{-2} which, although being lower than expected, was enough for processing a initial device, after simulation with DELTAFET.

2.3 Device processing and characterization

The processed device had a gate width of 1.2 μm, recessed to 500 Å. Ohmic contacts were fabricated using AuGe/Ni/Au and Ti/Au was used for the Schottky barrier gate. DC measurements showed a maximum current of 23 mA and I_{dss} of 0.8 mA. Maximum transconductance was g_m = 131 mS/mm, reasonable when considering the technology available. Parasitics resistances for source and drain were R_s = 11.75 Ω and R_d = 12.55 Ω. Characterization curves are shown in figure 2. The obtained data was used as inputs to DELTAFET program so as to test its reliability. The curves and output data are annexed in figure 3.

We observed good agreement between simulation and practice.

The simulated transconductance was 128.5 mS/mm, in comparison to 131 mS/mm obtained experimentally.

Due to the low density, we did not observe a flat region in the transconductance, once the gas is easily depleted with negative voltages and reaches the maximum density value (dopant density) for small positive voltages.

By increasing the density, we expect to enlarge the transconductance curve, which will show the flat region, and to reduce the parasitic resistances. Frequency characterization was done using a Cascade prober, revealing a cut-off frequency of 8 GHz.

3. Conclusions

The project of a planar doping transistor was developed, and the device seems to be suitable for low noise and high linearity applications.

Self consistent simulation was functional and of great utility during the first steps of the project, once allowing for definitions of influent parameters on the device performance, beside proving the expected device linearity.

Experimental first results of a device processed on a non-optimized film proved its feasibility, once a 130 mS/mm transconductance and a cut-off frequency of 8 GHz were obtained, results similar to comercial MESFETs using the same technology.

It is intended to improve the δ-FET performance by growing new films with higher planar densities, thus reducing parasitics resistances, lowering noise and flattening the transconductance.

4. Acknowledgements

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5. References

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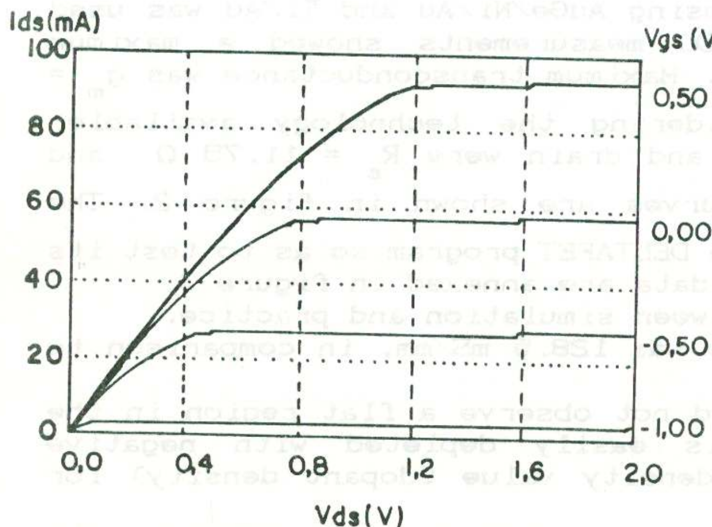

Fig.1 *Simulated curves using the following parameters:* $Nd=5e12\ cm^{-2}$ $Lg=1\ \mu m$ $\mu=3300 cm^2/Vs$ $Vbi=0.6V$ $d=250A$ $Rs=Rd=4Ohms$ $Rleak=1KOhm$

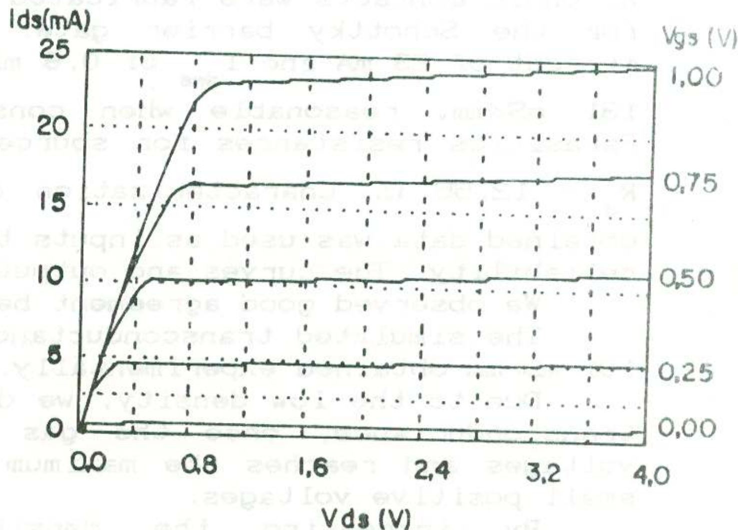

Fig.2a *Processed device drain characteristics*

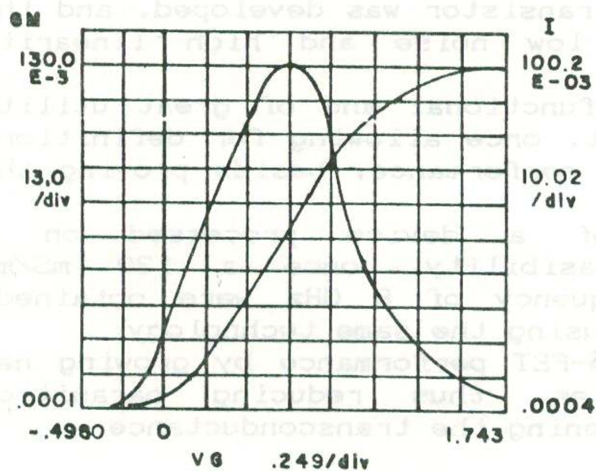

Fig.2b *Processed device* $I_{ds} \times V_{gs}$ *and transconductance*

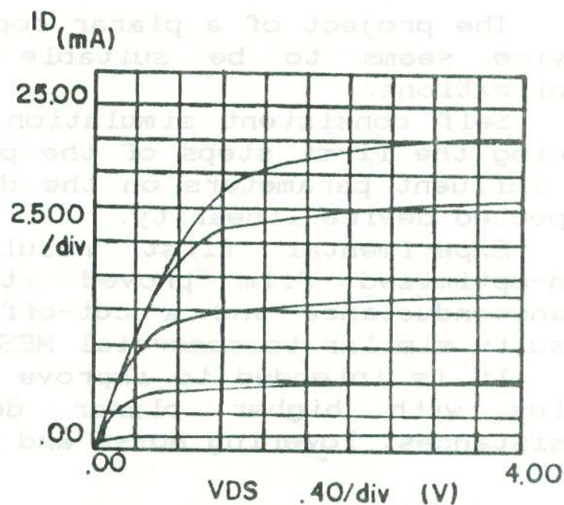

Fig.3 *Simulated curves using the real device parameters as program inputs*