STANDARD MULTIFUNCTION MMIC CHIP FOR PHASE LOCKED MICROWAVE OSCILLATORS

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ABSTRACT

This paper presents the design and realization of a new fully integrated multifunction circuit which is of great interest for all applications that need low cost phase locked microwave oscillators. The realization described here is in X band, but the design can be easily extrapolated up to millimeter frequencies. Experimental results are presented about all the MMIC's functions. A low cost package, also extrapolable up to higher frequencies is described.

INTRODUCTION

The main idea is related to the observation that for phase locked loops all necessary components are generally commercially available at low cost prices, except for the microwave circuits (i.e. all circuits above 5 to 10 GHz). Further, if a set of the necessary microwave circuits is sufficiently wideband, the exact desired frequency can be fixed with the same set by conveniently choosing the total division ratio, the reference quartz and the dielectric resonator. Finally, the low cost objective can be reached if this set of multiapplication functions are realized in GaAs MMIC technology on a single chip.

Figure 1 shows the block diagram of the integrated circuit. The following microwave functions were realized :

- negative resistance for oscillation
- cold FET varactor for tuning
- frequency multiplier
- analog frequency divider

In order to reduce the RF coupling between function, it is necessary to insert attenuators and buffer amplifiers. Actually, the main problem is to correctly match the input and output ports of a non linear circuit. An attenuator followed by a buffer amplifier is an effective solution to solve this problem, even if it decreases electrical chip efficiency. The design was made for an output frequency band of 10 to 12 GHz. An example of Voltage Controlled Dielectric Resonator Oscillator is given at 10.75 GHz. The oscillation is at F0/2, followed by a frequency multiplier and a frequency divider. This choice was a compromise between different considerations :

- to simplify the optimum setting of the resonator position for a DRO application. The difficulty increases with the frequency
- to minimize the size of the packaged module
- to reduce the off-carrier noise characteristics

The divided frequency F0/4 has a value compatible with existing digital dividers which allows to complete the phase locked loop.

This principle may be used up to millimeter frequencies with an optimization over the multiplier and divider ratio. For example, it is interesting to increase the multiplier ratio to keep easy the setting of the dielectric resonator coupling. The divided frequency has to remain as low as necessary to reduce the final cost.

The purpose of this paper is a description of design, measurement and packaging of the multifunction chip.

VOLTAGE CONTROLLED OSCILLATOR

The main problem is to integrate the varactor with a standard technological process. Several realizations were made [1], [2] with a specified process to obtain a 10 : 1 capacitance ratio, but the limitation is generally related to the low quality factor. This varactor usually must not be used over its whole capacitance ratio because of increasing series resistance with the reverse tuning voltage.

However, a wide band tuning is not necessary for this application and the use of low capacitance ratio is sufficient ($\simeq$ 2 to 4). The FET gate to source Schottky diode capacitance (Cgs) can be used as a varactor versus the gate to source voltage Vgs. A first approach consists of tuning directly the Cgs capacitance of the oscillating FET [3], but the main problem is the dependance between output power and frequency. Other possibility is the use of a cold FET as a diode. A non linear equivalent circuit is given in figure 2. Drain and source are connected and the non linearity Cgs is only depending upon the voltage Vgs (=Vgd). Capacitance ratio and quality factor can then be optimized in relation to the gate length. A short gate length provides a low capacitance ratio, but a high quality factor. A 0.5 to 1 µ gate length seems to be the best compromise.

An association between a biased FET to give the gain loop and a cold FET are an ideal integrated device to reach high frequency narrow band VCO. Since the FET is a 3 ports component, it allows a great versatility in the choice and realization of associated circuits. Figure 3 gives the oscillator circuit diagram. A compromise was made between bandwidth and linearity, and the best configuration is to put the varactor in the source to obtain the oscillating condition thanks to an inductance in the gate. This gate port is also chosen as for output port : for VCO application, the center frequency can be adjusted with external inductance ; for DRO application, it allows to couple the resonator.

FREQUENCY MULTIPLIER

An active FET frequency doubler is used. It operates as a "B class amplifier". In order to understand the behaviour of FETs operating as a frequency multiplier, it is interesting to consider the simplified model shown in Figure 4. A sinusoïdal gate voltage at F0, gives a drain current pulse signal which may be described in Fourrier series. The drain current component In at nF0 is a function of the gate conduction angle 20g and may be optimized. It can be shown that the optimum value is 0gopt = 120°/n [4]. Knowing 0gopt and the characteristic Id = f (Vgs, Vds) shown in Figure 4, the optimum gate bias voltage and/or the input power can be deduced. Using a gate self-bias condition (DC open circuit) the only remaining parameter is the input power. The optimum output load is given by the maximum peak to peak drain voltage and the optimum current at nF0. This load is generally made by a parallel tuned circuit at nF0 (the fundamental is short circuited). To improve the output power and the added efficiency, a feedback circuit can be added at nF0 from drain to gate. This approach may avantageously be used for specific designs.

ANALOG FREQUENCY DIVIDER

The analog frequency divider or dynamic frequency divider is based upon the frequency regenerative properties of a non linear device coupled to a feedback loop [5] [6]. Figure 6 shows an example of 1:2 divider. The working principle is based on a closed loop in which the output signal at the divided frequency is fed-back and mixed with the input signal to produce a lower sideband at the divided frequency which is filtered and injected through the input amplifier. The simplest way to realize such loop is by using a single FET whose non linearities allow :

- to oscillate at the desired output frequency
- to introduce a mixing functionality

Such dividers have a limited bandwidth but their simplicity and their ability to perform frequency division up to millimeter waves make them very attractive for communications purposes.

The circuit diagram is given in Figure 7. A first step in the design is to obtain the oscillation circuit at the output frequency (F0). A good isolation from the input port is obtained with a short circuit at F0. A parallel tuned circuit connected to the source localizes the FET negative resistance. A matching network at input frequency (2/F0) maximizes the gate injected power necessary to synchronize the oscillator.
Some applications may require stability in the absence of input signal. The simplest way is then to reduce the transistor gain by controlling the gate voltage. However, phase locked oscillators always drive the divider so that negative voltage may be removed.

PACKAGING

For VCO applications, small SMD packages can be used depending on the operating frequency.
For DRO applications, a low cost package was developped (Figure 8). It consists of an association of a glass teflonide substrate, MMIC chip, SMD external components, dielectric resonator, metallic support, cover and tuning screw. The MMIC is sticked on the substrate an bounded according to "ball bonding" process with gold wires or "wedge bonding" process with gold or aluminium wires. Low dielectric constant substrate ($\simeq$ 2.5) and mechanical tuning allow automatic positioning of the resonator. RF (and bias) transitions are developped up to 12 GHz using only a double sided printed circuit board. A hermeticity greater than 10^{-5} atm/cm^3 x s is obtained and insures a long term operation. This packaging together with the single chip design leads to a new product family much useful for low cost frequency synthesis.

EXPERIMENTAL RESULTS

Three chips were realized with the following functions
(1) - VCO and buffer amplifiers (two outputs)
(2) - Multiplier and divider
(3) - All the functions
The size is respectively 2x1, 2x1 and 2x2 mm^2
The following results have been reproducely achieved :

VCO (chip n°1, Figure 9)

Frequency bandwidth	: > 15 %
Center frequency	: 6 GHz
Output power (2 ports)	: > 14 dBm
Off carrier noise	: <-80 dBc/Hz at 100 KHz
	: <-105 dBc/Hz at 1 MHz
Harmonics	: <-20 dBc

Frequency multiplier (chip n°2)

Frequency bandwidth	: 20 %
Center input frequency	: 5.5 GHz
Input power	: 15 dBm
Output power	: 10 dBm
Harmonics and subharmonics rejection	: <-15 dBc

Frequency divider (chip n°2)

Frequency bandwidth	: 20 %
Center input frequency	: 5.5 GHz
Input power	: 15 dBm
Output power	: 11 to 14 dBm
Harmonics and subharmonics rejection	: <-15 dBc

DRO (chip n° 3, Figure 10)

At F0 port

Frequency	: 10.75 GHz
Electronic tuning	: >5 MHz
Output power	: >7 dBm
Off carrier noise	: -85 dBc/Hz at 10 KHz
	: -110 dBc/Hz at 100 KHz
Harmonics and subharmonics rejection	: <-15 dBc
At F0/4 port	
Center frequency	: 2.6875 GHz
Output power	: >7 dBm
Off carrier noise	: 12 dB lower than F0 port

CONCLUSION

An inovative multifunction MMIC chip has been developped, incorporating all the microwave analog circuits needed for phase locked oscillator applications. This work should contribute to reduce the size and the price of transmitters and receivers used in radio communication equipments. The presented realization concerns a 10-12 GHz frequency range, based on an oscillator at 5-6 GHz, a frequency multiplier and a frequency divider. This chip may be used as a VCO with 15 % tuning bandwidth and off carrier noise better than -80 dBc/Hz at 100 KHz. It may also be used as a DRO with tuning bandwidth greater than temperature shift and off carrier noise better than -85 dBc/Hz at 10 KHz. In both cases, output power is greater than 7 dBm at F0 and F0/4 port.
Single chip and packaging design can be extrapolated up to higher frequencies leading to a new product family.

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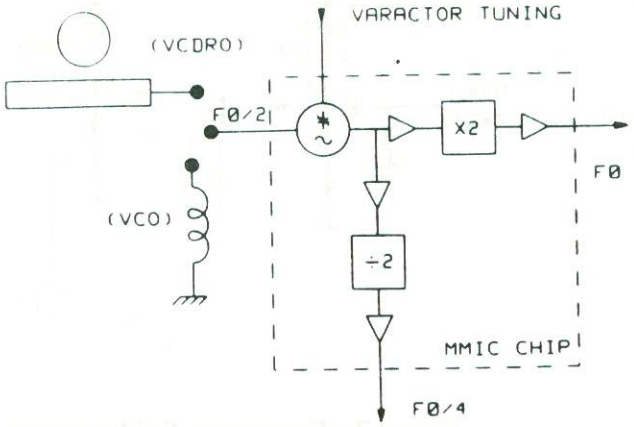

Figure 1 : Block diagram of integrated circuit

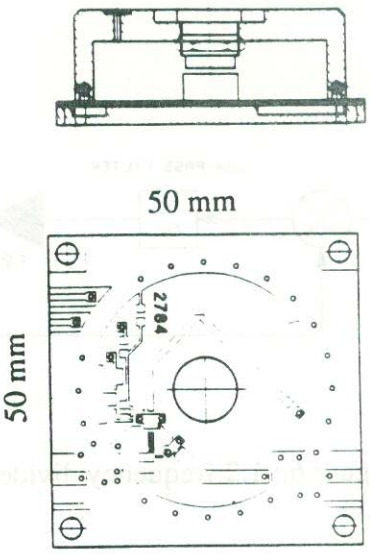

Figure 8 : Low cost DRO package

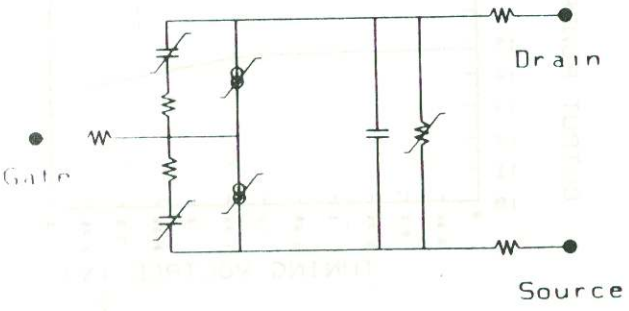

Figure 2 : Cold FET non linear equivalent circuit

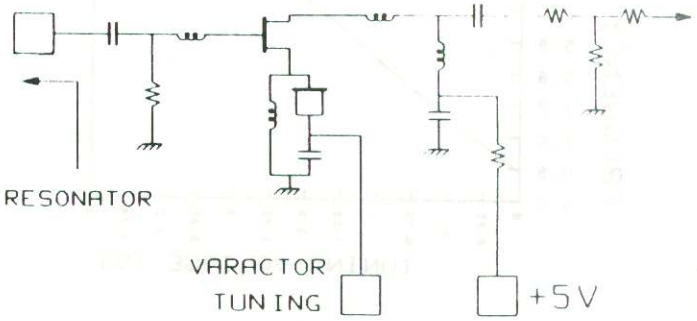

Figure 3 : Oscillator circuit diagram

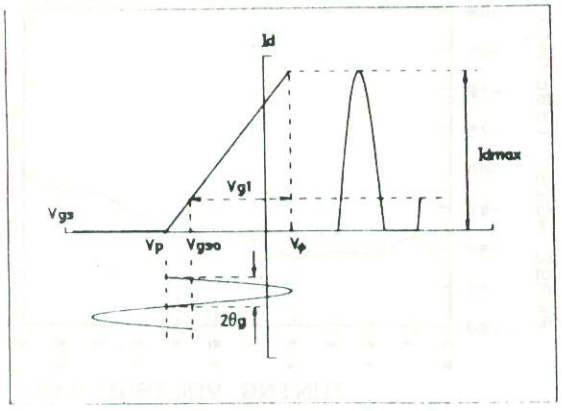

Figure 4 : Simplified model of operating multiplier

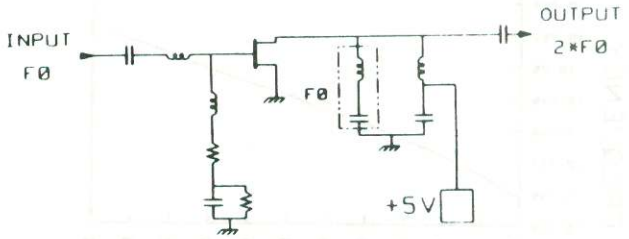

Figure 5 : Multiplier circuit diagram

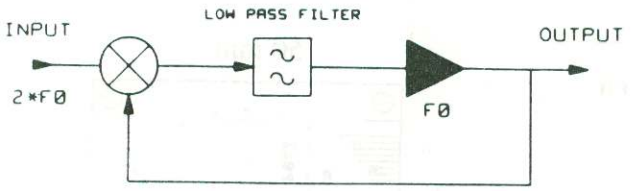

Figure 6 : 1:2 frequency divider loop

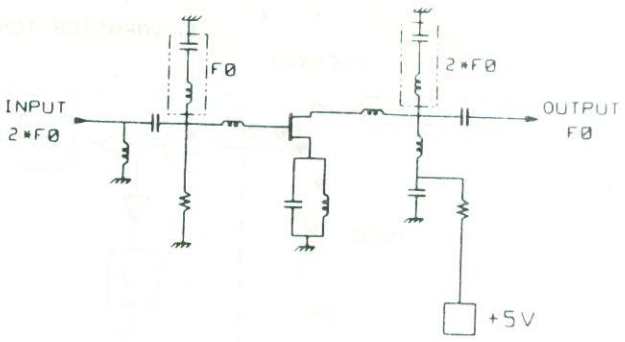

Figure 7 : Frequency divider circuit diagram

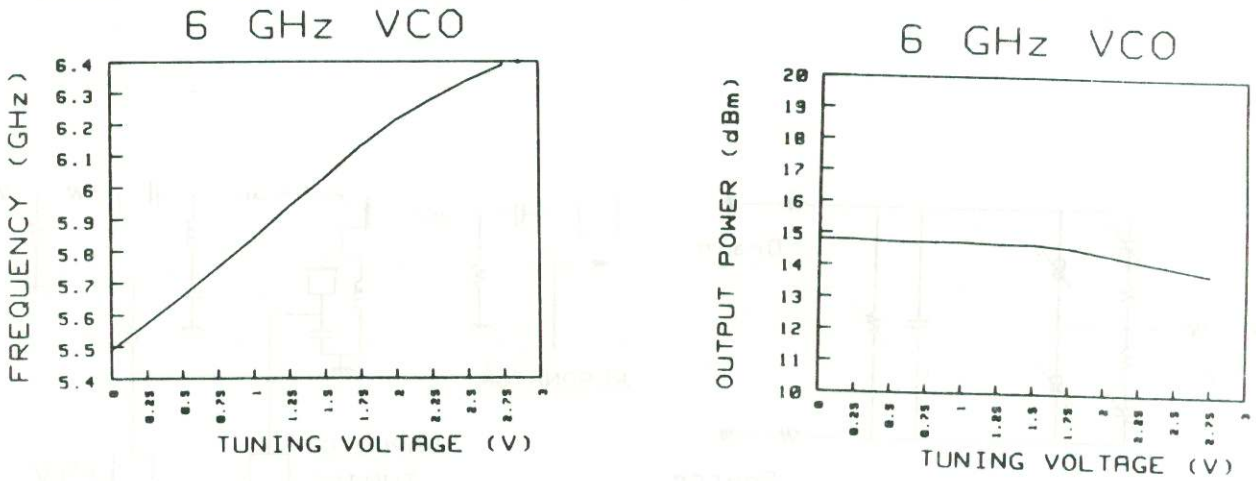

Figure 9 : VCO characteristics with chip n° 1

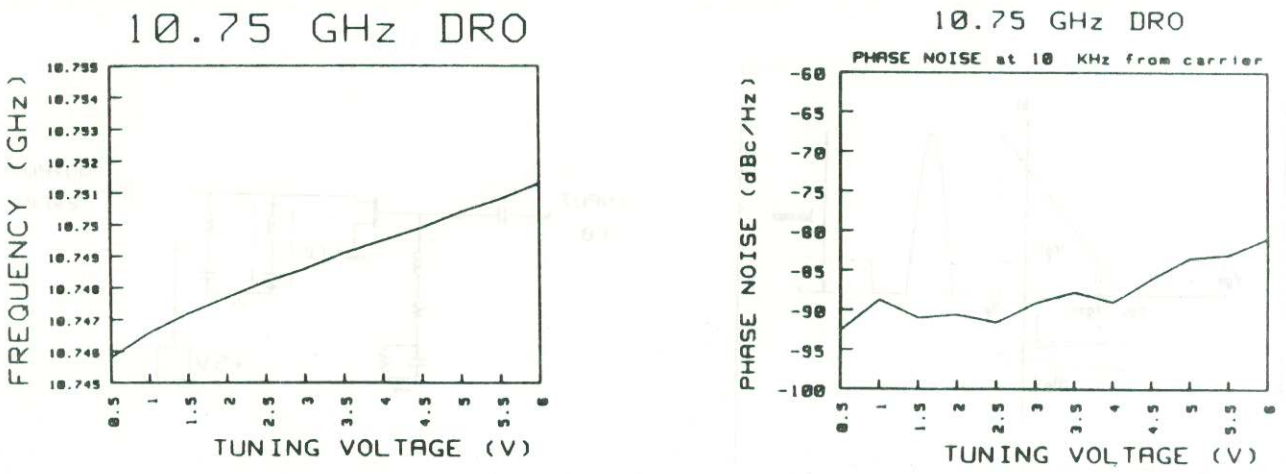

Figure 10 : DRO characteristics with chip n° 3