OPTIMIZATION OF MULTIHETEROJUNCTION AlGaAs/GaAs HEMTs FOR MICROWAVE POWER AMPLIFICATION

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ABSTRACT :

A theoretical and experimental study concerning a three channels power HEMT is presented. The structure has been, first, optimized using an adequate simulation. Then many technological realizations have been achieved at the laboratory. Measurements performed with these devices give results very encouraging and permit to foresee superior performances relatively to that of GaAs power MESFETs.

I. INTRODUCTION

In the last few years, the great interest of single heterojunction HEMTs for low noise amplification has been clearly demonstrated. More recently multiheterojunction HEMTs have been shown to be able to offer promising potentialities for power applications [1 - 4]. But until now only fragmentary studies have been carried out. The present paper reports a systematic study on this subject. It comprises, first, a device simulation with emphasis toward the particular structures suitable for power amplification and, second, experimental and technological optimization.

II. THEORETICAL EPILAYERS OPTIMIZATION

Multilayer structures with several 2D electron gas channels are very complex systems. Their simulation in reasonable time seems difficult, even impossible. Accordingly we have been only interested in the charge control of the channels without taking into account the application of the drain-source voltage. We have considered a one dimensional model based upon the solution of Poisson and current continuity equations using Fermi-Dirac statistics and taking into account the DX centers. With this model we determine all the charges existing in the structure and their command by the gate voltage V_{gs}.

The optimization criteria care for three points :

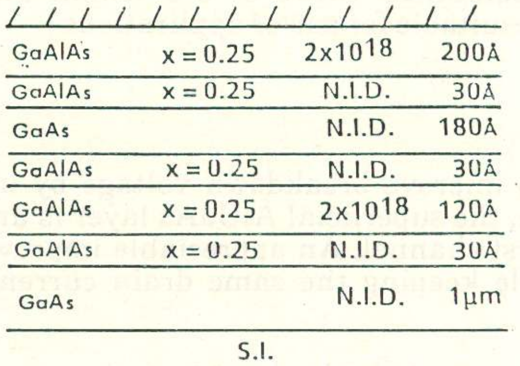
1. Good linearity of the total interfacial charge control $\partial N_s/\partial V_{gs}$. This condition implies evidently that the channels should be near each other, to conduct the current in relays without many discontinuities.

2. Maximum transconductance. This implies that the gate electrode should be as near as possible to the different channels.

3. Maximum saturation current I_{sat}. This condition implies a maximum interfacial charge N_s, which necessitates having the channels sufficiently separated from each other to avoid eletrostatic interactions.

These criteria can't be achieved simultaneously as it is illustrated in figures 1 and 2. The simulated structure corresponding to these figures, contains three heterojunctions with 30 Å spacers. It's patent that doubling the layer thicknesses results in a 35 % growth of N_S. But, in return, a pronounced non linearity makes the structure unsuitable.

Many other simulations were achieved. They tended to demonstrate that the structure shown in figure 1a constitutes a good compromise for the different above requirements.



GaAlAs	x = 0.25	2x10^18	200Å
GaAlAs	x = 0.25	N.I.D.	30Å
GaAs		N.I.D.	180Å
GaAlAs	x = 0.25	N.I.D.	30Å
GaAlAs	x = 0.25	2x10^18	120Å
GaAlAs	x = 0.25	N.I.D.	30Å
GaAs		N.I.D.	1µm
S.I.			

Fig. 1a

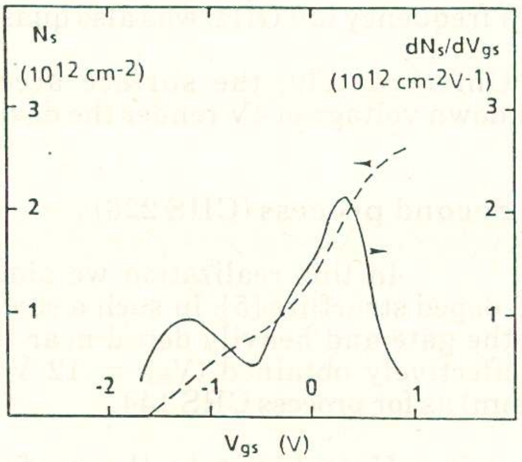
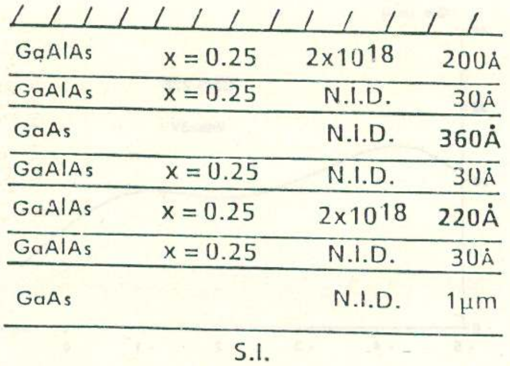


Fig. 1b



GaAlAs	x = 0.25	2x10^18	200Å
GaAlAs	x = 0.25	N.I.D.	30Å
GaAs		N.I.D.	360Å
GaAlAs	x = 0.25	N.I.D.	30Å
GaAlAs	x = 0.25	2x10^18	220Å
GaAlAs	x = 0.25	N.I.D.	30Å
GaAs		N.I.D.	1µm
S.I.			

Fig. 2a

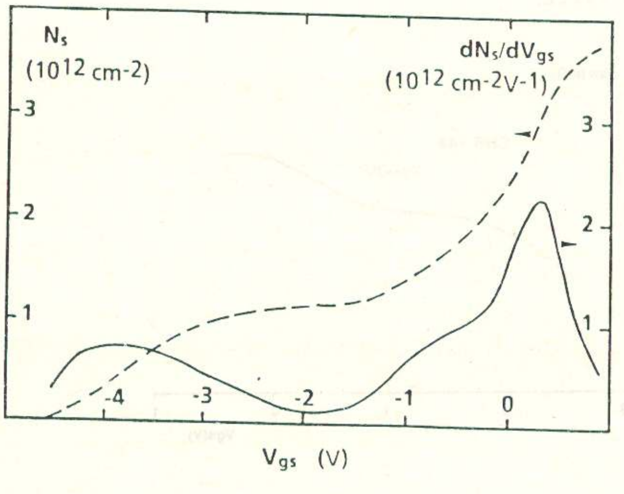


Fig. 2b

Figure 1 and 2 : Typical examples of the influence of the structure arrangement on the charge control.

III. TECHNOLOGICAL REALIZATIONS AND EXPERIMENTAL CHARACTERIZATION

1. First process (CHS 144)

This structure is issued from the simulation (figure 1a). It has a 0.8 µm gate length in a 2 µm recess. The access zones are realized using diffusion through a cap layer doped at 2.10^{18} cm^{-3} on a thickness of 2 000 Å. It's characterization showed a saturation current of 460 mA/mm and a pinch-off voltage of - 2.5 V. The transconductance evolution was much similar to that predicted by theory but with much less non linearity (figure 3). Its maximum value was 150 mS/mm. The current cut-off frequency (20 GHz) was also quasi independent of V_{gs}.

Unfortunately, the surface access resistance value of 0.8 Ω.mm and the breakdown voltage of 4V render the device unsuitable for power applications.

2. Second process (CHS 226)

In this realization we aimed to improve breakdown voltage by using a pulse-doped structure [5]. In such a structure, the superficial AlGaAs layer is undoped near the gate and heavily doped near the first channel. An appreciable improvement was effectively obtained (V_{br} = 12 V) while keeping the same drain current (470 mA/mm) as for process CHS 144.

Unfortunately the surface access resistance was again very high (1.1 Ω.mm), due to a too large recess width (0.5 µm gate length in 2 µm recess width). Its effect was disastrous on the transconductance and the current gain cut-off frequency, causing strong degradation of these quantities in the neighbourhood of 0 Volt (Fig. 4) and leaving finally a maximum available gain cut-off frequency f_{max} only of 27 GHz.

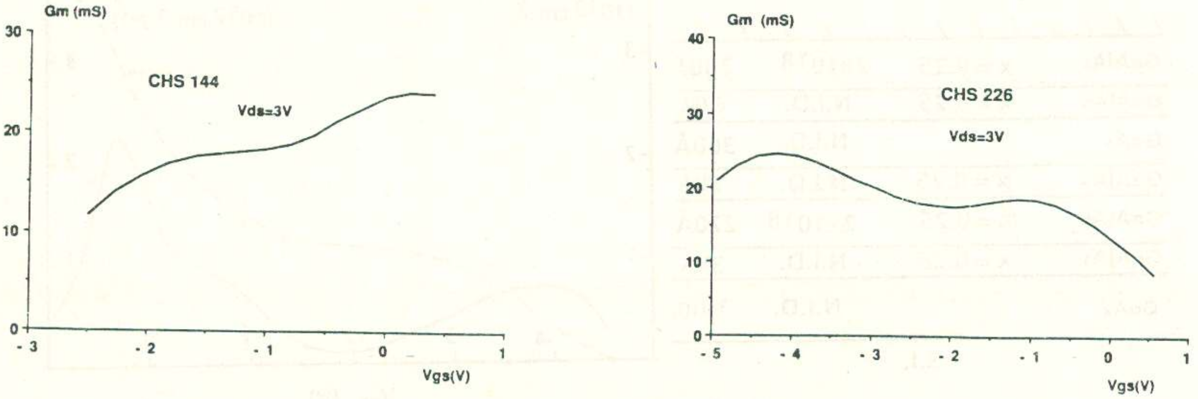


Figure 3

Figure 4

Figures 3 and 4 : Evolution of the transconductance as function of Vgs for the HEMT series CHS 144 and CHS 226.

3. Optimum process (CHS 233)

For this process (fig. 5) we used the same epilayer arrangement as in the previous process but a narrow gate recess (0.5 µm gate length in 0.8 µm recess width) was realized in order to reduce as much as possible the source resistance.

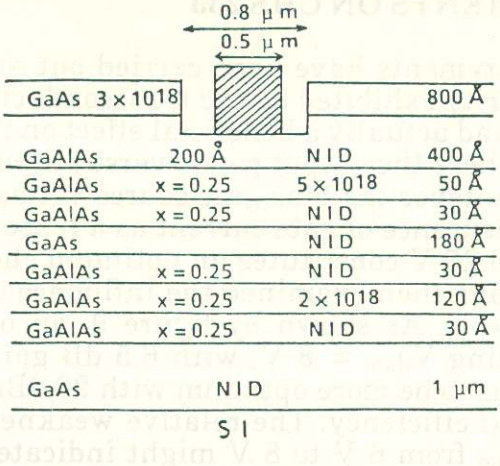


Figure 5 : Optimal HEMT structure : CHS 233.

The corresponding characterization results are summed up in table I where, for comparison, are also given the results obtained in the case of processes 144 and 226. It can be noted, in particular, very good values for breakdown voltage (15 V) together with a low source resistance (0.34 Ω.mm). On the other hand the maximum available gain extracted from scattering parameters, was found to exhibit a quasi flat response versus the gate-source voltage (Fig. 7). Such a behavior has to be correlated with both the transconductance and the current cut-off frequency responses of the device (fig. 6).

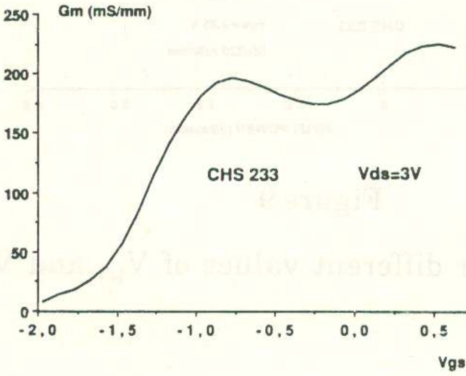


Figure 6

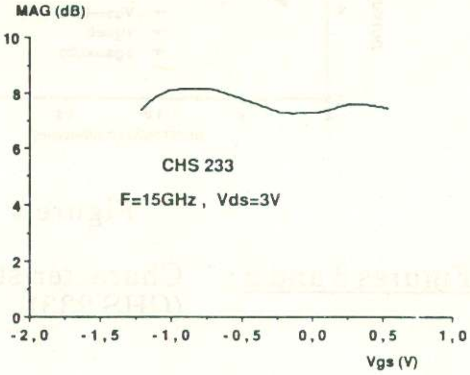


Figure 7

Figures 6 and 7 : Evolution of the transconductance and the maximum available gain of the HEMT CHS 233 showing its excellent linearity.

PROCESS CHS	Idss mA/mm	Vp volt	Gm max mS/mm	Rs Ω.mm	Fc GHz	Fmax GHz	Vbr volt
144	460	-2.5	150	0.8	20	35	4
226	470	-4.5	165	1.1	30	27	12
233	450	-2	210	0.34	25	42	15

Table I : Summary of the characterization of the different realized multichannel structures.

IV. POWER MEASUREMENTS ON CHS 233

All the measurements have been carried out at 15 GHz. We have, first, verified that the high linearity exhibited by the transconductance and the current cut-off frequency of the device had actually a beneficial effect on its power behavior. This is clearly shown by figure 8 where the output power versus input power response appears to be nearly unchanged whatever the bias gate source voltage is, from - 0.75 V to 0V. Nevertheless, taking the occurence of gate current as a reasonnable limit of operation, it appeared that V_{gso} = - 0.25 V constitutes an optimum choice. Retaining this gate-source bias condition we have then examined the influence on power performances of the drain-source voltage V_{dso}. As shown by figure 9, an output power of about 27 dBm/mm was obtained, using V_{dso} = 8 V, with 6.5 dB gain and 25 % power added efficiency. V_{dso} = 6 V seems to be more optimum with 26 dBm/mm output power, 6 dB gain and 30 % power added efficiency. The relative weakness of power enhancement provided by increasing V_{dso} from 6 V to 8 V might indicate that the device does not benefit entirely from the corresponding available output voltage swing. This point is the scope of a particular study carried on in our laboratory.

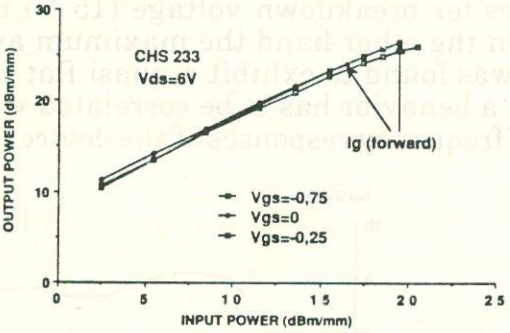


Figure 8

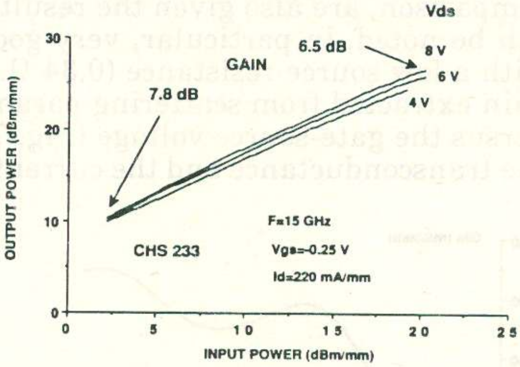


Figure 9

Figures 8 and 9 : Characteristics $P_{out} = f(P_{in})$ for different values of V_{gs} and V_{ds} (CHS 233).

IV. CONCLUSION

An optimized three channel HEMT, using AlGaAs/GaAs material system, has been demonstrated to be able to offer simultaneously a drain current of 500 mA/mm, a drain-source breakdown voltage at pinch-off about 15 V and a maximum available gain cut-off frequency higher than 40 GHz over almost the full range of the gate-source voltage. In contrast to what we thought at the begining of this study, we have found that the linearity is an advantage of the multilayer structure when this one is well optimized.

Promising power performances have been obtained, at 15 GHz, using a 0.5 μm gate length device, with 27 dBm/mm output power, 6.5 dB gain and 25 % power added efficiency. It may be though that substantial improvement can be achieved using a four channels structure. Such a device will be presented in a near future.

ACKNOWLEDGEMENT

The authors wish to acknowledge B. GRIMBERT, P. LEGRY and A.FATTORINI for processing of the above devices.

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