# RAPID THERMAL ANNEALING OF Si IMPLANTED GaAs IN ARSENIC OVERPRESSURE

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Abstract: A new method of rapid thermal annealing (RTA) in arsenic overpressure using a high thermal mass reactor and a very low thermal mass substrate holder has been developed.
Efficient activation of Si implantation has been obtained only with proper As overpressure. The design of the substrate holder allowed a very uniform activation of the implanted layers as well as a negligible formation of dislocation slips.
This method of rapid thermal annealing was successfully applied to the fabrication of broadband 4-8 GHz MMIC amplifiers.

## Introduction

Rapid thermal annealing (RTA) of ion implanted GaAs is a viable method to activate the implanted ion species minimizing dopant redistribution.
However, the thermal dissociation of GaAs cannot be ignored at the temperatures needed in this process, even in the shortest annealing cycles [M.Kuzuhara et al. Appl.Physics Letters 58 (3),1204 (1985)].
Conventional RTA reactors suffer from a poor temperature control and difficulty to safely supply an As overpressure during annealing, giving rise to non reproducible results in term of dopant activation and uniformity.
We propose an original solution to these problems by using a reactor with a high thermal mass and a substrate holder with extremely low thermal capacitance, allowing annealing times comparable to conventional infrared lamps heated susceptors, but with the advantages of maintaining the samples in a suitable As overpressure and at a well controlled and reproducible temperature.

## Experimental and results

2" semiinsulating GaAs wafers were implanted with doses of 5xE12 $cm^{-2}$ and 5xE13 $cm^{-2}$ of Si 29 at an energy of 100 keV. The samples were treated at 870°C, 900°C and 930°C for time periods ranging from 10s to 240s including the heating time.
A hot wall type reactor and a very low mass quartz sample holder were used to accomplish the annealing cycles.
Fig.1 shows a sketch-plan of the annealing equipment. A trimethylarsenic source was used to supply the needed As overpressure [M.Pillan et al.5$^{th}$ III-V Semiinsulating Materials Conference, Malmoe (1988) pp.87-92] and hydrogen was used as carrier gas.
Reproducible annealing cycles could be performed even at the shortest treatment times and due to the special design of the sample holder, the dislocation slip formation was almost avoided.

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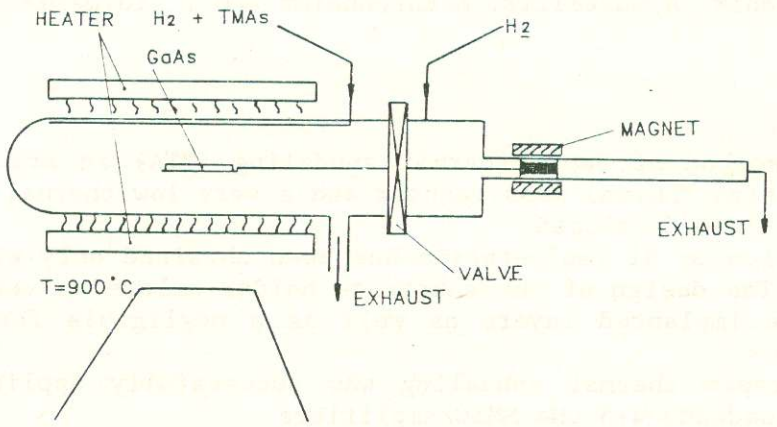


Fig.1 - Layout of the annealing apparatus.

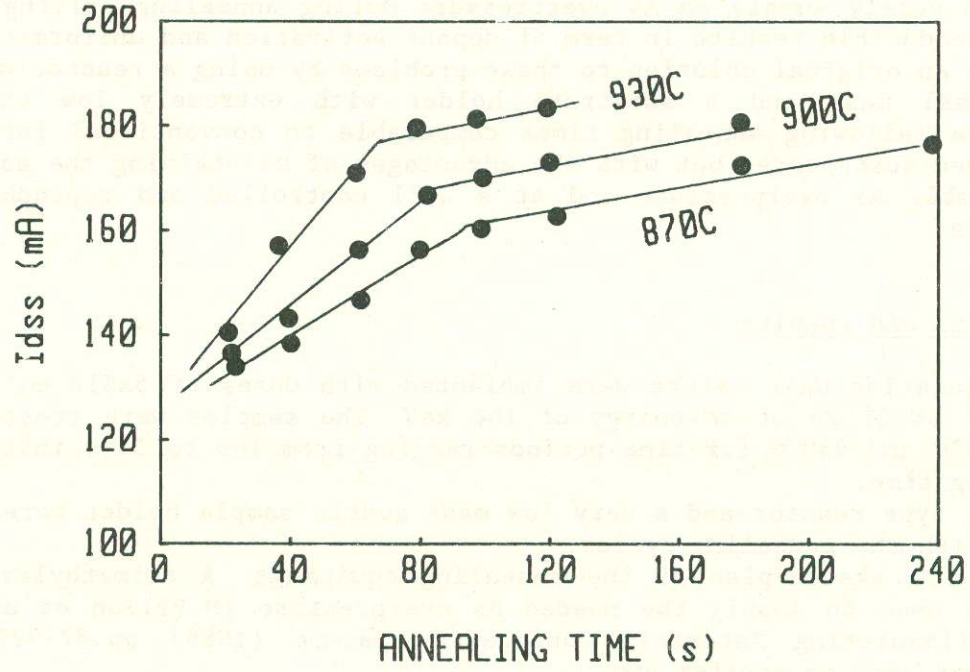


Fig.2 - Gateless FET saturated current as a function of annealing time for Si implanted GaAs with a dose of $N_D$=5XE13 $cm^{-2}$ at temperatures of 870°C, 900°C, 930°C, $P_{TMAS}$ = 2.5 torr.

The annealed samples were characterized by integrated test pattern containing gateless FET's, sheet resistance devices, long gate FET's and 1 micron gatelength FET's. Bidimensional mapping of the relevant parameters was also realized both in macro and microscale to assess their uniformity across a 2" GaAs wafer.
Fig.2 shows the plot of gateless FET saturated current for samples implanted with a dose of 5XE13 $cm^{-2}$ of Si29 as a function of the annealing time for three different temperatures of treatment: 870°C, 900°C, 930°C.
This is and indirect measurements of activation since:

$$I_{DSS} = q\, V_{SAT} \int_0^{\infty} N(x)\, d_x = q\, V_{SAT} N_S \qquad 1)$$

where $N_S$ is the activated dose which in our case will be underestimated by the presence of an asymmetrical space charge in the implanted layer due to a surface potential induced by surface charges.
At each annealing temperature, the current (i.e. the activation) is increasing linearly up to a value of about 175-180 mA and then its increase is very small.
We think that the activation of Si takes place in the first annealing stage and a slight Si redistribution begins during the second stage.

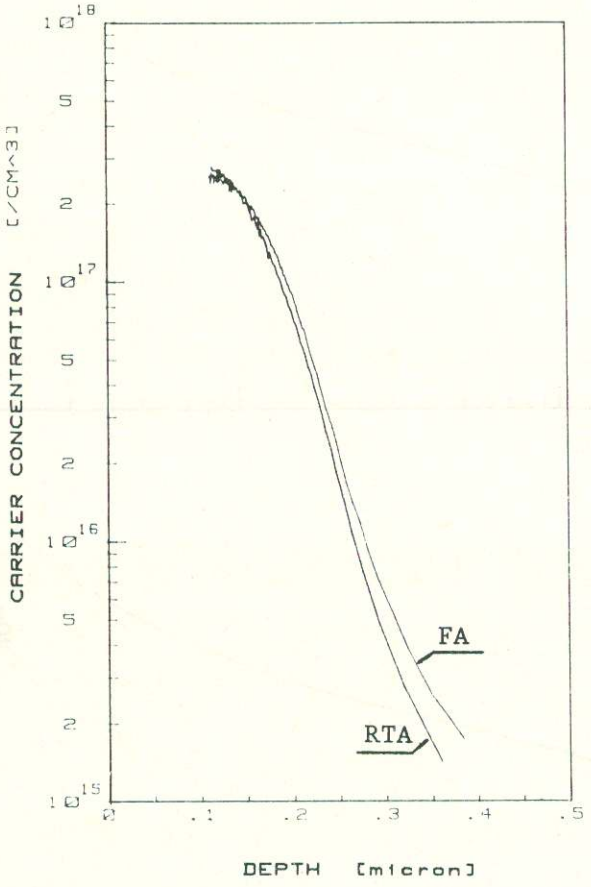


Fig.3 - Comparison between carrier concentration profiles of a conventional 850°C furnace-annealed and RTA 900°C annealed Si implanted wafers with a dose of 5XE12 $cm^{-2}$.

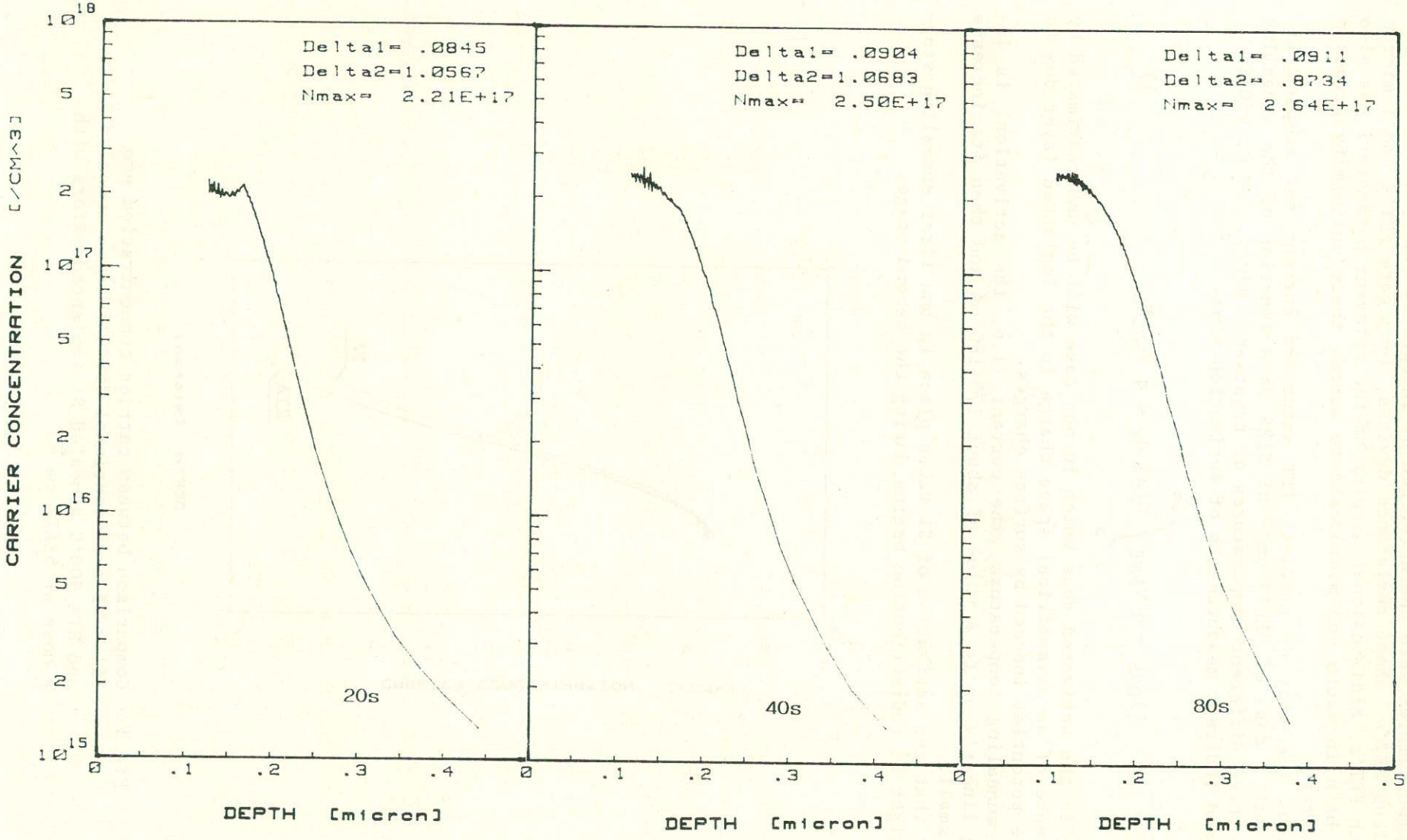


Fig.4 - Evolution of the carrier concentration profile as a function of the annealing time at 900°C for an implanted Si dose of 5XE12 $cm^{-2}$.

This statement is supported by the profile comparison of Fig.3 where 5xE12 $cm^{-2}$ Si implanted samples, RTA and furnace annealed are shown; the wafer treated by RTA exhibits a slightly narrower profile. Under this hypothesis the full activation for high dose implants ($N_D$ = 5XE13 $cm^{-2}$) is achieved between 60s and 100s respectively for temperature of 930°C and 870°C.
An analysis of the carrier concentration profiles of low dose Si implants ($N_D$ = 5XE$10^{12}$ $cm^{-2}$) tends to confirm these figures.
The carrier concentration profiles of low dose Si implanted wafers treated at 900°C at three different annealing times (20s,40s,80s) are reported in Fig.4. Two distinct phenomena are observed: the activation is reached earlier at the tail end of the profile than at the peak; secondarily a sharpening of the profile takes place between an annealing of 20s and one of 80s.

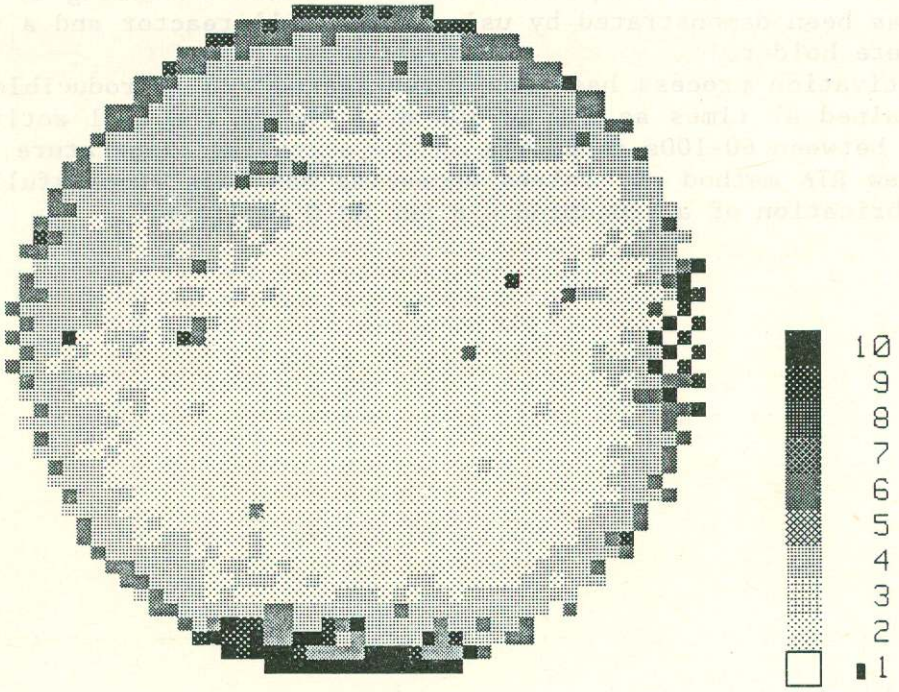


Fig.5 - Bidimensional map of sheet resistance of a Si implanted ($N_D$ = 3XE12 $cm^{-2}$) 2" GaAs wafer.
Each tone = 20 ohm/□ ;
Average sheet resistance = 985 ohm/□ ;
Standard deviation is = 26 ohm/□ .

The first effect is likely to be due to the higher energy required by the most damaged zones, like those around the doping peak, to get a full activation. The second one results in a progressive compensation of the doping tail, but it is not well understood and further study and investigation are required to explain it.

To ensure that comparable results to furnace annealing can be obtained by this method of RTA in terms of uniformity of electrical parameters across 2" GaAs wafers, bidimensional maps of the sheet resistance and peak carrier concentration have been obtained. The typical results are reported in Fig.5, where a map of sheet resistance is shown.
Routinely standard deviations of sheet resistance of 2-3% are now obtained not only on 100 keV but also on 70 keV Si implanted wafers.
This new method of RTA was applied to the fabrication of 0.5 micron gate FET monolithic amplifier in the range of 4-8 GHz and exhibiting an output power of 18 dBm at 1 dB of compression with an associated gain of 13 dB over the whole band.

## Conclusions

A new method of As overpressure rapid thermal annealing of Si implanted GaAs has been demonstrated by using a hot wall reactor and a very low mass substrate holder.
The activation process has been investigated and reproducible results can be obtained at times as low as 10s even though the full activation is obtained between 60-100s depending on the annealing temperature.
This new RTA method of capless annealing has been successfully applied to the fabrication of a broadband 4-8 GHz MMIC amplifier.