MMICS IN THE USA—STATUS AND MODELING ISSUES

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ABSTRACT

Significant developments in microwave device modeling and monolithic microwave integrated circuit (MMIC) technology have transpired in the USA during the last 3-4 years. These developments have been broad-based, encompassing both materials and device technology in a manufacturing environment as well as component and device modeling, off- and on-wafer testing, CAD software development, and packaging among others. Much of the impetus for this progress has been the substantial funding under the Microwave- and Millimeter-wave Integrated Circuit (MIMIC) program managed by the Defense Advanced Research Projects Agency (DARPA) and administered by the Tri-Service Agencies. Other important developments, outside of this effort, also have taken place, especially in HBT device and circuit design, as well as in civilian applications of MMICs such as GPS and wireless cable.

This presentation is a status review of some of the highlights in MMIC development in the USA during the last several years both within and outside of the MIMIC program. Also to be addressed are the major modeling issues that need be resolved to make possible high performance, low cost MMICs a reality.

Keywords: MMICs in USA, MIMIC program, modeling issues

1. INTRODUCTION

The monolithic microwave integrated circuits field is now in its second decade. Starting from early developments in the mid- and late '70s, this field has become, perhaps the most significant development in microwave circuit design technology within the last three decades. During the last decade, ground-breaking developments in low-noise and power amplifiers and multi-octave amplifiers on a single GaAs chips have become common place. Manufacturability and low cost are a reality.

The demanding needs of MMIC technology and design have lead to a pioneering development in CAD software and the first major effort in sophisticated modeling of microwave devices such as the FET under both small- and large-signal operation. The frequency limitations of device models has been pushed from below X-band to well over 40 GHz. Instrumental in this progress has been the advances in submicron gate FET technology and the development of sophisticated measurement techniques and instrumentation. Passive component models for distributed elements, inherited from the early '50s and '60s have been upgraded substantially by the advances in computational electromagnetic techniques.

Large-signal modeling of microwave FETs, practically non-existent prior to the MMIC development is an essential ingredient in MMIC design for power applications. Here frequency-based harmonic balance techniques for MMIC design have become essential and have largely supplanted time-domain approaches such as SPICE.

The major thrust of MMIC development in the USA during the first decade has been motivated by system needs for the military. This situation continues to the present. The catalyst for MMIC activity was the DARPA funded Department of Defense (DoD) based T/R module development program at Texas Instruments (TI), Raytheon, and General Electric in the late '70s and early '80s. The objective of this program was the demonstration of the feasibility of the MMIC approach for S-band and X-band modules. This successful program was followed by somewhat less ambitious programs funded by DoD.

During this same period some commercially-based efforts emerged for applications in telemetry, cable TV, and other systems. These were addressed by firms such as Minneapolis Honeywell and Pacific Monolithics. Commercial efforts, however, were hampered initially by difficulties in market definition.

During the present (second decade) the most significant stimulation in the MMIC field in the USA both in dollar magnitude and technical scope is the MIMIC program. This multi-phase program, now in its fourth year, is under the management of DARPA with participation by the Army, Navy, Air Force, and several other U.S. Government agencies. The major objective of this program is the development of techniques necessary for the manufacturability of broadly

applicable, high performance MMICs at an affordable cost. To date over $450M has been committed to this program. It is expected that many commercial "spinoffs" will emerge from this effort.

MMIC development under the MIMIC program has focussed on four application areas: (1) smart weapons, (2) electronic warfare (EW), (3) radar (T/R modules), and (4) communications. Time and space limitations prevent us from covering any of these areas in specific depth in this paper. Therefore, we shall direct our attention to generic circuit designs common to several or all of these application areas. For example, power amplifiers (PAs), low noise amplifiers (LNAs), phase-shifters, and oscillators will be presented as evidence of the present status of MMIC development in the USA for military applications.

2. MIMIC APPLICATION AREAS

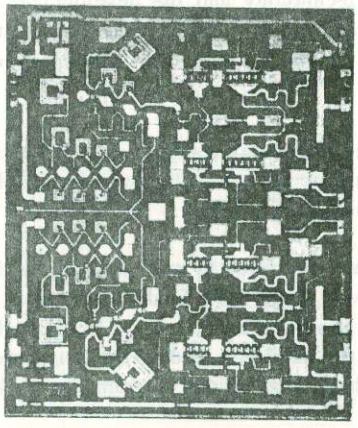
2.1 T/R and EW modules

2.1.1 Power amplifiers

Perhaps one of the most challenging efforts of the MIMIC program was the demonstration of a high-power, broadband power amplifier for radar and T/R applications. In this case the objective was a dual-channel amplifier operating over the 6-18 GHz band, with a linear gain of the order of 20 dB and a saturated power output at 2 dB compression of 1 watt.

This requirement not only pushed the state of the art in power FET technology, but also presented a difficult problem of large-signal modeling over this wide band, which modeling at the time was inadequate. The additional requirement of close-packing to confine the chip size introduced a serious problem of parasitic coupling which the existing circuit simulators were incapable of handling, and which the fledgling electromagnetic (EM) simulation software was, at best, only partially successful in treating. Much of the progress in the design of this circuit depended on the development of pulsed techniques to represent the IV characteristics of the power devices and the experience and good judgment of the circuit designer.

The results of this effort are shown in Fig. 1. Figure 1(a) is a micrograph of the 4-stage dual channel amplifier. The chip size is 4.4mm x 5.1 mm. Each channel consists of a parallel combination of a pair of 2-stage cascade amplifiers driven by a 2-stage distributed amplifier. Figure 1(c) demonstrates the excellent performance of the final design. Details of the design are described in (Ref. 1)



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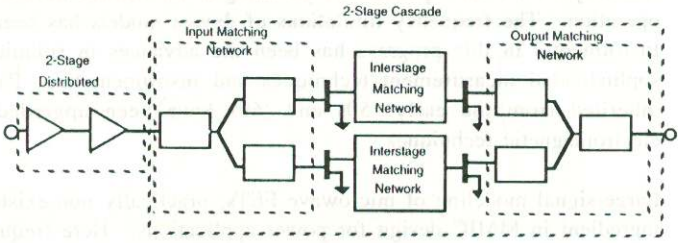

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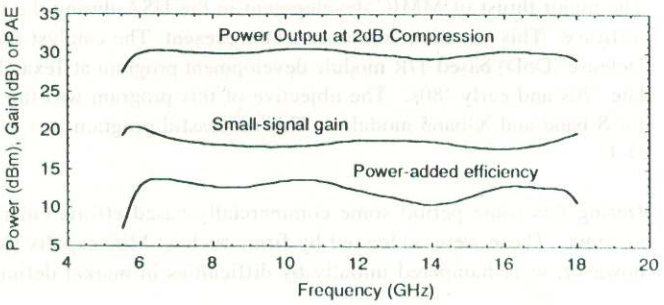


(c)

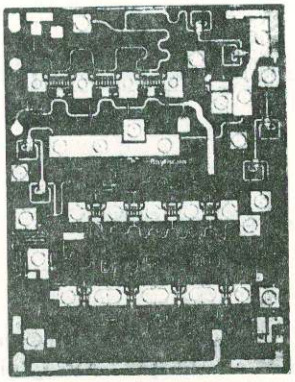
Figure 1 (a) *A C-Ku Band MMIC power amplifier chip, (b) its block diagram, and (c) its performance characteristics (Courtesy of A. Platzker, Raytheon Co.)*

2.1.2 Low noise amplifiers

The goal of the LNA development was the design and fabrication of a standard broadband, low noise amplifier that could meet the performance needs of several radar and EW systems. The generic nature of the LNA would make it suitable for several system applications and thereby increase the total production volume and minimize design costs.

The design objectives were a gain block with 15-20 dB gain across the 2-18 GHz band, with a maximum noise figure of 6.0 dB. In this case, although the device modeling did not present any serious problems, the circuit requirements severely tested the capabilities of the various sub-micron gate manufacturing technologies available at the time. A distributed amplifier configuration employing ion implanted, single recess 0.5 μM gate GaAs FETs was chosen for this design. The chip is illustrated in Fig. 2(a).

The chips consist of three stages of distributed amplification. The first two stages use dual gate FETs (four cells/stage) while the final stage consisting of three cells with either single or dual gate FETs. The chip is 3.1 mm x 4.0 mm in size. Bias networks are integrated on the chip in the form of spiral inductors and MIM capacitors. Figure 2(b) illustrates the respectable gain and noise performance of the final design. Performance and design details are described in (Ref. 2)



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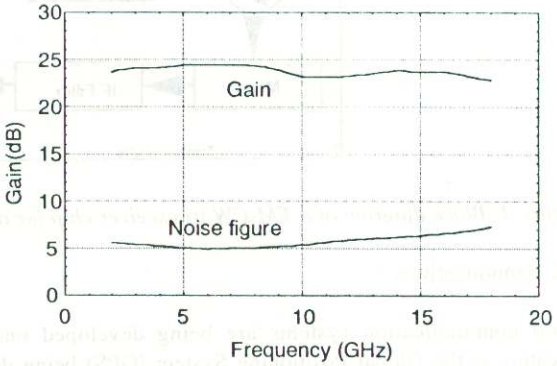
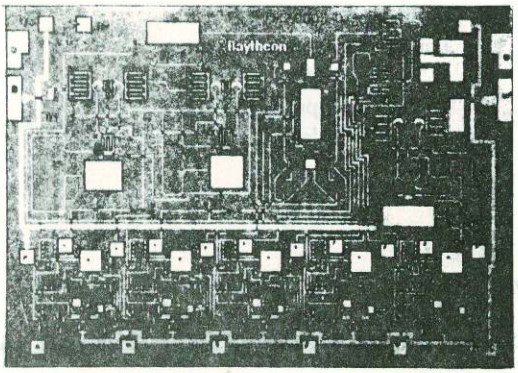


(b)

Figure 2 (a) High gain 2-20 GHz MMIC low noise driver amplifier, (b) gain and noise performance characteristics (Courtesy of T. Apel, Teledyne)

2.1.3 Phase shifters

Figure 3 illustrates an MMIC chip containing a 5-bit phase shifter and its associated digital switching circuit designed for an EW application. Differential phase shift is achieved with switchable FET-based high- and low-pass filter structures. FET parasitics are incorporated as filter elements in order to achieve broadband performance. The



Characteristics in the 6.5-18 GHz Band

RMS phase error < 10°

RMS amplitude error < 0.8 dB

Maximum insertion loss: 14 dB

Input return loss > 7.5 dB

Output return loss > 5 dB

Figure 3 Five bit MMIC phase shifter with on-chip digital switching circuitry and its performance characteristics (Courtesy of E. Schindler, Raytheon)

switch used in the phase shifter are N-channel depletion mode devices. All RF circuitry is dc offset so control can be achieved with a positive voltage.

The phase shifters were fabricated at both TI and Raytheon foundries with standard microwave power device processes. The demonstrated performance and reproducibility has qualified this phase shifter chip for insertion into wideband phased array systems. Details of the chip design are described in (Ref. 3).

2.2 Smart Weapons

A promising smart weapons application of the MIMIC program is in the Army's multi-option fuze for artillery (MOFA), a system under development. It is expected that MOFA will provide the most importance advance in fuze technology since WW II. Figure 4 is a block diagram of the chip for target velocity and range sensing used in this application. The chip consists of a complete FM/CW radar. A unique feature of this chip is its use of an active circulator. A successful design of this chip has been achieved by Hittite Microwave Co./TRW and demonstrated in the field. The chip has been implemented both with GaAs FET technology and also with a lower-noise, higher power version based on an HBT design (Ref. 4). The chip, only 1 x 2 mm in size, must cost less than $10 in production lots.

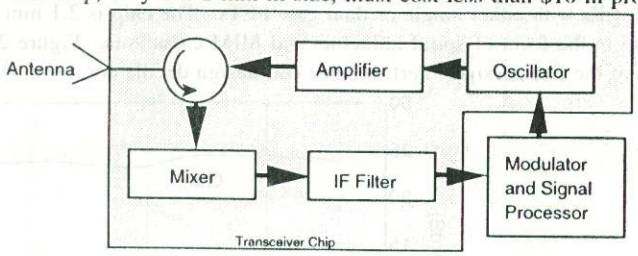
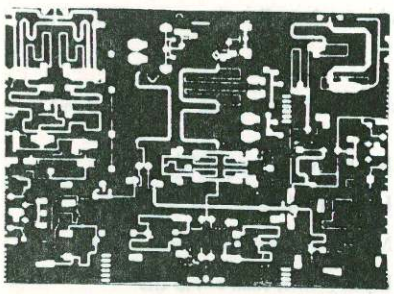


Figure 4 Block diagram of a FM-CW transceiver chip for a fuze application (Courtesy of E. Cohen, DARPA)

2.3 Communications

Several communication systems are being developed under the MIMIC program. Perhaps the highest volume application is the Global Positioning System (GPS) being developed by Hughes Aircraft Co. with systems integration being performed by E-Systems. The chips include an L-band LNA for the reference amplifier module and a power divider and complex weight chip for the active weight module. A second communications system for Q-band is under development by the Raytheon/TI team, with team member Magnavox involved. These chips include a VCO, LNA, PA, and mixer.

A third system developed by the ITT/Martin-Marietta team is a complete 16-function transceiver on a chip for a C-band phased array radar/communications use. The 12 x 17 mm chip, shown in Fig. 5, operates in the 5.2-5.8 GHz range. It provides complete transmitting and receiving functions. Performance characteristics are listed in Fig. 5.



Receiving section:
Gain = 22 dB
Noise figure = 4 dB
Transmitting section:
Gain: 42 dB
Power output = 3.5 W
Power-added eff. = 40%

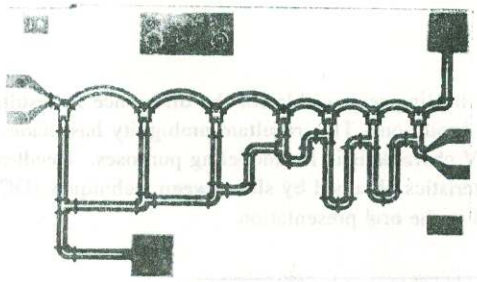
Figure 5 A transceiver chip for C-band phased array radar/communications (Courtesy E. Cohen, DARPA)

Considering the circuit complexity, impressive RF chip yields of 54% and 67% were achieved for the transmitter and receiver sections, respectively.

3. NON-MIMIC APPLICATIONS

Some of the most remarkable microwave performance from MMICs has been demonstrated outside of the framework of the MIMIC program. We cite as an example the record bandwidth achieved by Varian (Ref. 5) with an InP FET-based traveling wave amplifier. Figure 6(a) illustrates an MMIC amplifier with a demonstrated gain extending from

5-100 GHz—a record! Figure 6(b) is the measured gain across this band. This bandwidth, to the author's knowledge has never been achieved with a traveling wave amplifier of any other type before.



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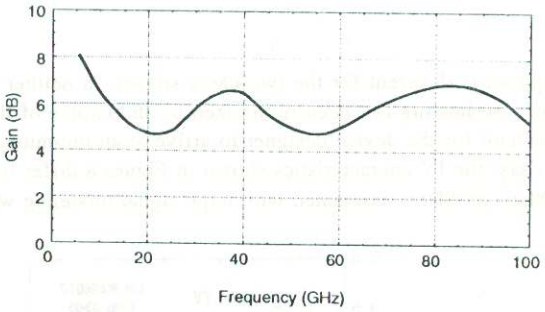
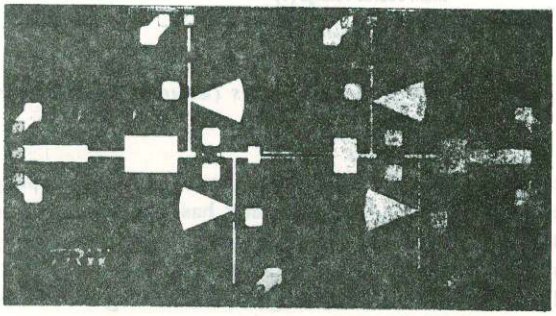


(b)

Figure 6 An InP FET based traveling wave amplifier with a record 100 GHz bandwidth (Courtesy R. Majidi-Ahy, Varian)

Another, more recent high-frequency result was reported by workers at TRW (Ref.6) is the W-band amplifier chip shown in Fig. 7(a). This is a 2-stage LNA chip with an average gain of 12 dB over the 91-95 GHz band. Note the use of radial stubs. Coupled microstrip lines provide the dc isolation and RF coupling between FET stages. Four such chips, cascaded on a hybrid substrate exhibited a average gain of 42 dB and a noise figure of 6 dB over the 91-95 GHz band as illustrated in Fig. 7(b)—a remarkable achievement.



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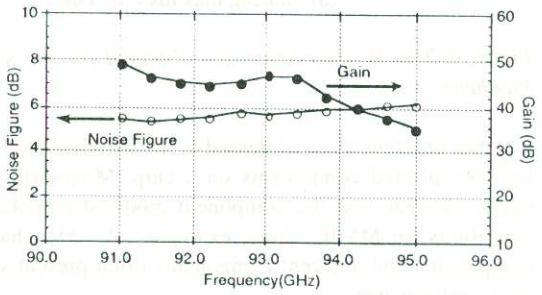


(b)

Figure 7 (a) An LNA chip for W-band operation (b) Gain and noise performance of a cascade of four chips (Courtesy B. Allen, TRW)

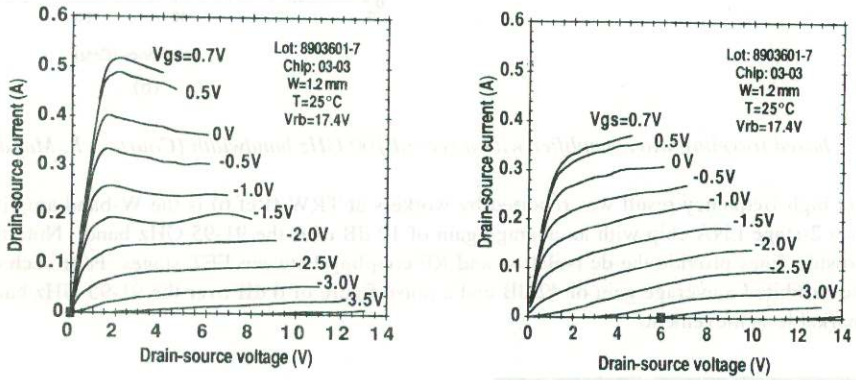
4. MODELING ISSUES

The high-frequency applications of the MIMIC program, as well as others, have fostered a concerted effort on the part of device engineers to extend the modeling accuracy of FETs to higher frequencies to match the progress in device development. As a result, significant improvements in the small-signal modeling of FETs has pushed the validity of the equivalent circuit approach to well beyond 40 GHz, from a starting value about 10 GHz at the onset of the MIMIC program. These improvements have been brought about largely by the development of very accurate and sophisticated microwave measurement systems in conjunction with improved de-embedding techniques. Highly automated software driven noise measurement techniques allows one to use the measured noise parameter data obtained at one frequency, suitably de-embedded, to predict the noise performance at any other frequency in the operating range of the equivalent circuit.

The progress in large-signal modeling has not been as successful. Admittedly, the nonlinear circuit simulation techniques have improved markedly with the adoption of the frequency-time domain based harmonic balance approach over that of the strictly time-domain approach, epitomized by the SPICE program. However, the improvements in accuracy of the analytically-based large-signal models of the active devices (FETs) used in such simulators has not kept pace. An important reason for this is that the dc IV characteristics used for fitting purposes in such models, more often that not, do not represent the dynamic performance of such devices because of trapping mechanisms. Therefore, device modelers have had to develop pulsed techniques for measuring the IV characteristics and fitting these to the analytic models. This has improved the design process, but not eliminated the problem, because the resulting IV characteristics are not unique but depend on the choice of the reference point from which the pulsed bias scan begins.

The problem is demonstrated in Fig. 8. Shown are two different IV characteristics for the *same* device derived from pulsed bias measurements. The only difference is that the starting point for the scan (indicated by the solid black

square) is different for the two cases shown. In neither case is thermal heating responsible for the difference in results, because heating has been minimized by the choice of the starting bias conditions. This resultant ambiguity has made it difficult for the device designer to arrive at an optimum choice of the IV characteristic for modeling purposes. Needless to say, the IV characteristics shown in Figure 8 differ from the characteristics obtained by slow sweep techniques (DC). Other problems associated with large-signal modeling will be addressed in the oral presentation.



(a) Starting bias Ids = 0, Vds = 0

(b) Starting bias: Ids = 0, Vds = 6V

Figure 8 Two IV characteristics obtained for the same FET by use of pulsed IV techniques (Courtesy A. Platzker, Raytheon Co.)

Another problem to be addressed is the deficiency of contemporary CAD software models to represent parasitic coupling between printed components on a chip. Microstrip type models, whether they be analytically based or numerical in nature, assume that the component modeled is isolated from the rest of the "world". However, under close-packing conditions on MMIC chips, examples of which have been shown above, undesirable coupling of these "isolated" components and adjacent components often present serious difficulties for the MMIC designer in achieving the desired chip performance.

5. SUMMARY AND CONCLUSIONS

Remarkable advances have been made in MMIC performance in the USA within the last 3-4 years. Many, though not all of these accomplishments have been promoted by the MIMIC program. Numerous issues remain, particularly with respect to the modeling of the large-signal performance of FETs and the parasitic coupling between passive elements.

6. REFERENCES

1. A. Platzker, K. Hetzler, and J. Cole, Highly dense dual-channel C-X-Ku and 6-18 GHz MMIC power amplifiers, *Proc. of the 1991 GaAs IC Symposium*, pp. 339-342.

2. T. Apel and S. Ludvik, A Compact high gain, 2-20 GHz MMIC amplifier, *Proc. of the 1991 GaAs Symposium*, pp. 311-314.

3. K. M. Simon, M. J. Schindler, V. A. MIeczkowski, P. F. Newman, M. E. Goldfarb, E. Reese, and B. A. Small, A production ready, 6-18 GHz five-bit phase shifter with integrated CMOS compatible digital interface circuitry, *Proc. of the 1991 GaAs IC Symposium*, pp. 251-254.

4. B. Maoz, L. R. Reynolds, and A. Oki, FM-CW radar on a single GaAs/AlGaAs HBT MMIC chip, *Proc. of the 1991 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp. 3-6.

5. R. Majidi-Ahy, C. Nishimoto, M. Riaziat, M. Glenn, S. Silverman, S. Weng, Y. Pao, G. Zdasiuk, S. Bandy, and Z. Tan, 5-100 GHz InP coplanar waveguide MMIC distributed amplifier, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 38, pp. 1986-1993 (1990).

6. T. N. Ton, B. Allen, H. Wang, G. S. Dow, E.Barnachea, and J. Berenz, A W-band, high-gain, low-noise amplifier using PHEMT MMIC, *IEEE Microwave and Guided Wave Letters*, Vol. 2, pp. 63-64 (1992).