HIGH BIT RATE FOUR PHASE MMIC REMODULATION DEMODULATOR AND MODULATOR.

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ABSTRACT

Four phase direct demodulation systems and high bit rate telemetry require four phase modulator. This work describes a four phase modulator development and a demodulator design at X-band frequency in MMIC technology. The modulator and demodulator MMIC design uses lumped elements networks and a 0.5 microns gate length process. Demodulator simulation results are presented. The modulator has been realized, it exhibits low consumption due to the use of cold FETs. Small phase switching times, less than 300 picoseconds, have been measured which confirm high bit rate modulator capability. Carrier rejection of about 28 dB and high clock rejection level are obtained in a QPSK modulation spectrum.

INTRODUCTION

Future radiocommunications satellites are expected to incorporate on-board data processing, which includes demodulation of the uplink microwave signal, data processing and remodulation before retransmission. This processing allows to know the message destination to choose the required beam for the next link. It can also improve the budget link by regenerating data.
In a typical regenerative channel (Figure 1) we find a four phase (QPSK) remodulation demodulator and a four phase emission modulator. The great number of channels in this kind of satellite induces the use of a great number of these functions. So the MMIC technology seems to be a very good solution for this application to reduce weight and size and to improve the reproducibility and the reliability.
New generations of earth observation satellites use high bit rate image telemetry which is an other interesting application for the QPSK modulator. MMIC technology allows to reach the high bit rate required for this application (more than 200 Mbits/s) with low consumption due to the use of cold FETs.

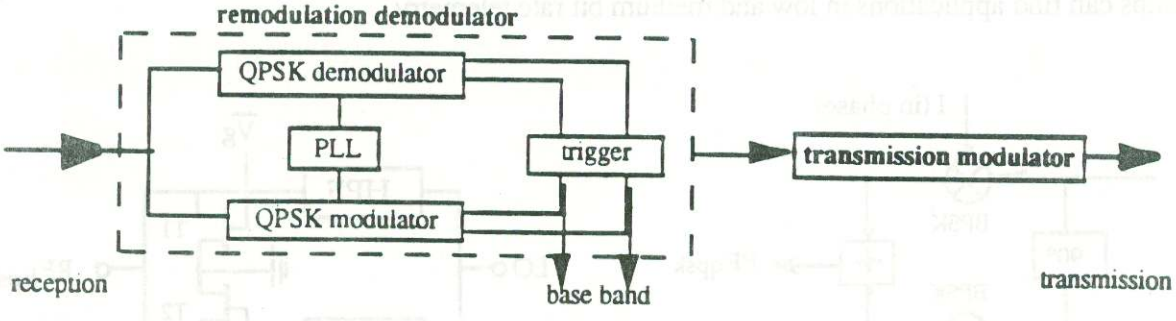

Figure 1 : *regenerative channel.*

REMODULATION DEMODULATOR CONFIGURATION

The four phase remodulation demodulator principle (Ref 1) is shown on Figure 2. In this equipment we find a QPSK modulator which restores the RF carrier by remodulating the

modulated RF signal with the demodulated I and Q streams in opposition. A phase locked loop regenerates this carrier and the four phase demodulator allows to recover the two bit streams (I and Q) which are triggered.

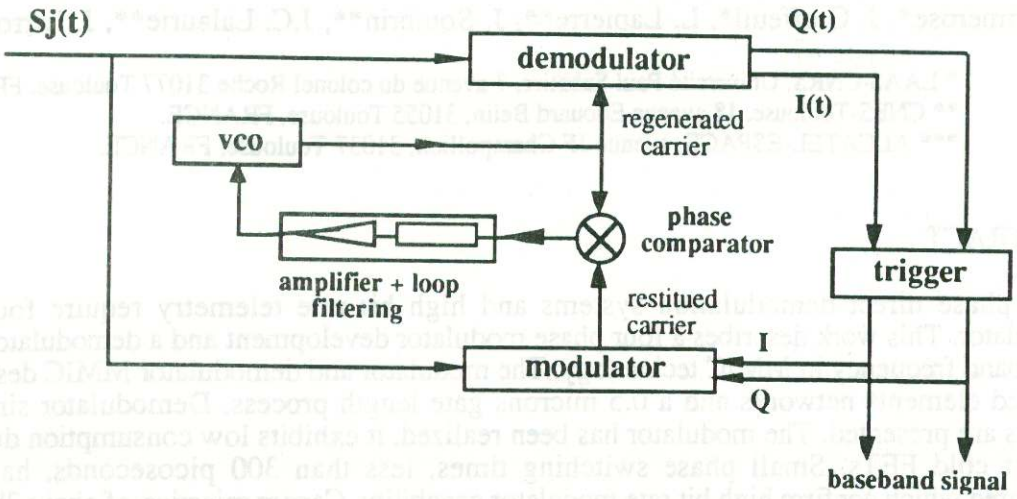

Figure 2 : *synoptic of the four phase remodulation demodulator.*

Our studies are performed to demonstrate the feasibility of the remodulation demodulator in MMIC technology and in a first time to focus our effort on the study of a four phase modulator which is the key element of the equipment.

QPSK MODULATOR DESIGN

We began by the design of the QPSK modulator (Ref 1) which is a parallel type (Figure 3.a). The RF carrier feeds in quadrature two BPSK modulators by use of a 90° hybrid coupler, then the two biphase modulated carriers are summed to realize the QPSK modulated RF signal. BPSK modulators are identical, they are described in Figure 3.b. The switch is constituted of two shunt MESFET transistors (Ref 2). The unmodulated RF signal is going through a lowpass filter giving -90° phase delay or through a highpass filter giving +90° phase advance (Ref 3). By combining these two signals we get the two phase states of the BPSK modulator.
The input quadrature divider and the output in phase combiner are respectively lumped elements versions of a 90° hybrid coupler (Ref 4) and a Wilkinson combiner. Those BPSK modulator chips can find applications in low and medium bit rate telemetry.

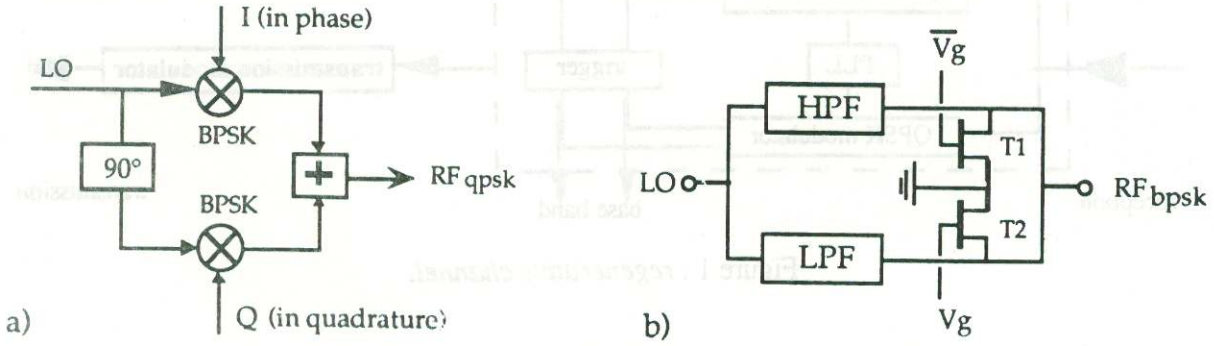

Figure 3 : *a) and b) synoptic of QPSK and BPSK modulators.*

The use of lumped inductances and MIM capacitances to realize the couplers and the BPSK modulators allows to reduce the chip size (2.5mmx1.6mm) and to improve the circuit bandwidth. The command signals drive the BPSK modulators by the MESFET gates. No drain bias is used, so very small DC consumption results due to the use of these cold FETs.
To analyze errors which can occur during manufacturing process we have designed separately all building blocks of the QPSK modulator. We find the BPSK modulator, the 90° hybrid coupler and the Wilkinson power combiner for on wafer testing.
All design works have been made at the CNES microwave laboratory.

QPSK MODULATOR RESULTS

These circuits have been manufactured in THOMSON/TCM GaAs foundry in the LN05 process. This MMIC technology allows the use of spiral inductances and MIM capacitances in silicon nitride. MESFETs are 0.5 micron gate length, the active area is made by ion implantation. Grounding is realized through via holes and crossing is possible by use of air bridges.
On wafer microwave measurements of all the MMIC chips manufactured indicate more than 77% and 91% yield for the QPSK and BPSK modulators respectively. All measured chips show analog results and confirm very good reproducibility of the functions.
Figure 4 shows the QPSK modulator chip photograph. The chip has been mounted in an RF test fixture by ALCATEL-ESPACE.

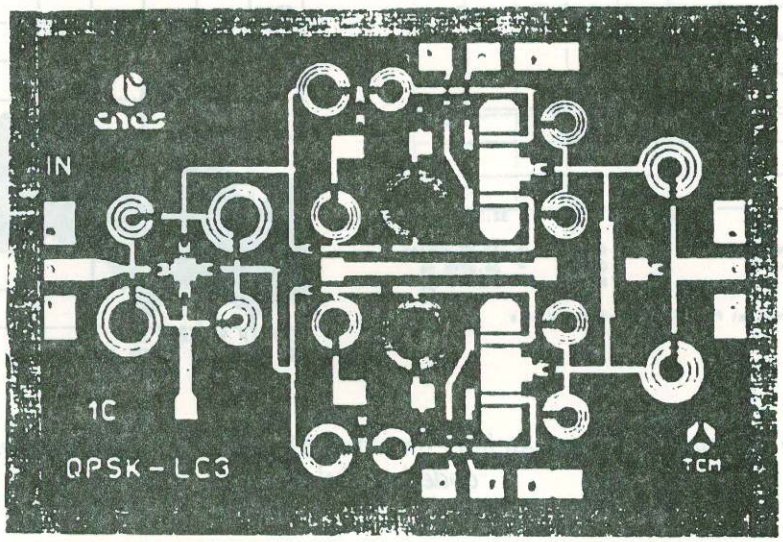

Figure 4 : *QPSK modulator chip photograph.*

Figure 5 shows measured and simulated static phase states of the QPSK modulator at 8.2 GHz. We have localized error origin between simulations and measurements in the 90° hybrid coupler building block which was tested separately. Phase state accuracy is about 2 dB and 8° peak to peak and insertion loss is about 8.5 dB.
Figure 6.a describes measurement of phase switching time for a square wave modulation signal at 500 MHz with 200 ps rise time and for a local oscillator frequency at 8.2 GHz. Measured switching time is less than 300 ps, demonstrating the high bit rate modulator capability without consumption.
Figure 6.b shows the spectrum of our QPSK modulator which is running in biphase mode (I=Q). We use a pseudo-noise coded modulation of 150 Mbits/s at 8.2 GHz local oscillator frequency. The modulator provides good clock rejection level and good sideband symmetry.

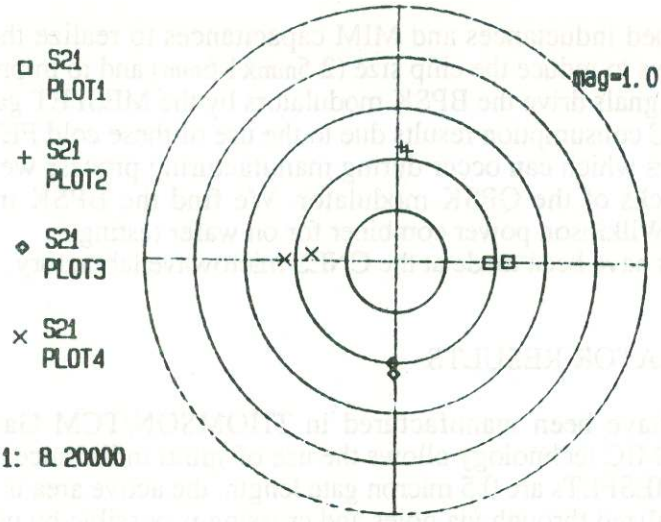

Figure 5 : *simulated and measured phase states of the QPSK modulators.*

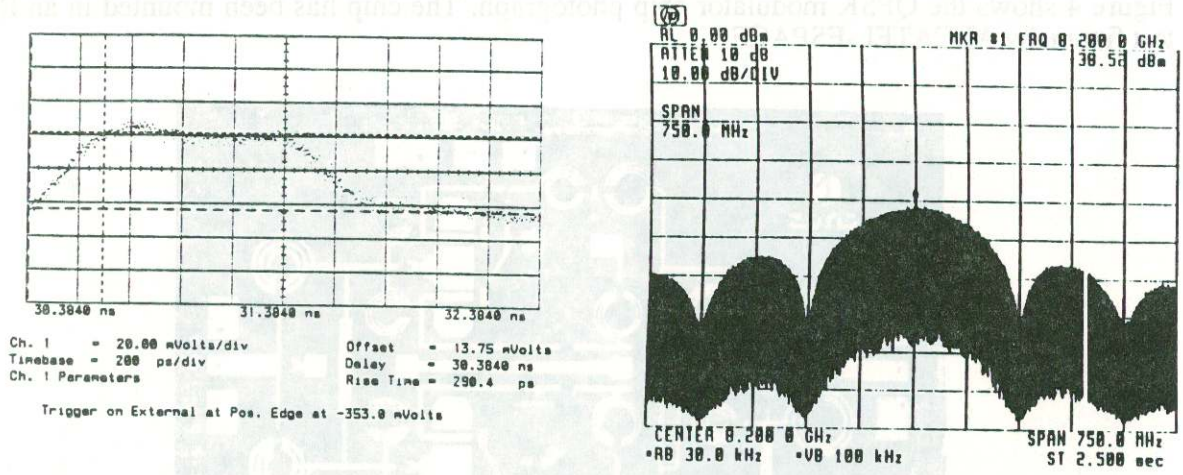

Figure 6 : *a) measured phase switching time and b) measured spectrum for 150 Mbits/s PN coded modulation.*

DESIGN CONCEPT OF THE QPSK DEMODULATOR

The second part of this study was to design a QPSK demodulator and a phase comparator. The principle of the demodulator is like the modulator one (Figure 7.a). The local oscillator feeds in quadrature two mixers by use of a 90° hybrid coupler. The RF modulated carrier feeds in phase the mixers, then the 2 demodulated bit streams of the QPSK modulation are recovered in the IF band of the mixers.

RF and LO signals occupy the same frequency band, so the use of a balanced structure to provide RF to LO isolation is necessary (Ref 5). Design concept of the balanced mixer (figure 7.b) uses a lumped element version of a 0°-180° hybrid coupler with 2 diodes connected to a pair of mutually isolated ports (Ref 4, 6). RF and LO are connected to the other pair of mutually isolated ports of the coupler. Diodes are fed in opposite by the LO and in phase by the RF.

Using a balanced diode structure gives potential capabilities for the QPSK demodulator to be used in modulator mode. In this case, IF output receives the modulation signal and we get the QPSK modulated carrier at the RF port.

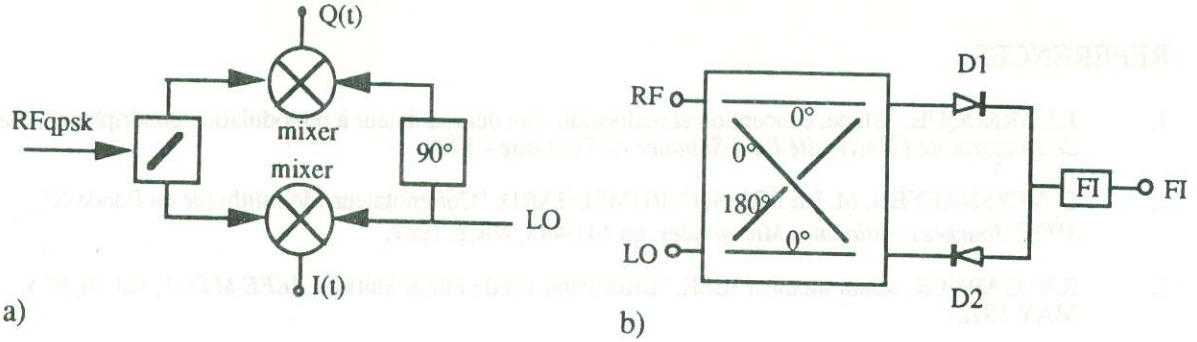

Figure 7 : *a) synoptic of the QPSK demodulator and b) principle of the balanced mixer.*

DEMODULATOR SIMULATION RESULTS

These circuits will be processed also by TCM in the LN05 process. Nonlinear behavior of the diodes has been modeled and circuits have been simulated using EESOF nonlinear CAD software, LIBRA. Figure 8.a shows the simulated conversion losses which are about 10 dB on the I and Q ports. Amplitude and phase precision of the two quadrature IF outputs are respectively less than 1 dB and 6° peak to peak. More than 30 dB LO to RF isolation and 20 dB LO return loss are expected. LO and RF levels are 12 dBm and -7 dBm, IF frequency is 200 MHz and RF frequency band is 7.6-8.8 GHz.

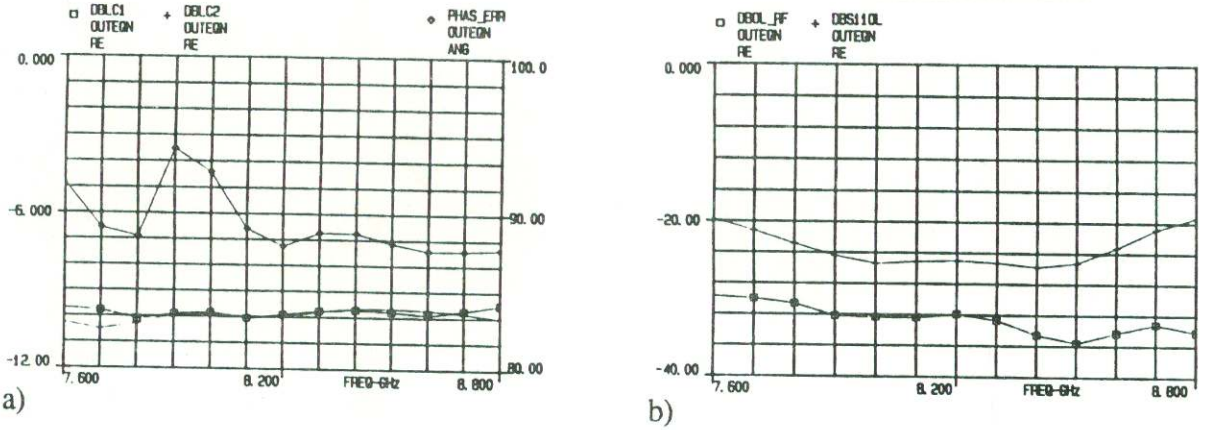

Figure 8 : *a) conversion loss and phase quadrature precision, b) LO to RF isolation and LO return loss of the QPSK demodulator.*

CONCLUSION

Static and dynamic measurements show that QPSK modulator concept without tuning is possible with good performances. We can reach several hundred of Mbits/s rate usable for payload telemetry. In the second part of this study, we made corrections of the QPSK modulator design with aim to increase phase states accuracy. The four phase demodulator and phase comparator design has required full nonlinear modelling and full nonlinear simulation using harmonic balance technic. We have a high confidence level in these designs due to good results obtained in the first run. These circuits will be processed also by TCM in the LN05 process, the final goal of this work is to integrate a microwave subsystem for the remodulation demodulator with all the MMIC chips we have realized.

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