AN ERROR TOLERANT, KU-BAND, GAIN/PHASE CONTROL MMIC

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ABSTRACT

A single chip, gain/phase control MMIC is described. The chip operates from 10.5 - 13GHz with 5 bit resolution and net gain. Numerical redundancy has been introduced to give tolerance to bit weight errors, the resulting advantage over a direct binary implementation is demonstrated.

Keywords: MMIC, Control, Error Tolerance.

INTRODUCTION

Each element of a Beam Forming Network (BFN) requires independent gain and phase control. This paper describes a single chip MMIC designed to fulfil this function in a telecommunications satellite BFN. MMIC realisation offers a component which is small, light weight and reproducible. All of these factors are extremely advantageous for both BFN components and space applications in general.

The primary band of interest is 12.5 - 12.75GHz but the chip has been designed to operate from 10.5 - 13GHz. The requirement was for 5 bit gain and phase resolution with digital control and net gain. The control range requirement was 360° of phase coverage and 20dB of gain coverage. These requirements could have been addressed with a direct 5 bit binary implementation but by using 6 bits, numerical redundancy is introduced. This numerical redundancy has been used to give significant tolerance to bit weight errors.

ERROR TOLERANT, NON-BINARY BIT WEIGHTING

The standard technique to realise 5 bit control resolution is to use 5 binary weighted bits. This is simple and efficient and if all of the bits have the correct weightings the control range is covered with adequate resolution. If however, any of the bits are in error, it is possible that the range or/and resolution requirement will not be met. The maximum total error which can be incurred whilst still achieving both range and resolution is ±1/2LSB (5.625° for phase control). This translates to ±1.6% for errors related to bit size, with the least significant bit (LSB) restricted to the minus tolerance only in order to satisfy the resolution requirement. Clearly ±1.6% represents a very tight tolerance, especially as it needs to allow for production process variations and design uncertainties.

If 6 bits of control are used instead of 5, but neither the range nor resolution requirements are increased, then the control system is numerically redundant. By appropriate choice of bit weights it is possible to significantly increase the tolerance of the control system to bit weight errors.

Consider an N bit, binary weighted control system with bit weights B_{N-1}, B_{N-2} ..... B_0. If n bits are used to realise this control function (where n is an integer greater than N) but the original range and resolution requirements are retained, a non-binary system can be realised. The new bit weights are then C_{n-1}, C_{n-2} .. C_0. With a direct binary realisation the bit multiplication factor is 2 (ie $B_{i+1} = 2B_i$). The new, non-binary control system has a bit multiplication factor ß such that $C_{i+1} = ßC_i$. Let the fractional tolerance of the new system to bit weight errors, be ∂. That is, each and every bit can be multiplied by any value between (1 - ∂) and (1 + ∂) without impairing either range or resolution.

For any given values of n and N it is possible to calculate Co (the new LSB), ß (the bit multiplication factor) and ∂ (the fractional tolerance to bit weight errors) for a non-binary system with optimum ∂. The equations governing the n bit non-binary system are listed below:-

$$ß = \sqrt[n]{2^N} \qquad (1)$$

$$\partial = \frac{2}{ß} - 1 \qquad (2)$$

$$Co = \frac{Bo}{1+\partial} \qquad (3)$$

Thus the equations (1) to (3) enable the bit weights and error tolerance of a non-binary n bit realisation of a direct binary N bit system to be calculated.

For the system under consideration the direct binary phase bit weights are 180°, 90°, 45°, 22.5° and 11.25°. The amplitude control bit weights are 12.8dB, 6.4dB, 3.2dB, 1.6dB and 0.8dB. Realising the same system with 6 bits of control gives ß = 1.7818 and ∂ = 0.12246 (ie all bits can tolerate errors of ± 12.2% whilst still meeting the range and resolution requirements of a direct 5 bit implementation). The new phase bit weights are then 180°, 101°, 56.7°, 31.8°, 17.9° and 10°. The amplitude bit weights are 12.8dB, 7.18dB, 4dB, 2.26dB, 1.27dB and 0.71dB.

The LSB is reduced in size to enable the resolution specification to be achieved when it is increased by the maximum tolerable error. Although the MSB is unchanged, the nominal range has increased, enabling the specified range to be achieved if all bits are decreased by the maximum tolerable error. Table 1 shows the bit multiplication factor, error tolerance and least significant phase bit for a 5 bit system realised with 6, 7, 8 and 9 non-binary bits.

n	Error Tolerance	ß	Co
6	±12%	1.78	10°
7	±22%	1.64	9.2°
8	±30%	1.54	8.7°
9	±36%	1.47	8.3°

TABLE 1: *Non-Binary Realisation Of a 5-Bit System.*

As the number of extra non-binary bits increases, the additional tolerance to errors achieved decreases. For the purposes of the circuit under consideration the 12% offered by a 6 bit non-binary system was considered sufficient. The idea of non-binary implementation is extremely versatile, in both application method and application area. One possibility which could be considered is to increase the bit multiplication factor and trade error tolerance for resolution. For example, increasing the value of ß to 1.88 gives an effective resolution of 5.5 bits with an error tolerance of 6%.

CIRCUIT DESIGN

As described in the previous section, the 5 bit gain and phase resolution is achieved using 6 non-binary bits. The circuit function required is therefore 6 bits of phase shift, 6 bits of gain control and net gain.

Realising some or all of the gain control actively has the advantage of compact size, since a gain function and a gain control function are realised simultaneously. This can be easily accomplished by applying analogue control to the gate voltage of FETs in an amplifier. However, digital control is a requirement of the circuit.

One method of realising an amplification and simultaneous digital gain control function is to use Segmented Dual Gate Field Effect Transistors (SDGFETs) (Ref.1). These are dual gate FETs configured such that a portion of the second gate can be selectively switched off. It was decided to realise the 4 LSBs of gain control using SDGFET amplifiers. The two MSBs were considered too large to realise using this technique and switched resistive attenuators were considered more appropriate.

Before the amplifier design could begin it was necessary to have an enabled width dependent model. It was decided to model the SDGFET as a standard, single gate FET. This was done for various fractional values of enabled second gate width and well behaved models were derived. These were then used to develop a single model which was scaleable with the fractional portion of enabled second gate width.

Two, 2-stage amplifiers were designed using SDGFETs with 100% enabled gate width. The appropriate fraction of second gate width, which needed to be switched out to realise the required gain steps was then determined. Each of the four SDGFETs was used to realise one bit of gain control, to guarantee multiplicative combination. The fully enabled gain of each amplifier was 12.75dB ±0.25dB from 10.5 - 13.5GHz.

The MSB of gain control uses Single Pole, Single Throw (SPST) switches to switch in and out a resistive ∏ attenuator. The next most significant bit also uses SPSTs but the resistive attenuator used is a bridged-T configuration to realise the lower level of gain control.

All 6 phase shifting bits were realised as switched filters (Ref.2). The three MSBs use Single Pole, Double Throw (SPDT) switches to switch between high pass and low pass filters whilst the three LSBs use re-configurable filters with the benefit of lower loss.

A block diagram of the circuit function is shown in Figure 1. The amplifiers are interspersed between the passive stages as a compromise between improved noise figure and improved linearity. In addition to the functions described above, there is also an on-chip temperature sensing diode. The gain variation of the chip with temperature can be compensated for by monitoring the diode and adjusting the gate 1 bias of all SDGFETs.

MMIC MANUFACTURE

The MMICs have been fabricated at the GEC-Marconi Materials Technology, Caswell, GaAs Foundry. A photograph of the 7.2 x 4.2mm chip is shown in Figure 2. Selective implantation has been used since the SDGFETs use a low noise implant, whilst the switch FETs use a low loss switch implant. Despite its high degree of functionality the chip is configured to be RF On Wafer (RFOW) testable, although full functionality can only be measured with the chip mounted in a module.

Each of the individual amplitude control and phase shifting circuits has been manufactured as independently functional sub-circuits for diagnostic purposes. A photograph of these sub-circuits is shown in Figure 3. From left to right and top to bottom these are: The two 2-stage SDGFET gain control amplifier; two 3-bit phase shifters; an active splitter (not part of the gain/phase control chip); SDGFET test components; switched resistive attenuators and, finally, a Wilkinson splitter/combiner (not part of the gain/phase control chip).

SIMULATED PERFORMANCE

At the time of writing the MMICs are just completing manufacture, RF On Wafer (RFOW) measurement will take place in the near future and it is hoped to present the results at the conference. The simulated results are presented here and show very good performance across both the primary band of interest (12.5 - 12.75GHz) and the design band of 10.5 - 13GHz.

Each of the individual sub-circuits was designed separately, matched to 50 ohms. The circuits were then cascaded as on the chip layout and the entire gain/phase control MMIC was re-simulated. Figure 4 shows the variation in phase shift from nominal setting, of the entire gain/phase control MMIC, in all 64 possible phase states. The total variation from 10.5 - 13GHz is about 6° for all phase states. This is well within the range of phase deviation which can be tolerated with the non-binary implementation. The theoretical maximum phase shift deviation from nominal which can be tolerated with this 6 bit non-binary approach is 48.6°. The numerical redundancy incorporated in the system allows the required phase state to be achieved (within ±1/2 LSB) with this level of phase error. The error can be either positive or negative and the only assumption made in this calculation is that the maximum phase error of each bit is proportional to bit size.

The variation in insertion loss (shown negative since the chip has net gain) of the circuit as it is switched through all 64 states is shown in Figure 5. The variation with phase state from 10.5 - 13GHz is less than ±1dB. This will not cause a worst case amplitude error of 1dB since the variation is well within the range of tolerable errors and can be calibrated out.

The input VSWR from 10.5 - 13GHz, for all phase states is less than 1.5:1, this is shown in Figure 6. The variation with phase setting is very small and this is a result of the high reverse isolation of the SDGFET amplifier at the input of the chip. The variation of output VSWR with frequency and phase state is shown in Figure 7. Once again there is virtually no variation with phase setting and the output VSWR is less than 1.3:1 from 10.5 - 13GHz.

GAIN/PHASE MAPS

The chip has 64 gain states and 64 phase states giving a total of 4096 possible gain/phase settings. Since 5 bit control is the requirement, calibration of the chip, or module in which it is used, is required. This necessity can be used to advantage in simultaneously calibrating out module to module variation.

An ideal 5 bit gain/phase map is shown in Figure 8. If a direct binary implementation were used and no errors were incured, this would be the resulting gain/phase map and good coverage of the gain/phase plain would be achieved. In practice this ideal case is not achievable and some discrepancies and process variations are inevitable. If the MSBs of gain and phase, with a direct binary implementation, were 10% high and all the rest 10% low, the resulting gain/phase map is shown in Figure 9. Gaps can now be seen opening up in the gain/phase plain. These gaps represent gain/phase states which cannot be addressed and no amount of calibration can alter this.

The gain/phase map for the MMIC has been simulated and is shown in Figure 10. There are 4096 gain/phase settings, in practice the most appropriate 1024 of these would be selected during calibration. This would give a 5 bit gain/phase control map with good gain/phase plain coverage. If the MSBs of gain and phase were 10% high and all other bits 10% low, the error tolerant nature of the non-binary realisation means that no gaps should

open up in the gain/phase plain coverage. This has been simulated and is shown in Figure 11. Clearly the gain/phase plain coverage is still excellent and 1024 points could be selected to give good 5 bit gain/phase control.

CONCLUSIONS

A gain/phase control MMIC has been described. The chip has been fabricated at the GEC-Marconi Materials Technology Limited GaAs Foundry. The chip is digitally controlled, has 5 bit resolution and uses numerical redundancy to achieve significant tolerance to bit weight errors. Good gain/phase plane coverage in the event of substantial bit weight errors has been demonstrated.

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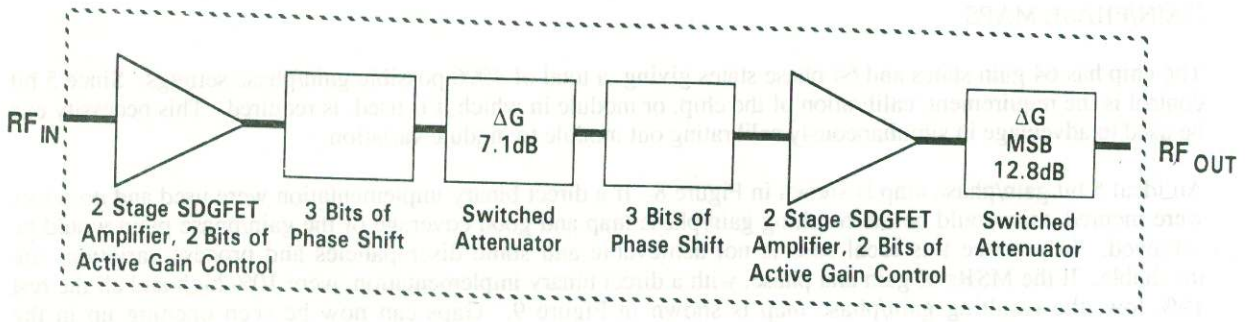

Figure 1 *Block Diagram of the Circuit Function*

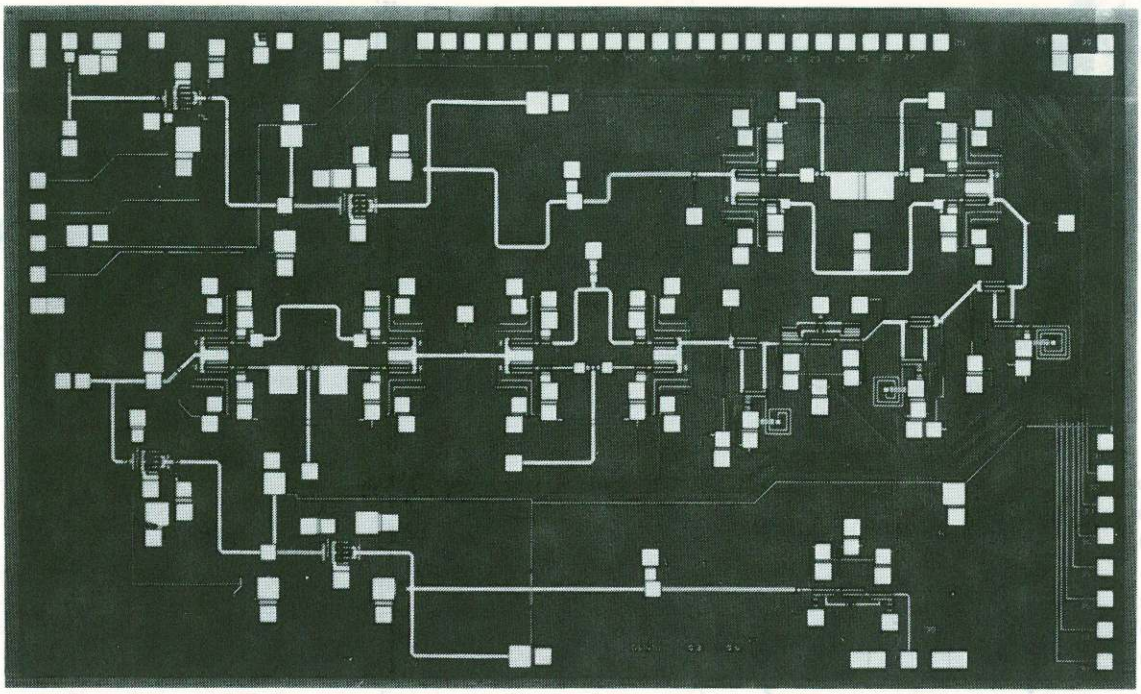

Figure 2 *Photograph of One Gain/Phase Control MMIC*

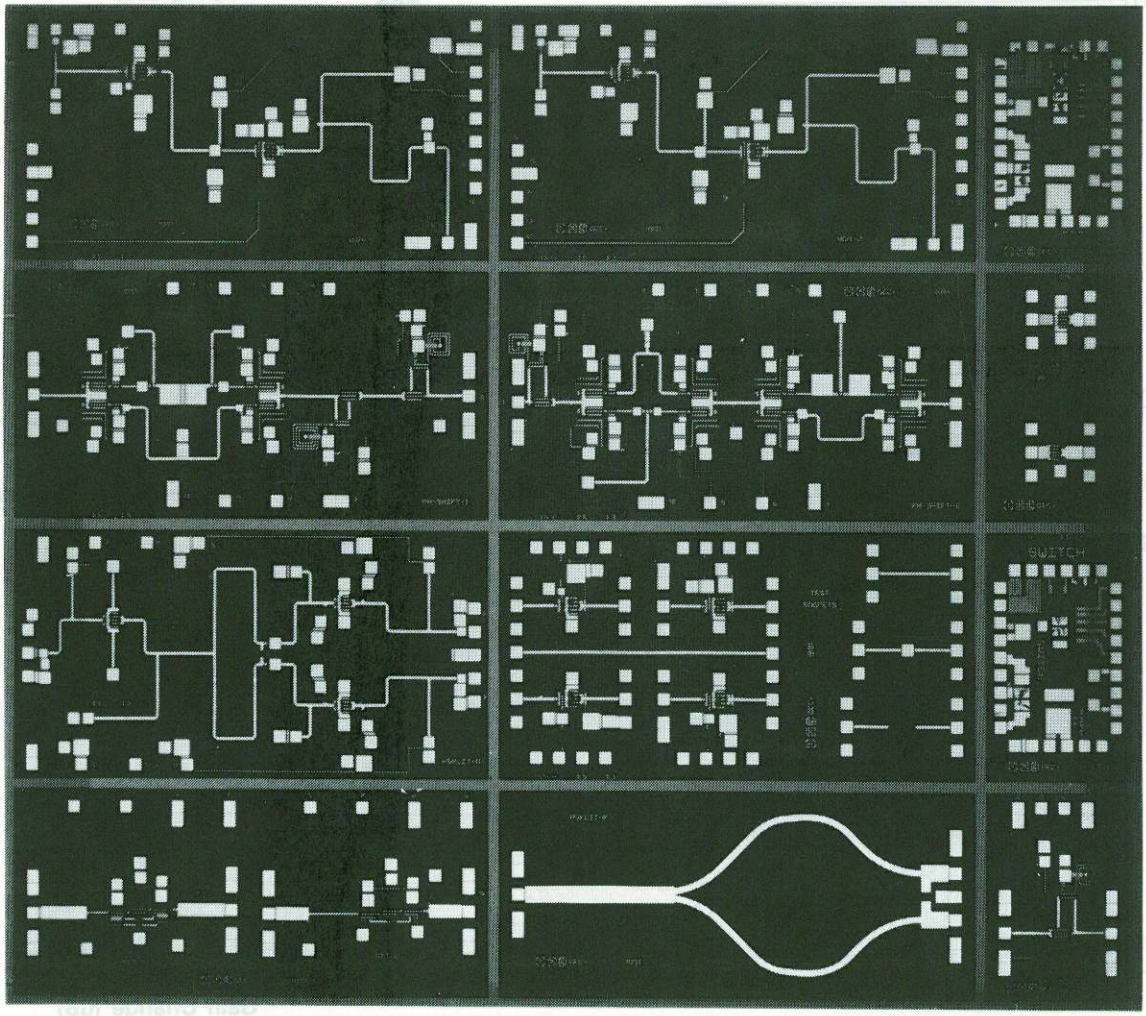

Figure 3 *Photograph of the Individual Sub-Circuits*

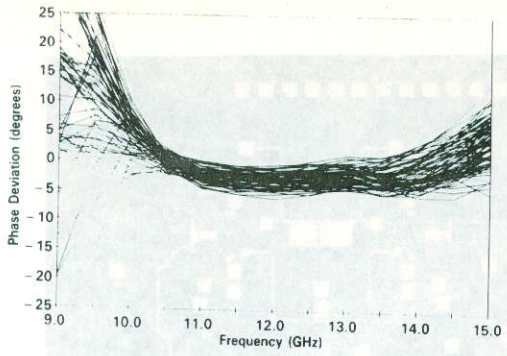

Figure 4 *Variation of Phase Shift From Nominal For All 64 Phase States*

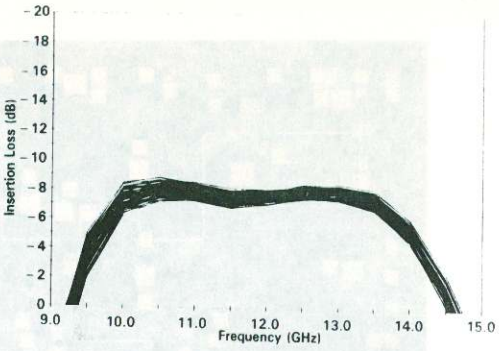

Figure 5 *Variation of Insertion Loss With Frequency For All 64 Phase States*

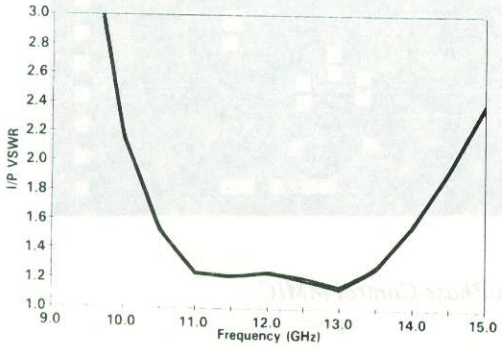

Figure 6 *Variation of Input VSWR With Frequency For All 64 Phase States*

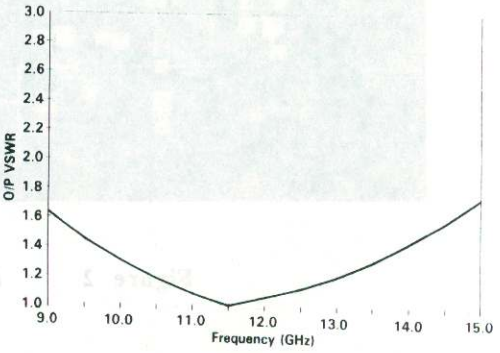

Figure 7 *Variation of Output VSWR With Frequency For All 64 Phase States*

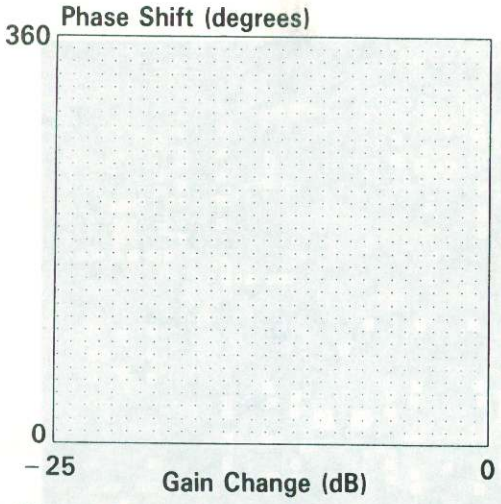

Figure 8 *Ideal 5 Bit Gain/Phase Map*

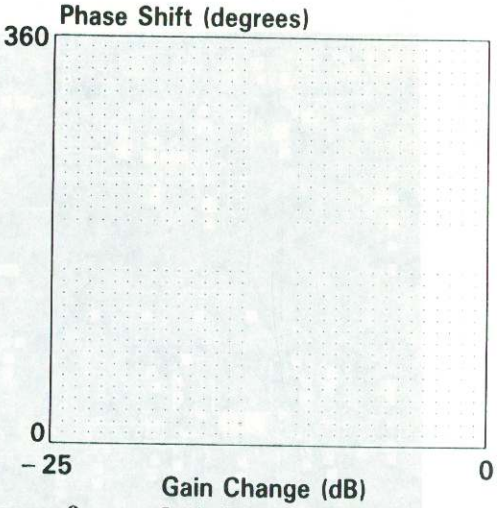

Figure 9 *5 Bit Gain/Phase Map With MSBs 10% High, Rest 10% Low*

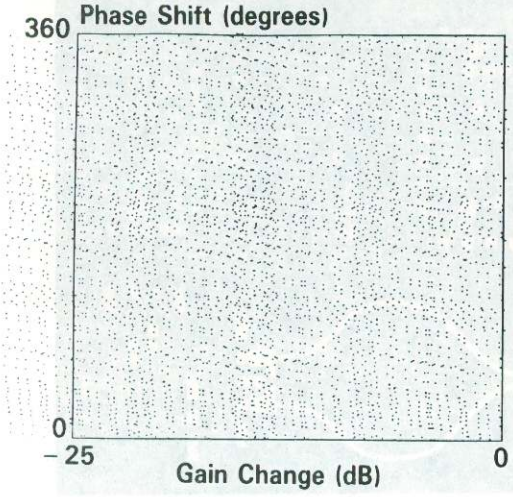

Figure 10 *Simulated Gain/Phase Map of the MMIC*

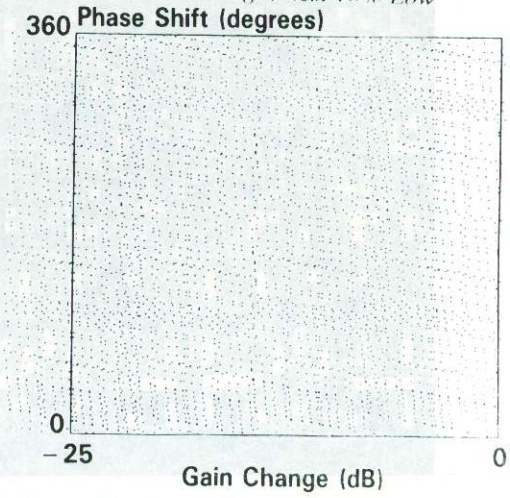

Figure 11 *Simulated Gain/Phase Map of the MMIC With MSBs 10% High, Rest 10% Low*