RF PERFORMANCE OF GaAs/Si/Si MESFETs FOR MIMICs

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ABSTRACT

It is shown that an intermediate Si epitaxial layer in the GaAs on Silicon system is critical for attaining state of the art MESFET microwave performance. Devices with gate length of 1.3μm and width 180μm showed unit current gain cutoff frequency (f_t) up to 18GHz and maximum power gain cutoff frequency (f_{max}) of about 30GHz. These results indicate that MMICs can be developed on GaAs/Si/Si wafers with a processing technology suitable for GaAs-Si monolithic integration. The critical requirements for MMICs on Si are also presented.

Keywords: GaAs on Si, MESFET, RF, epitaxy, MMICs, OEICs.

1. INTRODUCTION

Recently, the introduction of epitaxial buffer Si layers in order to improve the GaAs/Si structural quality and to reduce the preheating temperature for the preparation of Si surfaces has been investigated (Ref. 1). It is noted that material processing which is compatible with GaAs-Si monolithic integration should be carried out at the minimum temperature. Although a significant reduction in dislocation density was not observed, the GaAs/Si/Si material was reproducibly grown without any planar defects (stacking faults, APBs) and resulted in smoother surfaces and significantly better quality thin GaAs epilayers.

In the present paper, the microwave performance of GaAs/Si/Si MESFETs is presented including the measurement of maximum available gain (MAG), unit current gain frequency (f_t) and maximum power gain frequency (f_{max}). Since the device geometry was not optimized for performance, the effect of the grown structure with an intermediate silicon buffer layer on the MESFET parasitic characteristics (gate to source capacitance and output conductance) was determined and compared to the requirements for monolithic microwave integrated circuits.

2. EXPERIMENTAL DETAILS

MESFET structures were grown by Molecular Beam Epitaxy (MBE) on high resistivity (2KΩ·cm) p-type Si(001) substrates misoriented 3° towards a <110> direction. The MBE system has an independent silicon growth chamber which shares the same preparation chamber with the III-V MBE. Thus, following the deposition of 1μm non-intentionally doped (n.i.d.) Si, the GaAs growth was continued in the III-V growth chamber without breaking vacuum. A 1.5μm GaAs buffer layer was grown as described in Ref. 3, and finally a 0.12μm active layer doped at $3.5x10^{17}$ cm^{-3} and a 45nm contact layer doped at $2x10^{18}$ cm^{-3} was grown in order to complete the structure. The Source-Drain ohmic contacts were AuGe/Ni/Au formed by Rapid Thermal Annealing, while the Gate metallization was TiPtAu. The gate width and length

of the microwave transistors were 180μm and 1.3μm respectively, as shown in Figs 2a,b. The MESFETs were both DC and RF characterized. The S-parameters were measured - on wafer - up to 19GHz. Equivalent circuit extraction of parameters was used.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1. MESFETs characterization

The I-V characteristics of a typical GaAs/Si/Si MESFET are shown in Fig.1a. The I-V characteristics did not exhibit any significant light sensitivity, indicating the presence of a low trap density which does not affect the DC operation of the devices. In Fig.1b, the drain current and DC extrinsic transconductance, have been plotted versus the gate voltage (V_G) for a constant drain-source bias (V_{DS}) of 2Volts. The maximum extrinsic transconductance was 227mS/mm.

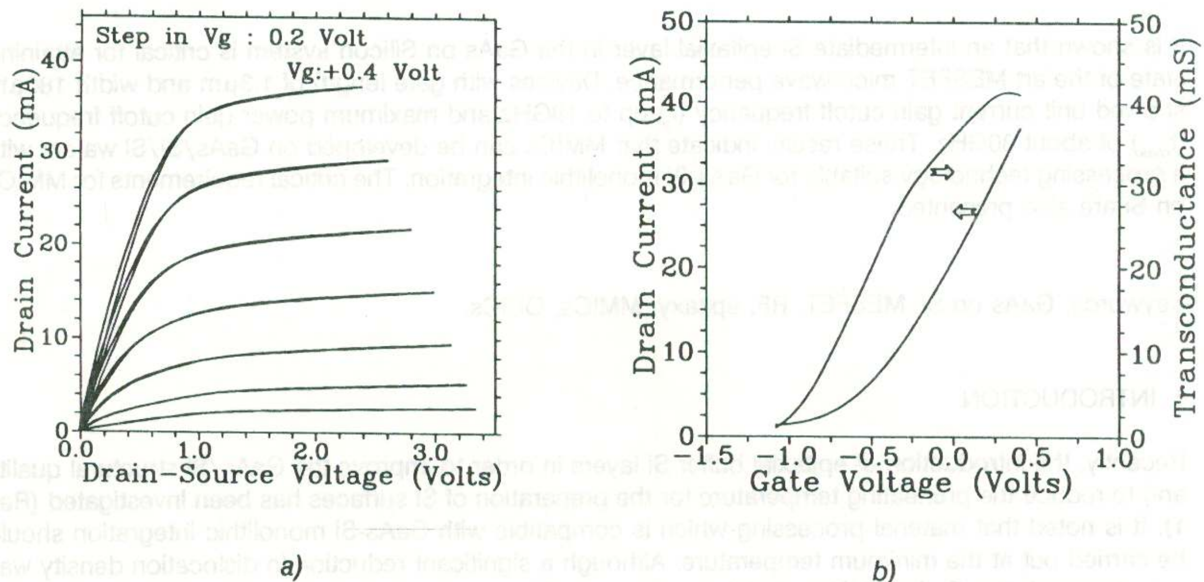

Figure 1: *a) I-V characteristics and b) DC extrinsic transconductance and drain current versus gate voltage at $V_{DS}=2V$, for a typical 1.3μm x 180μm GaAs/Si/Si MESFET.*

The typical S-parameters of the above device have been measured under DC bias conditions of V_{DS}=2Volts and V_G=-0.2Volts. From the current gain (h_{21}) versus frequency, as calculated from the S-parameters, the unit current gain cutoff frequency (0 dB of h_{21}) of 13.8GHz was deduced. The corresponding maximum power gain versus frequency was plotted and the extrapolated power gain cutoff frequency (f_{max}) was approximately 30GHz. This microwave performance was the typical one for GaAs/Si/Si MESFETs, and represents the state of the art performance for such relaxed geometry devices. The f_t measured and shown in Figure 2 extrapolates to better than 18GHz.

3.2. Analysis of RF measurements

The RF performance of the GaAs/Si/Si MESFETs has been analyzed in order to assess any limiting factors generated by the heteroepitaxial structure. Using the program SPECA (Ref.2) the equivalent circuits from the S-parameter measurements data were extracted. The equivalent circuit type used for this analysis is shown in Fig.3.

In Table I device material parameters are reported and are listed with the measured microwave performance (f_t and f_{max}) along with the corresponding values of the intrinsic elements of the equivalent circuit. The GaAs/Si/Si MESFET (T2) has been fabricated on high resistivity substrate which reduces the microwave losses and, permits the fabrication of MMICs (Ref.7). The previously reported GaAs-on-Si

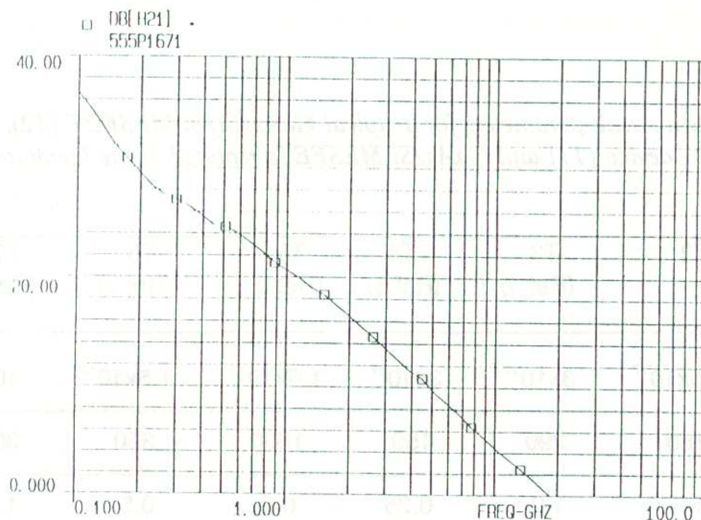

Figure 2: *Current gain (h_{21}) versus frequency for the best GaAs/Si/Si MESFET. The corresponding f_t is 18GHz.*

structures (T3-T7) (Refs. 4-8, respectively) are also presented in Table I, and with the exception of T6, are inadequate for MMIC fabrication (low substrate resistivity). The RF transconductance for T2 which appears in Table I is different from the DC maximum transconductance of the same device, and is noted that this is due to the different gate bias V_G which was used for the two measurements (V_G was +0.4Volt and -0.2V for the DC and RF measurements, respectively).

The GaAs/Si/Si MESFET (T2) is compared in the following section to a control homoepitaxial device (T1) and to the various GaAs/Si MESFETs reported in the literature (T3-T7):

(i) The equivalent circuit of T3 was recalculated by fitting the measured S-parameters in our equivalent circuit and the results are tabulated in Table I. The overall microwave performance of T3 is very similar to that of T2 indicating that some of the early GaAs-on-Si MESFET structures were of excellent quality.

The detailed comparison of T3 with T2 shows that the values of C_{gs} and g_{mo} (intrinsic transconductance) are similar despite the differences in the transistor parameters and their probable deviation from the nominal values. The discrepancy in the values of C_{gd} can be explained if the two transistors have

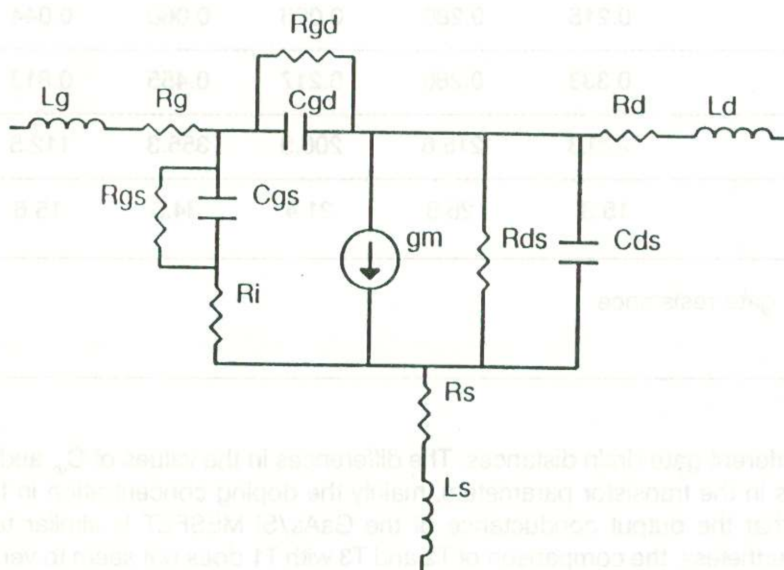

Figure 3: *The equivalent circuit which has been used to analyze the microwave measurements of the GaAs/Si/Si MESFETs. The definition of variables is the following:* **g_m**: *transconductance,* **R_s, R_D and R_g**: *source, drain and gate resistance, respectively,* **Ri**: *intrinsic input resistance,* **R_{gs} and R_{gd}**: *gate-source and gate-drain resistances, respectively, representing the leakage current of the Schottky contact,* **R_{ds}**: *output resistance,* **C_{ds}**: *output capacitance,* **C_{gs} and C_{gd}**: *gate-source and gate-drain capacitance, respectively* **L_s, L_d and L_g**: *source, drain and gate inductance, respectively.*

Table I. *RF Performance and equivalent circuit parameters for a typical GaAs/Si/Si MESFET (T2), a control homoepitaxial GaAs device (T1) and GaAs/Si MESFETs reported in the literature (T3-T7) (Refs 4-8).*

Transistor	T1	T2	T3 (Ref.4)	T4 (Ref.5)	T5 (Ref.6)	T6 (Ref.7)	T7 (Ref.8)
Doping (cm^{-3})	$4x10^{17}$	$3.5x10^{17}$	$3x10^{17}$	$3x10^{17}$	$1.5x10^{17}$	$1.5x10^{17}$	10^{17}
Gate width (μm)	180	180	290	150	1600	350	300
Gate length (μm)	1.3	1.3	1.2	0.25	0.8	0.5	1.0
Buffer thick (μm)	2.0	1.5	2.0	2.0	1.7	2.0	1.8
Epitaxial Si layer		YES	NON	NON	NON	NON	NON
Substrate (p^-) resistivity (Ω cm)	GaAs S.I.	Si 2000	Si	Si 10-20	Si 30	Si 1000	Si 50-100
f_t (GHz)	13.25	13.8	13.29	55			11.4
f_{max} (GHz)	~30	~30				~30	10.9*
C_{gs}(pF/mm)	2.465	2.280	2.450	1.570	1.125		
C_{gd}(pF/mm)	0.215	0.280	0.086	0.060	0.044		
C_{ds}(pF/mm)	0.333	0.280	0.217	0.455	0.813		
g_{mo}(mS/mm)	220.3	215.6	206.9	355.3	112.5		153**
g_d(mS/mm)	15.3	26.8	21.4	34.6	15.6		7.1**

* due to high gate resistance
** DC values

significantly different gate-drain distances. The differences in the values of C_{ds} and g_d can be explained by the differences in the transistor parameters, mainly the doping concentration in the active layer. In Ref.4 it is claimed that the output conductance of the GaAs/Si MESFET is similar to that of a GaAs/GaAs MESFET. Nevertheless, the comparison of T2 and T3 with T1 does not seem to verify that observation. The higher g_d for the GaAs/Si MESFETs is a fact indicating that parasitic path of current into the GaAs buffer layer is present (Ref.3). On the other hand, as long as the transistor capacitances are concerned there is no evidence that parasitic electrical charges are trapped at the GaAs/Si heterointerface. This observation was not expected for T2 which has a Si epitaxial layer with n^- non-intentional doping concentration. However, as described in Ref.1 high resistivity GaAs buffer layers were obtained by introducing the intermediate epitaxial Si layers which had a significant impact at the device characteristics. Georgakilas et al (Ref.1) explained the higher resistivity of GaAs buffer either by reduction in Si outdiffusion due to a better crystal structure in the GaAs interfacial region or to the existence of impurities on the Si surface which are burried by the Si buffer layers. By improving the epitaxial Si purity a significant impact at the MESFET RF properties is expected, but in addition, the above results indicate that high quality GaAs MESFETs may be developed on Si substrates containing intentionally doped layers.

(ii) The GaAs/Si material used for the fabrication of transistor T4 is very similar to that used for T3, however, the difference in gate lengths makes the comparison of T4 with the other transistor structures questionable. Nevertheless, by analyzing the data of Table I we can see that the various elements of the equivalent circuit of T4 are consistent with those of T3, with the exception of C_{ds}. In fact, the differences in the values of C_{gs}, C_{gd} and g_{mo} may be explained by the difference in gate length, while the higher value of g_d may be due to the short channel effects (Ref.9). However, the higher value of C_{ds} for T4 is inconsistent with the smaller gate length indicating either a significant difference between the two transistor patterns or parasitics due to GaAs/Si heterointerface or poor fitting of the extracted equivalent circuit to the measured S-parameters (Ref.5). Despite this problem, T4 is an excellent device which is comparable to an equivalent homoepitaxial GaAs MESFET.

(iii) T5 is a power MESFET and therefore the equivalent circuit used is quite different to the present one. Nevertheless, some comments are appropriate. From the data of Table I it is obvious that T5 is characterized by a high C_{ds} and g_d indicating clearly the presence of parasitic effects. Hence, it appears that even for a discrete GaAs-on-Si power MESFET, it is necessary to improve the GaAs buffer resistivity and to use the highest resistivity silicon substrates available.

(iv) T6 was processed on a high resistivity Si substrate adequate for MMIC fabrication. In spite of this, the transistor presented serious problems with parasitics. The defects were analyzed to be in the first 50nm of GaAs in the GaAs/Si interfacial region (Ref.7). This result indicates the importance of the starting Si surface and supports the growth of thin Si buffer layers. Contaminated Si surfaces not only may non-intentionally dope epitaxial layers, but in the case of GaAs/Si they may also lead to the creation of APBs (Ref.1). As described in Ref.1 the appearance of APBs for substrates misoriented from (001) in a <110> direction was associated with a large charge concentration near the GaAs/Si interface.

(v) The utilization of a low resistivity Si substrate for T7 was less important, since the goal of the study in Ref.8 was to fabricate digital circuits. A good f_t value has been obtained. The low f_{max} for T7 may be explained by the high gate resistance due to the transistor pattern (Ref.8). In addition, the low value for g_d may be explained by the fact that it is a DC measurement which systematically leads to lower values. Finally, the reported DC g_m can be considered as a very good value for the active layer doping concentration of 10^{17} cm^{-3}.

4. CONCLUSIONS

From the above discussion the following conclusions can be drawn:

Parasitic capacitances are not critical performance limitations for cases when the GaAs buffer layer is smaller than 2μm and the Si substrate is p^- type (001) misoriented towards <110>. The introduction of Si buffer layers has a positive effect since it leads to a significant increase of the resistivity of GaAs buffers.

The observed higher RF g_d for the GaAs-on-Si MESFETs may be explained by the fact that the GaAs buffer layers grown by MBE on Si substrates are slightly n-type doped (10^{14} - 10^{15} cm^{-3}) due to the Si outdiffusion. The conduction band of the GaAs buffer layer is lowered, which facilitates the injection of carriers from the channel into the buffer at the high field regions. Such deviations in g_D, however, may not significantly affect the RF power capabilities of the devices (Ref.9).

The GaAs/Si/Si epitaxial procedure has lead to the lowering of the Si desorption temperature to below 750°C. Finally, the results have identified the critical material parameters which must be optimized in order to achieve GaAs on silicon MMICs and OEICs.

5. ACKNOWLEDGEMENTS

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