PROCESS TECHNOLOGY EVALUATION FOR HIGH YIELD REPRODUCIBLE HEMT/PM-HEMT MMIC FABRICATION

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ABSTRACT

In this article we will report on a high yield HEMT/PM-HEMT technology, based an optimised ohmic contact formation and gate recessing. With this technology active device fabrication yields are better than 90% and corresponding key parameter tollerances always better than ± 5%, as required for high yield MMIC fabrication.

INTRODUCTION

The conventional AlGaAs/GaAs high electron mobility transistor (HEMT), introduced in 1981 [1] and the AlGaAs/InGaAs pseudomorphic high electron mobility transistor (PM-HEMT), introduced in 1986 [2] have offered both high speed and excellent gain, noise and power performance at microwave and millimeter-wave frequencies. Said devices have represented an evolutionary improvement in GaAs MESFET technology and as such, extensively used in both hybrid and monolithic microwave (MMIC) and millimeter-wave integrated circuits [3-7].

The performance advantage of heterojunction devices over conventional MESFET's are such that in the near future they will predominate in all high speed high frequncy applications. Nevertheless before this can come about the current limitation in fabrication yield must be overcome. Even thougth the processing technology for MESFET's and HEMT/PM-HEMT's is very similar, the same cannot be said for their corresponding production yields. The performance sensitivity of the latter devices on epilayer uniformity and defect density, source/drain ohmic contacts, and channel recessing and gate definition are such that their overall electrical yield can be very low. Infact current price differences (as much as a factor of five) between high and average performance commercial HEMT devices gives a clear indication that significant improvement in fabrication yield is still necessary.

In this article the critical aspects of the HEMT/PM-HEMT fabrication technology will be discussed, outlining where appropriate key technologies for improved uniformity, yield and reproducibility of heterojunction device MMIC fabrication.

TECHNOLOGY EVALUATION

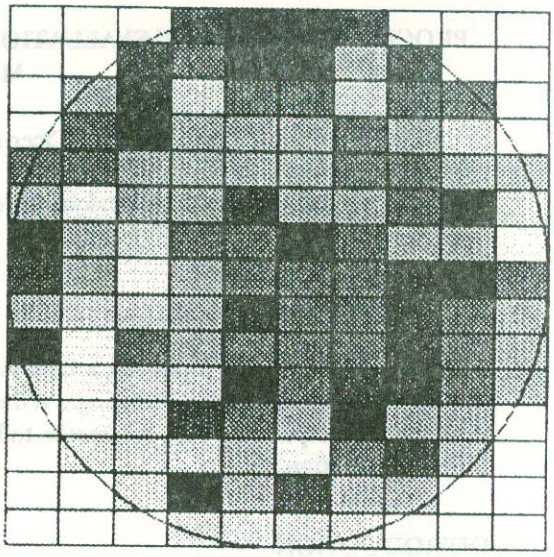
Epilayer Uniformity and Defect Density

For sucessful high yield monolithic integration of digital or microwave HEMT/PM-HEMT's, the quality of the heterojunction material is of prime importance. In particular, surface morphology (heterointerface roughness and compositional mismatch strain), layer thickness and doping uniformity should be well controlled and of high quality with minimal impurity and defect concentration.

Even thougth the molecular beam epitaxy (MBE) technique, with the ultimate in real time control of growth parameters, ensures very precise control of layer composition, doping profile and sharp layer transition, the final material quality is strongly dependent on pre-growth substrate preparation. The best results achieved with MBE growth are thickness/doping uniformity of ± 1% [8] and defect density of $50/cm^2$. Nevertheless, as will be demonstrated later, a layer uniformity of approximately ± 2% (see sheet resistance map in fig.1b) and defect density < $200/cm^2$, routenely achieved with well maintained systems, can be considered satisfactory for high yield MMIC fabrication.

The growth parameter details of the heterostructures studied in this work are presented in fig.1a. The n^+ - GaAs cap layer thickness, which can vary from 500 to 2000 Å, will be indicated where appropriate;

° GaAs:Si	500-2000 Å	$3.5x10^{18}$	
° AlGaAs:Si	300 Å	$1.0x10^{17}$	x(Al) = 0.22
° AlGaAs:Si	150 Å	$2.0x10^{18}$	x(Al) = 0.22
° AlGaAs	20 Å	undoped	x(Al) = 0.22
* InGaAs	130 Å	undoped	y(In) = 0.15
° GaAs buffer	5500 Å	undoped	x(Al) = 0/0.22



(a) (b)

Fig. 1 *Typical (a) HEMT (o) / PM-HEMT (o*) heterostructure utilised in this work and (b) material sheet resistance map for the PM-HEMT structure indicating typical on-wafer uniformity (i.e. 100 Ω / ± 1.8 %). Each gray tone corresponds to σ/3 variation.*

in particular the sheet resistance map in fig. 1b corresponds to a PM-HEMT structure with a 1000 Å thick cap.

Source/Drain Ohmic Contacts

Because HEMT's are large current and small voltage devices, the saturation voltage and transconductance are very sensitive to the contact resistance value. In fact to take full advantage of the HEMT potential, it is essential that extremely low contact resistances be achieved.

In general it is believed that the source resistance can be minimised by making the ohmic contact directly to the 2-DEG channel. Nevertheless with this approach it has been found that good, uniform contacts are difficult to achieve due to the presence of the highly reactive AlGaAs layer which can impede penetration to the 2-DEG channel. Even though many alloying techniques have been reported which utilise either high temperature (>500°C) annealing [9-11] and/or appropriate diffusion barriers [12-14] to overcome said inconvenience, from the reported results it is difficult to assess the validity of these techniques because either a one-layer TLM model (not valid for HEMT structures [15-17]) has been used, and/or no indication of on-wafer ohmic contact uniformity is given. Recently non-alloyed ohmic contacts to the 2-DEG [18] utilising a compositionally graded n^+ $In_xGa_{1-x}As$ ($0 \leq x \leq 0.5$) and heavily doped $In_{0.5}Ga_{0.5}As$ contact layer, have yielded better results with improved uniformity indicating that direct contact to the 2-DEG channel layer is not necessary [19] for low source contact resistance.

In the following we will illustrate that similar results can be obtained with conventional MESFET type alloyed contacts utilising Au:Ge/Ni/Au metalisation schemes. The basis of said approach is a good ohmic contact to the n^+ GaAs cap layer and tunnelling across the high band-gap AlGaAs layer [19] to achieve low contact resistance to the 2-DEG channel layer. The main advantage of this technique over the high temperature alloying techniques reported [9-14] is that by avoiding penetration across the AlGaAs layer good on-wafer contact uniformity can be achieved.

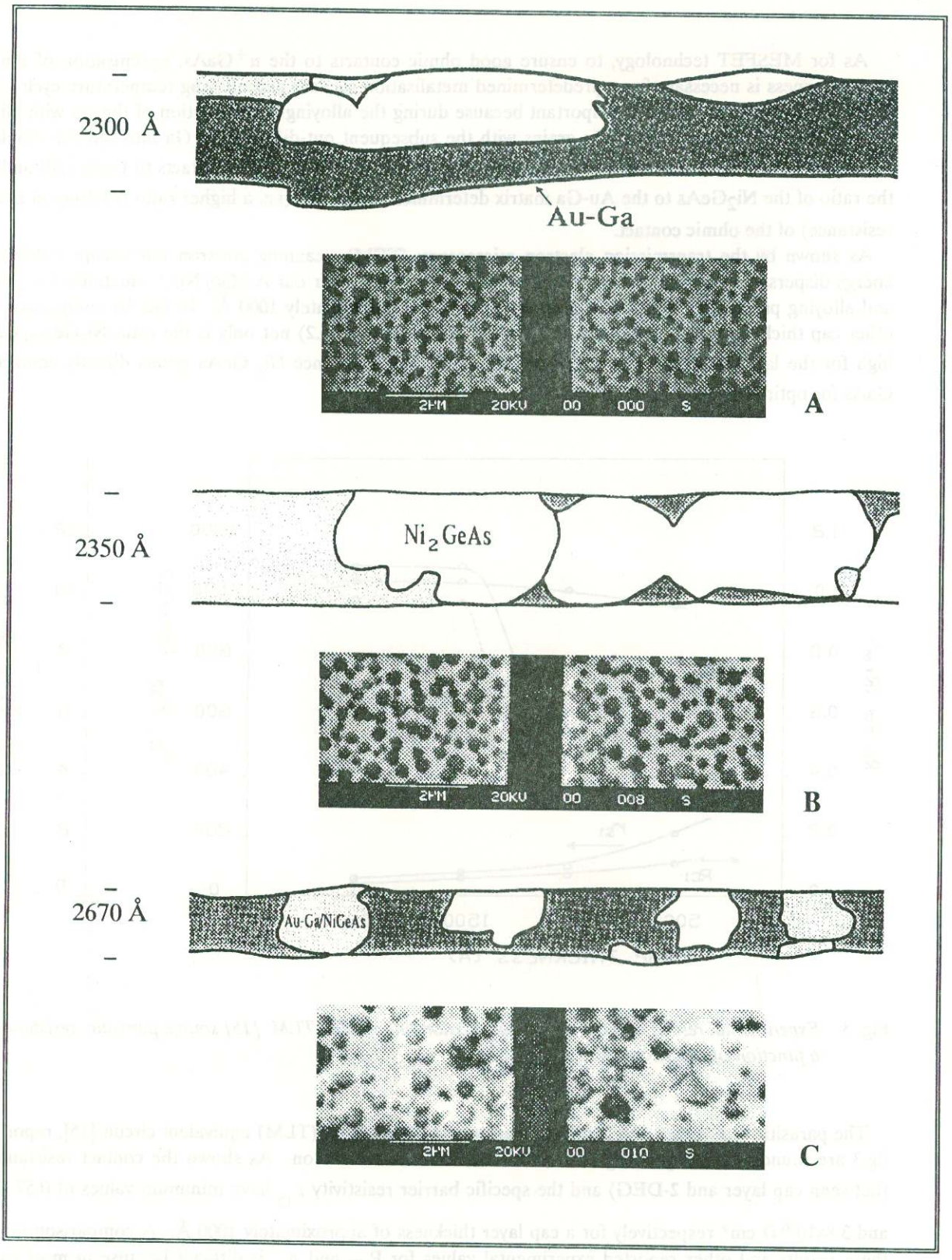


Fig.2 - *Schematic representation of TEM and SEM photographs for Au:Ge/Ni/Au contacts after alloying to (A) 500 Å, (B) 1000Å and (C) 1500 Å thick n^+ - GaAs cap layer.*

As for MESFET technology, to ensure good ohmic contacts to the n^+GaAs, optimisation of the cap layer thickness is necessary for a predetermined metalisation scheme and alloying temperature cycle. This optimisation phase is extremely important because during the alloying cycle reaction of the As with Ni and Ge to form low resistivity Ni_2GeAs grains with the subsequent out-diffusion of Ga into the Au should be critically controlled. In fact said Ni_2GeAs grains are understood to be good contacts to GaAs [20] and that the ratio of the Ni_2GeAs to the Au-Ga matrix determines the quality (i.e. a higher ratio resulting in a lower resistance) of the ohmic contact.

As shown by the transmission electron microscopy (TEM), scanning electron microscopy (SEM) and energy dispersive X-ray (EDX) analysis data presented in fig.2, for our Au:Ge/Ni/Au metalisation scheme and alloying profile the optimum cap layer thickness is approximately 1000 Å. In fact by comparison with other cap thicknesses (i.e. 500, 1500 and 2000 Å not shown in fig.2) not only is the ratio Ni_2GeAs/Ga-Au high for the latter condition but more important the low resistance Ni_2 GeAs grains directly contact the GaAs for optimum low resistance contact.

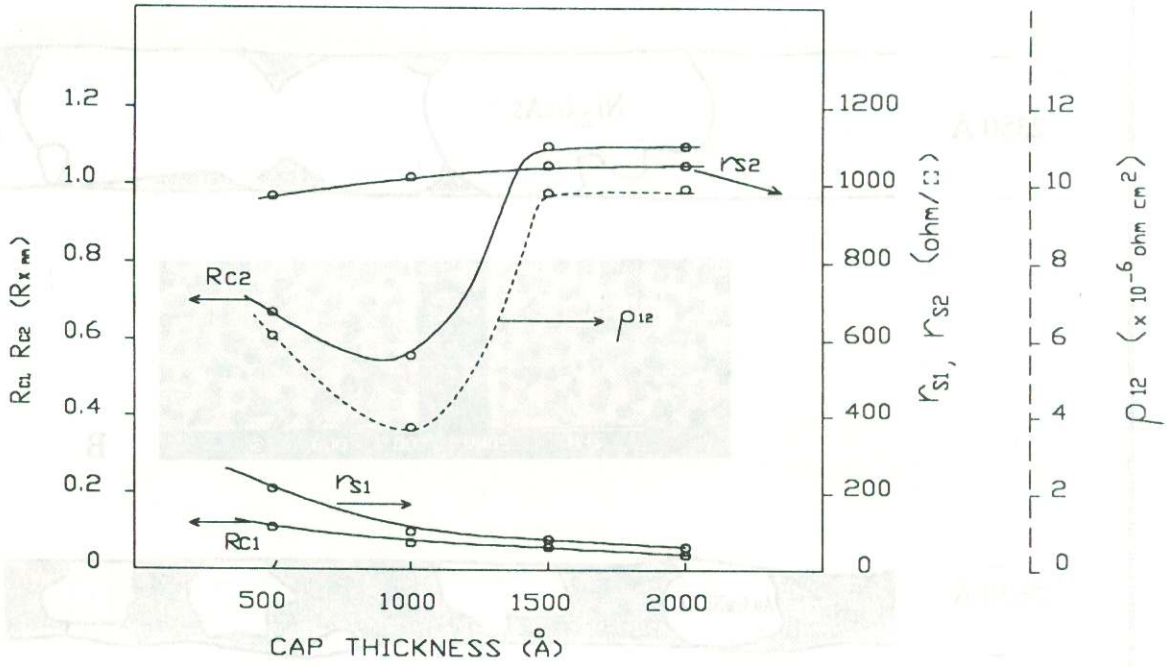


Fig. 3 *Experimental results of a two-layer transmission line model TLM [15] source parasitic resistances as a function of cap thickness.*

The parasitic resistances of a two-layer transmission line model (TLM) equivalent circuit [15], reported in fig.3 are found to be in good agreement with the above observation. As shown the contact resistanc R_{C2} (between cap layer and 2-DEG) and the specific barrier resistivity ρ_{12} have minimum values of 0.57 Ω mm and 3.8×10^{-6} Ω cm² respectively for a cap layer thickness of approximately 1000 Å. A comparison between these results and other reported experimental values for R_{C2} and ρ_{12} is difficult because in most cases a one-layer TLM has been used. Nevertheless said results compare favourably with Feuer's theoretical predictions [15] which for a HEMT structure, similar to that in fig. 1a, with a 500 Å thick cap layer gives $R_{C2} \approx 1.2\ \Omega \cdot$mm and $\rho_{12} \approx 1.5 \times 10^{-5}\ \Omega$ cm².

The one-layer contact resistances reported by others are equivalent to the contact resistance R_{C1} (between the alloyed metal and the n^+ GaAs cap layer) in the two-layer TLM equivalent circuit. As shown

in fig.3 said resistance is found to decrease with increasing cap thickness, ranging from 0.1 Ω·mm for a 500Å cap to 0.04 Ω·mm for a 2000 Å cap, in good agreement with other reported results [9-14]. As aspected the cap sheet resistance r_{s1} also decreases with increasing layer thickness whereas the channel sheet resistance r_{s2} remains constant at approximately 1000 Ω / .

Device r.f. noise performance at 12 GHz are in good agreement with the R_{C2} behaviour reported in fig.3. In particular the HEMT structure with a 500 Å cap yields noise figure of ≈ 1.3 db in comparison to ≈ 1 db with 1000Å cap and ≈ 1.5 db with the 1500 Å and 2000 Å cap. From the results presented in this section it is clearly evident that for best device performance the cap layer thickness must be optimised to the ohmic contact metalisation scheme and alloying temperature cycle. However what is not evident at this stage, but will be clarified in the final section, is that said optimisation also strongly influences the on-wafer device performance uniformity and as such fabrication yield.

Channel Recessing and Gate Definition

Because the HEMT/PM-HEMT donor layer is very thin and heavily doped, gate recessing of HEMT's is more difficult to control than MESFET's and as such the corresponding fabrication yield can be appreciably low if this process step is not critically controlled. To overcome this inconvenience highly selective wet chemical or dry plasma [21,22] etching, with controlled etch rate, undercutting and reproducibility, is mandatory for high yield HEMT fabrication.

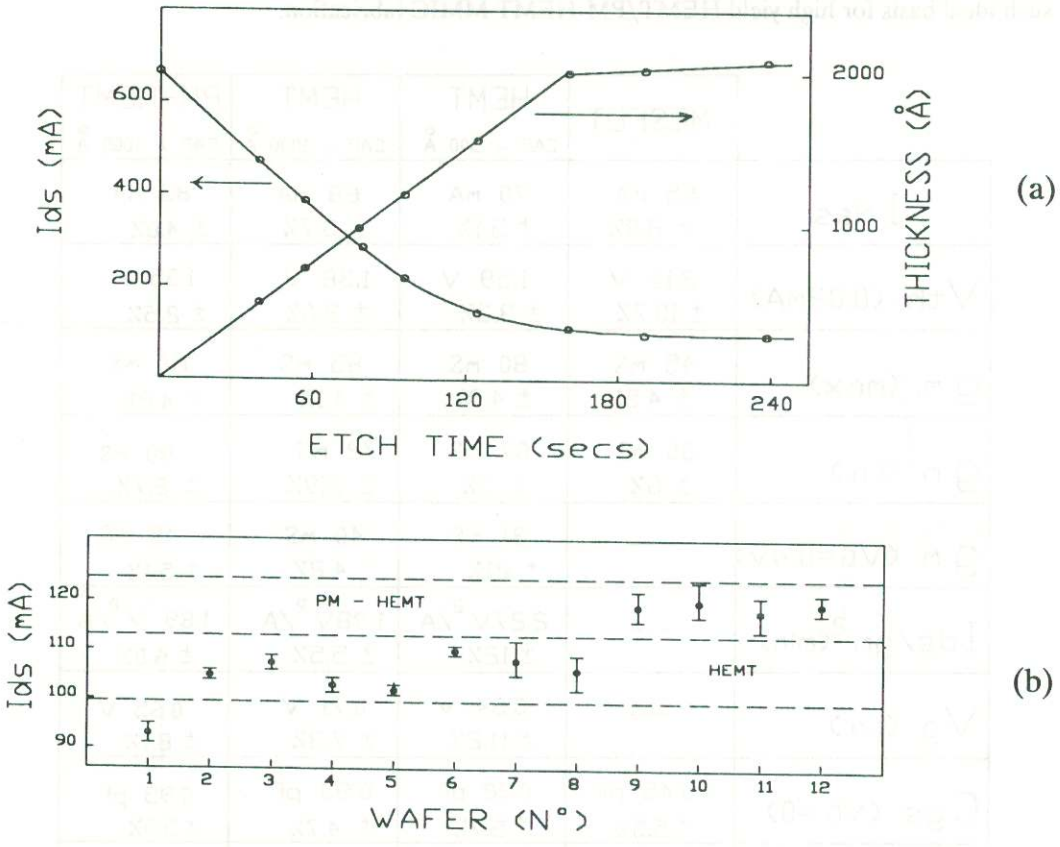


Fig. 4 *High selectivity wet etch solution for GaAs/AlGaAs (a) etch characteristics and (b) on-wafer and batch processing uniformity.*

In fig.4a we present typical etch profile characteristics of a solution with high etch rate selectivity between GaAs and $Al_{0.22}Ga_{0.78}As$ satisfying the criterion for high yield fabrication. As shown said solution has an etch rate of approximately 15Å/sec for GaAs and 1Å/sec for $Al_{0.22}Ga_{0.78}As$ with little to no undercutting. In fact for the latter parameter no degradation of device performance is observed with increase in donor layer "over-etch" time from 5 to 30 seconds.

As regards uniformity and reproducibility, the recessed channel drain currents (I_{ds}), presented in fig.4b, give a good indication of both on-wafer etch uniformity (± 2%) and uniformity from wafer to wafer (± 5%). Note that said uniformities also include inherent variations in donor layer (on-wafer and batch) doping and thickness variations.

The control of other gate parameters such as parasitic gate resistance, uniform submicron gate length and high gate-source alignment accuracy with short gate-source spacing is also important for high yield HEMT/PM-HEMT fabrication. Nevertheless after a conserted effort in this field in the early-mid eighties, these parameters are now fairly well controlled [23] and as such do not present a serious drawback to high yield device fabrication.

Device Performance and Yield

By incorporating the above aspects in our standard HEMT/PM-HEMT wafer-fab. processing technology which comprises: Au:Ge/Ni/Au alloyed ohmic contacts, proton isolation, Ti/Al gate metalisation, silicon nitride passivation and Ti/Pt/Au overlayer metalisation, high performance devices with better than 90% fabrication yields have been realised. Furthermore the improved ohmic contact and channel recessing technologies have resulted in excellent on-wafer uniformity and reproducibility (better than MESFET's) and as such ideal basis for high yield HEMT/PM-HEMT MMIC fabrication.

	MESFET	HEMT CAP ~ 500 Å	HEMT CAP ~ 1000 Å	PM-HEMT CAP ~ 1000 Å
Idss	65 mA ± 8.8%	70 mA ± 5.1%	68 mA ± 3.7%	83 mA ± 4.0%
Vth (0.02mA)	2.12 V ± 10.7%	1.59 V ± 3.3%	1.38 V ± 2.6%	1.35 V ± 2.5%
gm (max)	45 mS ± 4.5%	80 mS ± 4.9%	85 mS ± 4.1%	110 mS ± 4.2%
gm (l.n.)	30 mS ± 6%	67 mS ± 5%	72 mS ± 2.9%	90 mS ± 2.7%
gm (VG=0.4v)	—	31 mS ± 21%	40 mS ± 4.2%	45 mS ± 5.1%
Ids/gm^2(min)	—	$2.27V^2/A$ ± 12%	$1.98V^2/A$ ± 5.5%	$1.89\ V^2/A$ ± 6.0%
Vg (l.n.)	—	0.84 V ± 11.2%	0.71 V ± 7.3%	0.65 V ± 8.1%
Cgs (VG=0)	0.45 pF ± 5.5%	0.92 pF ± 5.7%	0.93 pF ± 4.7%	0.95 pF ± 5.0%
NF (12GHz) Gass (12GHz)	1.7 dB 7 dB	1.3 dB 10 dB	1.0 dB 11 dB	0.9 dB 13 dB

Tab. 1 *Noise performance and key electrical parameters for MESFET, HEMT and PM-HEMT devices fabricated with the same wafer fab technology.*

In table 1 we present the low-noise performance and key electrical parameters with corresponding tollerances for MESFET, HEMT and PM-HEMT devices fabricated with the same wafer-fab technology. To evidentiate the importance of ohmic contact optimisation, results from HEMT devices with a 500Å (resistive) and 1000Å (optimum) n^+GaAs cap layer thickness are included. From these results the following observations can be made:

i) selective channel recessing appreciably improves saturation current (I_{ds}) and pinch-off voltage (V_{th}) uniformity, i.e. standard deviation from mean value (S.D.) for MESFET is ± 10.7% whereas S.D. for HEMT/PM-HEMT is ± 2.6%;

ii) optimisation of alloyed ohmic contacts not only improves device performance (compare HEMT with 500 and 1000Å cap), but more important appreciably improves the on-wafer uniformity of key parameters such as, pinch-off voltage (from ± 3.3% to ±2.6%), transconductance for low-noise bias (from ± 5% to ± 2.9%), noise performance as indicated by I_{ds}/g_m^2 [24] (from ± 12% to ± 5.5%) and forward bias transconductance g_m (V_g= +0.4V) (from ±21% to ±4.2%). Note that the inverse of the latter condition is approximately proportional to the parasitic source resistance [25];

iii) gate definition is the same and as such input capacitance (C_{gs}) uniformity remains virtually unchanged for the different devices with SD approximately ± 5%.

CONCLUSION

In this work we have demonstrated that high performance HEMT/PM-HEMT devices can be fabricated with alloyed ohmic contacts which do not directly contact the 2-DEG. Said technique enables critical control of optimised ohmic contacts which together with a highly selective etch solution for channel recessing, enables very high yield/low tollerance active device fabrication, a necessary basis for high yield HEMT/PM-HEMT MMIC fabrication.

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