TECHNOLOGY, DESIGN AND RELIABILITY ISSUES IN GaAs POWER DEVICES

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Abstract

The paper gives an overview of the most important issues concerning technology, design, characterization, modelling and reliability of GaAs power devices with the purpose of highlighting the most critical factors which determine their performances.

Introduction

In spite of the fact that GaAs MESFET have an history of more than two decades [1], during the last few years, very remarkable advances have been obtained in GaAs power device basic performances, such as for example, operating frequency, output power and associated gain, power added efficiency and distortion characteristics.

Alcatel-Telettra has recently proven [2] its ability of efficiently produce state of the art power MESFETs. This fact involves the awareness and the solution of a wide number of problems concerning technology, measurements, modelling, design and reliability. This work gives an overview of the most important issues related to such a topic.

To this purpose the paper is divided in five sections. After a recognition of the basic design problems (section 1) the technological requirements needed for obtaining the desired performances are discussed (section 2). In section 3 a critical analysis is performed of the measurement techniques permitting an efficient power device design. Section 4 deals with the available tools and models for non linear design highlighting their practical capabilities in the development of high performance power circuits. Finally, in section 5, a synthetic description is given of the most relevant device reliability issues, including analysis procedures and failure mechanisms.

Basic design problems

The various class of operation (A,B,...) of the MESFET as power amplifier are well known from the basic electronics [3] and are founded on the behaviour of the device drain characteristics. From this simple d.c. analysis it follows that the power FET must have high gate to drain/source breakdown voltage, in order to be able to deal with high terminal voltages. Class A amplifiers, even if they have relatively low conversion efficiencies, play a major role in radio telecommunication equipments, because of their more linear performances.

In spite of its popularity, the analyses based on the power device d.c. I-V curves are scarcely representative of their microwave behaviour. In fact, at these frequencies, the breakdown voltages may have values much different from the d.c. ones [4], moreover the presence of surface states reduces the amount of the drain current which can be modulated by the r.f. signal, changes the breakdown voltages too and finally results in a consistent reduction of the device power handling capability.

These effects, which are difficult to control, are also responsible for the fact that the pulsed device I-V characteristics change with the FET d.c. bias point [5] and the fact that, for a fixed r.f. input signal and amplitude of applied voltages, gain and output power are higher when pulsing the drain than when pulsing the device gate [6].

An useful method for verifying the surface state effects is to look the frequency dispersion of the device transconductance at different gate biases. A good correlation exists between an high transconductance dispersion with frequency and a reduction of the device power handling capability [7].

Another important power FET design problem is due to their basically limited thermal dissipation capability. In fact GaAs has a thermal conductivity which is about three times lower that of the Si. This means that the device design must carefully consider all the means that aid the heat to be conducted away from the chip, such as for example mesh type topologies and wafer thinning to few tens of micrometers [8], properly fabricated heat sinks, etc..

Technology issues

While in the development of low noise devices the research work was mainly dedicated to advances in material quality and precision lithography, the power device development has mainly required improvements in channel and chip fabrication [1].

The achievement of good power device performances, as for output power, gain, conversion efficiency and distortion, implies specific technology features which permit to increase the FET breakdown voltages, keep the gain as most as possible constant under large signal operation, optimize the topology for reducing source inductance and losses or phase variations along the signal paths and, finally, decrease the thermal resistance.

On the side of material manufacturing good improvements

as for gain and distortion properties were made by adopting heterobuffer and hi-lo profile structures.

In Alcatel-Telettra an approach using a carbon p-buried layer under the Si implanted active layer was adopted. When used for fabricating power FETs, p-buried layers, which reduce the substrate leakage currents and make available very sharp doping profiles, allow, as well known [9], consistent improvements in output power and conversion efficiency.

In spite of its low diffusion coefficient and low amphotheric behaviour, C was rarely considered for producing p-buried layers, because of activation problems evidenced since the earlier reports [10]. A systematic experimental study performed at Alcatel-Telettra showed that, when a proper thermal annealing sequence is applied, extremely high C activations can be obtained.

This fact permitted the creation of a new capless thermal annealing procedure as well as fabrication and optimization of the coimplanted Si-C layers we currently use for power MESFET production.

In fig. 1, a comparison is reported between the typical doping profiles obtained with the old triple energy Si implant and the new Si-C coimplant: the new p-buried structure results in much steeper carrier drop at the interface.

In order to increase the gate breakdown voltages, attention must be paid in the device structure design (recessed gate, surface states, ...) to prevent the formation of locally concentrated electric fields.

The free surface of the channel is particularly exposed to possible damages during the thermal treatment dedicated to the ohmic contact formation. For this reason a procedure has been introduced where, during the process for ohmic contacts, the channel is covered by a properly optimized dielectric cap.

The effectiveness of this procedure is shown in Fig. 2 a and b, where the frequency dispersion curves of the device transconductance are reported for the new implant devices with passivation layer (curve b) and for the old implant FETs (curve a) respectively.

Finally, for reducing the thermal resistance a thinned device and a plated heat sink technology (bath tub, bell bottom), as well as an optimized FET topology were used.

Systematic load pull measurements performed at 5 GHz (with 8 V drain to source applied voltage and for class A operation) on 0.5*1200 μm test FETs of various processed wafers have shown the following mean results:

1. devices produced with the old process: output power at 1 dB gain compression P(1dB)=26.5 dBm, drain efficiency at 1dB compression deff=31%, linear gain G1=13.9dB, power added efficiency =29.5%;
2. device with the new Si-C implant and no dielectric layer: P(1dB)=27.3 dBm, deff=41%, G1=13.8dB, eadd=38.8%.
3. devices with the new implant and dielectric layer: P(1dB)=28.5 dBm, deff=50.1%, G1=14.2dB, eadd=47.6%.

A closed form analytical relationship, which permits of theoritically evaluating the power added efficiency of class A amplifiers under overdriven conditions, is reported in reference 1, chapter 1. The application of this formula to the above three cases yields:

eadd=30.9% for point 1 devices;
eadd=35% for point 2 devices;
eadd=40% for point 3 devices.

These results prove the effectiveness of the introduced process refinements, which allow the achievement of efficiencies even higher than those theoretically predicted.

Measurement techniques

The recent disclosure of large consumer markets to the use of power microwave devices opens a new phase where the increased need of competition for the products requires characterization procedures and models which allow consistent reduction of the project cycle times and offer a real possibility of first time success [4].

The efficient production of power FETs requires a great number of linear and non linear measurements to be made in d.c., in pulsed conditions, at low and at microwave frequencies on PCM (process contro monitor) devices with reduced gate width, on the elementary cells of the power FETs and, finally, on the power devices itselfs.

There is, on the subject, a wide literature which offer frequently different experimental solutions for enhancing the accuracy of the measurements [9,11-13]. For time and space saving reasons we will discuss here only the measurements we routinely perform [2,15-17].

The parameters extracted from d.c. measurements made on reduced gate width devices contained in the PCM are:

1. drain saturation current per unit gate width,
2. pinchoff voltage,
3. transconductance per unit gate width,
4. gate to source and gate to drain breakdown voltages,
5. active layer surface resistance,
6. gate length,
7. gate recess depth,

8. substrate leakage current,
9. ohmic contact resistance per unit contact width.

The parameters extracted from low frequency measurement on reduced width PCM devices are:

a) doping profile,
b) transconductance dispersion versus frequency.

Directly on wafer are also measured the scattering parameters of 200, 300 and 600 μm wide FETs, from which, with the technique described in section 3, are deduced the lumped element equivalent circuits. All the above measurements are mainly accomplished for evaluating the process quality.

On power FET elementary cells, having typically 1200 μm gate periphery, are first measured the pulsed I-V characteristics and the pulsed gate to drain breakdown voltage. Fig. 3 gives the block diagram of the used pulser, which allows a proper selection of the d.c. bias point and can be programmed via an HP IB interface.
Pulse rise and fall times are lower than 50 ns. Through the interface one can programme pulse width (between 200 ns and 10 ms), drain voltage amplitude (between 0 and +20 V) and gate voltage amplitude (between 0 and -20 V).
The maximum allowed drain current is 5 A.

Then, again on the elementary cells, linear S parameter measurements are made, directly on wafer, and the lumped element circuit is extracted. Subsequently, load pull measurements, as for output power and intermodulation products are made on the cells. Fig. 4 gives an example of load pull data so obtained.

Because of our special interest to the operation of the power FET in class A amplifiers, where the signal harmonic content is relatively low, the possibility of making load pull measurements where the load is varied also at the harmonic frequencies [18,20], was not considered.

Pulsed I-V measurements are also made on the final power FETs. For special applications [2,21], where particularly advanced device performances are needed, an on wafer selection of the power FETs can be also made, by means of a pulsed technique [2].

Models and design tools

Two basic types of models are available in the literature [22-25] for MESFET devices: behavioral and physics based. The former type makes use of equivalent circuits, mainly semiempirical, deduced with proper fitting procedures of experimental data. These models are largely inadequate for performance and yield optimizations requiring modifications of technological and processing parameters. The latter type of models [26-30] do not present such limitations, because the devices are described through physical models which provide the link between device performances and technological parameters.

The available physical MESFET models can have various complexity degrees, because they can vary from those which solve numerically the transport equation in a three dimensional space, to those numerical bidimensional or quasi bidimensional [31-32], until to the analytical bidimensional [29-30-34-35] ones.

Even if numerical device simulations have proven to be of some utility for us in the past for defining some basic parameters of the single power device [31], for the definition and the development of our products, which are typically class A power amplifiers in a given telecommunication band, the numerical models have proven to be largely unpractical because of the high computational effort required when dealing with harmonic balance circuit simulation or with performance optimization cycles.

In order to obtain simulation results reasonably close to the experimental ones physical models frequently require some manipulations usually called "model tuning". To this type of problems, particularly important for the forecast of the MMIC circuit yields, our laboratory has dedicated some original efforts [24,36].

The need of accurately forecast the power circuit performances, the difficulty of reaching satisfactory model tunings and the fact that, for the wide majority of our own applications no MESFET technological parameter variations are desired, put into evidence the very important practical role played again by the experimentally based device behavioral models.

An outstanding problem for these and for other models is the accurate extraction from the experimental data of their parameters. For linear models this is achieved trough fitting procedures which require, beside the measurement of the "warm" device S parameters, the availability of the "cold" device S parameters [37-41] and, sometimes, of other experimental data [24].

As for the practical design of power amplifier circuits is concerned, we observe that three basic methods are now available in the literature [42]. The first method requires the extraction of a bias dependent equivalent circuit from S parameters measured at different bias levels. The method is rather inadequate for designs with power FETs, because trapping and temperature effects are ignored. The second method makes use of I-V characteristics measured in pulsed conditions starting from the d.c. device bias point. This approach gives very accurate results only for small signals, because it ignores the temperature effects due to the power transfer from the device to the load. The third method makes use of pulsed S parameters measured by pulsing the applied voltages around the device d.c. bias conditions. This

approach also ignores the power transfer temperature effects and has a number of practical limitations [43]: it requires a network analyzer with pulsed bias ability and its full automatization is complex and relatively difficult.

For these reasons we generally prefer a fourth method [2] which permits to overcome the power transfer temperature effects and makes use of the S parameters measured at the FET bias point and of I-V characteristics obtained by driving the device at low frequency (2 MHz) with a load resistance which can be varied around the optimum value for output power. Reactive FET equivalent circuit parameters are extracted from S parameters while I-V curves are fitted by a Materka [44] or a modified Materka model [45].

When dealing with the thermal design of power MESFETs one must evaluate, on the basis of the device topology, the thermal FET impedance. An useful closed form semiempirical formula for obtaining this parameter is given in [46].

Numerical solutions to the problem are also available [47-51]. They are mainly based on the fact that the solution of thermal problems can be easily extracted for the microwave literature since thermal and electrical problems obey to the same partial differential equation [12,52,56].

GaAs power MESFET reliability issues

Power MESFET reliability control is mandatory for most telecommunication applications. Reliability assurance requires analyses of degraded and failed devices by both field and accelerated life tests. The results of d.c. accelerated tests seem to be sufficiently significant for study the device reliability and are much easier to perform than r.f. tests and no less meaningful. According to our experience [52-58], the following failure mechanisms play a major role:

a) degradation of GaAs surface between gate and source or drain;
b) degradation of ohmic contacts;
c) degradation of the gate Schottky barrier and of the channel region under the gate;
d) electromigration of the gate metallizations.

An intrinsic weakness of the GaAs devices is the absence of a stable native oxide (as in the case of Si based devices) therefore surface effects play an important role. In fact the use of surface passivations, in particular silicon nitride, improves the MESFET reliability [54,59,60].

Surface degradation appears as a drop in the isolation between gate and drain or source. The phenomenon is greatly enhanced by temperature and this seem to confirm the failure mechanism proposed by Capasso and Williams [61] which blames the free As, left by Ga oxidation, for the high leakage current.

A different explanation imputes the cause of failure to a field assisted metal diffusion, chiefly Au from ohmic contacts [62].

Results from life tests made in our laboratory confirm the existence of a surface phenomenon, since the leakage current is reduce by a light chemical etch.

A drop in the saturation current can be caused by degradation of the gate Schottky barrier or of the active channel portion under the gate, owing to metal-semiconductor interdiffusion. This type of phenomena is dependent on the materials used for the gate [60,63].

Al is still an used gate material, but is sensitive to electromigration and to Al-Au intermetallic formation and corrosion [59,64]. Gold based metallizations are frequently employed in power devices.

Unfortunately, Au and GaAs interact strongly at low temperatures, giving rise to intermetallic compounds that alter dimensions, stoichiometry and electrical characteristics of the channel region.

In order to avoid Au and GaAs interdiffusion, barrier layers such as Ti/W, Ti/Pt, or Ti/Pd are employed. However, the presence of a barrier layer does not guarantee against degradation, as shown in fig. 5, where the increase in the channel resistance [65] together with the fall in pinchoff voltage and saturation current point to Au GaAs interaction, caused by W barrier permeability [54].

The experience gained in evaluating both commercial and internal devices has enabled us to set up a complete test procedure for the reliability evaluation, based on specific studies of the possible failure mechanisms (see table 1).
HTS put into evidence degradations of GaAs surface and metallization.
HTOT, with d.c. bias, covers the combined effects of temperature and electric field.
HTRB is a specific test for surface effects and breakdown stability.
HFGC accelerates electromigration phenomena.

The knowledge of failure mechanisms and the relations between stress and device degradation is not sufficient for guarantee the reliability of the equipments.
Process control steps in the working cycle, several screening procedures as well as the verification (based on the knowledge of degradation factors and on accelerated stress tests) that the devices operate in cautionary condition enable to reach satisfactory results.

The effectiveness of this approach is supported by our results on MESFET reliability in field applications. The

observed failure rate is, in fact, less than 200 FIT in a 3 year's observation period.

For our devices, a close correlation between d.c. and r.f. parameters was obtained from an accelerated life test at Tcase=175°C, as shown in fig. 6. In particular, a 40% reduction in saturation current corresponds to 3dB output power degradation (at the 1dB gain compression point).

According to our experience the most significant between the d.c. tests are:

a) high temperature storage (HTS)
b) high temperature life test (HTOT)
c) high temperature reverse bias test (HTRB)
d) high temperature, high forward gate current test (HFGC).

Conclusions

Alcatel-Telettra has a solid background in developing and producing state of the art power MESFET devices. This fact involves the setting up of a large number of techniques and the solution of various problems concerning technology, measurements, parameter extraction, modelling and reliability. In this work a survey and a critical analysis has been given of the most important issues relevant to this topic.

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References

[1] J.L. Walker, "High power GaAs FET amplifiers" Artech House ed., Boston, USA, 1993.

[2] E.M. Bastida, G.P. Donzelli, F. Magistrali and M. Pagani, "Efficient development of power FETs and micromodules" Proc. 23th European Microwave Conference, pp.804-807, Madrid, Spain, Sept. 1993.

[3] J. Millman, "Microelectronics" Mc: Grew Hill ed. 1987.

[4] M. Golio, "Characterization, parameter extraction and modeling for high frequency applications" Proc. 23th European Microwave Conference, pp.69-72. [illegible]. Spain, Sept. 1993.

[5] A. Platzker, A. Pal[illegible] Nash, W. Struble and Y. Tajima, "Characterization [illegible] devices by a versatile pulsed I-V Measurement" 1990 IEEE MTT-S Symp. Dig. pp.1137-1140.

[6] P.C. Wade, "Pulsed GaAs FET operation for high pick output powers" Electronics Letters, vol.15, n.19, pp.591-593, 13th September 1979.

[7] B. Gabbrielli, F. Abate and C. Longari, "Caratterizzazione su fetta a bassa frequenza di anomalie di processo non evidenziabili mediante misure in continua" Alcatel-Telettra techn. note n.15/4178 July 1993.

[8] M. Fukuta, I. Mimura, I Isujimura and H. Ishikawa, "Mesh source type microwave power FET" IEEE Int. Solid-State Circuit Conf. Dig., 1973, pp.84-85.

[9] H.M. Macksey, G.E. Brehm and S.E. Matteson, "Improved power FET performance using Be co-implantation" IEEE El. Dev. Letters, Vol. EDL-8, n.3, pp.116-117.

[10] B.K. Shin, "Carbon coimplanted gallium arsenide" Appl. Phis. Lett., Vol.29, n.7, pp.438-440, Oct. 1976.

[11] G.D. Vendelin, A.M. Pavio and U.L. Rhode, "Microwave circuit design using linear and non linear techniques" J. Wiley and Sons ed. New York 1990.

[12] J.V. Di Lorenzo and D.D. Khandelwal, "GaAs FET Principles and technology" Artech House ed., Dedham, Ma USA, 1982.

[13] P.H. Ladbrooke, "MMIC design: GaAs FETs and HEMTs" Artech House, Noorwood, Ma, USA 1989.

[14] R.S. Pengelly, "Microwave field effect transistors: theory, design and applications" Research Studies Press ed., London, 1986.

[15] Final Report for Contract POEM-1 ASAR PHASE 2, Alcatel-Telettra Rept., Vimercate (Mi) Italy, Sept. 1993.

[16] "Design Manual for power and linear MMICs" Alcatel-Telettra ed., Vimercate (Mi) Italy, 1993.

[17] A. Castelli, C.L. Scopelliti and F. Rasà, "High power and high efficiency ion implanted GaAs MESFETs with buried p layers" presented at this Conference.

[18] A. Ferrero and O. Pisani, "A generalized harmonic load pull system" 3rd Asian Pacific Microwave Conf., pp.49-52, Tokio, Sept. 1990.

[19] A. Ferrero and O. Pisani, "Large signal second harmonic on wafer MESFET characterization" 36th ARFIG Conf. Dig., Nov. 1990.

[20] A. Ferrero, U. Pisani and M. Pagani, "Microwave devices for MMIC power amplifiers: non linear experimental characterization" Proc. 3rd Int. Works. on GaAs in Telecom., pp.97-103, Vimercate, Italy, March 1991.

[21] E.M. Bastida, C. Longari, F. Rasà and C.L. Scopelliti, "Microwave power modules for terrestrial and space applications" Proc. 4th Int. Works. on GaAs in Telecom., pp.15-22, Milan, Italy, April 1993.

[22] F. Filicori, G. Ghione and C.U. Naldi, "Physics based electron devices modeling and computer aided MMIC design" IEEE Trans. MTT, vol.46, pp.1333-1352, July 1992.

[23] J.W. Bandler, R.M. Biernaki, Q. Cai, S.R. Chen, S. Ye and Q.J. Zhan, "Integrated physics oriented statistical modeling, simulation, optimization" IEEE Trans. MTT vol.46, pp.1374-1400, July 1992.

[24] E.M. Bastida, G.P. Donzelli and M. Pagani, "Efficient development of mass producible MMIC circuits" IEEE Trans. MTT vol.46, pp.1364-1373, July 1992.

[25] E.M. Bastida, G.P. Donzelli, F. Magistrali and M. Pagani, "Design, yield and reliability issues in mass producible MMICs" Proc. 23th European Microwave Conference, pp.19-25, Madrid, Spain, Sept. 1993.

[26] R.R. Pantoja, M.J. Howes, J.R. Richardson and C.M. Snowden, "A large signal physical model for computer aided design and its applications" IEEE Trans. MTT vol.37, pp.2039-2045, 1992.

[27] Y.K. Feng and A. Hintz, "Simulation of submicrometre GaAs MESFET by using a full dinamic transport model" IEEE Trans. ED, vol.35, pp.1419-1431, 1988.

[28] B. Carnez, "Modelling of submicrometre gate FET including effects of non stationary electron dynamics" Jour. Appl. Phys., Vol.51, pp.784-790.

[29] A. Madjar and F. Rosenbaum, "A large signal model for the GaAs MESFET" IEEE Trans. MTT, vol.29, pp.781-788, 1981.

[30] M. Khatizbadeh and R. Trew, "A large signal analytic model for GaAs MESFET" IEEE Trans. MTT, vol.36, pp.231-238, 1988.

[31] G. Ghione, C.U. Naldi, F. Filicori, M. Cipelletti and G. Locatelli, "MESS-A two dimensional physical device simulator and its applications to the development of C-band power MESFETs" Alta frequenza, pp.295-309, Sept. 1988.

[32] C.M. Snowden and D. Loret, "Two dimensional hot electron models for short gate lenght GaAs MESFETs" IEEE Trans. on ED vol.34, pp.212-223, Feb. 1987.

[33] C.M. Snowden and R. Pantoja, "Quasi two dimensional simulation for CAD" IEEE Trans. on ED, vol.36, Sept. 1989.

[34] JK. Yamaguci and H. Kodera, "Drain conductance of junction gate

FETs in hot electron range" IEEE Trans. on ED, vol.23, pp.545-553, June 1976.
[35] P. Pouvil, J. Gautier and D. Pasquet, "A new analytical model for the GaAs power MESFET in the saturation region" IEEE Trans. on ED, vol.35, pp.1215-1222, Aug. 1988.
[36] E.M. Bastida and M. Pagani, "A new method for MMIC parametric yield realistic evaluations" Proc. of the 1992 GaAs Applic. Symp., Noordwjik, The Netherlands, April 1992.
[37] R. Anholt, R. Worley and R. Neidhart, "S parameter and equivalent circuit parameter statistics" 1990, 35th ARFIG Conf. Dig., pp.47-53.
[38] R. Anholt, J. King, R. Worley and J. Gillespie, "Relationships between process and material variations and variations in S and equivalent circuit parameters" 1991 Int. Journ. Microwave and MM-wave CAE, vol.1, pp.271-281.
[39] A. Ferrero, U. Pisani and C.L. Scopelliti, "From foundry to the model: fabrication, process characterization and modeling of MESFETs" 1990 Proc. GaAs Applic. Symp., pp.320-325.
[40] A. Ferrero and O. Pisani, "Computer aided characterization and small signal modelling of MESFETs" 1990 Eur. Trans. on Telecom. and Rel. Technol., vol.1, pp.477-486.
[41] F. Diamant and M. Laviron, "Measurement of the extrinsic series elements of a microwave MESFET under zero current conditions" Proc. of the 12th European Microwave Conference, pp.451-456, 1982.
[42] J.P. Vidalou, J.P. Grossier, M. Chaumas, M. Camiade, F. Roux and J. Obregon, "Accurate non linear transistor modeling using pulsed S parameters measurements under pulsed bias conditions" 1991 IEEE MTTS Dig., pp.95-98.
[43] J.P. Theyssier, R. Quéré and J. Obregon, "Accurate non linear characterization of microwave semiconductor devices using pulse measurement techniques" 1989 IEEE MTT/AB Work. Dig., pp.208-209, Ratingen, Germany.
[44] A. Materka and I. Kacprzak, "Computer calculation of large signal GaAs FET amplifier characteristics" 1985 IEEE Trans. vol. MTT-33, pp.129-135.
[45] W. Struble, S.L.G. Chu, M.J. Schindler, Y. Tajima and J. Huang, "Modelling intermodulation distortion GaAs MESFETs using pulsed I-V characteristics" 1991 GaAs Symp. Dig., pp.179-182.
[46] K. Ohta, "Microwave semiconductor devices" Fujitsu Scientific Technical Journal, Vol.24, n.4, pp.359-371, December 1988.
[47] G. Ghione and C. Naldi, "High resolution self-consistent thermal modeling of multigate power MESFETs" Proc. of the International Electron Device Meeting, pp.12.6,1-4.
[48] G.P. Donzelli, G. Ghione and C. Naldi, "Thermal models for low and high-power GaAs MESFET devices" Proc. of the 1990 GaAs Application Symp., pp.120-127, Roma, Italy, April 1990.
[49] G. Ghione, P. Golzio and C. Naldi, "Thermal analysis of power GaAs MESFETs" Proc. of NASECODE V., pp.195-200, Boole Press, 1987.
[50] G. Ghione and C. Naldi, "A self consistent thermal simulator of multigate GaAs active devices" Proc. of the 1989 ESPRIT Week, Bruxelles, Nov. 1989.
[51] V. Rizzoni, A. Lipparini, V. Degli Esposti, F. Mastri and C. Cecchetti, "Simultaneous thermal and electrical analysis of non-linear microwave circuits" IEEE Trans., Vol. MTT-40, n.7, pp.1446-1455, July 1992.
[52] F. Magistrali and M. Sangalli, "Reliability of High power GaAs FETs" Proc. 4th Int. Works. on GaAs in Telecom., pp.131-137, Milan, Italy, April 1993.
[53] C. Canali, F. Castaldo, F. Fantini, D. Ogliari, L. Umena and E. Zanoni, "Power MESFET reliability aspects and failure mechanisms" Microelectronics and Reliability, vol.24, pp.947-955, 1984.
[54] C. Canali and F. Magistrali, "Degradation mechanisms induced by temperature in power MESFETs" Electronics Letters, n.21, pp.600-601, 1985.
[55] C. Canali, F. Castaldo, F. Fantini, D. Ogliari, L. Umena and F. Zanoni, "Gate metallization sinking into the active channel in Ti/W/Au metalized power MESFETs" IEEE Elect. Dev. Lett., March 1986
[56] E.M. Bastida "Monolithic microwave integrated circuits design/qualification requirements" 1990 Final Report for ESA/ESTEC Contr. n.7419/87/NL, vol.1, pp.1-540.
[57] M. Zicolillo and G.F. Piacentini, "Affidabilità e analisi dei guasti nei dispositivi per microonde" Seminario Scientifico Tecnico di Lecce su tecnologie del GaAs e composti connessi, 183, pp.387-432.
[58] E.M. Bastida and G.P. Donzelli, "An experimentally based systematic approach for yield and reliability evaluation in GaAs MMICs" 1990 GaAs Appl. Symp., pp.290-295, Rome, April 1990.
[59] J.C. Irvin, "The reliability of GaAs FETs" in J.V. Di Lorenzo, DD. Khandelwall "GaAs FET principles and technologies" Artech House, Dedham, MA, USA, 1982 Chapt. B.
[60] J.M. Dumas, D. Lecrousier, J. Paugan and C. Vuchener, "Comparative reliability study of GaAs power MESFETs: mechanism for surface-induced degradation and reliable solution" Electr. Lett. 1985, n.21, pp.115-116.
[61] F. Capasso and G.F. Williams, "A proposed hydrogenation/mitridization ..." Journ. Electrochmical Society, n.129, pp.821-824, 1982.
[62] J. Dell, I.S. Kalkur, Z. Meglicki, A.G. Nassibianand and H.L. Hartnagel, "Au-Ge-Ni migration effects by operating conditions of GaAs MESFETs" Solid State Electronics, n.27, pp.447-452, 1984.
[63] C. Canali, L. Umena, F. Fantini, A. Scorzoni and E. Zanoni, "Increase in barrier height of Al/n-GaA contacts induced by high current" IEEE Elect. Dev. Letters, June 1986.
[64] J.V. Davey and A. Cristou, "Reliability and degradation of active III-V semiconductor devices" in M.J. Howes, D.V. Morgan "Reliability and degradation" Wiley ed., UK, Chapter 3.
[65] H. Fukui, "Determination of the basic device parameters of GaAs MESFET" Bell System Techn. Jour. n.58, pp.771-779, 1979.
[66] T. Itoh and H. Yanai, "Stability of performances and interfacial problems in GaAs MESFETs" IEEE Trans. vol. ED-27, pp.1037-1043, 1980.
[67] I. Drukier and J.F. Silicox jr., "On the reliability of power GaAs FETs" IEEE Reliability Physics Proceedings, 1979, n.17, pp.150-155.
[68] T. Ithoh and H. Yanai, "Stability of performance and interfacial problems in GaAs MESFETs" IEEE Trans. Vol. ED-27, pp.1037-1045, 1980.
[69] W.J. Roesh and M.F. Peters, "Depletion model GaAs I.C. reliability" Proc. of the 1987 GaAs IC Symposium, Portland, Oregon, October 1987.

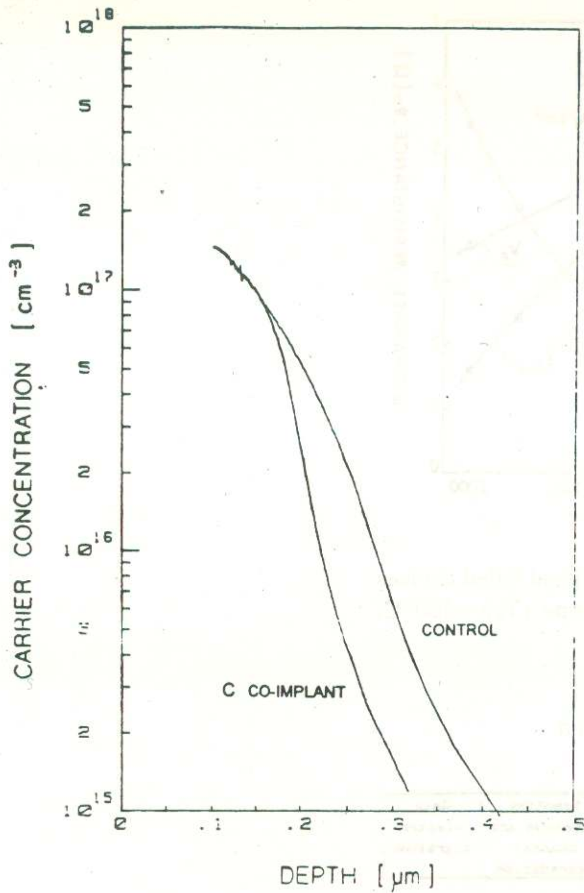


Fig. 1 - Carrier concentration profiles with and without C coimplant.

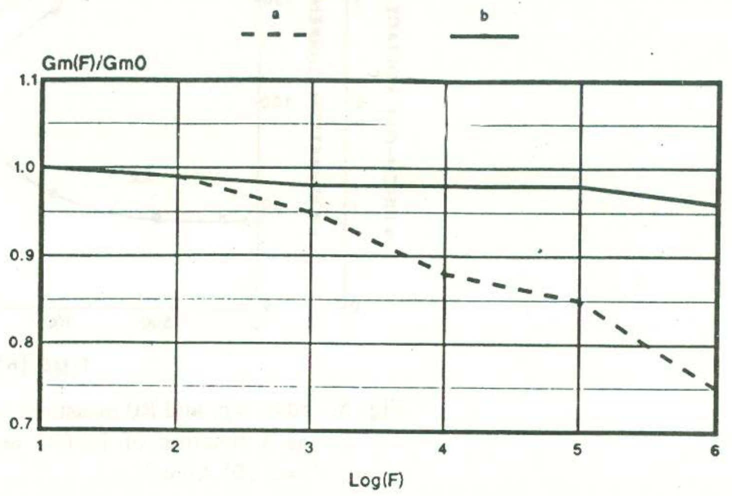


Fig. 2 - Gm frequency dispersion
a) control
b) p-buried / Si_3N_4 cap

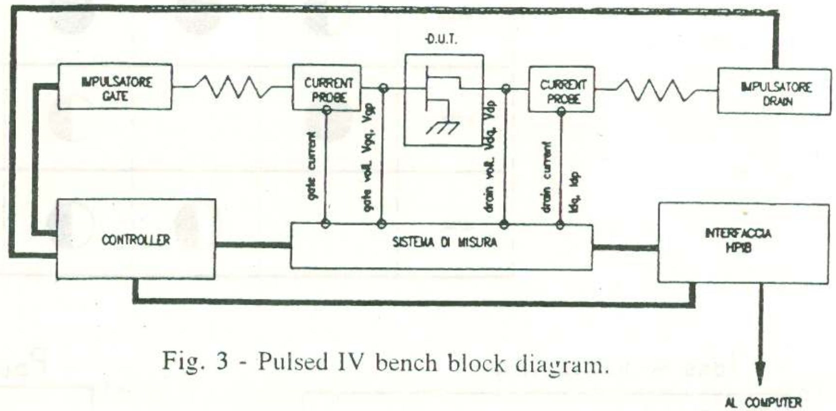


Fig. 3 - Pulsed IV bench block diagram.

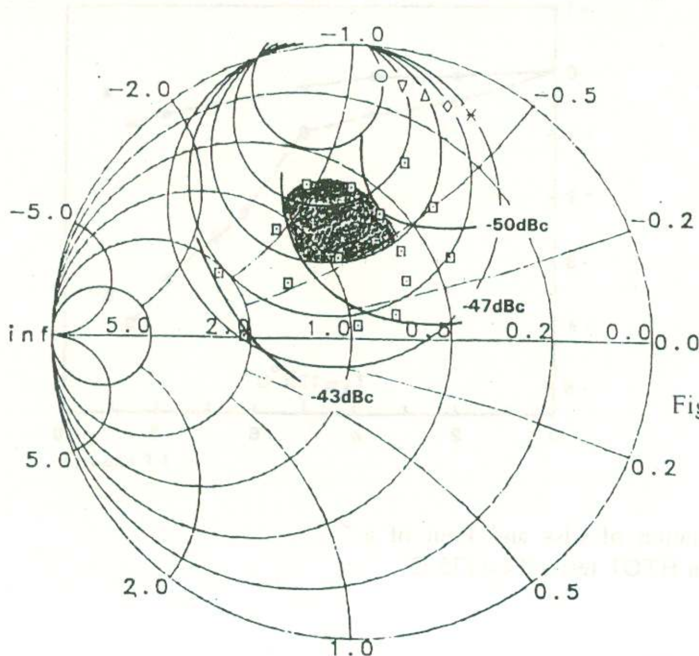


Fig. 4 - Load pull data for FET Elementary cell (1200μm wide).

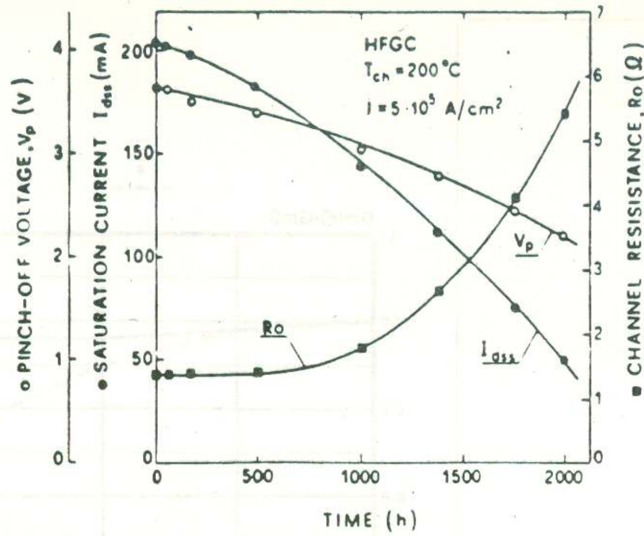
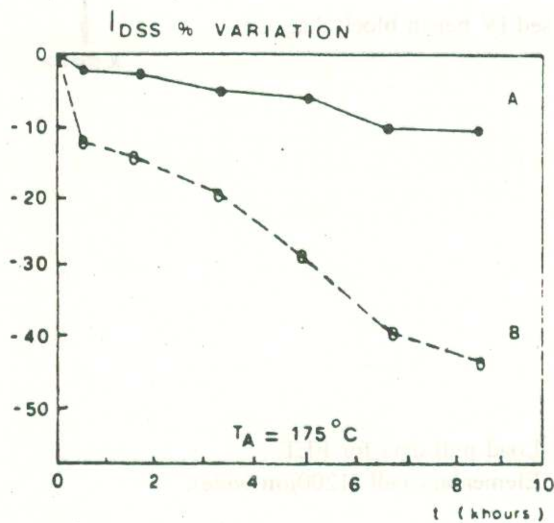


Fig. 5 - Idss, Vp_1 and R0 measured in typical failed devices as a function of HFGC test time (Tch=200°C, j=5·10^5 A/cm^2).

Table 1 - Reliability test plan.

Mechanism / Test	GaAs surface degradation	Ohmic contact degradation	Schottky junction and channel degradation	Gate electro-migration
HTS	●	●	●	
HTOT	◑	●	●	
HTRB	●		◑	
HFGC		◑	◑	●



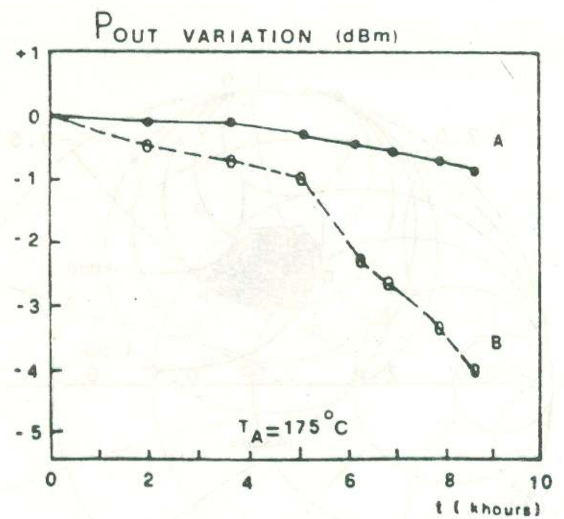


Fig. 6 - Comparison of variation of Idss and Pout of a MESFET stressed in HTOT test a Ta=175 C.