Setting Up a Full-Custom Design Environment on Cadence For GaAs Technology.

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Abstract

In this paper we present a complete set of arrangements made in the Cadence environment, to support full-custom design of digital integrated circuits for 0.8µm E/D MESFET GaAs technology. Schematic and layout capture, circuit analysis, layout verification and HSPICE electrical simulation can all be made in this environment. This work intends to help in the rapid dissemination of this advanced VLSI technology among University laboratories. Other related works on CAD tools for automatic synthesis of GaAs digital circuits are under development.

Introduction.

Advances in GaAs digital integrated circuits have made possible VLSI complexity levels and have very high speed circuits with low power consumption. A strong growth of the market share of GaAs technology in the fields of intensive data and signal processing has been forecasted for next years.

A large effort is being made by the scientific community to set up basic devices, logic families, device models, analysis and simulation tools, and design methodologies, able to support this technology. Some examples are found in [1], [2] and [3]. This technology also brings about several issues no dealt with in previous, well-established technologies. The work here reported aims to meet the demand of chip level design tools for GaAs digital integrated circuits. In particular, the tools have been used in several designs for 0.8 µm E/D MESFET DCFL GaAs technology ([4], [5], [6]).

The main idea behind this work is to use a design environment able to cover all phases of the design process within a single and same user interface and a single database. Cadence has been the choice because it features facilities for adapting different technologies and for integrating external tools into the environment[7], as well as it is available to the most universities in Europe.

The paper is structured as follow. Section 2 describes the adaptation and arrangements made in Cadence for design capture and layout edition. Section 3 presents those aspects related to layout verification for GaAs circuits. Section 4 give the results and conclusions of the work repeated and introduces further work that is currently under way.

Physical design in Cadence.

In this section we give some details about the tasks involved in the process of capturing the physical design of a circuit from transistor level down to symbolic and geometric layout. All layers required by the different layout masks, the design rules of this technology and the symbolic devices have been carried out.

A first design capture at transistor level, including transistor sizing, is done before layout to get a preliminary knowledge of the behaviour of the module under development. This design is then verified using HSPICE as electrical simulator with the corresponding MESFET models. This design is also useful later, for schematic versus layout comparison and for topological and dimensional module verification. For this purpose, the designer is provided with a set of basic gates that the netlist generator can recognize. The dimensions of transistors in these gates are parameterizable and can be easily configured, if desired. Otherwise, it is possible to use default dimensions, the most used in the design. NOR, NOR-OR, XOR, inverters, buffers and other MESFET-based (DCFL, SDCFL and SCFL) logic gates are provided.

Within Cadence tools have in common features as hierarchical design, multiwindow presentation, simultaneous edition of several circuits in different representations, and on-line access to verification. Basic tools available are a polygon editor, an editor of parameterizable cells, and an editor and compactor of symbolic layout. In the CMA setting up we have provided ready access to all these editors. As a result transistors, vias, contacts, basic gates, etc. are available and can be parameterized according to the dimensions specified by the user.

Using symbolic layout and compaction techniques can reuse the effort invested in layout design. In GaAs technologies, area and power are goals to optimize. Therefore, compaction is a critical step of layout design. The solution is to use a regular and structured layout technique as is presented in [1].

We have write the appropriate technology files to set up the symbolic layout design. Also it is necessary to develop a design methodology to cope with specific problems encountered. For example, the use of constrains, hences (soft and hard), the strategy of compaction (flat, or hierarchical).

Design analysis and verification from layout.

Cadence is technology independent and therefore can be configured for GaAs technology. This setting of the tools is done by generating the technology file containing the appropriate technology dependent information required by each tool, in a language known to the environment.

Netlist and electrical parameter extraction are carried out. The extractor has special functions for generating extracted representations. These are:

- Recognition of active devices.
- Extraction and measurement of device parameters.
- Recognition and extraction of parasitic devices.
- Storage of all selected data.

Objects extracted from layout belong to three classes: parameters, graphical (mask) layers, both original and derived, and terminals. Parameters define the variables related to each device and interconnect in the circuit. Values assigned to these variables are measured by the extractor and attached to each device.

In the parameter extraction task, length and width of each transistor gate, and therefore its loading capacity is measured. These data are used by HSPICE for simulation. Parasitic capacitances due to device interconnections depend on three magnitudes: area, perimeter and equivalent interconnection length. The method we have implemented for determining the equivalent interconnection length consists (Fig. 1) of finding the length of an equivalent rectangle whose area and perimeter coincide with those of the interconnection [8].

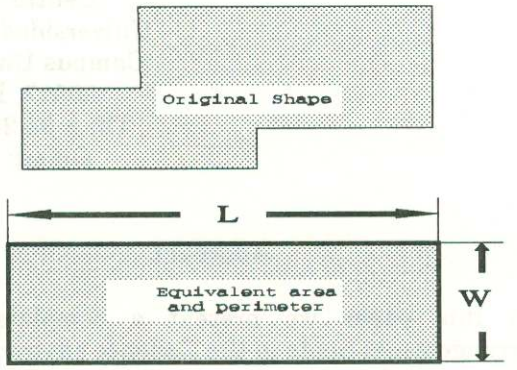

Fig. 1 Equivalent box for capacitance estimation.

Ground capacitances for each extracted node are computed by the following expressions:

$$C = L \cdot W \cdot C_a + 2 \cdot (L + W) \cdot C_p + MAX(W,L) \cdot C_l \quad (1)$$

As way of example, Fig. 3 show results after extracting a basic cell.

Layout versus schematic comparison is carried out in Cadence. In this way any discrepancy between both representations can be found and checked. Specified and extracted electrical parameters can be compared to each other. In our implementation for GaAs the specific technology file has been set properly for the topology option (only netlist are compared) and for the geometry option (both netlist and device geometries are compared).

Conclusions and further work

A complete set of arrangements made in the Cadence environment for GaAs technology is presented. Format converters and configuration and technology files developed give full support to full-custom design of digital integrated circuits for 0.8μm E/D MESFET GaAs logic, such as DCFL, SDFCL and SCFL.

With this environment all phases of the design

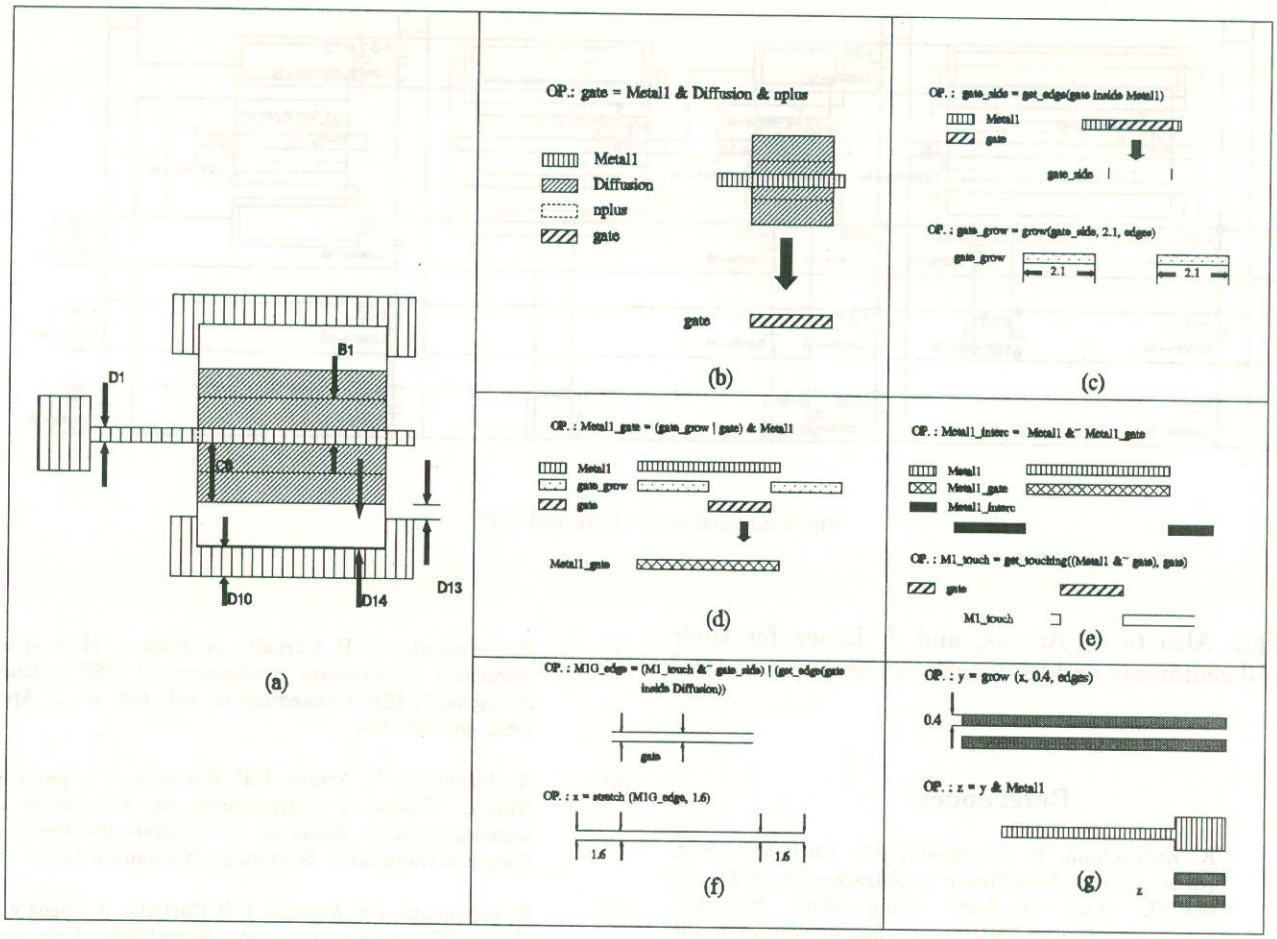

Fig. 2 Basic operations for layer processing.

process from layout edition to circuit analysis and verification from layout, including HSPICE electrical simulation, can be carried out.

Symbolic layout and parameterizable cell generation are supported to cope with technology evolution. Using this environment, several designs have been completed. Automatic placement and routing tools and other layout synthesis tools are now under evaluation to be integrated in this environment. For instance, module generators for multipliers, adders, registers, and RAMs are under development.

Finally, in another direction, behavioral and temporal models (in VHDL and Verilog HDL) are being developed. Also, logic synthesis models and methodology are being considering to be included in the design environment. This will be coupled with a mapping tool that permits us to get high quality high density designs of digital GaAs circuits. The GaAs circuit compiler will permit us to capture the design behaviour in a known HDL (Verilog or VHDL) and convert its description to GaAs implementation. Main goals are area minimization, interconnect lenght and power dissipation (in SCFL technologies). In this way we have developed OLYMPO, a full set of tools oriented to cell synthesis under "Ring Notation Methodology". This tool set includes floorplanning, placement and routing of cells. On top of OLYMPO, we are building block cells compilers (for data-path, hardware accelerators and ROM). With this contribution, GaAs design will be at the same level as CMOS design.

Acknowledgements.

Authors want to thank José Guerra for his cooperation in the implementation of the technology files, and Amalia Alemany for her work in symbolic

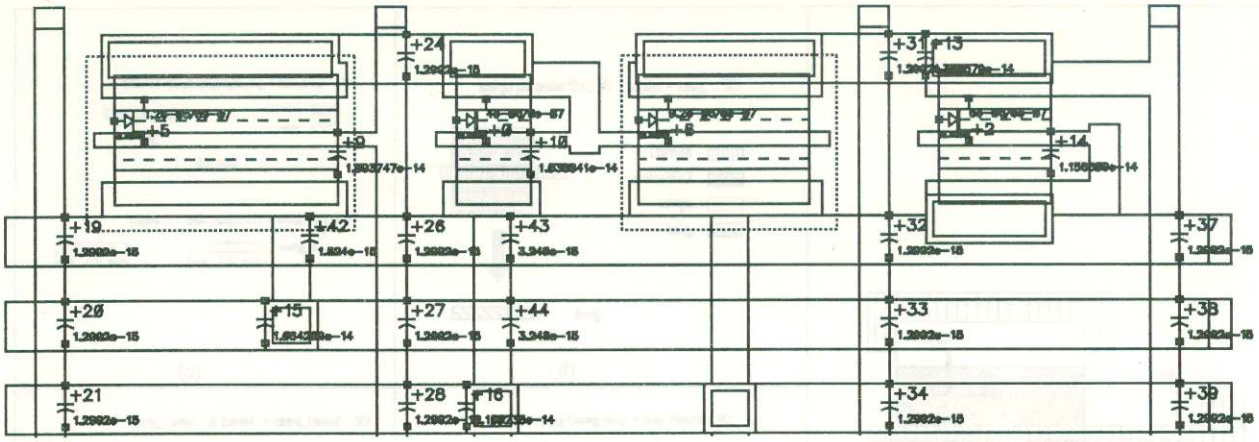

Fig. 3 Extraction of a basic cell (INV).

design. Also to V. Armas, and J. López for their useful comments and feedbacks as users of the tools.

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