THE HFETs IN CHARGE PREAMPLIFIERS FOR PARTICLEs PHYSICS APPLICATIONS

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Abstract

We analyse the performances of heterostructure field effect transistors (HFETs) for low-noise fast readout electronics for detectors of elementary particles. We discuss the advantages and the limits of these devices in comparison with silicon transistors. We also present the first integrated charge preamplifier fully based on HFETs and the experimental results obtained.

Introduction

A radiation detection system is schematically represented in Fig. 1. It is composed of a detector feeding a preamplifier followed by a filtering stage which increase the signal to noise ratio. The detector can be represented by a current source which delivers delta-like pulses $Q\delta(t)$, whose area Q is the charge generated by the ionising particle inside the detector. The detection system provides an output voltage pulse whose amplitude is proportional to Q [1].

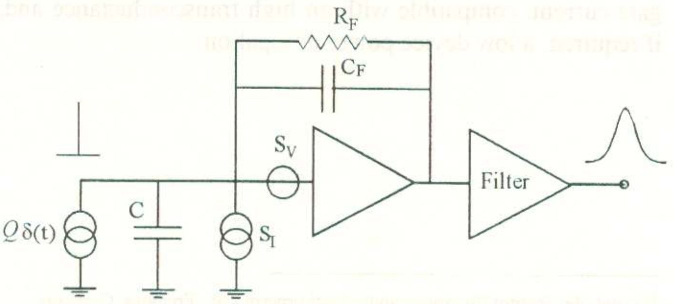

Figure 1. Schematics of the electronics for radiation detectors. The peak of the output pulse is proportional to the charge Q generated inside the detector by an ionising particle.

The preamplification stage is usually a charge amplifier, the noise of which depends mainly on the noise properties of its input transistor, that we will consider to be a FET. The noise at the preamplifier input can be characterised by the power noise spectra S_V and S_I of the series and parallel noise generators respectively:

$$S_V = a + \frac{A_F}{f} = \frac{2}{3}\frac{4KT}{g_m} + \frac{A_F}{f} \qquad [\mathrm{V^2/Hz}] \tag{1}$$

$$S_I = b = 2q\left(I_D + I_G\right) + \frac{4KT}{R_F} \qquad [\mathrm{A^2/Hz}]$$

in which K, T, q and f are the Boltzmann constant, the absolute temperature, the electron charge and the frequency, g_m is the input FET transconductance, A_F is a constant characterising the $1/f$ component of S_V, I_D is the detector leakage current and I_G is the input FET gate current, R_F is the feedback resistance. In the S_I expression the noise of the dielectrics is neglected [2]. The input FET contributes to the system noise with the whole series noise S_V and with the component of S_I due to I_G.

The resolution of a detection system is evaluated in Equivalent Noise Charge (ENC), which is the amount of signal charge (usually expressed in numbers of electrons) which injected at the preamplifier input generates an output signal whose amplitude is equal to the r.m.s. output noise voltage. The ENC of a system depends also on the filter, which is usually called 'pulse shaper' because it is customary to characterise it in the time domain rather than in the frequency one. The shaper can be synthesised with different weighting function (transfer function in the frequency domain) but the ENC can be expressed in the general form:

$$ENC = \sqrt{S_1 a C^2 \tau^{-1} + S_2 C^2 A_f + S_3 b \tau} \tag{2}$$

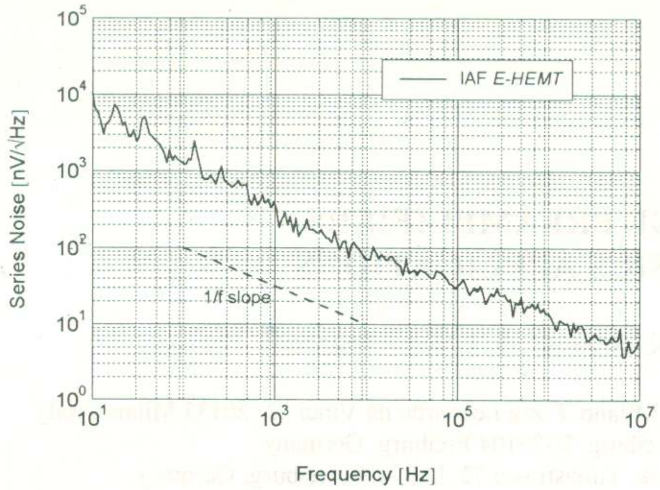

Figure 2 Input voltage noise spectral density of the IAF HEMT. The bias point is at 1mA drain current and 1V drain-source voltage. The transconductance is 12mS.

in which $C=C_D+C_F+C_G$ is the sum of the detector, feedback and input FET gate capacitances; S_1, S_2, S_3 are constants characterising the shaper and τ is the so called 'shaping time', which is related to the mid-band frequency of the shaper transfer function, or, in the time domain, it is related to the time-width of the shaper output pulse [1],[3].

It can be observed that a maximum charge resolution, that is a minimum ENC, can be obtained at an optimum shaping time τ_{opt}, at which the white series and the parallel noise contributions, that is the first and the third term in (2), are equal:

$$\tau_{opt} = C\sqrt{\frac{S_1 a}{S_3 b}} \propto \frac{C}{\sqrt{g_m\left(I_D + I_G + 4KT/R_F\right)}} \qquad (3)$$

$$ENC_{\min} = \sqrt{2C\sqrt{S_1 S_3 ab} + S_2 C^2 A_f}$$

The next future elementary particle physics experiments, based on high luminosity accelerators, will require to detect events by measuring the charge in a time interval in the range of tenths of nanoseconds [4]. In order to have a low $ENC_{\min}$ at a short shaping time, from (3) it can be observed that a small total capacitance C is required and a transistor with an high cut-off frequency $f_T=g_m/(2\pi C_G)$ is favourite. The HFETs, having f_T in the range of tens of GHz, are good candidate for these applications, in comparison with silicon JFET for which f_T is presently in the range of hundreds of MHz. Anyway also the series $1/f$ noise determine the $ENC_{\min}$ value, so that a comparative noise analysis is therefore essential to verify the possible advantage of HFET with respect to conventional silicon transistor.

Low-Frequency noise in HFET

In order to evaluate the performance of HFET in charge preamplifiers, it is necessary to know the parameter g_m, I_G, C_G and A_F which compare in (1) and (2). The power noise spectra S_V and S_I have to be considered in a bandwidth extended from dc to a frequency of the order of $10/2\pi\tau$. The upper limit of the bandwidth ranges from about 20MHz to 200MHz, for shaping time τ in between 100ns and 10 ns.

In figure 2 the measured noise spectra S_V of a HFET is shown. The HFET is an enhancement-type High Electron Mobility Transistor (HEMT) developed at IAF[1] [5]. The gate width is 50μm and the length 0.3μm. The transistor is biased at a drain-source voltage V_{DS}=1V with a drain current of 1mA, the gate current is 3nA and the transconductance is 12mS. In the considered bandwidth the noise of the HFET can be approximated to a $1/f$ component with $A_F=10^{-10}$ V^2, the expected white noise, measurable at higher frequencies, is 0.94 nV/Hz. A comparison with other device series noise spectra can be found in [6].

The gate capacitance of this HFET is about 80fF. Several semiconductor detectors for high energy physics have output capacitance in between 100fF and few picofarads. From (2) it is clear that detectors with low capacitance are preferable in order to have lower series white and $1/f$ noise contributions. Moreover it can be derived that, at a fixed detector capacitance C_D, a minimum contribution of the white series noise is achieved for $C_G=C_D$ [1]. Anyway increasing the HFET capacitance by increasing the gate width, causes also an increase of the drain current (at a fixed g_m/C_G), that is an increase of the dissipated power.

The gate current of the HFET ranges between 0.1 and 100nA depending strongly on the biasing point. For comparison silicon JFETs have gate current in the picoampere range, while bipolar transistors operating at the same transconductance of the HFET (10-100mS) would have a base current in the μA range. It is obvious that the best operating bias point of HFETs have to be chosen in order to make not dominant the noise contribution arising from its gate current, compatible with an high transconductance and, if required, a low device power dissipation.

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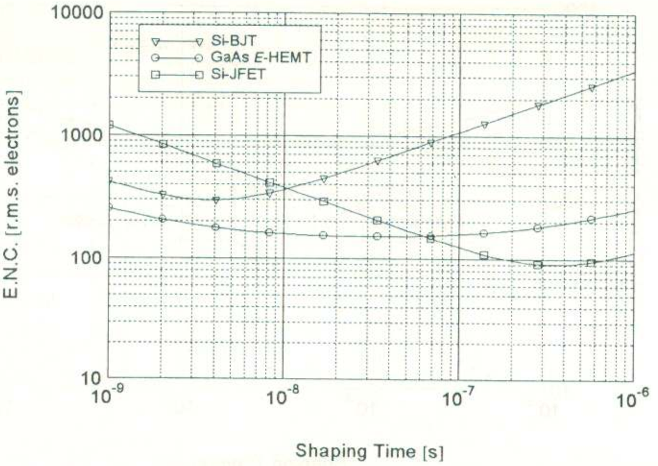

Figure 3 Equivalent Noise Charge as a function of the shaping time for the IAF HEMT, a silicon JFET and a microwave bipolar transistor. The detector capacitance is C_D=1pF and the its leakage current 1nA. The shaper is the commonly used RC-CR type.

HFET Performances in charge preamplifiers

Having all the set of noise parameters, the ENC of a detection system employing an HFET as input transistor, can be evaluated with (2). The result is shown in fig. 3, both for an HFET as for a silicon JFET and a bipolar transistor (BJT). The considered JFET is specifically designed for silicon radiation detectors [7], its gate width has been chosen in order to match the gate capacitance with the detector. The BJT parameters are relative to an advanced microwave device with f_T=2GHz at a collector current I_C=0.25mA with a current gain β=250. For the BJT the expression of S_V has been modified, taking into account the noise of the base spreading resistance [8]. As can be observed for shaping time shorter than 100ns the HFET input system shows the lowest noise. At 10ns, for example, the ENC^2 of the HFET is 4 times lower those one of the other devices. At short shaping time the JFET is noisier with respect to HFET because of the higher series white noise component. The bipolar transistor are noisier for the contribution of the base spreading resistance and the high base current. It can be observed that the flat part the ENC curve for the HFET is due to the dominating $1/f$ series noise, see (3), which makes wide the shaping time interval at minimum noise. The $1/f$ noise of HFET is under investigation by several researchers, a best understanding of its origin would result in better devices for applications [9],[10]. It has to be considered that the advantage of III-V HFET with respect to silicon FET is not only due to the higher mobility in the channel but also to their structure and to the technology used in their construction, which permit to realise submicron gate length (typical 0.2μm with respect to 1-5μm for the available JFETs).

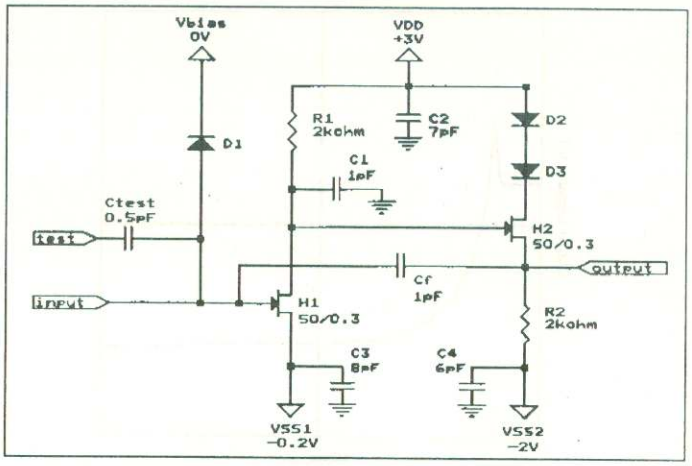

Figure 4 Schematics of the integrated charge preamplifier based on enhancement-type IAF-HEMTs.

Integrated HFET charge preamplifier

On the basis of these results we designed a first integrated charge preamplifier fully based on HFETs [11]. The schematics is shown in Fig.4. It is constituted by two stages in order to minimise the power dissipation, which is 9mW. The HFET are enhancement-type IAF-HEMTs [5]. The diode D1 and the capacitor C_{test}, integrated with the amplifier, simulates the detector. The HFETs work at 1mA drain current with 12mS transconductance. The open loop voltage gain is about 20.

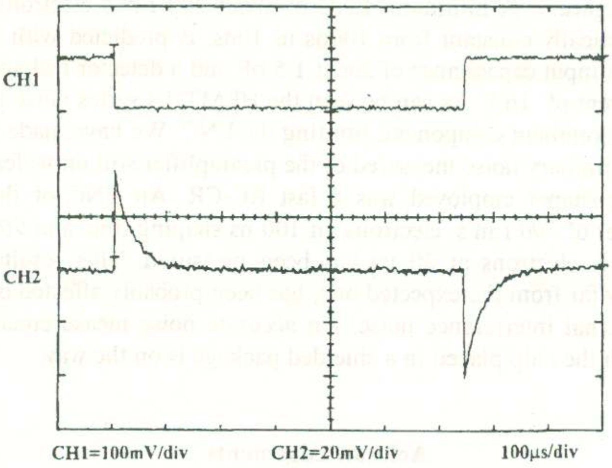

Figure 5 Time response of the integrated HFET charge preamplifier (lower curve) to a square wave.

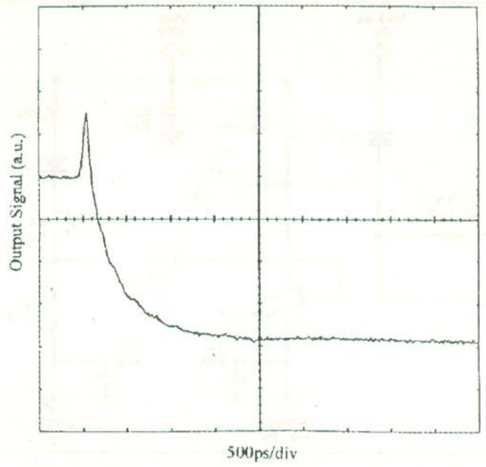

Figure 6 Response of the integrated HEMT charge preamplifier to a delta like current injection. The rise time is 0.7ns. The narrow positive peak is due to the direct feed-through of the input signal.

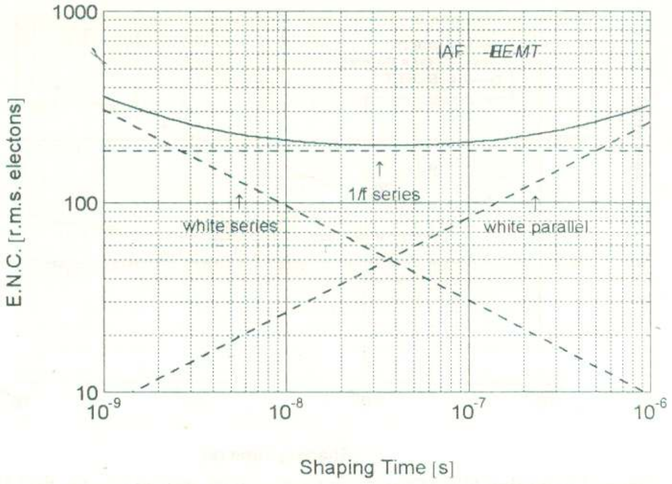

Figure 7 Expected Equivalent Noise Charge of the integrated HEMT preamplifier. The three noise component are plotted in dashed lines.

An innovative aspect of this preamplifier is constituted by the exclusion of the feedback resistor [12]. The gate of the input transistor is biased in slightly forward conditions by the leakage current of the detector. The discharge of the feedback capacitance C_f is achieved through the gate junction of H1. The difficulty of integrating an high value low excess noise feedback resistor is overcome without inserting a switching transistor in parallel to C_f. In figure 5 the response of the amplifier is shown. The rise time, see Fig.6, is 0.7ns when the output is loaded to 50Ω. The expected noise performances of this amplifier has been evaluated and shown in figure 7. A minimum ENC of about 200 r.m.s electrons, practically constant from 100ns to 10ns, is predicted with a total input capacitance of about 1.5 pF and a detector leakage current of 1nA. As can be seen the HEMT 1/f series noise is the dominant component, limiting the ENC. We have made a preliminary noise measured of the preamplifier still on wafer. The shaper employed was a fast RC-CR. An ENC of the order of *700* r.m.s. electrons at 100 ns shaping time and *900* r.m.s. electrons at 20 ns has been measured. This results, very far from the expected one, has been probably affected by external interference noise. An accurate noise measurement with the chip placed in a shielded package is on the way.

Acknowledgements

The authors wish to thank the Fraunhofer-Institut für Angewandte Festkörperphysik of Freiburg for the production of the preamplifier and for the hospitality offered to the authors during the design and the testing of the circuit. In particular we are grateful to M.Berroth, W.Bronner, V.Hurm, G.De Geronimo, M.Webel and C.Weber for their support and co-operation. This research has been partially supported by Italian INFN.

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