Enabling RFCMOS solutions for emerging advanced applications

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***Abstract* — The enablement of advanced RF applications with CMOS is discussed. This is accomplished through a broad menu of low-cost and high-performance modular technology features with accompanying scalable devices models which are accurate to frequencies well above application conditions.**

I. Introduction

Examples of successful implementation of RF circuits using digital CMOS with no or few added features abound in recent literature. Furthermore, applications at frequencies and bandwidths until recently the sole domain of SiGe HBTs or III-V semiconductors are being demonstrated in CMOS. Fig. 1 summarizes CMOS publications for recent conferences as noted. Significant RF and analog design activity is occurring in CMOS spanning 90nm through 0.35µm nodes. The node with greatest design activity is a function of circuit type; for example, Cellular is implemented in more mature technologies, high-speed serial in leading-edge nodes and WLAN implementations exist across all nodes. Clearly, RF CMOS design activity proceeds at a vigorous pace with higher performance applications focused in highly scaled technology nodes.

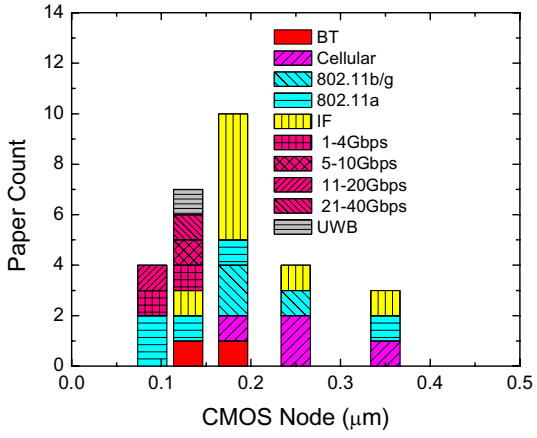

Fig. 1. Summary by node of CMOS applications published at the CICC and ISSCC in 2003 and RFIC and CICC in 2004.

These applications are feasible in CMOS because of the increasing performance of scaled digital CMOS. The most straightforward measure of transistor performance is the unity current-gain frequency or cutoff frequency, f_T. Recent publication of NFET f_T of 243GHz[1] and 209GHz[2] demonstrate the ability of the FET to have sufficient usable gain for applications at 24GHz and perhaps up to 77GHz. Fig. 2 shows recent data and a projected trend [3].

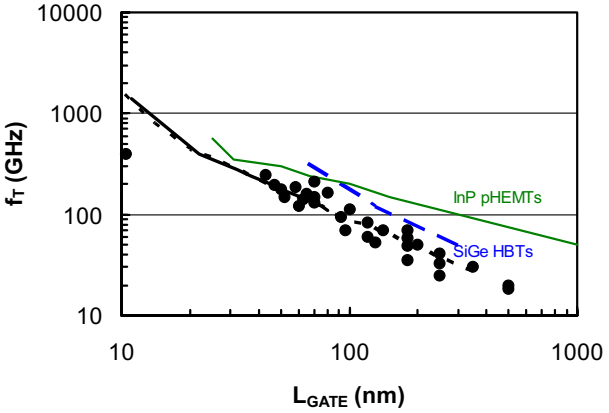

Fig. 2. Cutoff frequency of NFETs from recent publications [3]. Added lines show f_T from InP HEMTs and from SiGe HBTs where the gate length from the corresponding NFET in IBM's BiCMOS technologies is used as a technology reference.

Lower cost is the prime motivator for the use of CMOS over BiCMOS or III-V technologies. Considering f_T as a measure of performance, the SiGe BiCMOS HBT has comparable performance to the NFET at roughly twice the minimum feature size. For stand-alone RF functions, where area is dominated by passive devices and I/O pads, BiCMOS may be the lower-cost option despite the approximately 20% additional process complexity required to form the HBT. III-V transistor performance at substantially relaxed lithography dimensions is competitive with leading edge CMOS. So, again for purely RF devices, III-V implementations may be lower cost especially when utilizing existing designs and time-to-market is considered. However, when even small amounts of digital logic are to be integrated, CMOS has a clear advantage as circuit density and chip size scale with the square of the minimum lithographic dimension.

II. Challenges

Increased performance in scaled CMOS is accompanied by some device characteristics that

complicate conventional implementations of needed RF functions. Consider the scaling of FET parameters for the bulk-silicon CMOS technologies shown in Table I.

TABLE I
PARAMETERS OF THE DIGITAL NFET IN IBM CMOS

Node	nm	250	180	130	90	65
L_{GATE}	nm	180	130	92	63	43
t_{OX}(inv.)	nm	6.2	4.45	3.12	2.2	1.8
V_{DD}	V	2.5	1.8	1.5	1.2	1
V_T	V	0.44	0.43	0.34	0.36	0.24
peak g_m	µS/µm	335	500	720	1060	1400
g_{ds}*	µS/µm	22	40	65	100	230
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.1
f_T	GHz	35	53	94	140	210
M2 pitch	µm	0.8	0.56	0.4	0.28	0.2

*at peak g_m

Smaller geometries result in higher parasitic impedances and increase variation. Smaller film thicknesses and shorter gate lengths result in higher leakage currents and drain conductance. These are in part compensated by lower supply voltage but that increases sensitivity to variation by reducing voltage headroom. In order to overcome these challenges a number of enhancements to digital CMOS are needed. First is a set of modular high-performance devices that can be added if a particular application requires it. Second is a suite of sophisticated device models that capture high-frequency behavior, geometry scaling, process variation, and second-order effects. Last is the integration of these models with commercial design tools such schematic simulators and parasitic extraction.

In subsequent sections, we will discuss some of the challenges introduced by the characteristics of highly-scaled CMOS and of the performance requirements of emerging applications. In each example, will introduce model enhancements or technology features that help meet application specifications and increase the likelihood of first-time successful designs.

III. COST VS. PERFORMANCE

Significant design effort is now focused on combining diverse functions striving ultimately for system-on-chip (SoC) product applications. Blocks of digital circuitry will want to utilize the fast, dense FETs available in aggressively scaled CMOS. RF and analog blocks will tend to avoid that trend; the existence of proven designs in mature technologies, the significant chip area utilized by passive elements and some of the undesirable properties of scaled FETs all increase cost and must be considered in SoC decisions. To ease the cost burden of integrating RF and analog functions with digital logic, technology offerings should include support for optional devices that could be utilized only as needed for each given application.

Beyond digital FETs, the base CMOS process allows the formation of a suite of passive devices that only require the support of models and design tools. Resistors can be formed from the implanted N-well, the gate polysilicon or the source/drain active areas. Capacitors and varactors can be formed from the junctions and MOS gates of the FET. Inductors can be formed using the standard wiring. A MIM capacitor having very good performance, which we discuss below, can also be formed using the standard wiring. A crude bipolar transistor, formed by the p-type active area, is also created by the base CMOS process. All these devices become usable if they are supported by scalable parameterized layout cells (p-cells) and corresponding models. The goal of cost-conscious designs is to implement every function with just these base CMOS devices. However, if application specs require higher performance, a suite of optional high-performance devices should be available.

A. Additional transistors

One type of additional device, almost ubiquitously included in CMOS technologies and employed in almost every design is the IO FET. These are FETs with a thicker gate oxide, made to resemble FETs of previous nodes, and used to create IO interfaces that support higher voltages. Fig. 3 shows the 2.5V IO FET option from IBM's 90nm technology compared with the digital FET from the 0.25µm node. A SoC design hoping to migrate RF function from an earlier node and combine it with leading-edge digital could, in principle, save time to market by using the IO FETs that resemble the FETs used in the earlier node. Even new designs could find the IO FETs more suitable to their application when higher voltage tolerance or lower leakage is required.

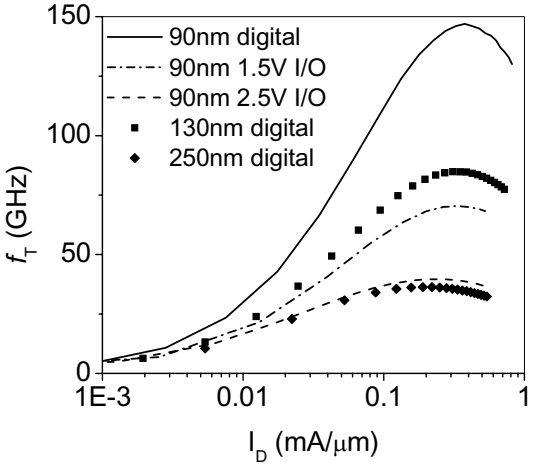

Fig. 3. f_T vs. I_D for selected FETs from IBM's 0.25µm, 130nm and 90nm CMOS nodes illustrating the similarity of IO FETs from newer nodes to digital FETs of earlier nodes. The difference between the 130nm FET and the 90nm 1.5V FET in this example results from a sharing of implant. The properties of the 1.5V FET could be tuned with independent implants.

As transistor dimensions shrink, off-current, leakage currents and output conductance (g_{ds}) all increase to the point where they noticeably influence performance. For short channel devices, g_{ds} is related to drain induced barrier lowering (DIBL) which results from electric field at the source side of the FET under conditions of high drain bias. g_{ds} will increase as V_{DS}/L_{GATE} increases. This ratio is growing because V_{DD} is not scaling as fast as gate

length. Furthermore, beyond 90nm, gate leakage restricts the scaling of the oxide so that L_{GATE} and t_{OX} cannot be reduced proportionally. Since g_m scales with L_{GATE}/t_{OX} , this results in a precipitous drop in the self-gain, g_m/g_{ds}, for the digital FET at the 65nm node as shown in Table I. This presents a problem, for example, for Low Noise Amplifier (LNA) designers hoping to realize significant gain.

Technology elements such as high-K gate dielectric, metal gates and double gate structures will be needed to address this issue[4]. However, an asymmetrically-doped FET, with the halo implants removed from the drain, allows lower g_{ds} even down to short channel lengths. We have employed an approach proposed by Hook, et al. [5] to block the halo implant from the drain side of the FET thereby reducing g_{ds}. Counter-intuitively, long-channel digital FETs have high g_{ds}. This results from the halo implant making the V_T of the channel region near the drain a little higher, creating a barrier to current flow. As the V_{DS} is raised that barrier is lowered allowing more current. Since the asymmetric FET has no drain-side halo, this effect does not occur. Fig. 4 illustrates the benefit of this asymmetric FET design showing that self-gain is higher even at relatively small gate lengths. We observe that both devices show similar values for g_{ds} and DIBL at short channels suggesting the source-side halo controls these short-channel phenomena. Biased at equal current, both devices exhibit the same g_m for a given length. Therefore, we see that g_{ds} decreases by a factor of five at 3X-minimum gate length. Also, because the halo implant is blocked from the drain, we observe lower gate overlap capacitance. However, the photoresist that blocks the halo implants will necessitate larger spacing between gates in multi-fingered devices thereby increasing the drain to body capacitance.

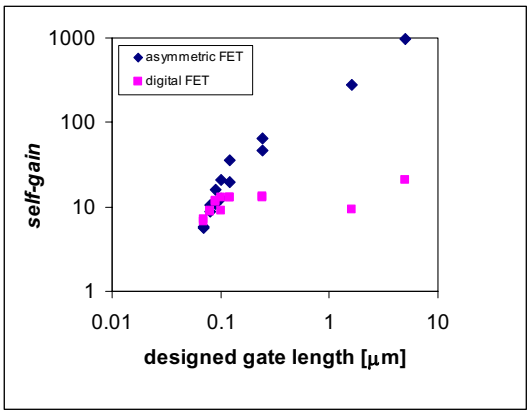

Fig. 4. Shows g_m/g_{ds} comparing the digital FET to the asymmetric FET in 90nm CMOS. Here g_m and g_{ds} are both measured at 10X the drain current corresponding to threshold.

B. Resistors

Two of the most widely used resistors in circuit designs using CMOS technology are the silicide-blocked N-type diffusion resistor and P-type polysilicon resistor. The former is widely used in IO circuits while the latter is employed in most analog circuits where matching and a low temperature coefficient are paramount. The properties of these resistors (sheet resistance, tolerance, temperature coefficient, etc.) are determined by the design of the FET. High-performance resistors with lower overall tolerance can result in low power designs and improved circuit performance. These devices generally require and additional mask level for improved process control. Another high-performance resistor can be created by adding a thin metal film embedded in the wiring levels. These resistors have good tolerance and low parasitic capacitance because they are further above the silicon substrate. [6]

C. Varactors

Accumulation-mode MOS varactors can be provided in each oxide thickness and have high capacitance density, a large tuning range and high Q. Reverse-biased junctions can be used as varactors where fine tuning of capacitance is required. However, low-phase-noise, low-power VCOs demand varactors with both high linearity and wide tuning range. To enable such critical circuits, we have developed an optional hyper-abrupt (HA) junction varactor with a nearly linear *C-V* tuning ratio of 3.1 and a Q exceeding 100 at 2 GHz. To illustrate the different tuning behavior, Fig. 5 compares the normalized *C-V* characteristics of the HA junction varactor and MOS accumulation varactors at the 130nm node.

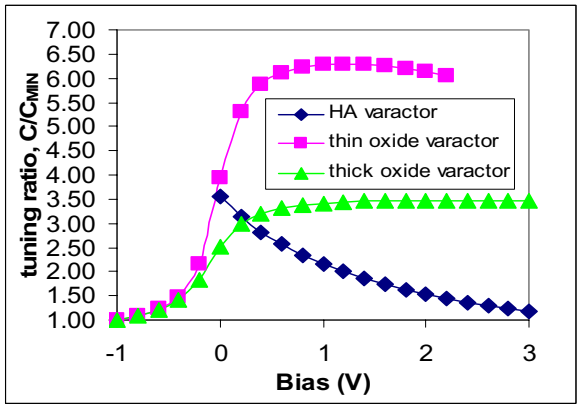

Fig. 5. Normalized C-V curves for MOS and HA varactors in IBM's 130nm CMOS.

D. Inductors

Thick added metal layers can be employed to build inductors with very high quality factors [6]. However, in this section we will highlight inductors made with standard wiring levels in our 90nm node. In technologies with copper wiring, low resistance vias make symmetric inductors feasible. We provide layout cells and models for symmetric spirals optimized for differential operation and suitable for single-ended or floating configurations. To maintain high Q, the spirals consist of parallel combinations of two or more thick Cu metal layers connected together through continuous Cu vias. An additional 1.2µm final aluminum layer is also available for parallel combination with the Cu levels. By use of a parallel combination of two 2X-pitch (0.5µm thick) wires and two 4X-pitch (0.81µm thick) wires and the final Al layer, a very low net sheet resistance of 0.006 Ω/ can be achieved. Many digital applications employ these thick wiring levels for power and clock distribution. However, for applications requiring high-Q inductors that do not utilize the full wiring stack, an optional single 3µm thick Cu wire achieves the same performance. A

Faraday shield ground plane is provided as an option to enhance Q even further while more effectively isolating the spiral from noise coupling to/from the substrate. Table II shows Q for 1.0nH spirals in the various combinations of metal stacking and groundplane choice. Fig. 6 shows representative Q vs. frequency curves.

TABLE II
INDUCTOR PARAMETERS

Spiral Metal	Q@5GHz, L=1.0nH
2-2X, no M1 ground	9
2-2X, with M1 ground	10
2-2X+Al, no M1 ground	12
2-2X+Al, with M1 ground	14
2-2X+2-4X, no M1 ground	14
2-2X+2-4X, with M1 ground	17
2-2X+2-4X+Al, no M1 ground	15
2-2X+2-4X+Al, with M1 ground	19

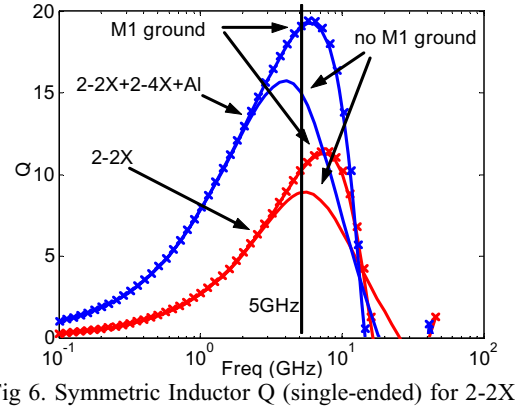

Fig 6. Symmetric Inductor Q (single-ended) for 2-2X and 2-2X, 2-4X+Al options (with and without M1 groundplane).

E. VNCAPs and the MIM capacitors

The vertical natural capacitor VNCAP [7] consists of via-connected stacks of inter-digitated metal combs including all thin wires and optionally including the 2X-pitch wires. Device layouts have been optimized for reliability and performance and implemented in scalable p-cells. Capacitors constructed in our 90nm technology with 4 thin wires and 2 2X-pitch wires in oxide dielectric have a capacitance density of 1.73fF/μm^2. This same structure fabricated in low-K dielectric gives 1.58fF/μm^2. Fig. 7 shows the high-frequency behavior a 90nm, low-K VNCAP with Q of 125 for a 1.6pF capacitor at 4GHz. Frequency characteristics of devices in oxide and low-K dielectric are very similar indicating good integrity of the low-K films.

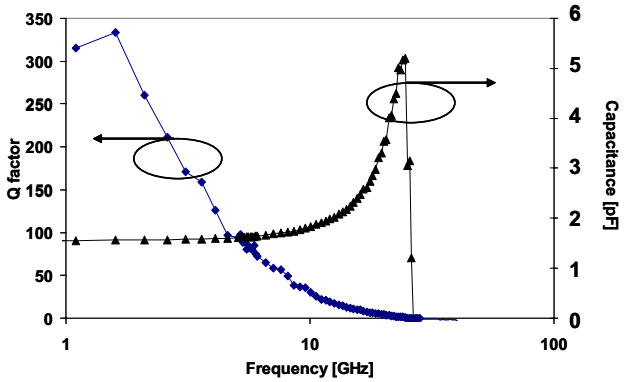

Fig. 7. VNCAP C, Q vs. frequency measured on our 90nm CMOS with low-K dielectric. Capacitor area is 50 X 20 μm^2.

Parallel-plate MIM capacitors require two additional masks. However, they have tighter tolerance limits and can achieve higher capacitance density either by stacking plates or introducing high-K material and they can be optimized for loss giving high-Q. For example, in our 90nm CMOS an optional, parallel-plate high-Q MIM with low plate resistance features a capacitance density of 2fF/μm^2 and Q in excess of 200 at 5GHz for a 20X20μm^2 plate. This device enables the pairing of large capacitors with small inductors in circuits such as VCO tanks, for an overall high-Q as well as an area savings.

IV. MODELS

A. High-frequency models

The shrinking geometries, shown in Table I, increase the significance of parasitic resistances of the narrow lines and parasitic capacitances of the small spacing between the lines. Accurate high-frequency models need to be extracted while paying careful attention to these parasitics. They will allow the designer to optimize physical design for performance as illustrated by this simple example.

One indicator of transistor bandwidth is the unity gain frequency of the short-circuit current gain, the cutoff frequency, given by

$$f_T = \frac{g_m}{2\pi C_{in}} \quad . \tag{1}$$

f_T can be shown to be proportional to the inverse of L_{GATE} in the velocity saturation limit and this is consistent with the data in Table I. A more comprehensive indicator of useable bandwidth is the unity gain point (f_{MAX}) of Mason's Unilateral gain (U). Simplified expressions, for example,

$$f_{MAX} = \frac{f_T/2}{\sqrt{g_{ds}(R_{in}) + 2\pi f_T R_{in} C_{GD}}}, \tag{2}$$

have been examined by various authors (for example [8]) as studies of technology scaling. Morifuji's [9] analysis showing the effects of technology scaling and parasitic losses is repeated in Fig. 8. We observe that f_{MAX} has a peak value at some optimum width above which it is limited by physical gate resistance and below which it is limited by parasitic losses in the FET structure. For a given layout, the optimum device width shrinks as the unit gate resistance increases with smaller and smaller gate lengths. Care must be taken in FET layout to minimize parasitic gate capacitance which will limit f_T and gate resistance which will limit f_{MAX} and noise figure.

While the above analysis indicated that f_{MAX} increases with technology scaling, in practice this is quite difficult to achieve despite the increase in f_T [10]. One reason is the increasing impact of the non-scaling parasitics in the device layout. High-frequency behavior is greatly influenced by the impedance of the wiring leading up to the device[11] and the substrate below. In

order to reduce the infinite set of layout variations that contribute these parasitic impedances, we employ p-cells which control layout variations to a few scalable parameters and binary options. The high-frequency model is built to accurately reflect the allowed variations of the p-cell. Fig. 9a shows the FET p-cell from IBM's 90nm CMOS. The scalable parameters are gate length, device width and number of fingers. The binary options are substrate contact ring, one or two sided gate contact and one or two rows of diffusion contacts. Other options, for example the number and placement of contacts and the spacing of the substrate contact, are controlled to assure a good model fit over the allowed layout variations.

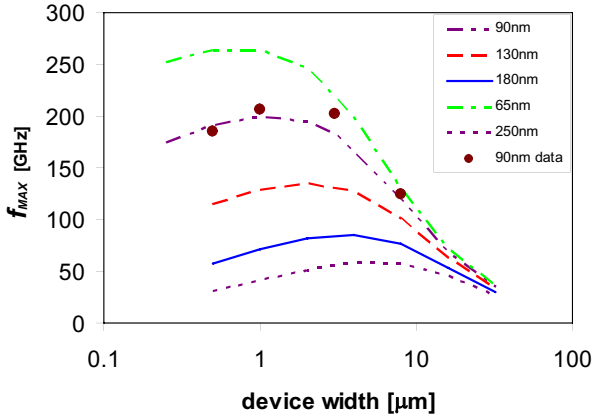

Fig. 8. Calculated f_{MAX} (according to method in [8]) for different technology nodes as a function of FET width. Data from IBM's 90nm node qualitatively show the predicted dependence. However, this simple model under-predicts measured f_{MAX}.

The high-frequency model, which consists of the low-frequency FET model surrounded by a subcircuit network representing parasitics is shown in Fig. 9b. The model and p-cell have corresponding scaling variables and options. It is important that the schematic, layout and parasitic extraction tools all recognize the p-cell, its options and especially its boundaries in order to avoid double-counting of these parasitics by the model and extraction tools.

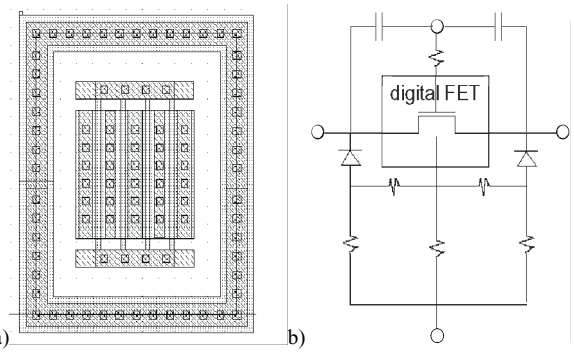

Fig. 9 a) shows an RF FET p-cell illustrating the optional substrate ring. b) shows the high frequency model as a sub-circuit surrounding the low-frequency FET model.

B. Modeling process variation

The shrinking geometries of Table I also result in increased variation in device performance. As geometries scale down, the impact of dimensional variation to device properties becomes more pronounced and device areas decrease to the point where statistical fluctuations in the count of dopant atoms becomes evident in electrical characteristics. We introduce a sophisticated model methodology for capturing process variation in scaled CMOS technologies.

One can visualize process variation as a multi-dimensional space. Each point in the space represents a particular combination of things that can vary in the process; NFET channel length, PFET mobility, oxide thickness, etc. The Monte Carlo model represents this space by independently varying each of the most important process variables. Fig. 10 shows three dimensions of this space, NFET channel length, NFET mobility and NFET base V_T. The Monte Carlo model is represented as a sphere in this picture because any combination of these three parameters (within the process tolerances) can occur in a Monte Carlo simulation. The complete Monte Carlo model has more dimensions but more than three is difficult to draw. The user-defined corner model is a projection of the Monte Carlo model onto a smaller number of dimensions or corner parameters. In the illustration NFET channel length is retained as an independent corner parameter (cor_pc) but mobility and V_T are collapsed to a single dimension labeled "cor_nmos". The user-specified corner model is represented by a plane in this picture. Only points on this plane can be specified using the two corner parameters. The foreshortened circle is the portion of this plane containing reasonable process values. Fixed corner models appear as single points in this picture.

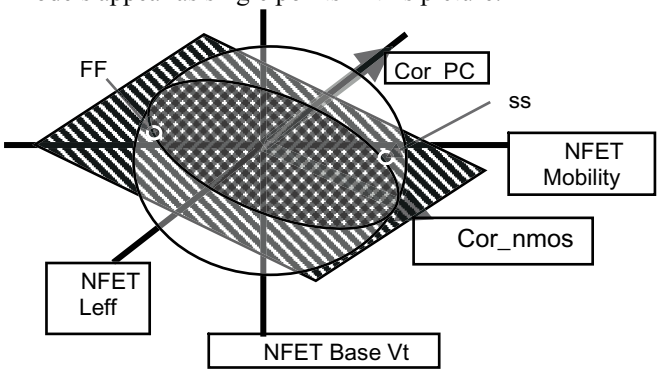

Fig. 10. The Monte Carlo model represented as a sphere provides the most complete coverage of the process space. The user specified corner models covers only the the 2-D plane and the fixed corner models each covers only a single point.

For static CMOS logic, fixed corners which represent extremes of gate delay (FF and SS) and extremes of N to P mismatch (FS and SF) may be provide all the information needed about process variation. However, these points in the process space probably do not represent other extremes of interest such as op amp gain or bandwidth. We recommend that designers use Monte Carlo simulation to understand how critical circuit characteristics vary across the process space and then use corner parameters to define corners that represent interesting extremes of circuit behavior.

Not all of the points within the space defined by the process controls limits are physically realizable. This is

because some parameters are correlated. For example, poly gates for all FET types are printed together and so L_{GATE} for all FET types are at least partially correlated. If multiple FET types are used in a chip design the correlations between FET types must be modeled. We have measured the variation of correlation of $I_{D,sat}$ and $V_{T,sat}$ for various FET types and constructed a Monte Carlo model in which correlated L_{GATE} and base V_T distributions reproduce the measured variance and covariance. Using corner parameters specific to each FET type, the user can specify corners which model extremes of circuit behavior.

Similar behavior is seen in the RC delay of different wiring layers, i.e. all wires on a given wiring layer will be slow or fast by a similar amount on a given chip. But wires on different layers vary independently of one another. So, for our Monte Carlo model, we provide independent distributions for width of wires on each wiring level and the thickness of each interlay dielectric. For corner analysis we provide independent corner parameters for each wiring level.

Within a single chip there is also variation among FETs of identical length and width. We model three sources of across chip FET variation. Variation of FET electrical parameters due to random density and placement of dopants under the FET channel which we will call V_T matching. Variation of the length of the FET channel due to variation in poly gate etched dimensions which we call across chip length variation (ACLV). Variation of width of the FET channel which we call across chip width variation (ACWV).

For ACLV we model variation due to three layout variables. Distance between the devices in question, orientation of the gates (vertical or horizontal) and spacing to the next poly line (poly pitch). ACLV due to line edge roughness and other uncategorized effects is included in the V_T matching term This and the other four ACLV effects are represented as random distributions in the Monte Carlo model.

It is important to model these various effects independently because the designer can choose to improve tracking between all FETs in a design or just particular sensitive FETs by layout style, e.g. by requiring FETs to have the same orientation. We provide a combination of local and global parameters which allow the designer to quantify the improvement due to such restrictions and make appropriate design trade-offs.

Fig. 11 illustrates the effect of across chip variation on ring delay. Each group of symbols represents the delay of one particular ring oscillator plotted against the average of the delay of the four rings on that chip. The vertical separation between the groups of symbols is due to the distance part of ACLV and ACWV which is correlated between FETs within a ring and uncorrelated between FETs in different rings. The vertical spread within one group is due to the other sources of ACLV, ACWV and the dopant mismatch are all uncorrelated with a ring. Overall upward trend of each group of data is due to the many sources of chip mean variation.

C. Variation of Flicker noise

Although a low-frequency phenomenon, 1/*f* or flicker noise has direct impact on the close-in phase noise of a VCO as well as on baseband noise in circuits such as zero-IF (ZIF) receivers. Fundamentally, 1/*f* noise appears in the drain current and arises from fluctuation in the number of channel charge carriers as these carriers are captured and released at random by traps located near the oxide/silicon interface. The magnitude of this noise is determined by the density of these traps, by the density of channel charge (and thus by g_m and C_{OX}) and by the overall gate area, as described by (3):

$$S_{Id} = \left(\frac{1}{f}\right) \Big/ WL_{GATE}C_{OX}^2 \cdot \qquad (3)$$

Alternately, the same noise can be input-referred and described as a voltage noise source on the gate, S_{Vg}, by dividing by g_m^2. This format is particularly useful for comparing noise with the input signal of a baseband amplifier.

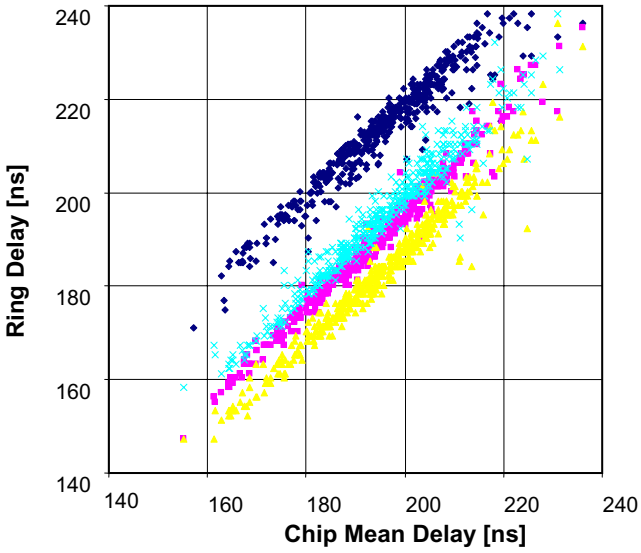

Fig. 11. Ring by ring delay vs. chip mean ring delay. Four identical rings at different locations on a chip show both correlated and uncorrelated variation.

As t_{OX} decreases with technology generation, both g_m and C_{OX} increase proportionally. Thus, devices of fixed width, W and length, L_{GATE} should experience no change in 1/*f* noise, assuming that trap density can be kept constant. If L_{GATE} is allowed to scale to minimum dimensions, however, 1/*f* noise will indeed increase with generation even without a change in trap density, due to both the decrease in L_{GATE} as well as the consequent increase in g_m.

As transistor area is reduced, RTS (random telegraph signals) of individual traps dominate the low-frequency spectrum as can be seen from the Lorentzian signature of RTS in Fig. 12. This is a significant modeling challenge, since an analytic model can no longer capture the noise spectra due to the site-to-site variations in effective trap density. A statistical model can enable designers to run Corner and Monte Carlo noise simulations. To implement a statistical noise model, nominal values for three BSIM

noise parameters NOIA, NOIB, and NOIC are extracted from large area, multi-finger devices. In addition to the mean value, a statistical distribution also gets assigned to each parameter. The spread of this distribution is determined from measurements taken from a large sample of single-finger and multi-finger devices. Fig. 13 shows spectra for several identical single-finger devices along with the modeled spectra for nominal and 3-sigma corners. Such a model enables accurate statistical phase noise simulations for VCOs and aides in first pass design success of RFICs.

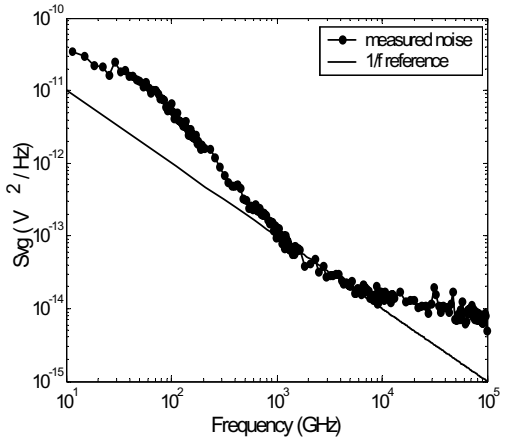

Fig.12. Low-frequency noise showing the Lorentzian signature of discrete trap RTS (nFET, w=10um, l=0.08µm).

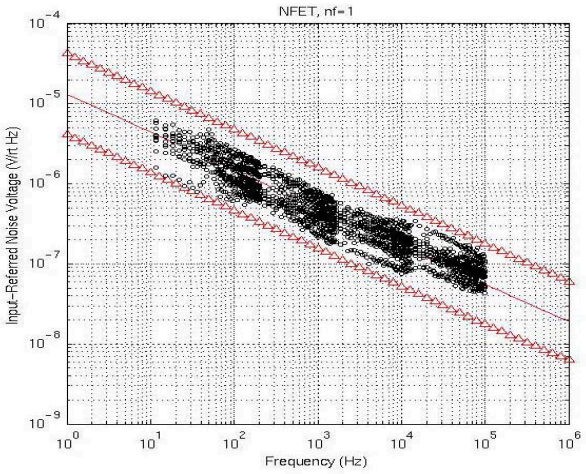

Fig.13. Low-frequency noise spectra of multiple identical devices with corresponding model and 3-sigma corner values. (nFET, w=10um, l=0.18µm).

VI. Conclusion

The lower cost of CMOS is motivating serious design effort across the spectrum of technology nodes. Essential elements of a RFCMOS technology offering are a broad menu of FETs and passive devices each supported by scalable, statistical models that correlate to scalable p-cell structures which are, in turn, coordinated with schematic, layout, and parasitic extraction tools. We have presented examples where model sophistication is growing in response to issues affecting the efforts of and being raised by RF and analog designers. By working closely with technology providers, designers can help focus the developing capability of CMOS technology, models and design tools to meet the challenges of emerging RF applications.

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