Specific methodology for the design of new monolithic millimeter wave integrated circuits. Combination of several simulation and modeling tools.

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Abstract :
The design of new millimeter wave monolithic integrated circuits needs the availability of accurate model tools such as physical simulations and experimental parameters extraction methods. Accurate electrical models have been built even in the difficult case of submicrometer dual gate pseudomorphic HEMTs. Their validity has been clearly demonstrated by the design of 60 GHz mixers.

Introduction

The design of monolithic integrated circuits needs the availability of accurate electrical models, both for active devices and passive components, and the use of appropriate softwares. Usually such models are based on a large data base; the corresponding data are extracted from experiments performed on a great number of test elements with large variations of technological parameters and realized with the same technology than the final integrated circuits. But this approach cannot be used for the design of future or very prospective products for which the technology is not fully stabilized and all the test elements are not available. In this case, another approach based on the combination of several simulation and modeling tools must be used.

The purpose of this paper is to give an example of such an approach that we used for the design of a 60 GHz mixer based on a dual gate pseudomorphic HEMT technology in the context of the European Project CLASSIC (Components for large signal sixty GHz GaAs Integrated Circuits). The corresponding work has been done in collaboration with the Companies and Institutes of the consortium, mainly with THOMSON TCS, that has fabricated the devices and the integrated circuits and IRCOM, that has performed a lot of measurements and modeling works on single gate devices.

At the beginning of the study no accurate electrical model of dual gate pseudomorphic HEMT was available. Moreover, some uncertainties were remaining concerning the topology of the device equivalent circuit and these of the electrical model. Finally, only 0.25 µm gate PHEMTs were available in foundry and we did not know what should be gate lengths of the dual gate device, for satisfying the requirements at 60 GHz. For answering these questions, we have combined the results of physical model and of a new experimental parameter extraction method and then built a new electrical model. Finally, this electrical model has been used for the design of several 60 GHz mixers, using dual gate pseudomorphic HEMT technology. These different steps will be described in this paper.

Physical simulation tools :

At this level, two physical simulation tools have been used :

- a two dimensional hydrodynamic energy model (1)
- a quasi two dimensional model derived from HELENA software (2).

The two dimensional hydrodynamic energy models (1,3,4,5) take into account the main physical phenomena that occur in submicrometer gate PHEMTs : velocity overshoots, quantum effects, impact ionization.... They are based on the solution of a lot of equations derived from Botltzmann transport equation : particle, momentum and energy conservation equations which are associated with Poisson's equation. These equations are solved numerically using a finite difference method with a non uniformed mesh and variable time steps. By using this kind of model, it is possible to obtain a good understanding of physical phenomena that occur in the device by means of appropriate representations : equiconcentration, equienergy, and equipotential contours or current flows for instance. Moreover, it is possible to extract the d.c. and a.c. characteristics, and then to evaluate the expected performance. It is also possible to study the influence of technological parameters (recess configuration) on the main device limitations, such for instance breakdown voltage.

Before, this 2D model was devoted to the simulation of single gate devices (4). It has been modified in order to be able to treat dual gate HEMT. Mainly, two gates were introduced : the intergate distance and gate length can be easily changed. Several boundary conditions can be introduced in the intergate space allowing to consider various configurations of this region, with respect to the recessed zone : individual recess for each gate, floating electrode... As an example, fig 1 gives a representation of physical device behaviour by showing equiconcentration, equipotential and equienergy contours, for a typical dc bias used, in mixer applications $V_{ds} = 3V$, $V_{g1s} = 0V = V_{g2s}$. In this case, the first equivalent transistor operates under linear regime and the second one is saturated : the equivalent drain source voltage is close to 0.5 V for the first transistor. This model has been used in order

to evaluate in what conditions such device can be equivalent to two single gate HEMTs under cascode configuration, by considering the spatial variations of channel potential (fig.2).

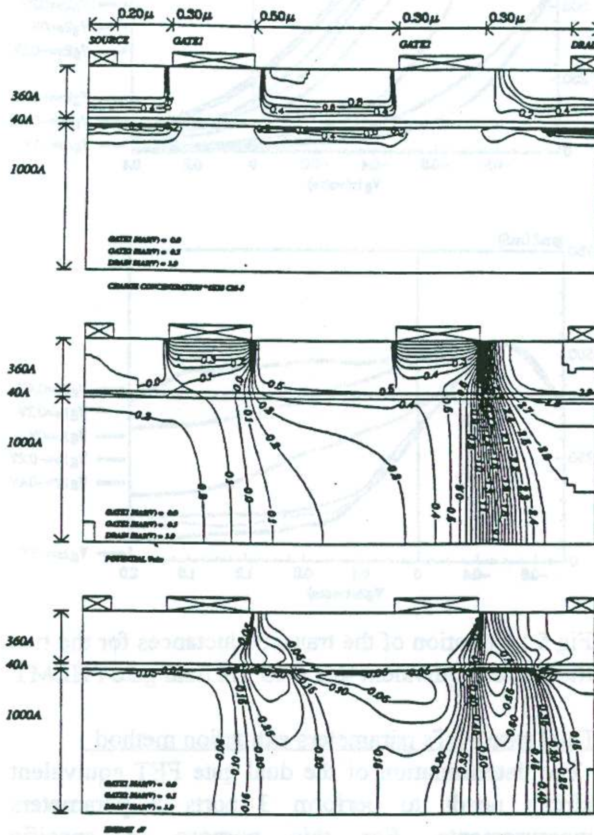

Fig 1 : Equiconcentration, Equipotential and Equienergy contours in a 0.3 µm dual gate HEMT.

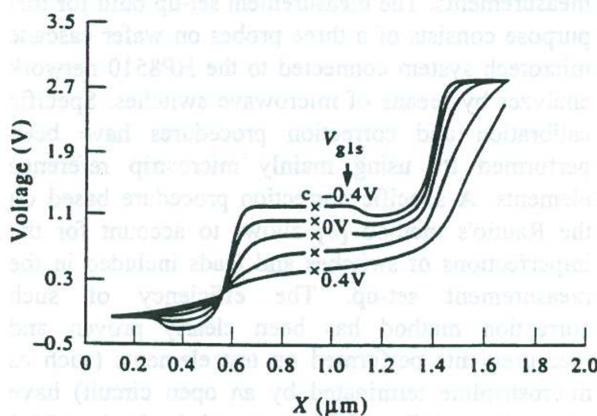

Fig 2 : Spatial evolutions of the channel potential in a dual gate HEMT for different values of V_{g1s} (l_g = 0.3 µm, V_{ds} = 3 V, V_{g2s} = 1V).

However, these 2D hydrodynamic energy models need long computational times (for instance 20 to 30 mn for one d.c. bias value) and powerful computers. In order to save computation time and to allow device optimization, several simplified models have been conceived based on one dimensional solution of semiconductor equations (6,7) . Such a model is the base of the HELENA software [2], that is now commercially available and allow to simulate the main kinds of available FETs.

The main assumption of these quasi 2D models is that the equipotential lines in the equivalent channel are perpendicular to the source to drain axis, then the device can be divided into slices. In each slice, a charge control law relates the charge carrier to the local potential difference between gate and channel. Along the other axis, the electron transport is described by means of particle, momentum and energy relaxation equations that can be combined on the form of a quadratic equation which is solved for each slice. Small signal and noise properties are extracted using the concept of non uniform active noises line (2), by affecting to each slice a dynamic equivalent circuit including noise sources and summing them from source to drain. Then, such a model is able to determine d.c. characteristics, small signal characteristics and expected performance including noise figure. Ionization effects have been recently introduced in order to predict breakdown voltage (5). In the context of this work, such a model has been modified in order to be able to treat dual gate pseudomorphic HEMT's.

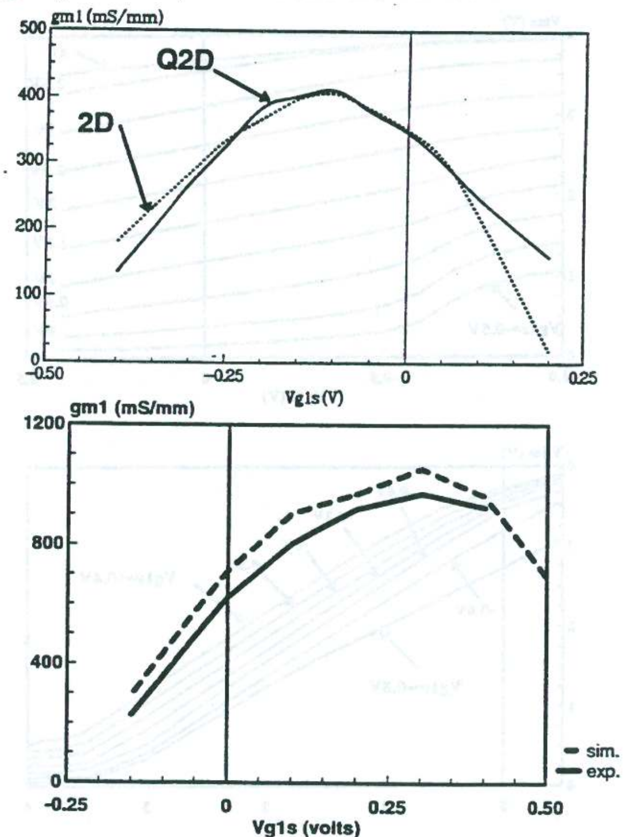

Fig 3 : Comparison of transconductance variations deduced from 2D and quasi 2D models (HELENA software) for a 0.3 µm gate pseudomorphic HEMT.

The quasi 2D model has been validated by means of systematic comparison with predictions deduced from the 2D model. A typical example is given in fig 3, that shows a very satisfying agreement. It has been systematically used for studying the influence of the technological parameters (gate length, doping profile, recess configuration) on the performance. From the evolutions of current gain cut-off frequencies, we deduce that gate lengths must be smaller than 0.15 µm in order to satisfy the requirements for a frequency of operation close to 60 GHz. For the electrical modeling of the device under cascode configuration, it is important to determine the variations of the potential at the middle of the intergate distance as functions of d.c. bias conditions (V_{g1s}, V_{g2s}, V_{ds}) : fig 4 gives an example of such evolutions.

For the same purpose, we need the dependence of transconductances, input and feedback capacitances on d.c. bias conditions : at it is shown in fig5, the transconductances may be high or low according to the operating regime (linear or saturated) of each equivalent transistor.

Such results have constituted the basis of our electrical modeling effort, before that 0.15 µm dual gate PHEMTs were available. But for validating this theoretical approach and constituting an other basis, we have developed a specific parameter extraction suitable for dual gate FETs.

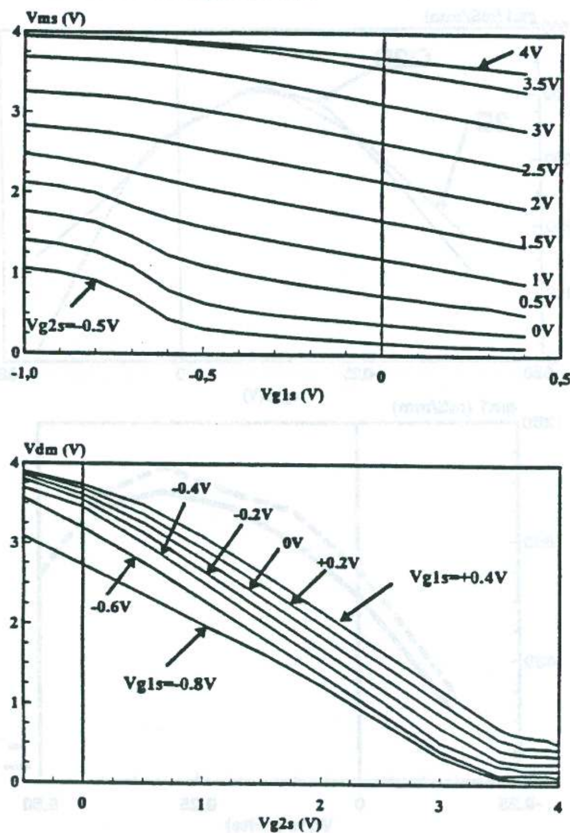

Fig 4 : Variations of the pseudopotentials V_{ms} and V_{dm} versus gate biases V_{g1s} and V_{g2s} in a dual gate HEMT (quasi 2D model).

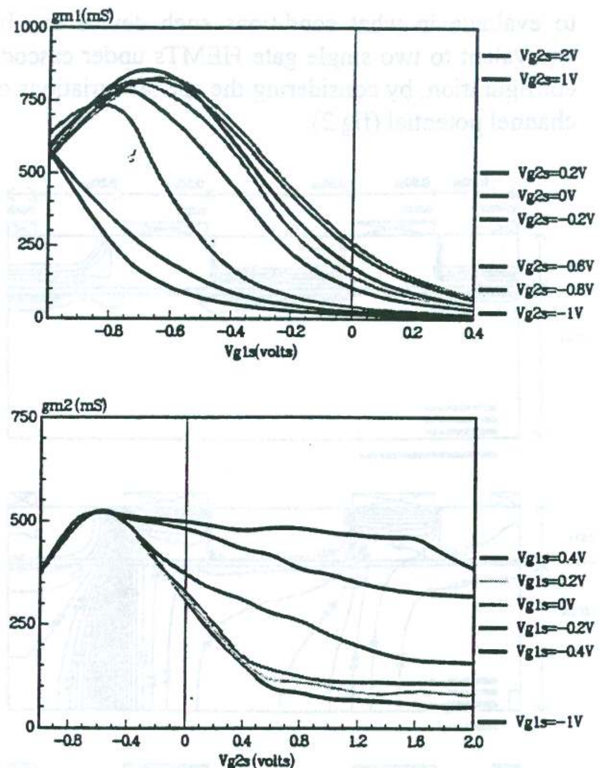

Fig 5 : Variation of the transconductances for the two transistors equivalent to a 0.15 µm dual gate PHEMT

Dual gate FETs parameters extraction method :

The determination of the dual gate FET equivalent circuit needs to perform 3 ports S parameters measurements. For this purpose, a specific measurement set-up has been developed, by using a two port HP 8510 network analyzer. The nine three port S parameters of the dual gate can be extracted, with the same redundancy for the three two ports measurements. The measurement set-up built for that purpose consists of a three probes on wafer cascade microtech system connected to the HP8510 network analyzer by means of microwave switches. Specific calibration and correction procedures have been performed by using mainly microstrip reference elements. A specific correction procedure based on the Rautio's method [8] allows to account for the imperfections of switches and loads included in the measurement set-up. The efficiency of such correction method has been clearly proven and measurements performed on test elements (such as microstripline terminated by an open circuit) have shown the validity of this approach in the 1 to 26.5 GHz frequency range.

The basic equivalent circuit of a dual gate FET under cascode configuration (fig 6) including parasitic access network comprises 26 elements. Then, it is not possible to envisage conventional extraction procedure based on optimisation method, so a specific one [9, 10] has been developed. It comprises a two steps procedure :

- the extraction of the parasitic access elements, the two equivalent devices being biased at $V_{ds} = 0$

- the extraction of the intrinsic elements.

Additional d.c. measurements provide subsidiary information to complete the set of equations.

Note that this procedure is derived from a direct extraction method developed for single gate devices by Dambrine and Cappy [11].

The access network includes two kinds of extrinsic elements :

- for extracting series elements such as self inductances and resistances, each gate is largely forward biased (always with $V_{ds} = 0$). The S matrix is converted in a 3 x 3 Z matrix. The self inductances are directly deduced from the frequency variations of the imaginary parts of Z_{ij} elements. The equations of the real parts are solved taking into account the results of additional d.c. measurements ; then parasitic resistances can be determined

- for the extraction of parallel elements, such as parasitic capacitances, each gate is largely reverse biased (pinch-off condition).

From the frequency dependence of Y matrix elements, it is possible to deduce directly all the capacitances.

The determination of the intrinsic elements (g_m, g_d, C_{gs}, C_{gd}) needs also a two steps procedure, in order to distinguish the two equivalent FETs under cascode configuration :

- in the first step, the first transistor is cold (internal $V_{ds} \neq 0$) and the second B is biased exactly in the regime we are studying.

The elements of the second transistor B are directly evaluated from frequency variations of the four Y_{ij} parameters (two ports) deduced from the nine Z_{ij} parameters of the dual gate FET (three ports) by assuming that in cold regime, the relationship Z_{22} # $2Z_{12}$ is always satisfied [12].

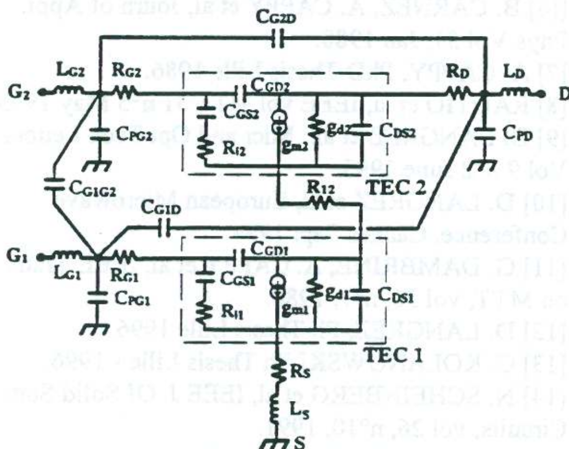

Fig 6 : Equivalent circuit of the dual gate FET

- In the second step, the same procedure is applied to the reverse situation : second transistor cold and first transistor under regime we are studying.

We have studied systematically the dependence of parasitic element values upon gate configurations, number of fingers, individual gate widths... In general, the results are in satisfying agreement with those that can be expected qualitatively considering these device topology and for instance the influence of air bridges and gate pads. Then, accurate results can be expected for the intrinsic elements. Fig 7 gives examples of typical results concerning the main elements of the equivalent circuit for a 0.15 µm dual gate PHEMT : transconductances, output conductances, gate to drain capacitances. It can be noted that even under linear regimes, accurate determinations can be obtained.

Electrical modeling

The electrical models are deduced from theoretical predictions and experimental data obtained by the different methods previously described.

Note that the design of dual gate HEMT mixers needs very accuracy HEMT electrical models both for linear and saturated regimes. As the models available did not satisfy these requirements, we have developed in house models better suited for this particular purpose [13].

Moreover, we had to account for the particularities of cascode configuration, in which the equivalent drain to source voltage of each individual transistor is unknown for a given value of the total drain to source voltage V_{ds}. Then, it constitutes a result of the simulation by imposing that the drain current is the same in the two transistors.

The two drain current generators are taken dependent on individual gate to source and drain to source voltage (V_{ds}). The corresponding analytical functions are obtained by integration of transconductance variations versus V_{gis} and V_{dis}.

Then variations can be fitted by hyperbolic tangent function for low V_{ds} values and by polynomial dependences for larger V_{ds} (with a degree that may reach 6) : moreover MDS step functions are applied to the g_m formulae when the gate to source voltage becomes lower than the pinch-off one :

$$I_{ds} = \tanh(\gamma V_{ds})(1 + \xi V_{ds}) \cdot \int_{V_{F1}}^{V_{gs}} F1(V_{gs})\, dV_{gs} + \int_{V_{F2}}^{V_{gs}} F2(V_{gs})\, dV_{gs}$$

Where F1 and F2 are polynomial functions V_{F1} , V_{F2} are limits of step functions, close to pinch-off values.

The capacitance dependencies $C_{gs} = f(V_{gs}, V_{gd})$ and $C_{gd} = f(V_{ds}, V_{gd})$ are approximated by analytical formulae which are close to the Scheinberg model [14], where polynomial and step functions are introduced in order to have a better fit with

experimental results in the whole V_{ds} and V_{gd} dynamic range.

$$C_{gs} = \frac{\partial Q_{gs}}{d V_{gs}} \quad and \quad C_{gd} = \frac{d Q_{gd}}{d V_{gd}}$$

$Q_{gs} = \alpha C_{gs0} V_{gd} + C_F \text{Ln} [\cosh [S_g (V_{gs} - D_c \tanh (D_k V_{gd}))]]/S_g$

$Q_{gd} = \beta C_{gd0} V_{gd} + C_{F1} \text{Ln} [\cosh [S_g (V_{gd} - D_c \tanh (D_k V_{gs}))]]/S_g$

α, β, C_F, C_{F1}, S_g, D_c and D_k being fitting parameters.

This electrical model gives results in very good agreement with theoretical predictions deduced from physical simulation and experimental data deduced from parameters extraction. Fig 8 shows a typical example of such a comparison concerning eight elements of the equivalent circuit for a 3 x 25 µm x 0.15 µm dual gate PHEMT. This shows clearly the accuracy of this electrical model.

Example of application :

Finally, this electrical model has been used for the design of several mixers in the 60-65 GHz frequency range (13, 15). Such model has been implemented in MDS software. The monolithic integrated circuits have been designed in cooperation with a group of Thomson TCS and fabricated in Thomson foundry. A 0.15 µm T gate AlGaAs/InGaAs pseudomorphic HEMT has been used. A layout of a typical circuit is represented in fig 9. The dual gate mixer operates under low noise mixer configuration : the signal is applied to the first gate and the local oscillator is connected to the second one.

The d.c. biases are chosen in order to the first transistor operates under linear regime and the second one is saturated.

Open stubs, and capacitors are used to obtain matching and isolations at the inputs and suppression of high frequencies components at the output. Very promising performance have been obtained, even for the first one, such as a maximum conversion gain of - 3 dB, for a LO power close to 9 dBm, and a LO to RF isolation better than 30 dB in the whole frequency range for the version Mix 100.

Moreover, a very good agreement is obtained between experimental results and theoretical predictions that shows the validity of electrical models developed in this approach. As examples, fig 10 and fig 11 represent a systematical comparison between simulation and measurement for :

- OL/RF and RF/OL isolation (fig 10)
- conversion gain as function of LO and RF input power (fig 11).

Conclusion

We have shown that a specific methodology must be used for the design of new monolithic millimeter wave-integrated circuits. By combining the theoretical predictions of several physical simulation tools and the experimental results of parameters extraction it is possible to build very accurate models.

A very demonstrative example has been given, by considering the case of a submicrometer dual gate pseudomorphic HEMT, with the purpose of realizing a 60 GHz frequency mixer.

Even for an equivalent circuit including 26 elements, it is possible to evaluate accurately the parameter variations versus d.c. biases to build a very precise model and to design a monolithic circuit, with a high degree of safety.

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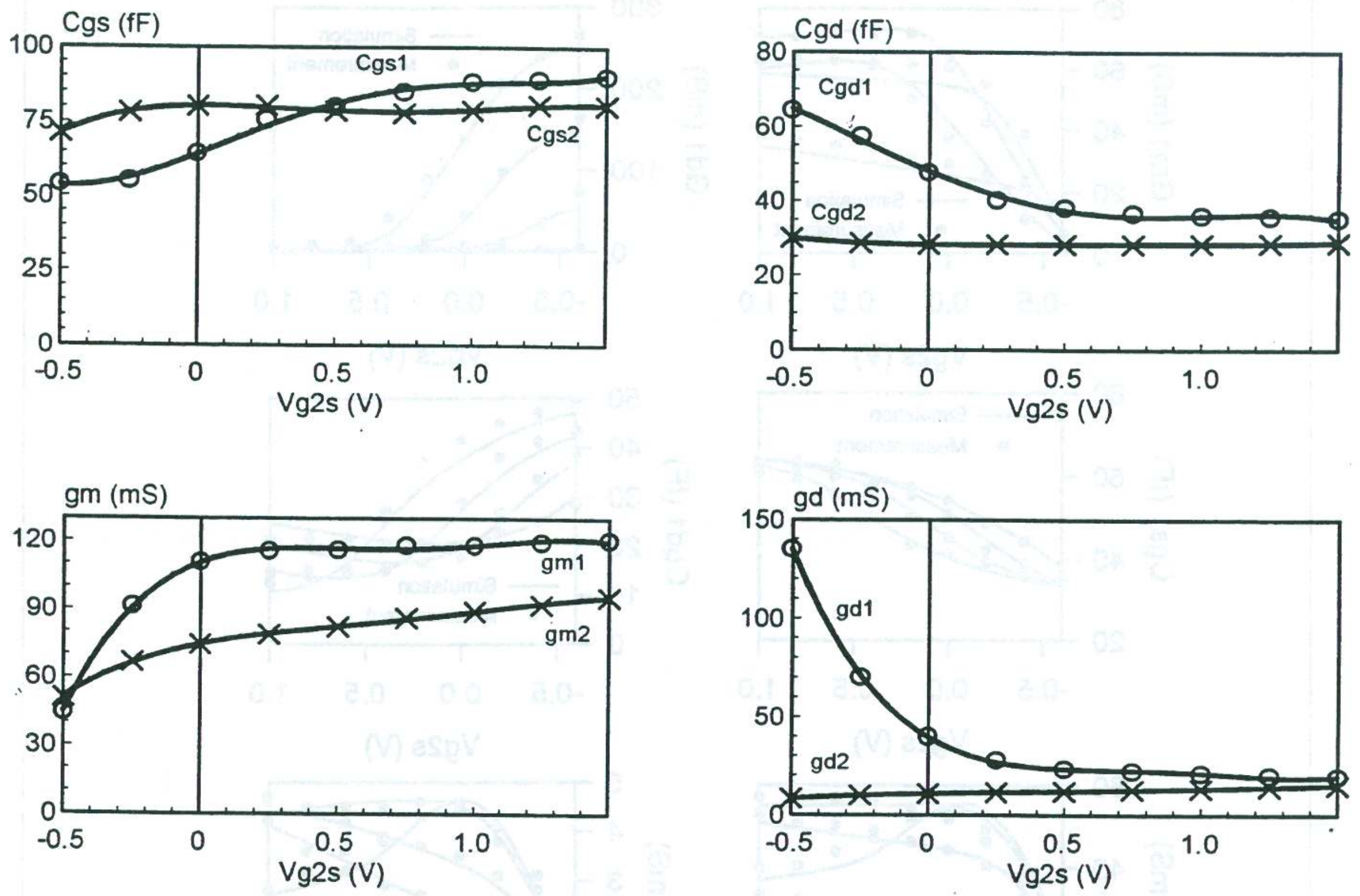


Fig. 7 : Variations of the main elements of the equivalent scheme versus V_{g2s} for a 0.15 µm dual gate pseudomorphique HEMT (Z = 3x50 µm ; V_{ds} = 3V ; V_{g1s} = 0 V).

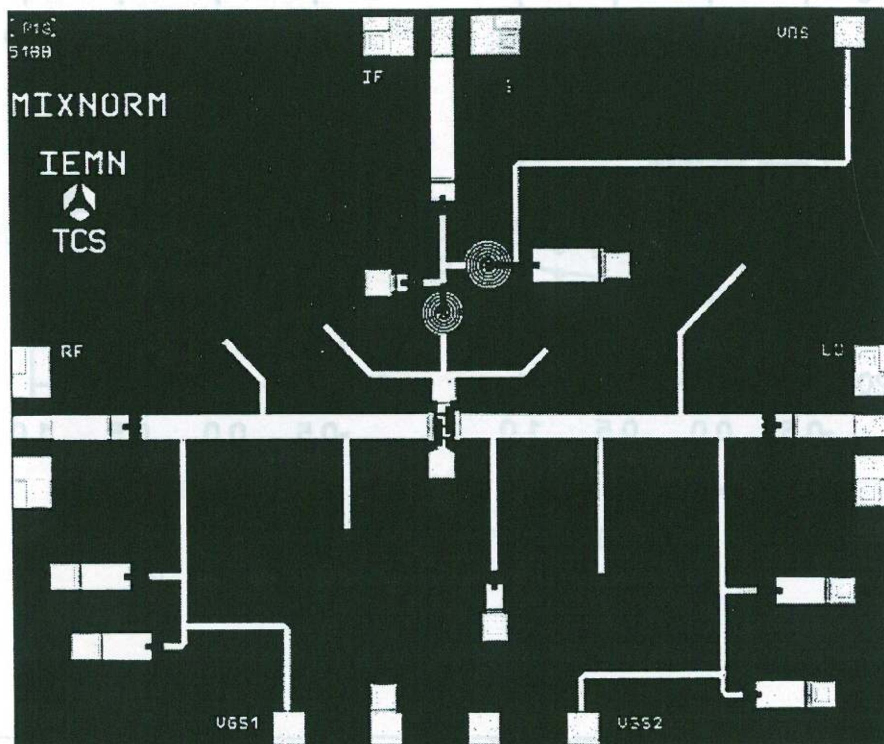


Fig. 9 : Layout of a typical dual gate mixer.

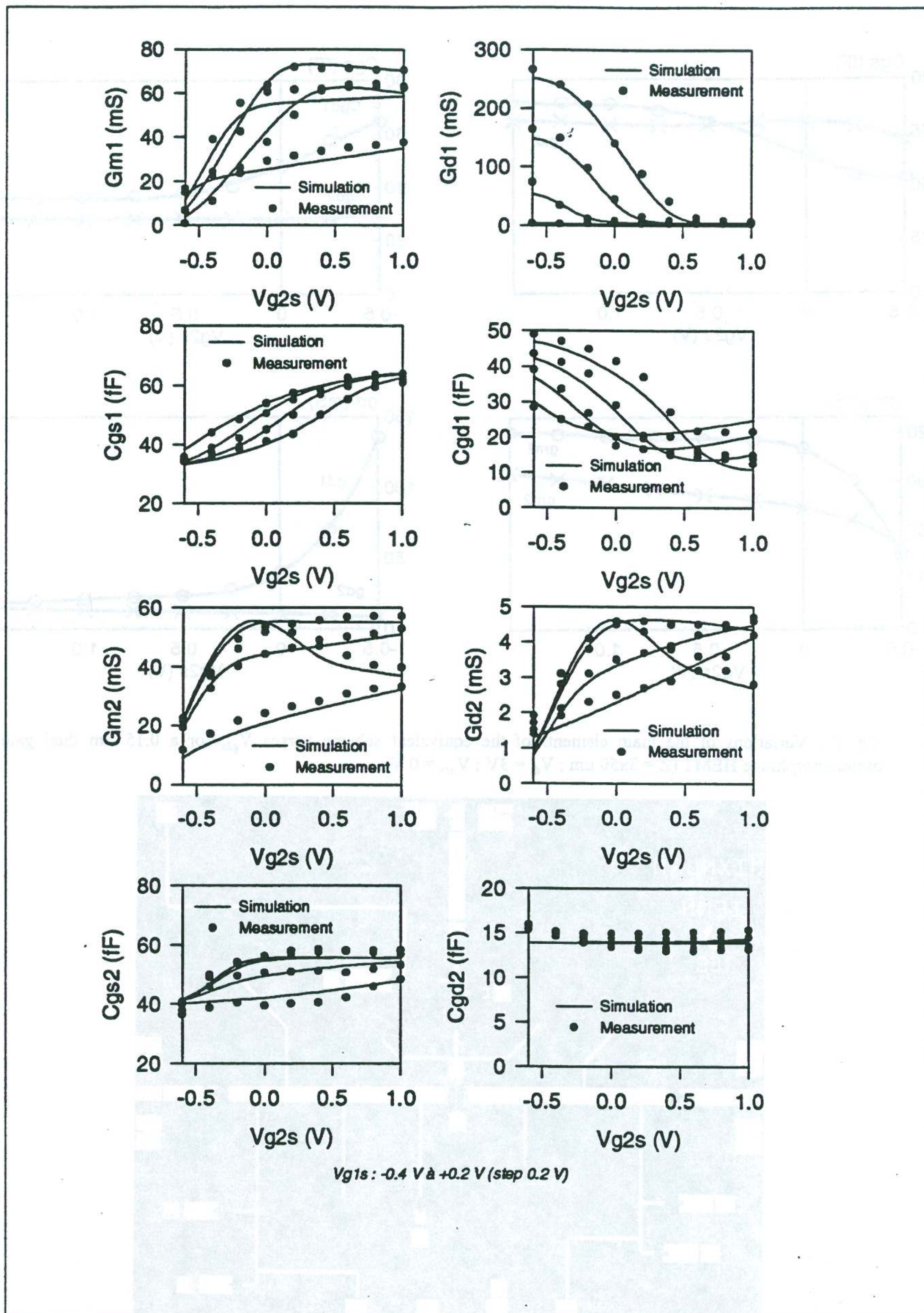
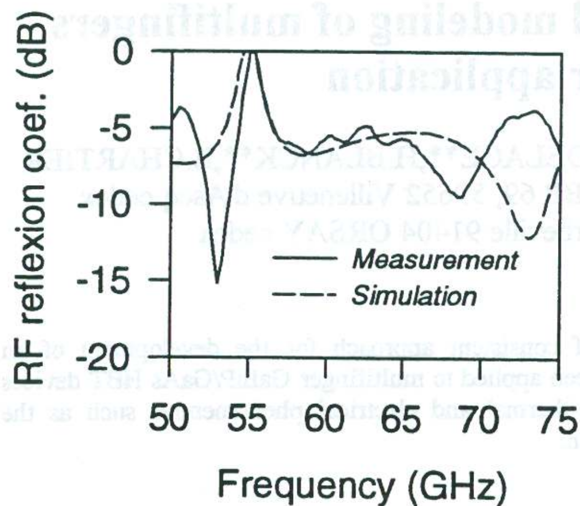
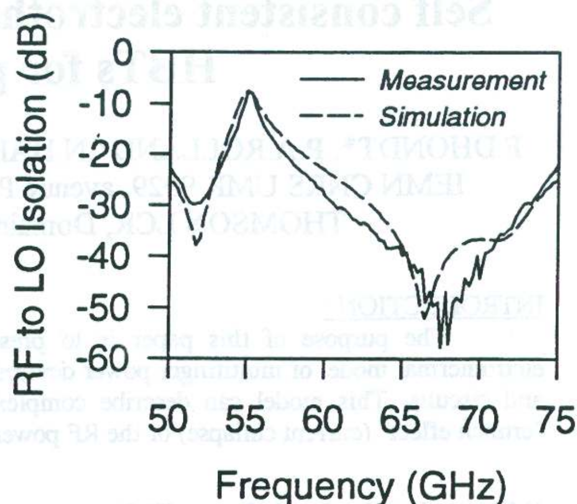
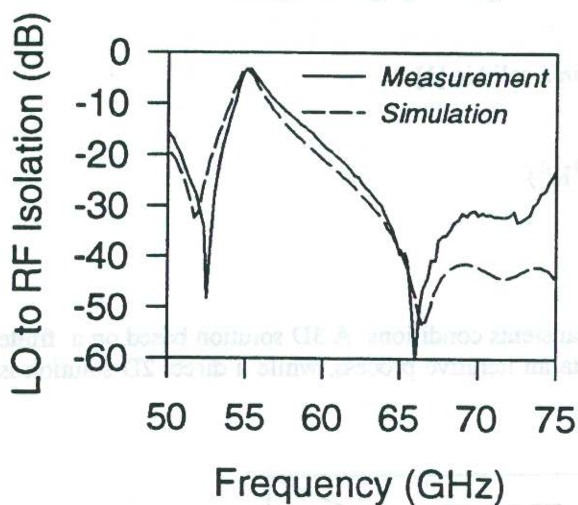


Fig. 8 : Comparison between the predictions of the electrical model and experimental results for a 3x25x0.15 µm dual gate PHEMT (V_{ds} = 3 V).







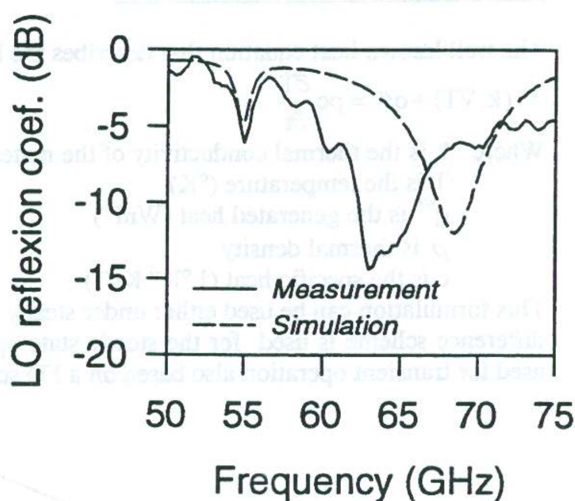
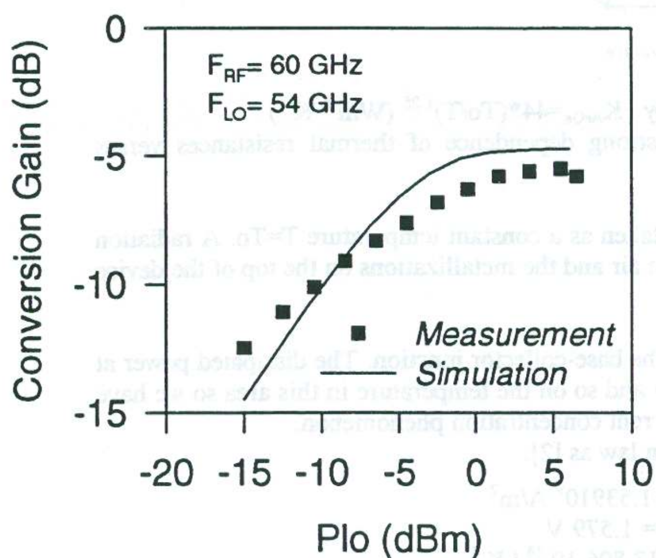


Fig. 10 : Comparison between theoretical predictions and experimental performance for a dual gate mixer : RF/OL and OL/RF isolations.



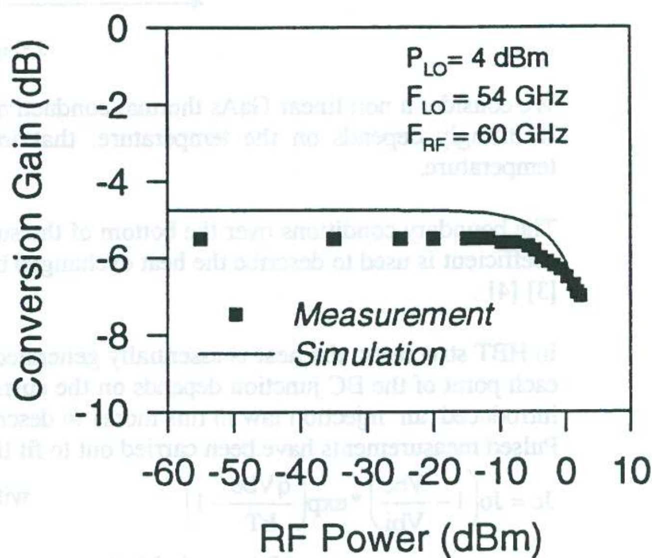


Fig. 11 : Comparison between theoretical prediction and experimental performance of a 0.15 µm dual gate mixer (MIXNORM version) : dependances of conversion gain on RF and LO powers.