A High CMRR GaAs Single-Input to Differential Convertor

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Abstract

In this paper a new topology for Single Input to Differential convertors is presented. Among the capabilities of convertors realised with this topology, 6 dB of extra conversion gain respect to a single differential cell and suppression of the common mode can be mentioned. An exact model of the circuit and considerations about design optimisation are also presented.

Introduction

GaAs technology and monolithic integration allow the circuit implementation of functions originally used in low-frequency ICs. One of the most relevant difference with respect to hybrid microwave circuits is the possibility of using differential signals and topologies. By using this approach many circuit topologies become available to implement the basic system functions (Amplification, Signal Generation, Mixing and Multiplication). As a consequence of the differential processing of signals Single-Input to Differential and Differential to Single-Ended convertors are needed (SI-D, D-SE).

To implement in GaAs technology the function D-SE a circuit based on current mirrors has been proposed [1]. To obtain the opposite function a single differential cell can be used successfully up to a frequency of some GHz depending on the technology used. This solution suffers from frequency limitations due to parasitic capacitances of active devices used in the current source.

In this paper we present a topology for single-input to differential convertors showing a conversion gain approximately 6 dB greater than the one of a single differential cell. An analysis which leads to a characterisation of the convertor by a block scheme of the circuit is also presented. Computer simulations results for a simple realisation of the convertor are shown.

Basic scheme

The basic circuit concept is to use an inverting amplifier to sense the common mode voltage on the common source node to drive the second input of a differential cell, which is usually grounded.

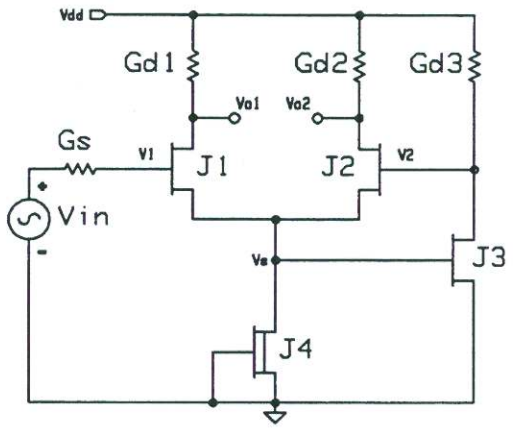

Fig. 1 - Convertor basic circuit

As an example the simple circuit in Fig. 1 can be used to realise the convertor: the feedback amplification of the common mode signal is provided by a single FET in a common source configuration. In this circuit the gate of the FET J_2 is provided with a voltage approximately equal and opposite to the input voltage on the gate of J_1. As far as this effect is considerable, the pair J_1-J_2 is driven by a differential input signal close to $2V_1$ and a common input suppressed by the feedback.

Circuit modelling

A complete characterisation of a SI-D convertor can be obtained by finding its input impedance and the input-output differential and common mode transfer functions. An effective approach can be followed if two blocks (the differential cell and the feedback amplifier) are identified. By this choice a system analysis based on the characterisation of the two blocks and useful for any circuit realisation of the convertor can be found. The main difficulty of this approach is the modelisation of the mutual loading effects of the two blocks in the feedback loop. To solve this problem a representation with n-port networks can be used. In Fig. 2.a the network described by the admittance matrix Y^A represents the differential cell (with its current source) where port 1 and 2 refer to the gate nodes and port 3 refers to the coupled sources node. The network Y^B represents the feedback amplifier.

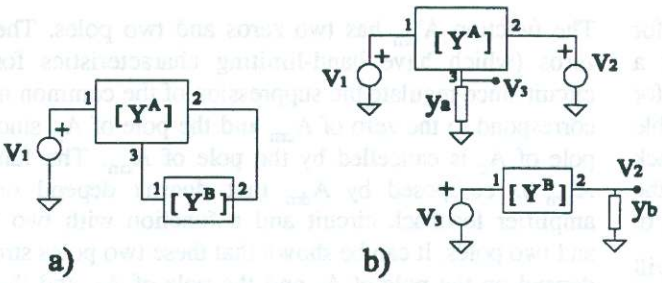

Fig. 2 - a) Circuit representation with Y-matrices
b) An equivalent representation

Admittance matrices have been chosen to describe the networks since in this case they provide the simplest form for the characteristic functions of the circuit.

Due to the feedback connection of the two networks, the representation of Fig. 2.a leads to a characterisation of the circuit quite complex and not easily usable in a design phase. An equivalent and more effective representation can be carried out breaking the connection between the two networks and introducing two equivalent admittances y_a and y_b and two voltage generators as in Fig. 2.b.

From such a representation four transfer functions can be calculated:
A_{dm}, A_{cm} (differential and common mode amplifications of the differential cell) and $A_c = \frac{V_3}{\left(\frac{V_1+V_2}{2}\right)}$ are easily obtained from the 3-port network loaded with y_a on port 3; $A_f = V_2 / V_3$ is obtained from the 2-port network loaded by y_b on port 2. These four functions with the input impedance completely characterise the circuit since

$$V_2 = \frac{A_c A_f}{2 - A_c A_f} V_1 \qquad (1)$$

$$V_{id} = 2\frac{1 - A_c A_f}{2 - A_c A_f} V_1 \qquad (2)$$

$$V_{ic} = \frac{1}{2 - A_c A_f} V_1 \qquad (3)$$

and obviously $V_{oc} = A_{cm} V_{ic}$ and $V_{od} = A_{dm} V_{id}$.

The input admittance in terms of Y-parameters is:

$$y_{in} = y_{11}^A + y_{13}^A \frac{y_{31}^A (y_{11}^A + y_{22}^B)}{(y_{31}^A + y_{12}^B)(y_{13}^A + y_{21}^B) - (y_{11}^A + y_{22}^B)(y_{33}^A + y_{11}^B)} \qquad (4)$$

The equivalent admittances y_a and y_b can be easily calculated from the parameters of the two networks once the symmetric form of the differential cell is considered :

$$y_a = y_{11}^B - y_{12}^B \frac{y_{13}^A + y_{21}^B}{y_{11}^A + y_{22}^B} \qquad (5)$$

$$y_b = y_{11}^A - y_{13}^A \frac{y_{11}^A + y_{22}^B}{y_{13}^A + y_{21}^B} \qquad (6)$$

The circuit can then be described by the block scheme shown in Fig. 3.

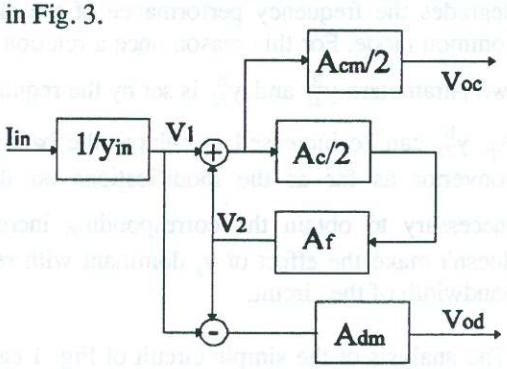

Fig. 3 - Block scheme of the circuit

This scheme points out the feedback loop on the common mode signal that generates the second input V_2. A stability analysis is easily carried out studying the loop gain.

Optimisation criteria

The optimisation of the circuit is aimed to two different and opposite design goals: a high DC symmetry and high bandwidth of the differential conversion gain.

A possible way to proceed in the design of the circuit is to assume the differential cell as given and to find an opportune feedback amplifier to satisfy the requirements in terms of symmetry and bandwidth. Since the amplification A_c (being the voltage amplification of a source follower) is close to unity the DC characteristics of the feedback loop are essentially dependent on the DC gain of the amplifier A_f. Defining a merit figure for the symmetry (a possible choice is the DC value of V_{ic}/V_1) the DC gain of A_f can be found by the equations previously shown. Since in terms of Y-parameters A_f can be expressed as

$$A_f = -\frac{y_{21}^B + y_{13}^A}{y_{22}^B + y_{11}^A} \qquad (7)$$

where the parameters of network A are fixed, the couple of parameters (y_{21}^B, y_{22}^B) must then be found to achieve the required value for A_f.

The frequency analysis of the circuit is quite complex for the general case and will be then carried out for a simplified case in which Y-parameters are characterised for a particular topology and technology. It is anyway possible to remark that the frequency characteristics of the feedback amplifier play a key role in the overall performance of the convertor. Since the amplifier A_f drives the second input of the differential cell a greater output admittance y_{22}^B will enlarge the bandwidth of the circuit. Besides, its input port loads the common source node of the differential cell by the equivalent admittance y_a and an increase of the latter degrades the frequency performance of the circuit on the common mode. For this reason once a relation between the two parameters y_{21}^B and y_{22}^B is set by the required value for A_f, y_{22}^B can be increased to enlarge the bandwidth of the convertor as far as the modifications on the amplifier (necessary to obtain the corresponding increase of y_{21}^B) doesn't make the effect of y_a dominant with respect to the bandwidth of the circuit.

The analysis of the simple circuit of Fig. 1 can express in more detailed terms these considerations. Representing each FET by a model comprising a voltage-controlled current source with transconductance g_m, an output conductance g_{ds} and a gate-source capacitance C_{gs}, it is possible to proceed to the optimisation of the circuit as in the following. Given a value for the symmetry factor SF (defined as the ratio V_{ic}/V_1 at zero frequency) we obtain for the DC case:

$$\frac{g_{m3}}{g_{ds3}+G_{d3}}=\frac{1-2SF}{A_cSF}$$

where the first member is equal to $-A_f$ and A_c is approximately 1. Therefore a first condition is set on the choice of FET J_3 and its load resistor G_{d3}. As an example using a feedback amplifier with Af=20 we obtain a SF approximately equal to 0.045 and thence a differential input to the cell J_1-J_2 $V_{id} \approx 1.91V_1$.

In order to analyse the frequency behaviour of the circuit two functions can be defined: A'_{cm} (common conversion amplification) as the ratio of the common mode output and the input V_1; A_{dm} (differential conversion amplification) defined as the ratio of the differential mode output and V_1. These two function can be expressed as:

$$A'_{cm}=A_{cm}\frac{1}{(2-A_cA_f)} \qquad (8)$$

and

$$A'_{dm}=A_{dm}2\frac{(1-A_cA_f)}{(2-A_cA_f)} \qquad (9)$$

The function A'_{cm} has two zeros and two poles. The two zeros (which have band-limiting characteristics for the circuit since regulate the suppression of the common mode) correspond to the zero of A_{cm} and the pole of A_f, since the pole of A_c is cancelled by the pole of A_{cm}. The function A'_{dm} is composed by A_{dm} that doesn't depend on the amplifier feedback circuit and a function with two zeros and two poles. It can be shown that these two poles strongly depend on the pole of A_c and the pole of A_f, and that the latter is dominant. From these considerations and further observing that the pole of A_f is expressed by:

$$p_f=-\frac{G_{d3}+g_{ds3}}{C_{gs1}},$$

the bandwidth optimisation can be carried out increasing the value of G_{d3} (using a smaller load resistor), keeping the DC gain of A_f constant. This can be achieved by using a FET J_3 with a larger channel (and thence a larger g_m).

Limitations exist to this optimisation approach since if a larger channel FET is used as J_3 a larger parasitic capacitance loads the sources of the differential couple. Since the pole of A_c and the zero of A_{cm} are expressed by:

$$p_c=-\frac{G_{d1}(g_{m1}+g_{ds1})+g_{ds4}(G_{d1}+g_{ds1})/2}{(G_{d1}+g_{ds1})(C_{gs3}/2+C_{gs1})}$$

$$z_{cm}=-\frac{g_{m1}g_{ds4}}{g_{m1}C_{gs3}-2g_{ds1}C_{gs1}}$$

an increase in the value of C_{gs3} tends to reduce their values and could make them comparable with p_f. Therefore the bounds on the value of the resistor loading J_3 can be easily found comparing the expression of p_f, p_c and z_{cm}, for a given differential cell and a preassigned DC gain of the feedback amplifier.

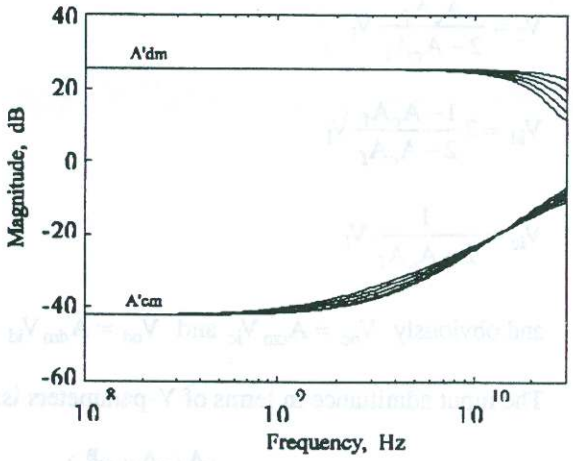

Fig. 4 - Bandwidth variations for different G_{d3}

In Fig. 4 the functions A'_{dm} and A'_{cm} with a fixed DC gain of A_f=14 are plotted for five values of G_{d3} in the range 2600-1000 Ohm. Further reductions of the resistance degrade the bandwidth of A'_{cm} since z_{cm} becomes

dominant. The functions are calculated using the parameters of the linearised model for the active devices from IAF DPD-QW GaAs process [2].

Spice simulations (using P-HEMTs from the same process as active devices) have been performed to evaluate the bandwidth of the circuit and the results in terms of a CMRR are presented. We have defined the quantity CMRR' as the ratio of the differential output voltage to the common mode output voltage. In Fig. 5 the results in terms of CMRR' of two convertors with different DC conversion gain are shown and a comparison with respect to the simple differential cell is made. An increase in the CMRR' of about 20 dB is obtained with the solution proposed.

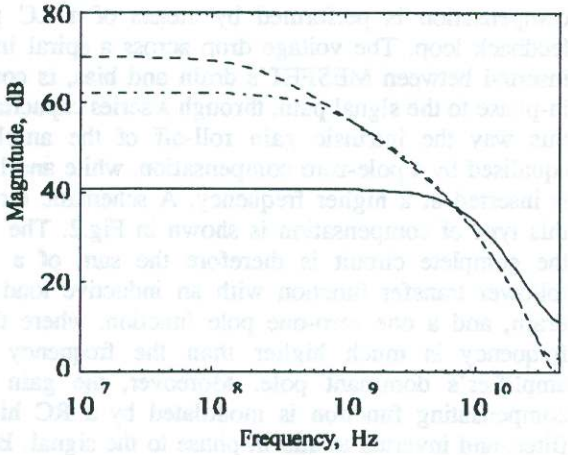

Fig. 5 - CMRR's of the proposed convertor with A_f=14 (dashed-dotted line), with A_f=26 (dashed line) and of a single differential cell (solid line).

A Root-locus analysis has shown that the stability is ensured within wide margins in AC optimisation.

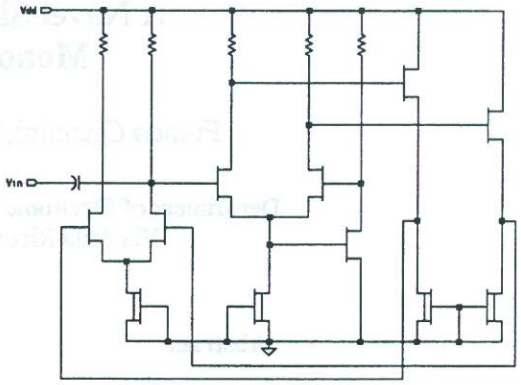

Fig. 6 - A self-biasing circuit for the convertor

The feedback loop which sustains the differential mode amplification makes the circuit very sensitive to DC mismatching and requires a very careful consideration of the biasing aspects. In Fig. 6 a scheme that comprises a DC feedback path able to ensure self-biasing capability to the circuit is shown.

Conclusions

A new topology for Single Input to Differential convertors has been presented. A useful general model in terms of Y-parameters has been found for this topology. Considerations regarding the design of the feedback amplifier have been discussed in order to optimise the circuit in terms of frequency response. Spice simulations of a simple realisation of the convertor have been shown and compared to a simple differential cell used as a convertor.

References

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[2] K. Koehler, P. Ganser, K. H. Bachem, M. Meier, J. Homung, A. Huelsmann, "Advanced high-electron concentration GaAs/$Al_xGa_{1-x}As$ pulse-doped double heterostructure for device application," Ins. Phys. Conf. Ser. 112, IOP Pub. 1990, pp. 521-526.