High-efficiency Powerful Millimeter Wave Varactor Multiplier

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Abstract

The paper describes development and investigation of varactor doubler from input frequency 36 GHz to output 72 GHz. To increase the output power two diode balance multiplier circuit was used. The multiplier was developed for output power no less than 100 mW and conversion efficiency no less than 50%.

Introduction

There is a problem to create solid state millimeter wave high-efficiency powerful source. At the same time there are powerful ($P \geq 1.5$ W; $\eta \geq 15\%$) GaAs IMPATT diode sources at 30-40 GHz frequency band, which can be used as a pump for frequency multiplier for to get LO power level at upper millimeter or submillimeter wave lengths frequency bands. Many papers [1]-[9], concerning multipliers investigation, shown possibility of more that 50% efficiency at millimeter wave frequency band. The key point for high power multiplier is low losses in diodes and circuits. To reduce power losses monolithic two diodes balance multiplier circuit was used.

Monolithic circuit

GaAs $i\text{-}n^{++}\text{-}n_1\text{-}n_2$ type semiconductor wafer was used for the monolithic circuit, where i is intrinsic semiconductor; doping levels equal to $4\cdot10^{18}$ cm^{-3}, $8\cdot10^{16}$ cm^{-3} and $2\cdot10^{17}$ cm^{-3} were realized for n^{++}, n_1 and n_2 respectively. Lengths 0.4 μm and 0.1 μm were realized for n_1 and n_2 layers respectively. Two different doping n_1 and n_2 were used for increasing varactor capacitance $C(0)/C(V_{br})$ ratio. The device fabrication process begins with deposition of Ti/TiN/Ti/Au. Ti layer form Schottky barrier, TiN is used for thermal stability. After photolithography and Au galvanic deposition processes an anode was formed, as shown 5 on Fig.1. The diode anode had dimensions 6 x 170 μm. Next by chemical etching layers n_1 and n_2 in area 3 were removed and Ni/Au/Ge layer was evaporated. Then, the ohmic contacts were alloyed at 420 C for 30 seconds in a forming gas ambient. A specific contact resistance 0.025 ohm·mm was obtained. The boron implantation process was than used to isolate the active region, which is below 6 level on Fig.1. Diodes with circuits elements are shown on Fig.1. Total size of monolithic circuit was 0.8·0.8·0.2 mm^3.

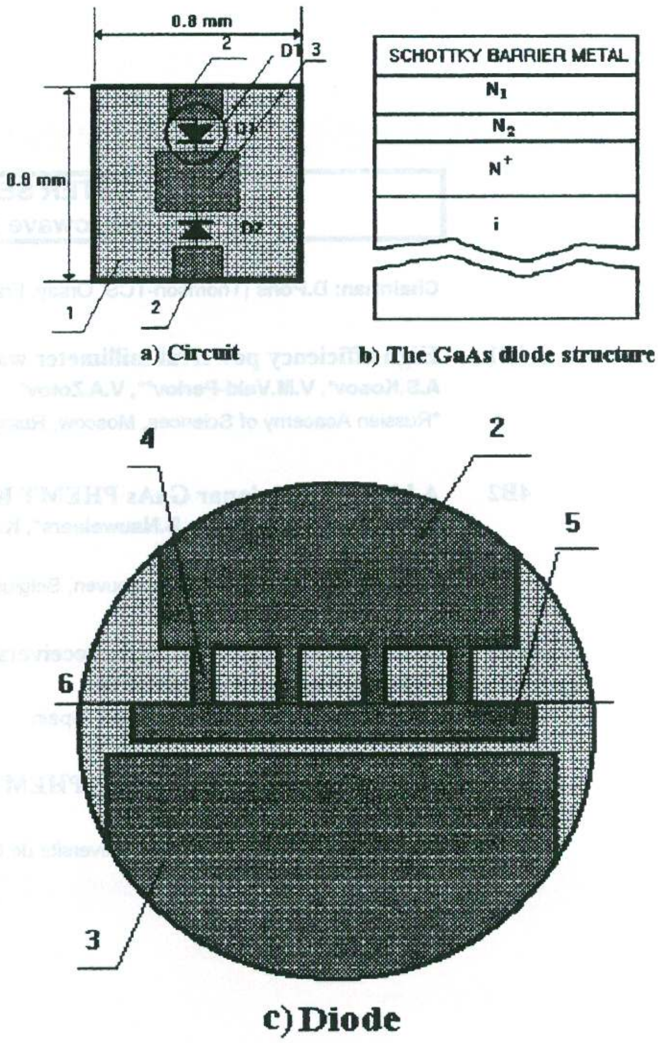


Fig. 1. Monolithic circuit of doubler: a) semiconductor chip; b) diode structure; c) varactor diode

The doubler performance depends upon total losses resistance R_s,, $C(V)$ and breakdown voltage V_{br}.

Measured $C(V)$ dependence of single diode is shown on Fig.2. $C(0)$ was near 1.4 pF, the $C(0)/C(V_{br})$ was near 7, V_{br} was equal to near 12 V.

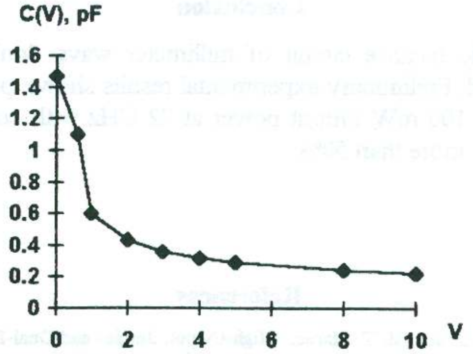
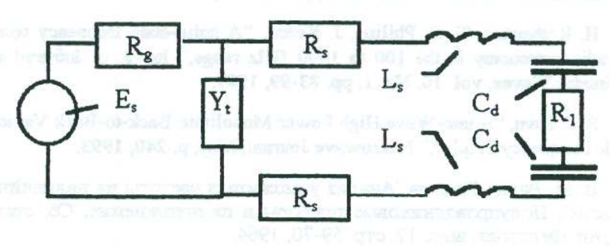


Fig.2. C(V) dependence of used diodes.

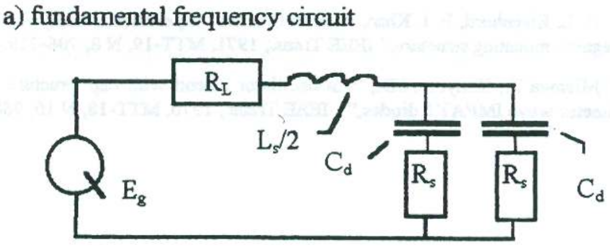
There is a weak dependence of losses resistance on diode bias and lies is range 0.28-0.33 ohm.

Doubler circuit and performance

The circuit of balance doubler is shown on Fig.3, where R_g is impedance of input power source, which is equal to characteristic impedance of input waveguide. For 0.8 mm waveguide height R_g is equal to near 180 ohm. R_s is losses resistance of diode and circuit, E_s is input power generator, C_d is mean diode capacitance, R_1 is losses, associated with power conversion to higher harmonic, R_L is load resistance at second harmonic frequency. E_g is voltage generator associated with power conversion from input to second harmonic and L_s are inductances formed by strips 3 and 4 on Fig.1(a).



a) fundamental frequency circuit



b) second harmonic circuit

Fig.3. Doubler circuit

To achieve optimum performance of the doubler the transformed resistance of input power source R_{gt} must be equal to R_1 plus two R_s. The value of R_1 can be obtained from [10] and Fig.4, assuming that amplitude of harmonic current I_n is equal to zero if n>2.

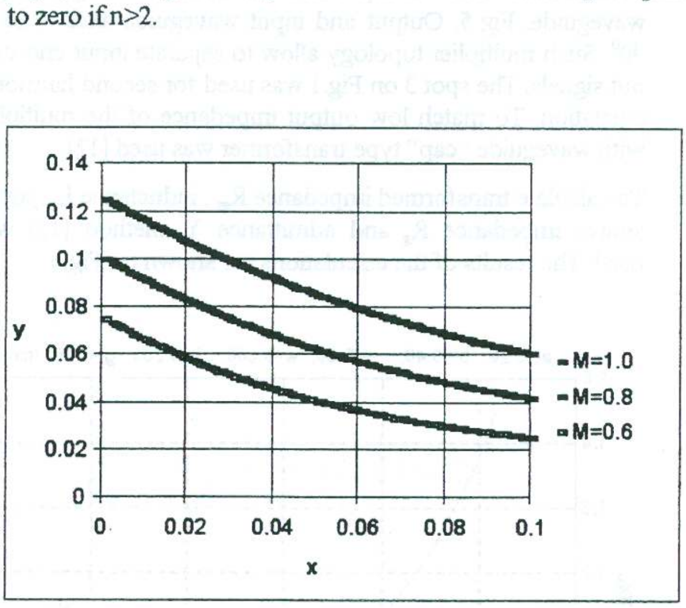


Fig.4. Dependence of $y = R_1\omega C_d / 2$ upon diode parameter $x = R_s\omega C = \dfrac{1}{Q_d}$ for three values of $M = \dfrac{I_1}{\omega C_d(\varphi + U_0)}$; where I_1 - fundamental frequency current amplitude; φ - barrier height, U_0 - mean voltage on diodes.

From diode data it can be calculated that x=0.02 and M=0.8 under maximum input power, which corresponds to voltage swiping from zero to V_{br}. From Fig.4 we can obtain that $y=8.5\cdot 10^{-2}$ and R_1=2.5 ohm. Following [10] R_L is equal to $(R_s+R_1/2)/2$=0.75 ohm.

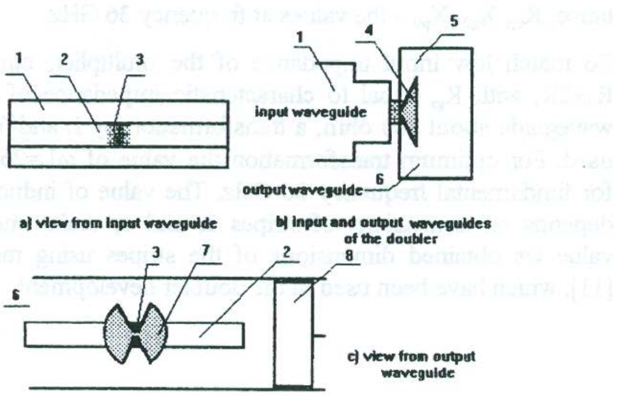


Fig.5. Sketch of the doubler: a) viewed from input waveguide; b) input and output waveguides of the doubler; c) view from output waveguide

The circuit was incorporated in reduced height input waveguide, Fig.5. Output and input waveguide axes were at 90^0. Such multiplier topology allow to separate input and output signals. The spot 3 on Fig.1 was used for second harmonic excitation. To match low output impedance of the multiplier with waveguide "cap" type transformer was used [12].

To calculate transformed impedance R_{gt}, inductance L_s, power source impedance R_g and admittance Y_t method [11] was used. The results of the calculations are shown on Fig.6.

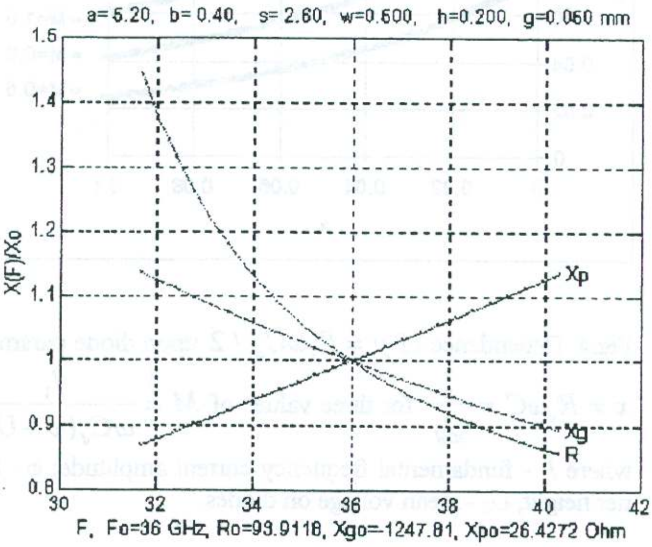


Fig.6. Fundamental frequency input circuit impedance for doubler, shown of Fig.5: a - waveguide width; b - waveguide height; s - strip location in waveguide; w - strip width; h - gap location in waveguide; g - gap width; F - frequency; R - waveguide characteristic impedance; X_g - reactive impedance of gap capacitance; X_p - reactive impedance of strip inductance; R_0, X_{g0}, X_{p0} - the values at frequency 36 GHz.

To match low input impedance of the multiplier, equal to R_1+2R_s with R_g, equal to characteristic impedance of input waveguide about 180 ohm, a transformation by L and Y was used. For optimum transformation the value of ωL=26 ohm for fundamental frequency 36 GHz. The value of inductor L depends on dimensions of stripes 2, and to realize needed value we obtained dimensions of the stripes using method [11], which have been used in the doubler development.

Conclusion

Monolithic balance circuit of millimeter wave doubler was developed. Preliminary experimental results shown possibility to realize 100 mW output power at 72 GHz with conversion efficiency more than 50%.

References

[1] J. W. Archer, M. T. Marec, "High-Output, Single- and Dual-Diode, Millimeter-Wave Frequency Doullers," IEEE Trans., vol. MTT-33, No 6, pp. 533-538, June 1985.

[2] T. Takada, T. Makimura, M. Ohmori, "Hybrid Integrated Frequency Doublers and Triplers to 300 and 450 GHz," IEEE Trans., vol. MTT-28, No 9, pp. 966-973, Sept. 1980.

[3] A. Rydberg, B. N. Lyons, S. U. Lidholm, "On the Development of a High Efficiency 750 GHz Frequency Tripler for THz Heterodyne Systems," IEEE Trans., vol. MTT-40, No 5, pp. 827-830, May 1992.

[4] T. J. Tolmunen, A. V. Raisanen, "An efficient Schottky-varactor frequency multiplier at millimeter waves. Part I: Doubler," Int. J. of Infrared and Millimeter Waves, vol. 8, pp. 1313-1336, 1987.

[5] T. J. Tolmunen, A. V. Raisanen, "An efficient Schottky-varactor frequency multiplier at millimeter waves. Part II: Tripler," Int. J. of Infrared and Millimeter Waves, vol. 8, pp. 1337-1353, 1987.

[6] T. J. Tolmunen, A. V. Raisanen, "An efficient Schottky-varactor frequency multiplier at millimeter waves. Part III: Quadrupler," Int. J. of Infrared and Millimeter Waves, vol. 10, No. 4, pp. 475-504, 1989.

[7] T. J. Tolmunen, A. V. Raisanen, "An efficient Schottky-varactor frequency multiplier at millimeter waves. Part IV: Quintupler," Int. J. of Infrared and Millimeter Waves, vol. 10, No 4, pp. 505-518, 1989.

[8] H. Rothermei, T. G. Philips, J. Keene, "A solid-state frequency source for radio astronomy in the 100 to 1000 GHz range," Int. J. of Infrared and Millimeter Waves, vol. 10, No. 1, pp. 83-99, 1989.

[9] R. J. Hwu, "A mm-Wave High Power Monolithic Back-to-Back Varactor Diode Frequency Tripler," Microwave Journal, May, p. 240, 1993.

[10] В. М. Вальд-Перлов,"Анализ умножителя частоты на нелинейной емкости", Полупроводниковые приборы и их применение, Сб. статей под ред. Федотова, вып. 12, стр. 59-70, 1964.

[11] R. L. Eisenhard, P. I. Khan, "Theoretical and experimental analysis of a waveguide mounting structure," IEEE Trans., 1971, MTT-19, N 8, 706-719.

[12] Misawa T., Kenyon N.D., "An oscillator circuit with cap structure for millimeter wave IMPATT diodes," - IEEE Trans., 1970, MTT-18, N 10, 968.