X BAND HIGH PAE MMIC HPA FOR SPACE RADAR APPLICATIONS

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Abstract

A MMIC 2-Watt 5-stage amplifier (HPA) has been successfully designed in one foundry run. This HPA, developed for a space Radar application at X band, has a 40dB linear gain, an output power of 34dBm with a 32% associated Power Added Efficiency (with a maximum of 39%) and uses the THOMSON TCS HP07 technology (Lg=0.7um) which is on the way to be qualified for Space Application. The tests have been performed both on wafer and in package.

Introduction

Thanks to its intrinsic properties (size, weight, reliability), MMIC technology has already proved to be highly useful for space applications like Radar active antenna.

The CNES (French National Space Agency) provided the specifications of the HPA to be integrated in T/R modules of X band SAR antenna. The antenna is composed of a few thousands of modules.

The strong requirements attached to Space Technology have been satisfied by using an extensive set of design rules. These rules, associated to a Design Process Methodology based on Dassault Electronique experience, are included in a document called " Dassault Electronique MMIC Manual".

On-wafer and in-package tests have been performed by Dassault Electronique and Thomson TCS.

Design

On the basis of our methodology rules, a design process includes the following requirements to be taken into account from the very beginning of the design:

- Reliability: a 6-year life time is expected for such a Space application.
- Environmental considerations, including mechanics and temperature: pads, bonding wires and connections have been taken into account so that the HPA exhibits the specified performances when embedded in the package.
- Stabily study : stage by stage, the impedances presented to the transistor are compared to its stability circles.
- Testability: the bias pads have been arranged to allow both a full on-wafer probing capability (pads on both sides of the chip) and a convenient bonding configuration requiring pads along a single chip edge upon packaging specifications.
- Automatic layout generation: The chip has been laid out using this type of automatic generation under HP/MDS environment. This allows a perfect conformance, at any time, between the schematic view and the layout view of a circuit along the whole design process.

The design frequency band ranges from 8.5 to 10.8 GHz. All the models we used were supplied by the foundry and, as far as the FETs are concerned, we used both linear and non linear (for class A and class AB) models.

To reach the output power specification, the last stage has a total gate length of 4.32mm and is biased at Vd=10V, and to reach the

linear gain specification, 5 stages are needed. The maximum power added efficiency (PAE) has been obtained by using a class AB bias for the last 2 stages (Idss/5) and a class A bias for the first 3 stages (Idss/2).

The power matching has been carried out using a backward design flow: from load pull simulation, an output matching network has been calculated and synthesized. Back from this point (at 5th stage drain level), inter-stage networks have been designed, on power, stability and PAE considerations for the last 2 stages and for maximum linear gain and stability for the first 3 stages.

Figure 1 shows a photograph of the HPA.

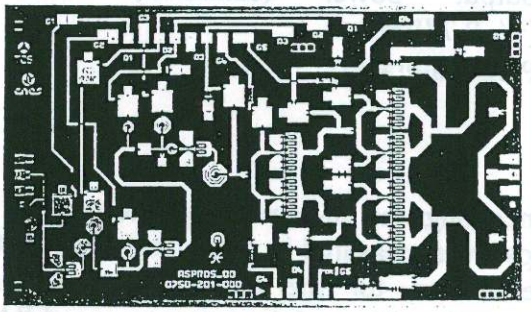

Figure 1 : HPA layout, 4.85mm x 2.85mm

The HPA design included a linear stability study and also a linear and non linear sensitivity study to check the good HPA behaviour upon changes in temperature conditions and process characteristics.

The simulated performances are presented on Figure 2 (linear gain and K factor between 7 and 12GHz) and Figure 3 (Output power and PAE versus input power for the centre frequency).

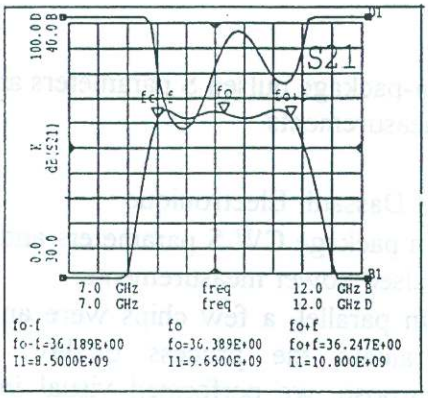

Figure 2 : S21 and K versus Frequency

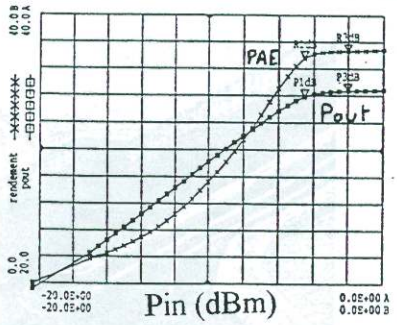

Figure 3 : Output power and PAE versus input power

Processing and tests

Process :

The circuits have been processed with the Thomson TCS HP07 technology; this MMIC MESFET process features a 0.7um gate lenght, with a typical output power of 600mW/mm gate width.

The choice of this technology has been led first by its adequacy with the required performances and, second by the MMIC Space Evaluation/Qualification programme underway at Thomson TCS. The HP07 process is now being jointly evaluated by CNES and ESA (European Space Agency) in order to assess the use of HP07 devices for future space applications.

Tests :

At Thomson TCS :

- Fully automated on-wafer pulsed power measurements. The functional RF on-wafer yield obtained is about 67%.

- In-package pulsed S parameters and power measurements

At Dassault Electronique :

- In package CW S parameters and CW and pulsed power measurements.
- In parallel, a few chips were analysed to evaluate the process quality. For this purpose, we performed visual inspections and analysis of cross-sectional views obtained by cutting the chip. As an example, Figure 4 shows a view of a gate finger (with a x5000 scale).

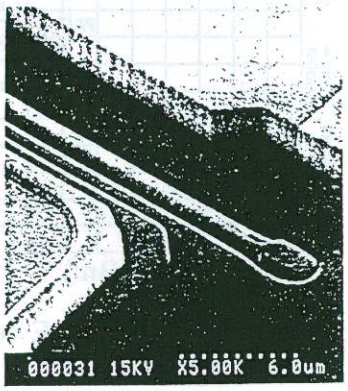

Figure 4 : View of a gate finger

Results

Figure 5 shows the on-wafer output power pulsed measurements on 20 chips (30 chips had been measured on this wafer) and Figure 6 shows the on wafer PAE on the same chips.

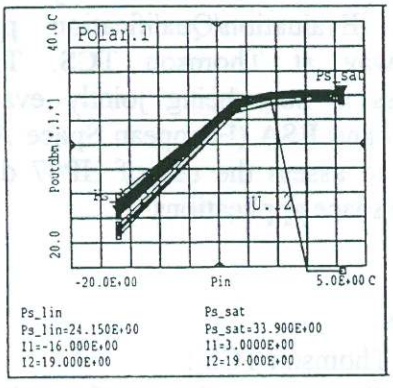

Figure 5 : On-wafer output power of 20 chips

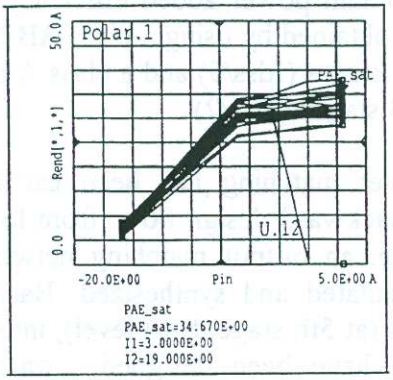

Figure 6 : On-wafer PAE of 20 chips

So, the typical on wafer main performances are :

- linear gain : 40dB (+/- 1dB)
- output power (saturated): 34dBm (+/- 0.7dBm)
- PAE (saturated) : 32%.

Concerning the in-package performances, 6 chips were measured in pulsed mode at 25°C. The results, for the center frequency are presented on Figure 8 (output power and PAE versus input power).

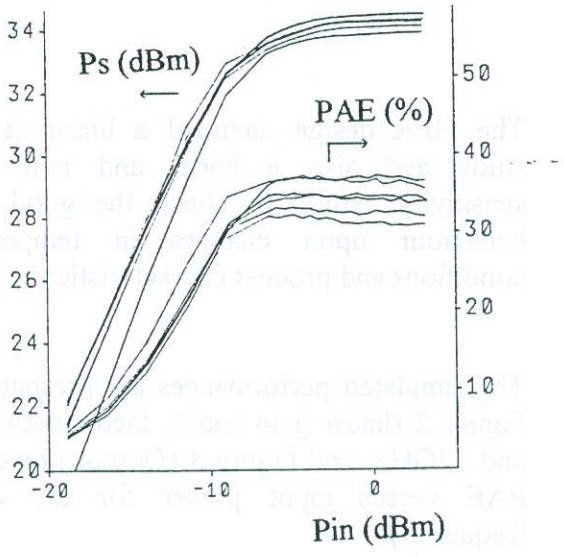

Figure 7 : In-package Output power and PAE versus input power of 6 chips

So, in this configuration, the main characteristics are :

- linear gain : 40.5dB
- output power (saturated) : 34.1dBm
- PAE (saturated) : 34%.

Those performances tend to be better than the on-wafer ones because the design took into consideration the chip environment.
In the same time, the input and output reflection losses are about 10dB.

Moreover, Figure 8 and Figure 9 show the output power and the PAE of the 6 packages measured in pulsed mode at 25°C over the frequency band : 9.35 to 9.95 GHz.

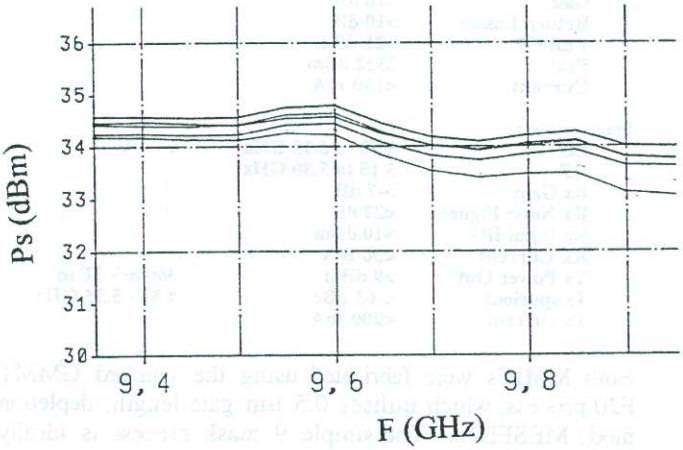

Figure 8 : In-package output power of 6 chips versus frequency (9.35 to 9.95 GHz)

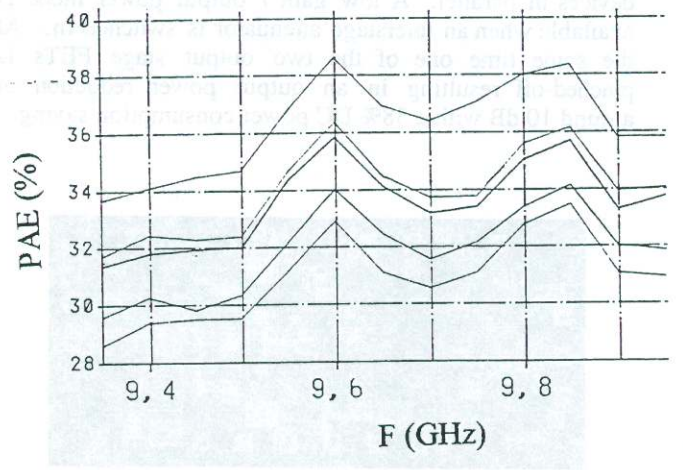

Figure 9 : In-package PAE of 6 chips versus frequency (9.35 to 9.95 GHz)

Finally, over the specified frequency range (300Mhz) and temperature range (-25°C to +50°C), the minimum main performances are :

- linear gain : 37dB (35dB specified)
- output power : 33.2dBm (33dBm specified)
- PAE : 30% (31% specified).

Conclusion

Thanks to the use of the Dassault Electronique design methodology and the accurate model library of TCS HP07 process, remarkable results have been obtained after only one foundry run, with a good agreement between the simulations and the measurements.
The MMIC HPA exhibits a linear gain of 40dB, an output power greater than 2 Watts and a PAE of 32% in X band.
This HPA, using a space qualifiable process, is dedicated to Space SAR applications.

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