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# Distributed GaAs-PHEMT 0.2µm preamplifier for 20 Gbit/s photoreceivers.

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## Abstract

A 20 Gb/s photoreceiver module has been realized with a transimpedance of 63 dBΩ. The bandwidth is 16 GHz, and the average equivalent input noise is 13 pA/√Hz up to 14 GHz. This photoreceiver is realized by cascading three distributed preamplifiers processed in a GaAs PHEMT 0.2µm gate length technology.

## Introduction

20 and 40 Gbit/s optical fibre telecommunication systems are now actively investigated. For such systems, high performances E/O and O/E interfaces are needed. We have designed distributed preamplifiers for photoreceiver applications. With these circuits, 20Gbit/s photoreceivers have been fabricated.

## Photoreceiver design

The photoreceiver is designed to receive and amplify a 20 Gb/s soliton or NRZ signal. As the optical level is around 0 dBm, and the required electrical level at the input of the decision circuit is 0.6 $V_{peak-peak}$, the gain of the photoreceiver has to be close to 30 dB, corresponding to 64 dBΩ.

A distributed amplifier is a well-suited structure for bandwidths higher than 10 GHz. As the gain of a distributed amplifier is close to 10 dB, three such amplifier-chips must be cascaded to get the required amount of gain.

These three amplifier-chips, are then assembled with a vertically illuminated AlGaInAs/InP PIN photodiode, on an alumina substrate.

As described in [1], the input and output impedances of the chips are higher than 50 Ω, except for the output of the last stage, in order to match the last amplifier to an ouput impedance of 50 Ω. The first and the second amplifiers are approximately 70 Ω/70 Ω amplifiers (type A), and the last one is a 70 Ω/50 Ω (type B).

As the PIN photodiode capacitance ($C_d$) is 100 fF, the first preamplifier stage input-impedance can be higher than 50 Ω. Between two stages, there is no need to be at a standard 50 Ω impedance. So we have designed two kinds of chips : one to handle the photodetector signal or the signal from a previous stage, the other to both amplify the signal and convert the impedance from the internal level (70 Ω) to the output level (50 Ω) (fig.1).

The capacitance of the photodiode limits the gate line impedance to about 80 Ω at 20 GHz ($Z=1/C_d\omega$). A compromise is obtained between this target impedance and the technological feasibility of gate line width without excessive losses. The gate line primary impedance is 96 Ω (without the gates connected), corresponding to a global gate line impedance (gate line plus HEMT gate capacitance) of 70 Ω. Then the drain line is adjusted to this impedance, in order to match it with the gate line impedance of the next stage.

The chips have been designed for 20 and 40 Gbit/s operation. The 40 Gb/s bit rate will be possible with a 50 fF capacitance high-bandwidth photodiode. The measured S21 of the distributed amplifiers (fig 2) shows a -3 dB bandwidth of 40 GHz with 12 dB average gain for type A chips, and 38 GHz, with 9 dB gain for type B chips.

## Technology

The distributed preamplifiers are realized with a 0.2 µm gate length GaAs PHEMT technology from a commercial foundry (Philips Microwave Limeil). The transition frequency (Ft) of the transistor is 55 GHz, and the pinch-off voltage is -0.9 V.

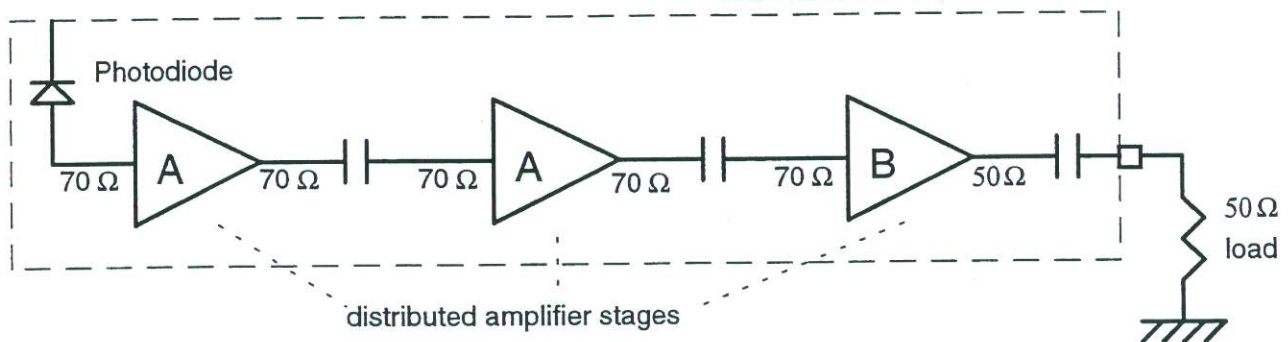


**Fig 1:** Schematic of the photoreceiver. By-pass capacitors are used between each stage. The 50 Ω load represents the load circuit, external to the module.

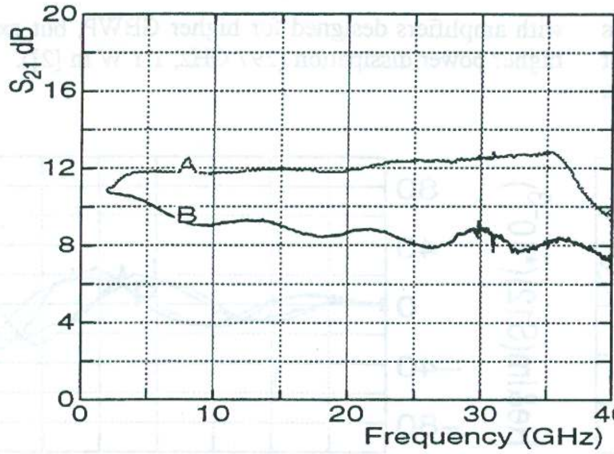


**Fig 2 :** |S21| of type A and B circuits, measured on wafer with a 50 Ω network analyser.

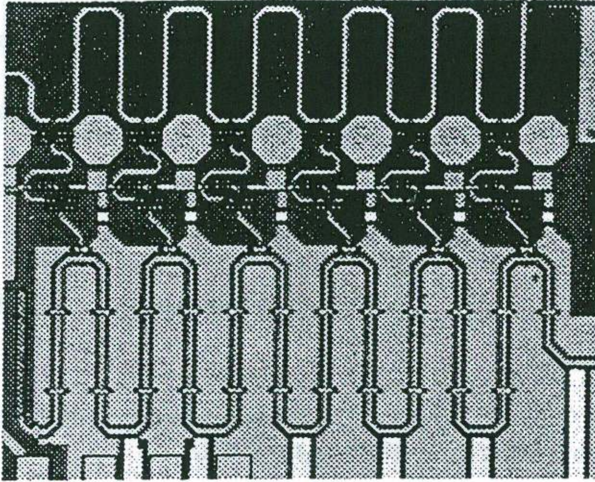

**Fig 3:** Type B amplifier chip. A microstrip line is used for the gate while a coplanar line is used for the drain.

## Distributed preamplifier design

In this section, the design of the distributed amplifier is explained.

*Gain considerations*

For an amplifier with the same input and output impedance, a simplified expression for the current gain is given by

$$g_m.Z_g/2 \quad (1)$$

where $g_m$ is the total transconductance of the raw of HEMTs, $Z_g$ the characteristics impedance of the gate line also equal to $Z_d$, the impedance of the drain line. So an impedance of 70 Ω instead of 50 Ω leads to a gain of 13.1 dB instead of 10.2 dB for $g_m$=130 mS, corresponding to a 2.9 dB improvement per distributed amplifier.

*Noise considerations*

The equivalent input noise current density of the photoreceiver can be calculated from the equivalent noise of the first distributed amplifier. For the complete expression of the different contributions, one can refer to [2,5]. In order to give a qualitative evaluation of the noise behavior of the amplifier, we have calculated numerically the different noise contributions with our photoreceiver design model, turning on and off the noise sources with our simulation software. The major sources of noise are the HEMTs noise (26%) and the thermal noise from the gate line load resistance (37%). The drain line load resistance represents 2% of the total noise. The remaining contributions are 35%, resulting from losses in lines, photodiode parasitic resistance...

The HEMT numerical noise model is based on a Van der Ziel representation [4], including a noise current source $i_g$ and a drain current source $i_d$. Noise current densities are given by

$$d\langle i_g^2\rangle/df = 4kT\omega^2 C_{gsi}^2 R/g_{mi} \quad (2)$$

$$d\langle i_d^2\rangle/df = 4kTPg_{mi} \quad (3)$$

ig and id are correlated with an essentially imaginary correlation coefficient C .

$C_{gsi}$, $g_{mi}$ are gate-source capacitance and transconductance of the $i^{th}$ HEMT while R and P are constant coefficients.

We found that the gate current generator contribution (2) is negligible with respect to the drain current generator contribution (3) for 20 Gb/s. A simplified expression for the noise of the HEMTs can be written as

$$d\langle i_h^2\rangle/df = 4kTP/(g_m Z_g^2) \quad (4)$$

The noise contribution of the gate line matching resistor (Rg) is

$$d\langle i_{Rg}^2\rangle/df = \alpha 4kT/R_g. \quad (5)$$

where α takes into account propagation of the noise current accross the gate line, backward to the signal direction, and its reflection on the photodiode impedance. α is around 0.25 from numerical simulations.

From this analysis of the main noise sources, an increase of the characteristic impedance $Z_g$ reduces the equivalent input noise of the preamplifier, both for the HEMT contribution as well as for the gate line matching load.

*Number of stage in each amplifier :*

An other important criteria for the amplifier design is the chip power dissipation. The designer has to make a compromise between a maximum gain per amplifier, leading to a high number of stages per amplifier, and the power consumption leading to reduce the number of stages below the number leading to the maximum gain.

6 stages per amplifier have been chosen. Each stage is a cascode inverter. The cascode configuration has a higher power consumption but reduces the parasitic transfer of the signal from the drain line to the gate line. A flatter and more reproducible response is expected from such a configuration, and the $S_{12}$ parameter module is lower.

The power dissipation of the type A chip is 0.25 W, for a gain-bandwidth product (GBWP) of 160 GHz. This is a low power consumption in comparison with amplifiers designed for higher GBWP, but exhibiting higher power dissipation (297 GHz, 1.1 W in [2]).

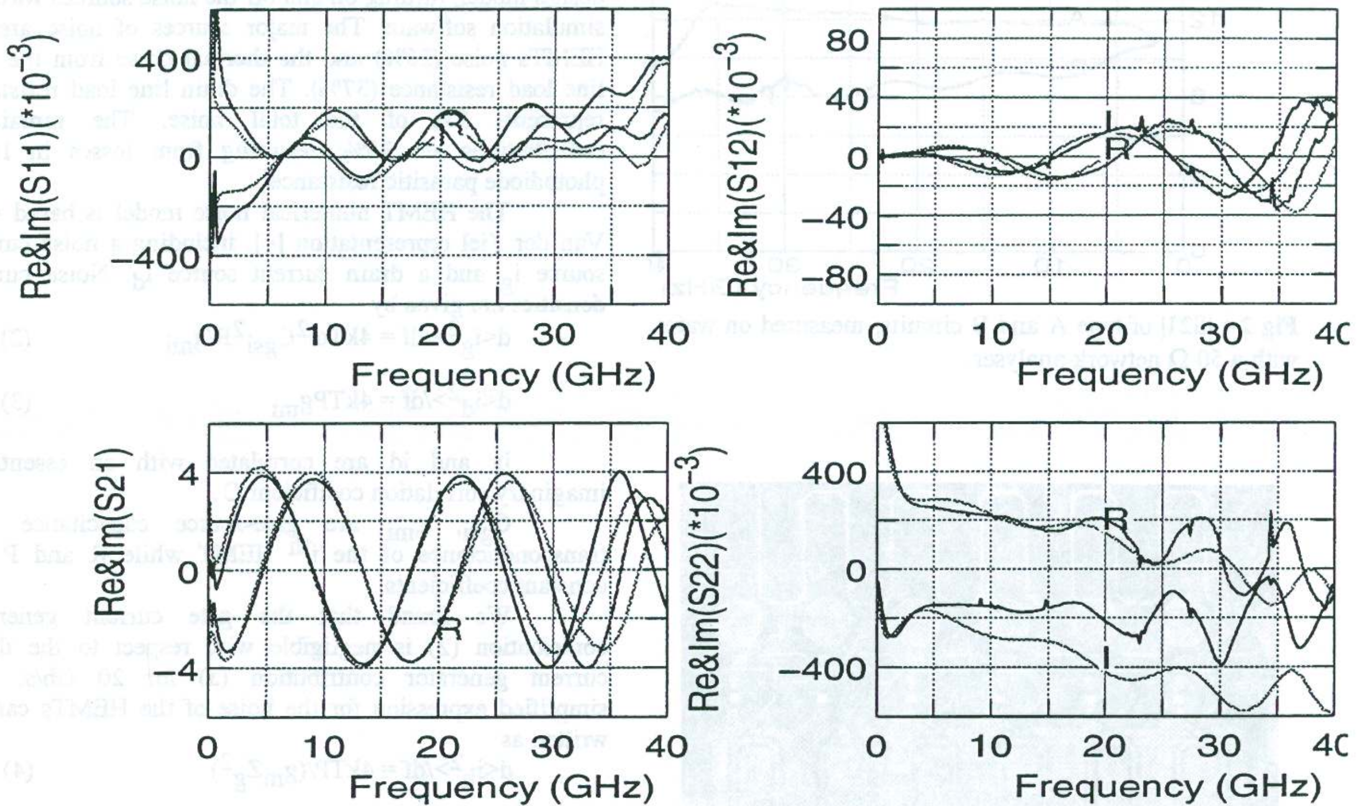


**Fig 4:** Type A circuit : Real and Imaginary parts of the S parameters :
dark lines = measurement, grey lines = simulation.
The $S_{11}$ and the $S_{22}$ correspond to an impedance varying from 70 to 60 Ω and 80 to 55 Ω respectively up to 40 GHz. The cascode configuration is the reason why the $|S_{12}|/|S_{21}|$ ratio is better than -40 dB up to 40 GHz.

## Photoreceiver module characteristics

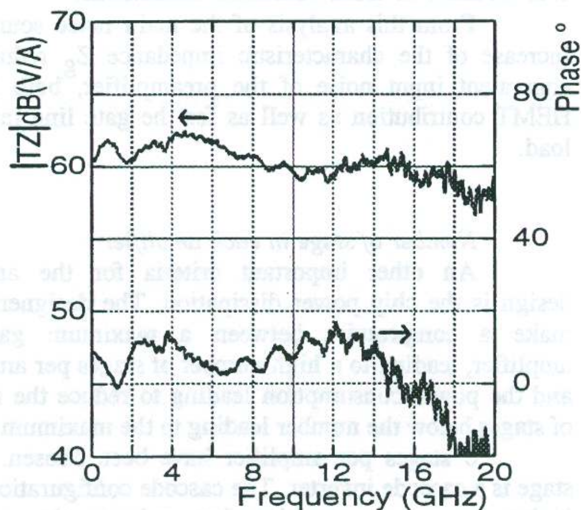


**Fig 5:** Transimpedance of the photoreceiver in module and phase.

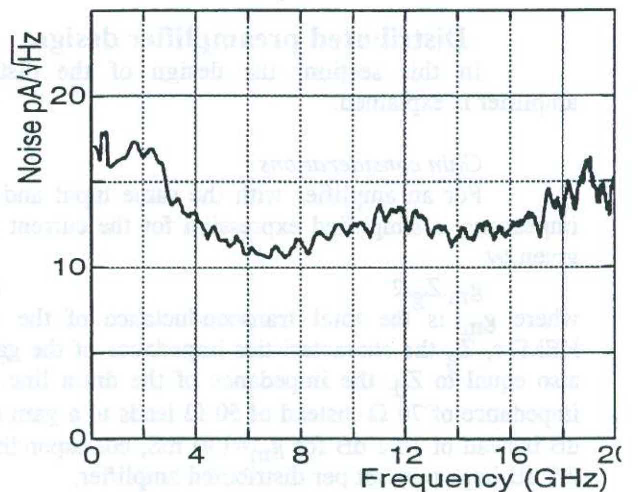


**Fig 6:** Equivalent input noise. The average equivalent input noise is 13pA/√Hz over 14GHz.

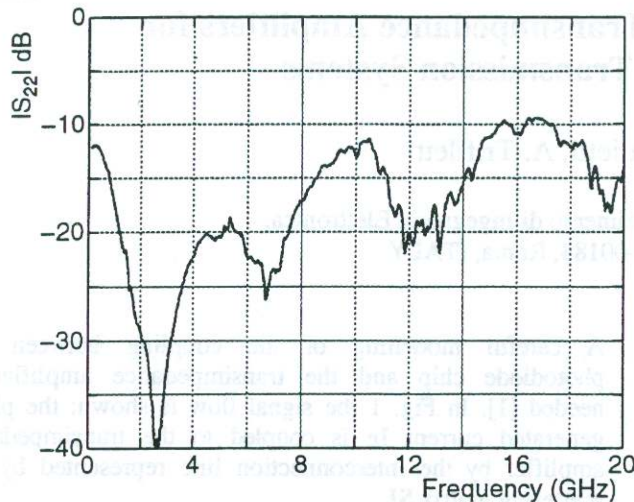


Fig 7: $S_{22}$ for the photoreceiver module.

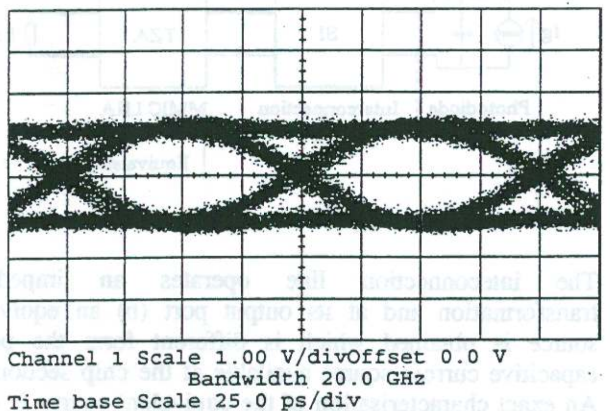


Fig 8: Eye diagram for a 10Gbit/s pseudo-random NRZ sequence.

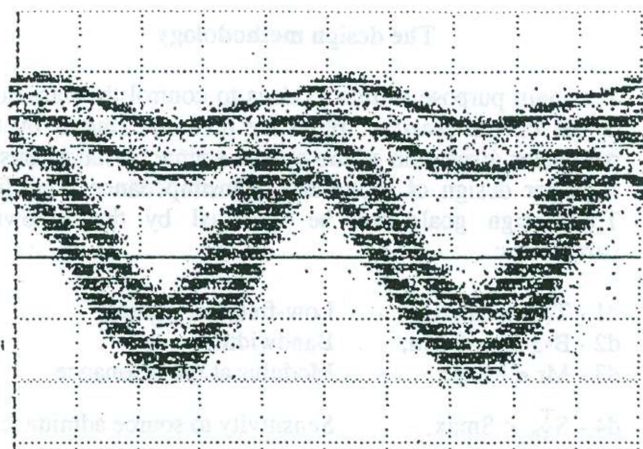

Fig 9 : Eye diagram for a 20Gbit/s pseudo-random RZ sequence. Time scale 10ps/div - Vertical scale 100mV/div.

The photoreceiver has been tested at 10 Gb/s and 20Gb/s.

A sensitivity of -19 dBm has been measured at 10 Gb/s with a $2^{31}$-1 pseudo-random sequence, which is very close to the sensitivity infered from the equivalent input noise, -19.4 dBm from an average noise of 14pA/√Hz up to 7GHz. The sensitivity is not modified when the sequence length is varied, due to the low cut-off frequency of the module equal to 1MHz. 37 dB gain amplifiers, and a fast decision circuit are used in addition to the photoreceiver module to measure this sensitivity.

The 20 Gb/s sensitivity infered from the noise is -18 dBm. Experiments are presently under process to measure the actual sensitivity.

## Conclusion

A 20 Gb/s photoreceiver has been reported, based on the assembly of an AlGaInAs PIN photodiode, and of three cascaded distributed-MMIC amplifiers, processed in a GaAs 0.2 µm PHEMT technology.

Specific distributed amplifiers have been designed using high impedance gate and drain lines in order to obtain a high gain and a low equivalent input noise from this GaAs MMIC technology.

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