A NEW GATE PROCESS FOR THE REALIZATION OF LATTICE - MATCHED HEMT ON InP FOR HIGH YIELD MMICs.

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ABSTRACT

A new gate process for the realization of ultra short gate HEMT on InP is presented. In this technology, the top of the gate is deposited on a Si_3N_4 layer. This gate process leads to small footprints, mechanically strong devices and good yield. Using this gate technology, HEMT with high Ft were realized and characterized. The influence of the Si_3N_4 removing was also investigated.

INTRODUCTION

The realization of millimeter wave ICs is a need for future applications such as LMDS, LANs, satellite constellations as well as passive imaging systems. In the millimeter wave range GaInAs/AlInAs/InP material based transistors are being used increasingly as alternative to PM-HEMT on GaAs. In this communication, a new gate process for the realization of high performance HEMT on InP is presented. This gate process is especially developed for millimeter wave integrated circuits in V and W bands using coplanar wave guide technology.

DEVICE PROCESSING

The lattice-matched InAlAs/InGaAs HEMT active layer was grown by molecular beam epitaxy in our laboratory using a solid source MBE 2300 Riber system. This heterostructure consists of an InAlAs buffer layer, an undoped InGaAs channel, an InAlAs spacer, a single Si δ-doped layer, an InAlAs schottky layer and finally a heavily doped InGaAs cap layer. A schematic cross section of this epilayer is shown in Fig. 1. At room temperature, the square resistance is 190 $\Omega/\square$, the sheet carrier density is 3.48 $10^{12}cm^{-2}$ and the electron mobility is $9600cm^2/v/s$. At 77K, the square resistance is 60 $\Omega/\square$, the sheet carrier density is 3.45 $10^{12}cm^{-2}$ and the electron mobility is $32000cm^2/v/s$.

The device processing steps can be summarized as follows. The active zone is defined by mesa etching using a H_3PO_4:H_2O_2:H_2O solution. Then, we selectively etch the InGaAs channel at mesa sidewalls with SA(succinic acid):H_2O_2 solution. The aim of this step is to avoid direct contact between the gate metal and the channel and to prevent gate-leakage current problems. We realize ohmic contacts by evaporating Ni/Ge/Au/Ni/Au metalization followed by a 310°C, 60s, rapid thermal annealing under N_2/H_2

atmosphere. Then, we cover up the device with 800Å silicon nitride film deposited by PECVD. This dielectric layer will protect the active zone and support the top of the T-shaped gate. In the case of circuit realization, this layer may be also used as the dielectric of MIM capacitors. The 0.1 μm gate length is defined by electron-beam lithography using PMMA resist. Exposure and development in a (MIBK:IPA) mixture results in 90 nm resist opening. To define the footprint and to shorten the gate length Lg, we etch the Si_3N_4 using a highly non-isotropic CF_4/CHF_3 RIE process. This technique reduces the overetch of the resist. Thus, we achieve a footprint size in the Si_3N_4 layer of about 0.1μm. We define the top of the gate (0.3μm) by using a (PMMA-P(MMA-MAA)) bilayer resist. It should be noted that this second exposure has no effect on the footprint size. The complete process sequence for gate fabrication includes a soft O_2-plasma after development, in order to obtain homogeneous recess etching. Gate recess is performed in a SA:H_2O_2 wet etching solution followed by Ti/Pt/Au metalization. A schematic cross section of the device is shown in Fig.1 and a SEM cross section is shown in Fig.2. The T-gate profile obtained using a Si_3N_4 silicon nitride layer presents several advantages. This Si_3N_4 film which covers the source-to-drain channel and supports the top of the gate metalization is also the passivation layer. This process leads to small footprints and mechanically strong devices. Moreover, it allows a large cross sectional area, which gives low gate resistance values and improves the device noise performance.

However, the presence of this dielectric layer increases the parasitic capacitances, especially the gate-to-drain capacitance Cgd. To further improve the device cutoff frequencies (especially Fmax), it is possible to remove this Si_3N_4 film using reactive ion etching (RIE). Two different gases, SF_6 and CF_4, which present naturally different etching properties, were used. For SF_6, we optimized the DC-bias, RF power and pressure to emphasize isotropic etching profile. Thus, we remove all the Si_3N_4 under the top of the gate metalization. For CF_4 on the contrary, we selected the plasma parameters to favor non-isotropic etching profile. In this case, the top of the gate metalization is used as a mask leaving two pieces of Si_3N_4 on both side of the gate foot. Thus, CF_4 etching will assure devices more robust than SF_6 etching but with higher parasitic capacitances. SEM cross sections of the gate structure are shown in Figure 3 and 4 after Si_3N_4 removing using SF_6 and CF_4 respectively.

DEVICE PERFORMANCE AND DISCUSSION

We successfully fabricate several wafers with almost identical device performances. S-parameters were measured from 1 to 50 GHz using on-wafer probing techniques. Three cases will be successively considered. Firstly the performance before Si_3N_4 removing, secondly after Si_3N_4 removing using SF_6 and thirdly after Si_3N_4 using CF_4.

- Figure 5 shows the distribution of the extrinsic current gain cutoff frequency Ft measured on several devices of the same wafer before Si_3N_4 removing. The average Ft is 190 GHz with a standard deviation of 20GHz. The small-signal equivalent circuit was extracted from the measured S-parameters in the 1-50 GHz frequency range. Figure 7 presents the small-signal equivalent circuit as a function of the drain-source current. The results are summarized in Table 1 for two different bias points: the maximum transconductance and the low noise conditions (Ids=100mA/mm). We obtain a maximum transconductance Gm of 1400 mS/mm and an intrinsic current gain cutoff frequency Fc= 268 GHz for a drain-to-source current Ids= 340 mA/mm. We can note that Gm and Fc remain very high even at low drain current (925 mS/mm and 210 GHz respectively at 100 mA/mm).

- After the Si_3N_4 removing using SF_6, several points should be noted. The maximum Gm (1230 mS/mm) and the corresponding DC drain current (192 mA/mm) decrease. This can be explained by the damages introduced at the surface of the epilayer by the plasma and/or the modification of the surface potential. At lower drain current (100 mA/mm), the surface effects are less important and the opposite variation is observed. We can note that Gm increases while Cgs diminishes. In his case, Fc increases from 210 to 242 GHz which is well suited to provide high noise performance. Figure 6 shows no reduction of the extrinsic current gain cut-off frequency Ft. Moreover, a dramatic decreases of the gate-to-drain capacitance Cgd, which improves the maximum oscillation frequency, can be also noted in figure 7.

- Following the CF_4 RIE process, no clear improvement of the device performance is observed and very large variations in device performance are obtained across the wafer. In fact, the decrease of the capacitance value is associated with important damages induced at the surface of the epilayer and the use of this plasma usually leads to a drastic decrease of the transconductance Gm. In this case, the particularities of this plasma (high DC-bias and high RF-power) are probably the main reason of the device degradation.

CONCLUSION

A new gate process is presented for the realization of ultra short gate HEMT on InP. High Ft devices were realized using this gate technology with a good yield. The Si_3N_4 etching by RIE using SF_6 and CF_4 was also investigated. Device performance improvement was observed with SF_6 especially at low drain current (low noise conditions) while CF4 leads to degradations and strong device performance variations which are not compatible with MMICs realization. The realization of V and W band MMICs using this gate technology is in progress.

(1) : « *60- and 77- GHz monolithic amplifiers utilizing InP-based HEMTs and coplanar waveguides* » ; M. Berg, J. Dickmann, R. Guehl, W. Bischof, Microwave and optical technology letters, Vol. 11, No.3, p.139-145 , February 20 1996.

(2) : « *A super low noise AlInAs/InGaAs HEMT processed by selective wet gate recess etching* » ; N. Yoshida, T.Kitano, Y. Yamamoto, and S. Mitsui, IEEE transactions on electronic devices, Vol. 43, No.1, p.178-180, January 1996.

(3) : « *A 155-GHz Monolithic InP-Based HEMT Amplifier* » ; H. Wang, R. Lai, Y.C. Chen and B. Allen, p.1275-1278, 1997 IEEE MTT-S Digest.

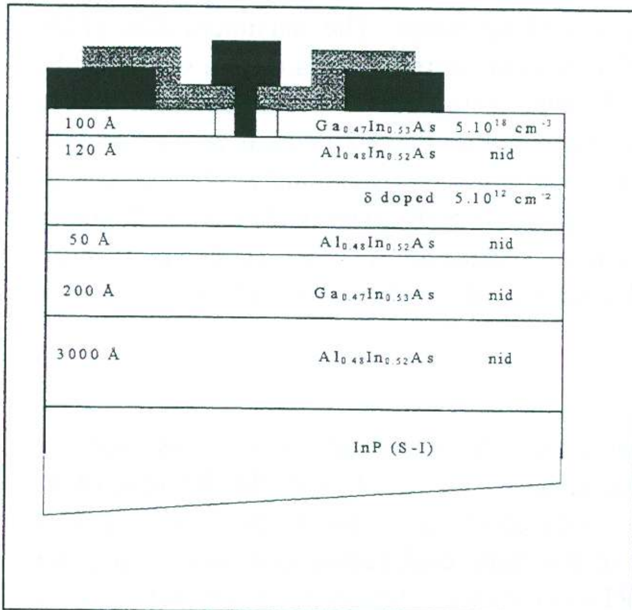


Fig.1. Structure of the active layer and schematic device cross section

Fig.2. SEM picture of a 0.1 μm gate deposited on the silicon nitride layer.

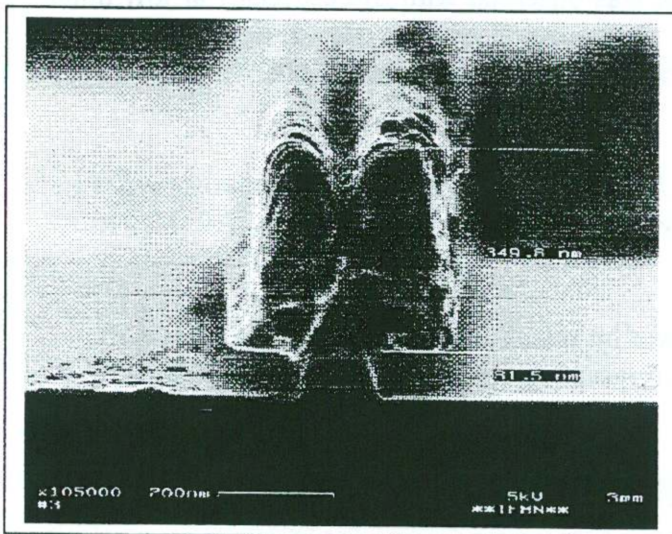


Fig.3. SEM device cross section after isotropic silicon nitride removing using SF_6

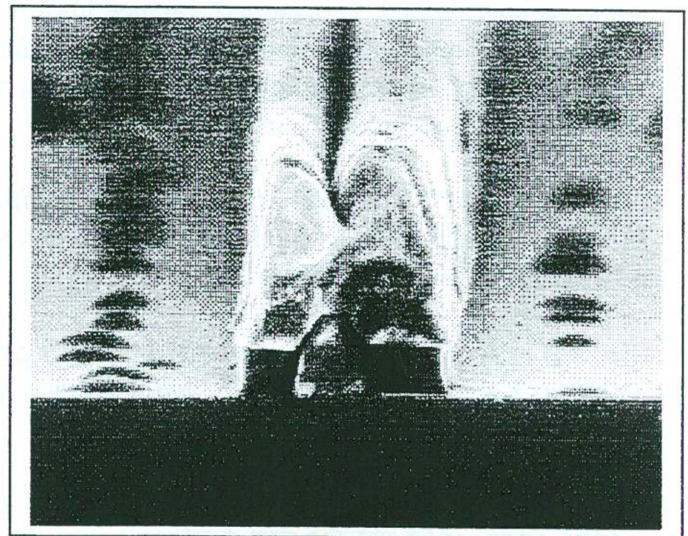


Fig.4. SEM device cross section after anisotropic silicon nitride removing using CF_4

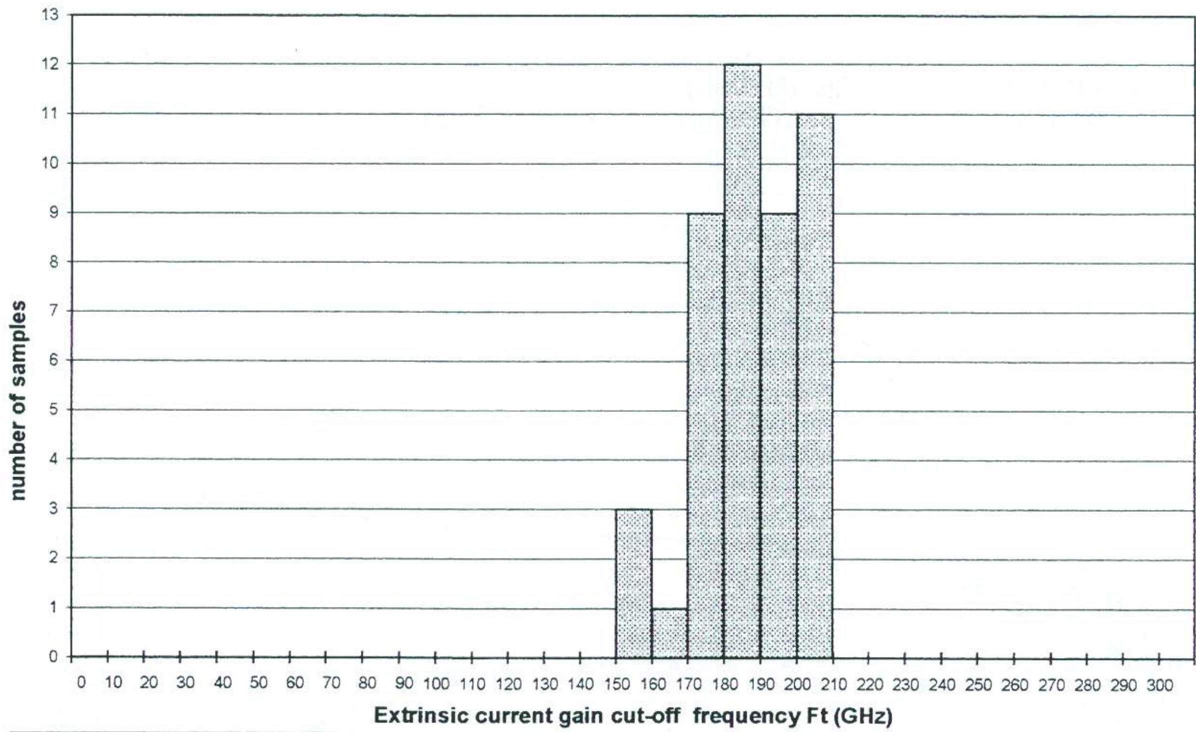


Fig.5. Distribution of the extrinsic current gain cutoff frequency Ft for several devices of the same wafer

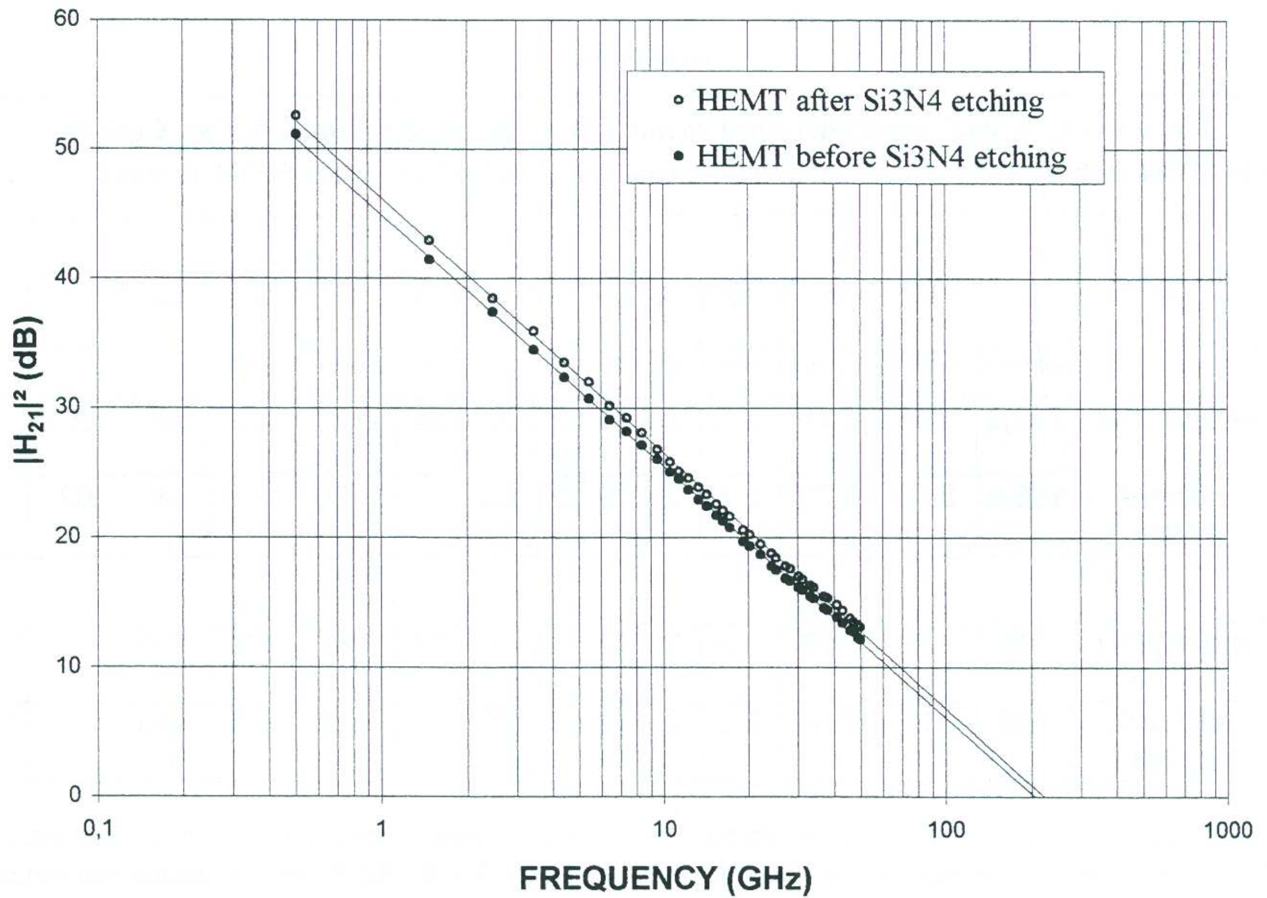
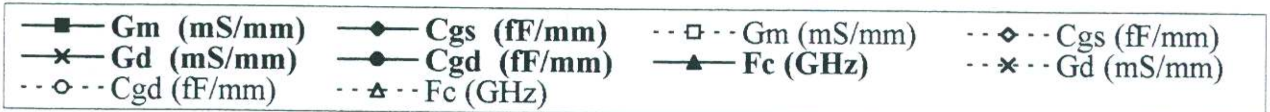


Fig.6. Extrinsic current gain cutoff frequency Ft for HEMT before and after Si3N4



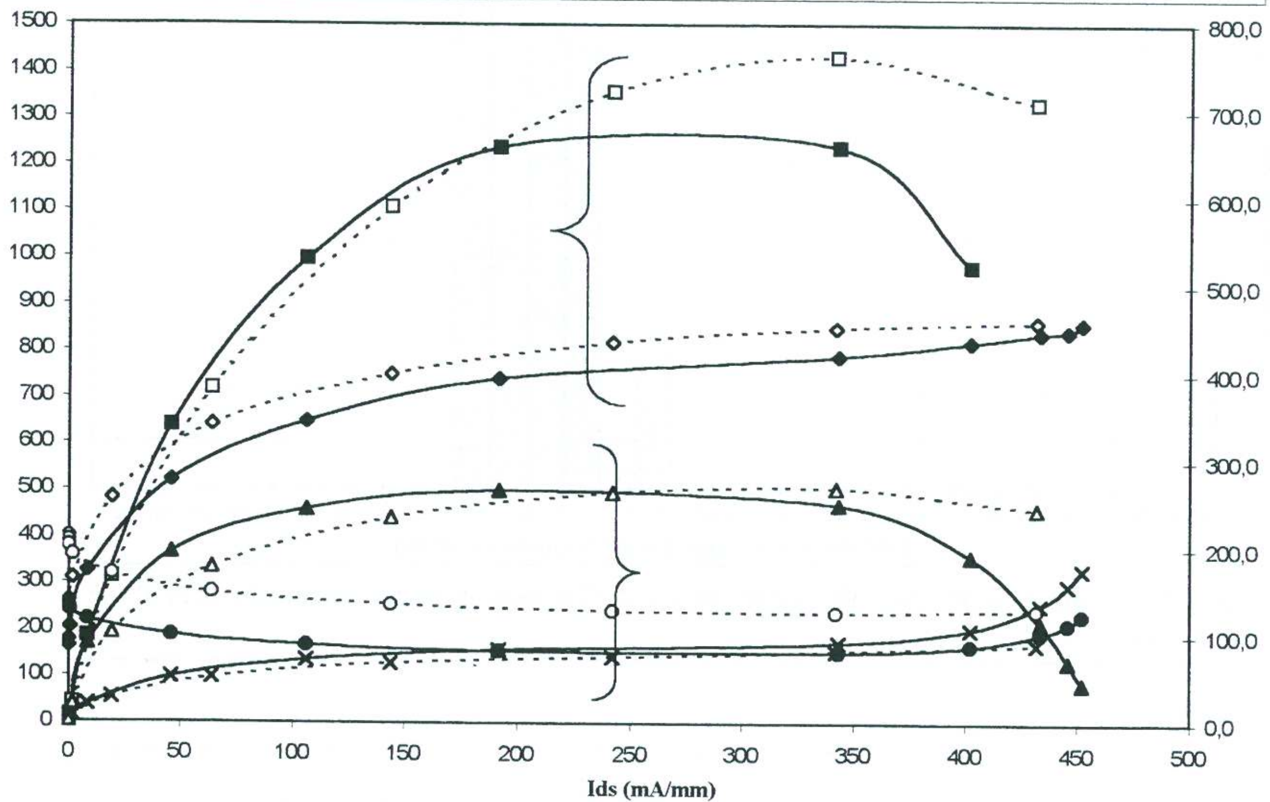


Fig.7. Elements of the small signal equivalent circuit (-■-×-●-◆-▲-) **Gm, Gd, Cgs, Cgd, Fc after Si3N4 etching** and (-□-×-○-◇-△-) Gm, Gd, Cgs, Cgd, Fc before Si3N4 etching.

	type	Ids	Rs	Rd	Rg	Cpg	Cpd	Ls	Ld	Lg	Gm	Gd	Cgs	Cgd	Fc
dim		mA/mm	ohm.mm	ohm.mm	ohm	FF	fF	pH	pH	pH	mS/mm	mS/mm	fF	fF	GHz
2x25 µm	**with Si3N4**	**342,0**	0,28	0,28	2,3	2	13	2	25	25	1430	82	848	126,6	268
2x25 µm	**without Si3N4**	**192,0**	0,36	0,33	2,3	2	10	2	25	25	1236	83,4	740	82	266
2x25 µm	**with Si3N4**	**100**	0,28	0,28	2,3	2	13	2	25	25	925	60	700	140	210,42
2x25 µm	**without Si3N4**	**100**	0,36	0,33	2,3	2	10	2	25	25	975	65	640	90	242,59

Table1. Elements of the small signal equivalent circuit (Vds=1V). Rs,Rd,Rg are the access resistances, Cpg and Cpd the pad capacitances, Ls,Lg,Ld the parasitics inductances while Gm, Gd, Cgs and Cgd are the usual intrinsic small signal elements.