A MONOLITHIC TEMPERATURE COMPENSATED 1.6 GHz VCO

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ABSTRACT

A temperature compensated fully integrated 1.6 GHz harmonic VCO with GaAs E/D-MESFET technology has been designed for telecommunication applications. The circuit has a measured tuning range of over 400 MHz and it shows a good tuning linearity in the range of 1600 - 1700 MHz. With the proposed temperature compensation scheme the measured frequency drift is reduced from 36 MHz to less than 8 MHz in the temperature range of -20 ...+70°C.

INTRODUCTION

In this paper a monolithic fully integrated voltage-controlled oscillator based on the well-known common-gate Colpitts configuration is presented. The circuit is meant for sub-2 GHz telecommunication applications and its features are large tuning range, low supply voltage and high output power. The inductive portion of the resonator is partly external thus enabling wide selection of operation bands. During the design project the temperature stability of an ordinary monolithic LC-oscillator was observed to be unacceptably poor. Therefore, we developed a simple method for internal temperature compensation. Significant reduction on the temperature sensitivity of the oscillation frequency is achieved with the proposed method.

BASIC OSCILLATOR

A common-gate Colpitts oscillator is shown in Figure 1. The circuit includes an oscillating FET, an LC-resonator and a bias resistor. The feedback loop utilizing the reactive divider C_f-C_v generates negative resistance $R_{neg} = -g_m/(\omega^2 C_v C_f)$. If we use a simple small-signal model for the transistor including a transconductance g_m, an output conductance g_o and a gate-source capacitance C_{gs}, and the inductor has a series resistance R_{ind}, we can find the characteristic matrix Y of the circuit. For an oscillator case, the determinant of the characteristic matrix must be equal to zero to ensure the existence of non-trivial solutions, thus $|Y| = 0$. Solving this equation, we may derive formulas for the oscillation frequency ω_0 and the required transconductance. Slightly simplified and embedding C_{gs} into C_v, they can be expressed as

$$\omega_0 = \sqrt{\frac{1}{LC_{eff}}}, \quad \text{where } C_{eff} = \frac{C_f C_v}{C_f + C_v} \tag{1}$$

$$g_m > \frac{C_f}{C_v}\frac{1}{R} + g_o\frac{C_v}{C_f} + \frac{1}{R_{ind}}\left(2 + \frac{C_f}{C_v} + \frac{C_v}{C_f}\right) \tag{2}$$

The second equation gives some guidelines how to design the oscillator. First of all, we can compare the three terms in Eq. 2 and note that the first one is insignificant, while the second term depends on the bias point and the third one is usually dominant. Output conductance increases with the bias and therefore the bias point should be low. A low bias point will also reduce phase noise. However, a low bias point implies that a large device with a large C_{gs} will be used and because C_{gs} is in parallel with the varactor diode C_v, the tuning range is somewhat reduced. The ratio between the size of the varactor diode capacitance C_v and the feedback capacitance C_f plays a major role. Equation 2 indicates that one should keep the ratio near to one to minimize the required transconductance. However, the tuning range is also affected by this ratio. Hence, there is a trade-off between the tuning range and the transconductance requirements.

TEMPERATURE COMPENSATION

The basic idea of the temperature compensation is to apply temperature dependent biasing to the oscillator and hence vary the operation point according to temperature. A small variation in the bias point of the oscillator causes a respective variation in the oscillation frequency. When properly designed this variation cancels out the natural temperature variation of the oscillation frequency, which is mainly due to the variation of the capacitance of the varactor with temperature. In our approach the bias resistor in the basic oscillator circuit is replaced with a transistor acting as a tunable current sink, and a temperature dependent bias voltage is connected to the gate of the transistor. Three alternative approaches for generating temperature dependent voltage V_{temp} are shown in Figure 2. The circuits A and B utilize DFETs, while the third one includes EFETs. All the circuits generate linearily temperature dependent voltage. With a 3-V supply the V_{temp} variation in the temperature range of -20 ...+70°C is less than 10 mV for the circuit A, less than 100 mV for the case B and eventually in the EFET case it exceeds 400 mV. In addition, with DFETs in the cases A and B only one design parameter, the ratio of the channel widths of the DFETs, is available, while in the EFET case designer may also vary the bias point of the lower FET. This additional design parameter somewhat alleviates the design procedure for the desired characteristics. The current consumption is also slightly lower in the EFET case, although in our circuit the current consumption of the temperature compensation circuit is insignificant compared to the amount of current consumed in the amplifier stages.

COMPLETE CIRCUIT

The entire VCO circuit consists of the temperature compensation circuit, the oscillator and a buffer-amplifier as depicted in Figure 3. The oscillator itself consists of an integrated inductor, an oscillating FET, a current source, and a series connection of a feedback capacitor, a bypass capacitor and a varactor. The varactor is built up from a MESFET with the drain and the source connected together. Unfortunately, this Schottky-diode varactor has quite a limited capacitive tuning range, and the strongly non-linear series resistance further limits the useful range as illustrated in Figure 5. The entire tuning range of the varactor is 8.3:1, but only 1.8:1 at the low loss region. Due to process variations, part of the inductance has to be external for post-process tuning of the center frequency. A short microstrip is adequate for the purpose. On the other hand, the external part of the inductance enables wide frequency range, and the circuit operates at 1 - 2 GHz range with different settings of the external inductance. The upper limit is set by the internal inductor and the inductance of the lead and the bond wire, altogether about 4 nH. The lower limit is not precise and the circuit oscillates at least at 0.5 GHz. However, as the buffer-amplifier is AC-coupled the output power remains low, and hence the circuit is not useful below 1 GHz. The voltage generated in the temperature compensation circuit is further inverted for achieving an appropriate slope. The temperature compensation circuit has an additional bias point for post-tuning, which can be used for achieving optimal performance, or if dramatic failure exist the compensation circuit can be externally disabled. This type of temperature compensation scheme essentially increases pushing (sensitivity of the oscillation frequency to the supply voltage level). A simple supply voltage regulating circuit was included to reduce the pushing figure. An buffer-amplifier is required to isolate the oscillator from the load and to deliver the desired output power. The requirements for the buffer-amplifier are high input impedance, high gain, high output power and good tolerance against process variations. The common-drain buffer has high input impedance for preventing excessive loading of the oscillator. The amplifier itself consists of an actively loaded common-source stage with a self-regulating DC operating point, and a common-source

stage with an inductive load. The latter is required for +10 dBm output power from a 3-V supply. The dual supply voltage and grounding scheme was applied to avoid nasty feedback effects caused by the package parasitics. We utilized the package model presented in [1] for SOIC-8 package in our work. The package model was included in the design from the very beginning since this type of cheap plastic package with poor high frequency characteristics has severe effects on the circuit performance. Each lead and the corresponding bond wire have a total inductance of about 2 nH. The die photograph is presented in Figure 4. The layout is not very dense, because the size of the die, 1 x 2 mm^2, was fixed in the beginning of the project and therefore we were able to make a spacious layout.

EXPERIMENTIAL RESULTS

Five oscillator variants were processed with the Philips Microwave ER07AD process, which is 0.7 μm MESFET process with both the depletion mode and enhancement mode transistors. The oscillator variants differ mainly by the structure of the core oscillator and they can be categorized briefly as follows: 1) EFET-core, internal inductor, no temp. compensation, 2) DFET-core, external inductor, no temp. compensation, 3) EFET-core, partly external inductor, no temp. compensation, 4) EFET-core, partly external inductor, internal temp. compensation, 5) EFET-core, internal inductor, internal temp. compensation. The circuit variants with internal inductors were measured on-wafer and the variants which required external inductors were bonded onto a PCB for measurements. All five variants operated as expected and on the basis of these measurements one of the variants, the circuit described earlier, was further packaged into the SOIC-8 package. The tuning characteristics of the circuit are shown in Figure 6 and the linear tuning range, specified in the design project, is shown in Figure 7. In Figure 8 the sensitivity of the oscillation frequency to temperature variation (-20 ... +70 °C) is plotted. The third oscillator mentioned above was used as a reference because it gives about the same performance characteristics as the VCO reported here. The frequency stability over the defined temperature range varied from 18 to 36 MHz depending on the tuning voltage for the uncompensated circuit. For the compensated circuit it was from 6 to 20 MHz. Finally, we used the possibility to externally tune the bias voltage. Simply a 0.3 V voltage with a 180 Ω source resistance was added to the bias node (see Fig. 3, label add.bias). With this post-tuning the frequency stability improved even more and it varied from 0 to 8 MHz. The performance characteristics of the VCO are summarized in Table 1.

CONCLUSIONS

In this work we have developed a temperature compensation scheme for an integrated high frequency LC-VCO. The measurement results indicate proper functionality for the entire circuit and show that significant improvement is achieved with the proposed temperature compensation technique. The limits for the usefulness of this approach are set by device model accuracy and process tolerances.

ACKNOWLEDGEMENT

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REFERENCES

[1] Ndagijimana et al.: The inductive connection effects of a mounted SPDT in a plastic SO8 package. IEEE MTT-S Symp. Dig. 1987, pp. 109-112.

Linear tuning range	1600-1700 MHz
Output power	+ 10 dBm
Distortion (THD)	-21 dBc
Frequency stability vs. temp.	8 MHz
Output power stability vs. temp.	1.5 dB
Temperature range	-20 °C...+ 70 °C
Pulling VSWR=1.67	5 MHz
Pushing Vdd±5%	5 MHz
Phase noise @100 kHz	-95 dBc/Hz
Supply voltage	3.5 V
Current consumption	100 mA

Table 1. The measured characteristics of the VCO.

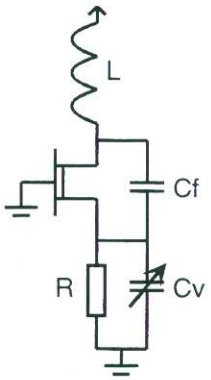

Fig.1. Common-gate Colpitts Oscillator.

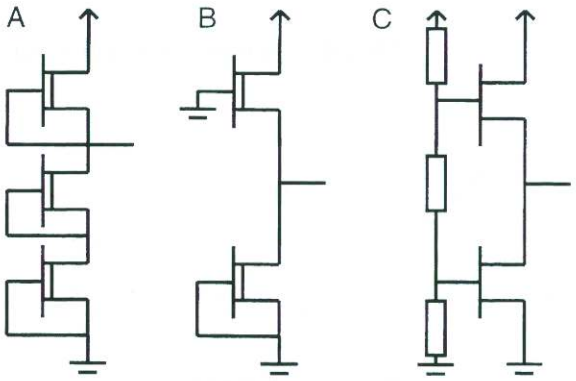

Fig. 2. Temperature dependent voltage generators; A & B are DFET-circuits and C is an EFET-circuit.

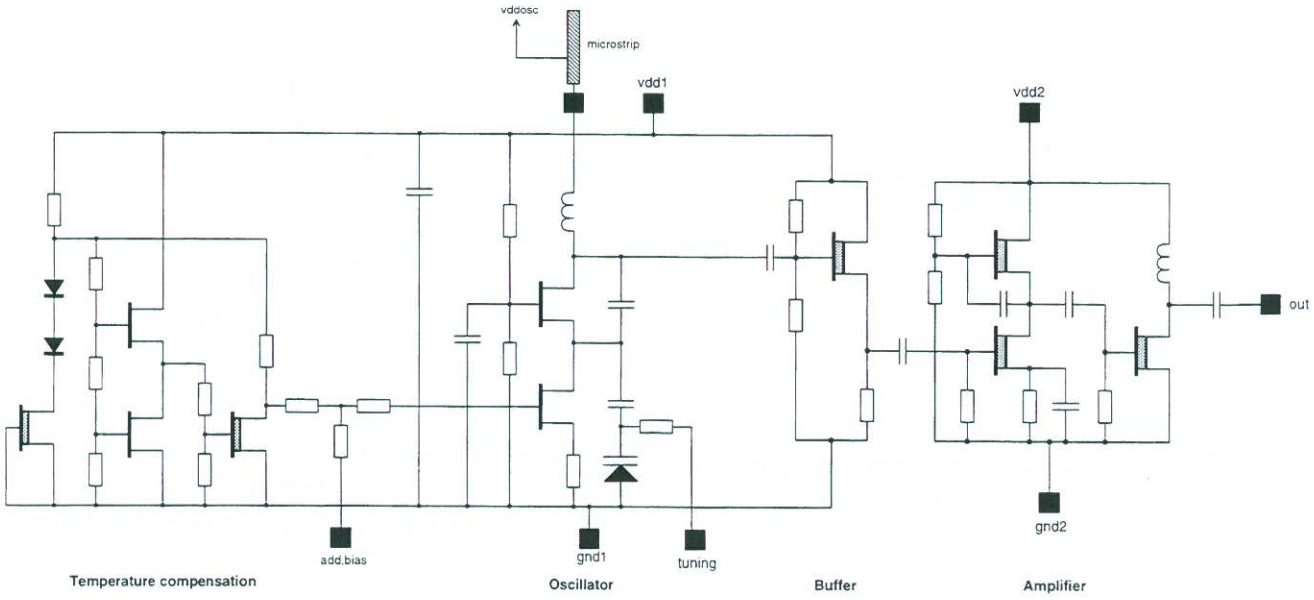

Fig 3. VCO circuit schematic. The black boxes indicate bonding pads (8-lead package).

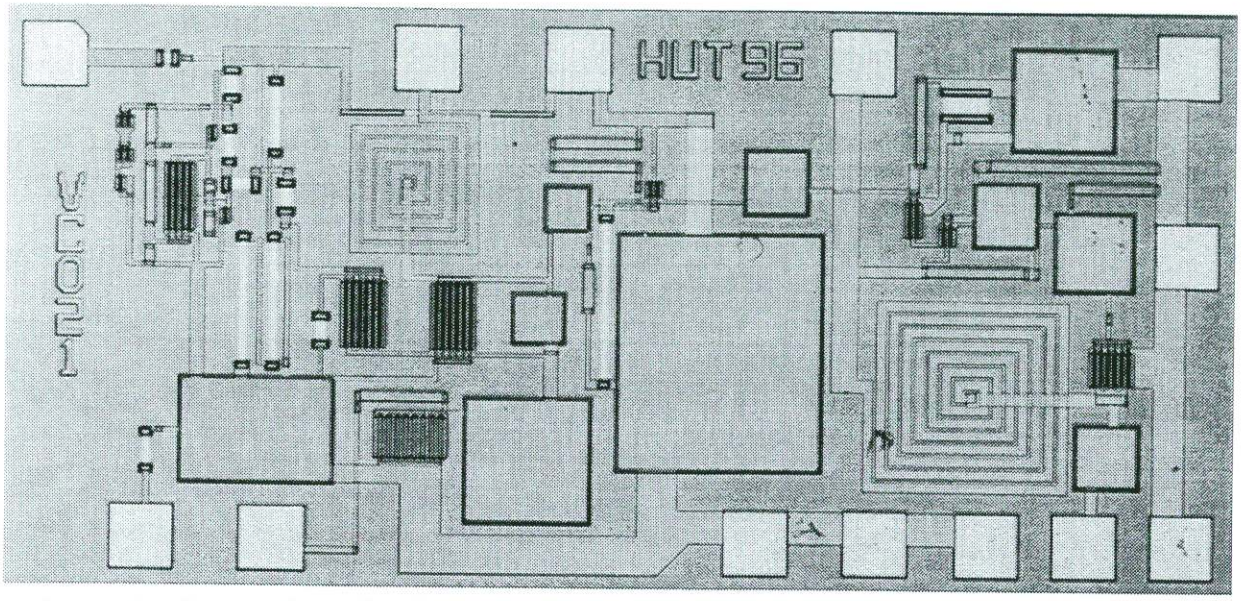

Fig. 4. Microphotograph of the VCO 1x2 mm^2 die.

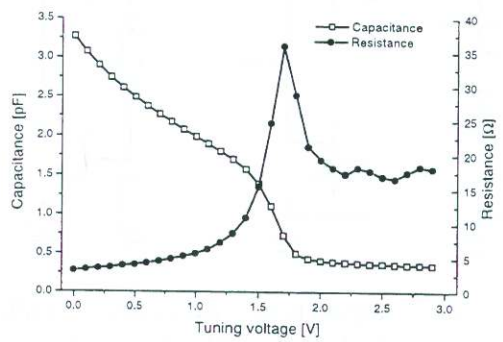

Fig. 5. Measured capacitance and series resistance of the varactor vs. tuning voltage.

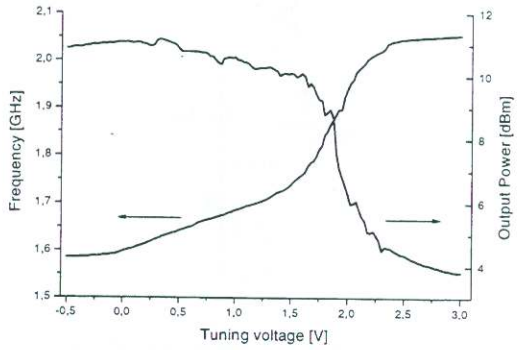

Fig. 6. Measured oscillation frequency and output power vs. tuning voltage.

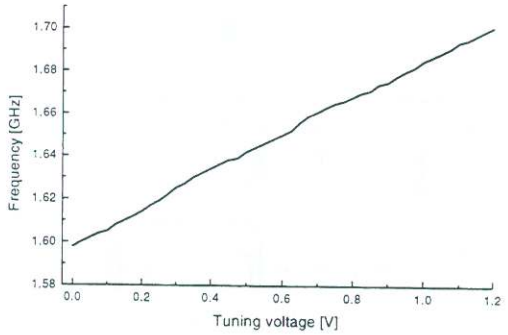

Fig. 7. Measured oscillation frequency vs. tuning voltage (linear tuning range).

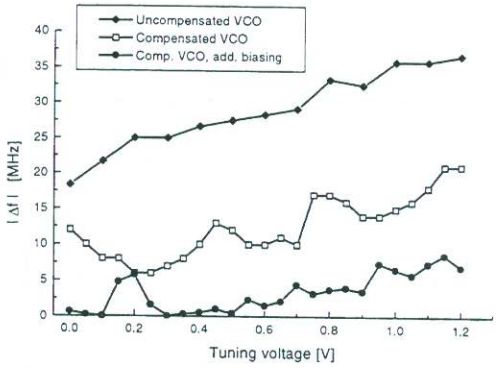

Fig. 8. Measured oscillation frequency drift due to temperature variation. Temperature range is -20 °C...+ 70 °C.