High Performance InP HBT Technology for Analog-to-Digital Conversion

Joseph F. Jensen, Gopal Raghavan, Bob Walden, and Bill Stanchina
HRL Laboratories, LLC, 3011 Malibu Canyon Road, CA 90265
Phone: (310) 317-5250 FAX: (310) 317-5450
E-mail: jfJensen@hrl.com

Abstract

The trend in modern communications and radar systems is to move the analog-to digital interface as far forward in the signal path as possible toward the antenna or sensor. Moving the digital interface forward in the signal path eliminates stages of downconversion and analog filtering that are bulky, expensive, drift with temperature, and require calibration. Ultra-fast device technologies are required to perform direct analog-to-digital conversion on radio frequency (RF) or intermediate frequency (IF) signals that enables moving the digital interface forward in the signal path. This paper describes the performance limits of current analog-to-digital converters (ADCs) and shows how the ultra-fast performance of InP HBT technology is extending the performance of ADCs to higher levels to enable all digital approaches to communications receivers.

Introduction

A typical receiver for digital communications is shown in Figure 1. A simplistic approach to a future all digital receiver is shown in Figure 2. This receiver digitizes the input signal at the antenna and performs all other receiver functions in software. Eliminating the analog functions of conventional receivers can significantly reduce the size, weight and cost for receivers in high end systems.

The challenge to implementing the receiver in Figure 2 is obtaining an ADC with performance capabilities that can meet the receiver requirements. An all digital receiver approach drives ADCs to high sample rates. A sample rate of twice the RF frequency is required to replace stages of down conversion based on Nyquist. High performance all digital receivers stress ADC fundamental limits. Ultra-fast IC technology will have a major impact in digital receiver technology. This paper will examine the impact of ultra-high speed InP HBT IC technology on ADCs and digital receivers.

InP HBT ADC IC Results

Figure 3 is a plot of sample rate versus effective number of bits (SNR) for a number of ADC reported in the literature over the past several years (1). Over 100 converters, including experimental ICs, and commercially available parts, are represented in the graph. Also shown on the graph are curves corresponding to various values of comparator regeneration times, thermal noise, and aperture jitter limits. As shown in the graph the current state-of-the-art is described by an aperture jitter of ~3ps and a regeneration time constant that corresponds to a value of f_T~50 GHz. To extend ADC performance to higher levels as required for digital receiver applications we have fabricated ADCs using InP HBT IC technology with a variety of ADC architectures.

As a demonstrator we developed a 3-bit flash ADC in our InP HBT IC technology (2). A die photo of the ADC is shown in Figure 4. The circuit contains approximately 900 transistors and has a die size of 2.2 mm x 2.7 mm. The power dissipated (including testing functions) is 3.5 W. The converter demonstrated an SNR equal to 18.1 dB (2.71 ENOB) up to a clock rate of 12.7 GHz for a low input frequency sinewave (27 MHz). The SNR is found to be 16.1 dB giving an effective number of bits equal to 2.4 bits for Nyquist testing up to a sampling rate of 8 Gsamples/sec.

Linearity of multibit quantizers are limited by accuracy of voltage thresholds which are determined by the uniformity of the process technology used in ADC fabrication. We can increase the resolution of a single bit ADC by using oversampling. Since the quantization noise of a Nyquist ADC is uniformly spread from 0 to Fs/2, oversampling (averaging) can improve the SNR by 3dB (0.5 bits) for every doubling of the clock rate. Using this technique, however, requires very high oversampling rates. For example, to achieve 10 bit resolution on a 50 MHz signal with a single bit ADC requires a 12.5 THz sample rate. A more practical solution to oversampling with a single bit ADC is to add a loop filter inside a feedback loop. This is the basic concept behind delta-sigma modulation.

Delta-sigma ($\Delta\Sigma$) modulation has become the method of choice for high-resolution analog-to-digital conversion. The primary advantage of the delta-sigma approach is the ability to achieve high resolution without a complicated fabrication process or active trimming techniques. These converters also simplify system integration by reducing the burden on supporting analog circuitry. Specifically, they do not require precision sample-and-hold circuitry and they relax performance requirements on the analog anti-alias filter that precedes the sampling operation. The purpose of $\Delta\Sigma$

modulators is to trade higher sampling speed (i.e., higher f_S) for obtaining higher resolution (3). For example, a 2nd order low pass ΔΣ modulator achieves a 15-dB reduction of the baseband quantization noise for each doubling of f_S.

We have also demonstrated a 2nd order ΔΣ modulator in InP HBT IC technology (4). We use continuous-time Gm-C fully differential circuitry to implement the 2nd order ΔΣ modulator. Figure 5 shows a die photo of the InP HBT 2nd order ΔΣ modulator. The chip operates from ± 5 V supplies and dissipates 1 W. At a sample rate of 3.2 GHz and a signal bandwidth of 50 MHz (OSR of 32 and 100 MSPS Nyquist rate) the modulator demonstrates a SFDR of 71 dB (12-bits dynamic range and the ideal signal-to-noise ratio of 55 dB for a second-order modulator at an oversampling ratio of 32. For an oversampling ratio of 256, the modulator achieves a peak SNR of 70 dB.).

Bandpass ΔΣ modulation tunes the region of surpressed quantization noise from DC to IF by replacing the integrators in conventional ΔΣ modulators with a bandpass filter. The primary motivation of bandpass converters is the simplicity they impart to systems dealing with narrow-band signals. The use of a bandpass ΔΣ modulator permits a direct conversion of an analog signal to digital form at IF for RF communication and radar systems.

Figure 6 shows the architecture of our fully differential realization of a second order 1-bit output bandpass ΔΣ modulator [5], which is an extension of the design in [4] and is similar to the architecture proposed by Shoaei and Snelgrove (6). The performance of this architecture is determined primarily by the Q of the resonator used in the feedback loop. The major changes from the architecture described in [6] are the insertion of tunable transconductance (g_m) cells in the feedback path of the resonator, inclusion of an extra half clock cycle delay following the comparator and use of current-mode logic in the design. The first of these changes permits the resonator center frequency to be varied from DC to a maximum designed value. The extra half clock cycle delay following the comparator results in matched output rise and fall times which allows us to use a NRZ DAC. The use of current-mode logic reduces switching noise and also eliminates the requirement for high gain operational amplifiers in the design. Figure 7 is a micrograph of the die containing the modulator and a 1:16 DEMUX. The modulator is located in the bottom right hand corner of the die. The modulator measures 750 μm x 750 μm and dissipates 1.4 W. The 1-to-16 DEMUX dissipates 0.5 W, and the 16 ECL output buffer dissipate 2 W.

Measurements on this bandpass modulator yield SNR values ranging from 89 dB over a 366 kHz bandwidth to 42 dB over a 62.6 MHz bandwidth. Figure 8 shows the output spectrum for various center frequencies and demonstrates notch tunability. A peak SNR of 84.9 dB, 81.2 dB and 80.5 dB was obtained corresponding to notch positions of 62.5 MHz, 41.4 MHz and 24.4 MHz respectively.

Conclusions

The trend in modern communications and radar systems is to move the analog-to digital interface as far forward in the signal path as possible toward the antenna or sensor. Ultra-fast device technologies are required to perform direct analog-to-digital conversion on radio frequency (RF) or intermediate frequency (IF) signals that enables moving the digital interface forward in the signal path. We have demonstrated an 8 GSPS 3-bit flash ADC, a low pass 2nd order ΔΣ modulator sampling at 3.2 GHz producing 70 dB dynamic range for 50 MHz signal bandwidth, and 4 GSPS sample rate 2nd order bandpass ΔΣ modulator producing SNR values ranging from 89 dB over a 366 kHz bandwidth to 42 dB over a 62.6 MHz bandwidth centered at an IF of 60 MHz. The ultra-fast InP HBT technology demonstrated in this work has established the feasibility for all digital receivers.

References

1. R.H. Walden, "Analog-to-Digital Converter Technology Comparison," Technical Digest, GaAs IC Symposium, 1994, pp217-219.
2. C. Baringer, J. Jensen, L. Burns, B. Walden, "3-bit, 8 GSPS Flash ADC," 1996 Indium Phosphide and Related Material Technical Digest, pp. 64-67.
3. J.C. Candy, G.C. Temes, "Oversampling Methods for A/D and D/A Conversion," IEEE Press Collection of Papers, "Oversampling Delta-Sigma Data Converters Theory Design and Simulation," 1992, pp 1-25.
4. J.F. Jensen, G. Raghavan, A.E. Cosand and R.H. Walden, "A 3.2-GHz Second-Order Delta-Sigma Modulator Implemented in InP HBT Technology," IEEE J. Solid State Circuits, Vol 30, No. 10, October 1995, pp. 1119-1127.
5. G. Raghavan, J.F. Jensen, R.H. Walden, W.P. Posey, "A Bandpass ΔΣ Modulator with 92 dB SNR and Center Frequency Continuously Programmable from 0 to 70 MHz," 1997 ISSCC Technical Digest, pp. 214-215
6. O. Shoaei and W.M. Snelgrove, 1994 IEEE Symposium on Circuits and Systems, Vol. 5, Pg. 489.

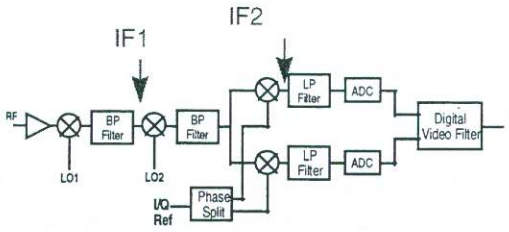

Figure 1. A conventional analog I/Q digital communication receiver.

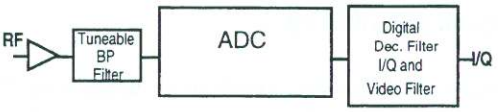

Figure 2. An all digital implementation of a communications receiver.

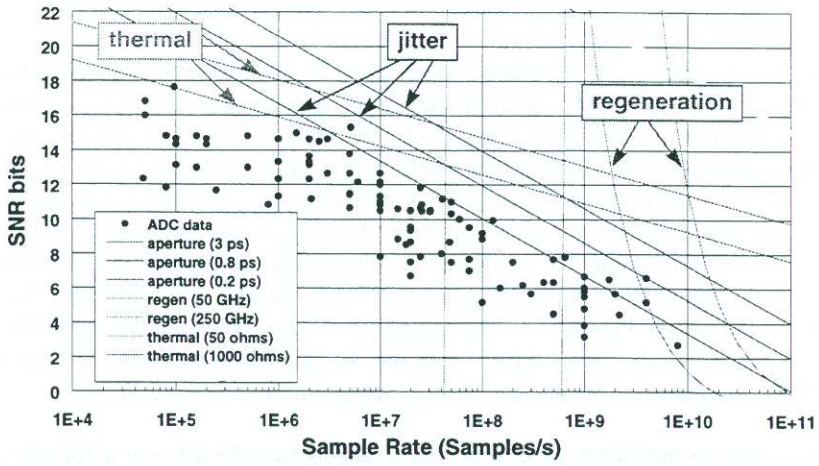

Figure 3. Survey of ADCs as a function of SNR bits and ADC limitations.

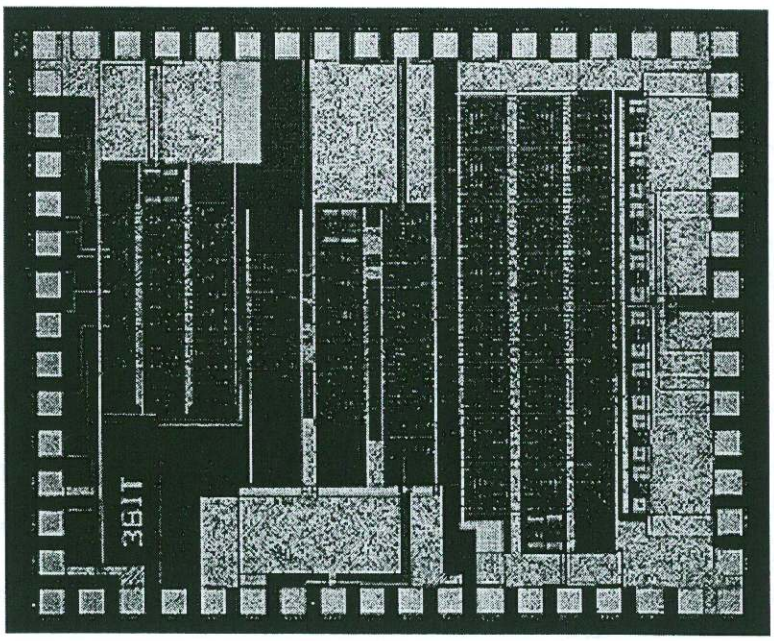

Figure 4. Die photo of 3-bit flash ADC implemented in InP HBT IC technology.

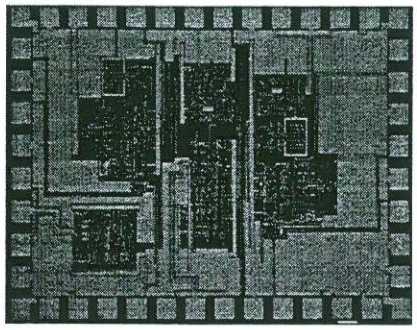

Figure 5. Die photograph of the InP HBT 2nd order ΔΣ modulator.

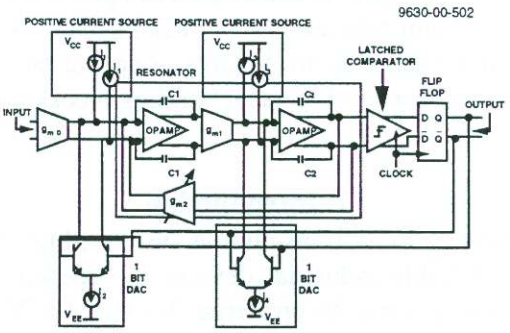

Figure 6. The architecture of a fully differential realization of a second order 1-bit output bandpass ΔΣ modulator.

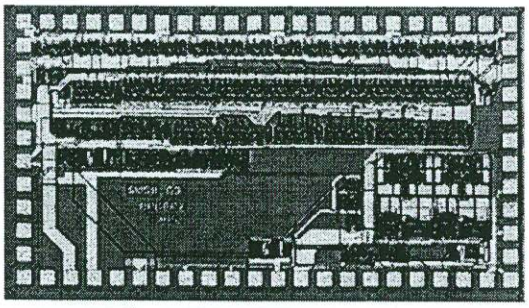

Figure 7. A photograph of the InP HBT bandpass ΔΣ modulator and a 1:16 DEMUX.

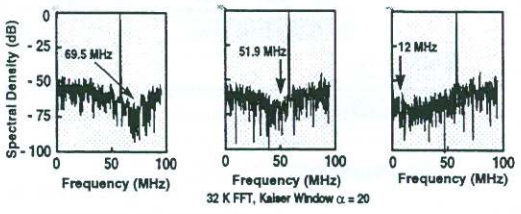

Figure 8. The output spectrum of the tunable 2nd order bandpass ΔΣ modulator for various center frequencies.