

CHARGE INJECTION E/D MESFET STRUCTURES FOR HIGH SPEED AND LOW POWER APPLICATIONS

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ABSTRACT

In this paper new dynamic charge injection E/D logics are presented and compared with traditional dynamic ones such as TDFL (Two Phase Dynamic Fet Logic). The main drawbacks of TDFL will be analyzed together with the advantages offered with respect to the static DCFL based topologies; a tentative structure has been derived (MTDFL - Modified TDFL) to comply with the VLSI requirements; then the advantages of the charge injection principles applied to the design of new logic topologies are inspected and used in a pseudo complementary structure (PCDL - Pseudo Complementary Dynamic Logic). The results of the simulations for these structures are presented together with the design of a 4-bits pipelined adder simulated at 2 GHz with a power dissipation 20 times lower than a DCFL implementation.

INTRODUCTION

For silicon VLSI circuits, the use of dynamic logics allows a drastic reduction of area and power dissipation of highly pipelined digital structures; also for GaAs digital circuits some experiments have been carried out to obtain a reasonable trade off among area, speed and power. In fact the use of Gallium Arsenide technology in the past was restricted by power dissipation problems that limited the complexity of the implemented architectures. Dynamic structures such as the TDFL logic overcome [1] this problem and introduce great advantages in the implementation of pipelined structures [2]. Using this technique each logic level has an associated latching function, therefore the critical paths are reduced with respect to traditional design styles as DCFL and pipelining is obtained with no additional cost.

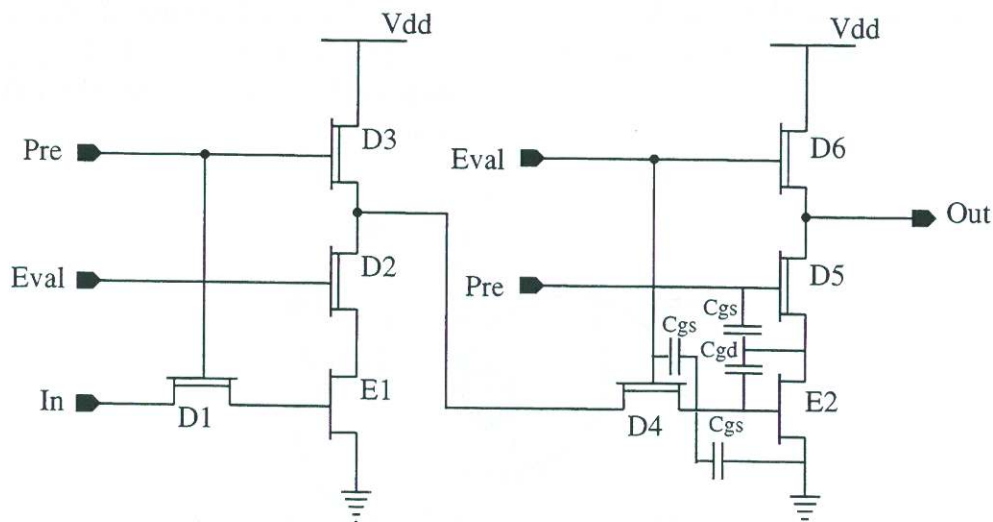


Figure 1: TDFL cascaded inverters: the most significative capacitances are drawn on the second inverter

The TDFL, developed by Nary and Long in 1992, is based on the structure of figure 1 and has been presented as a very low power dissipation logic. It is based on E/D MESFET devices: three depletion transistors (D1,D2,D3) and an enhancement one (E1) constitute the basic self latching inverter. Each basic structure has two phase clocks acting as precharge and evaluation signals. During the precharge, the output is tied to VDD

(0.7 V) while the gate of E1 follows the input signal In . During the evaluation phase, D1 and D3 become non conducting and the precharged output can be discharged only if the data stored on the gate of E1 is high.

The main problem of this topology is related to the low fan out that reduces the designing capabilities. If a TDFL inverter is connected to drive n others TDFL gates, the charge on the output node is transferred to the input capacitances of the driven gates. This *charge sharing* mechanism degrades the output level proportionally to the number of driven gates. A possible solution could be to increase the power supply voltage but the output node high voltage cannot exceed 0.6 V due to the leakage current at the E2 gate-source junction [3]. This is quite evident in the second ($V(DUTin)$) and third ($V(DUTout)$) waveforms of figure 2 where, while V_{DD} rises to 1.5 V, the output high voltage at the end of the Evaluation phase is not higher than 600 mV due to the leakage current of E2. The situation is even worsened by the increase of fan-out (the signal $V(DUTout)$ drives 4 loads while $V(DUTin)$ drives a single load). The first waveform ($V(E2gate)$) represents the voltage on the gate of the enhancement MESFET.

A further problem of the TDFL structure is related to the *charge injection* mechanism that arises when two gates are cascaded: the circuit works properly only if the two phases (*Eval* and *Pre*) exchange their functions in consecutive gates. In this way, with the "transmitter" in the evaluation phase, the "receiver" is precharging its output and is transparent on its input. When the "transmitter" is precharging its output, the "receiver" is evaluating the data sampled during the previous phase. In more details, when the phase *Eval* has a transition from high to low the transmitter goes from evaluation to precharge phase and the receiver from precharge to the evaluation; on the gate of the transistor D4 there is a falling edge of the *Eval* phase signal but its coupling with the transistor E2 by means of the intrinsic capacitances C_{gs} creates a voltage drop on the memory node (the gate of E2) and degrades the logic level. The voltage drop can be estimated through the following equation:

$$V_{drop} \approx (V_{HI} - V_{LO}) \frac{C_{gsD4}}{C_{gsD4} + C_{gsE2}}$$

where $V_{HI} - V_{LO}$ is the range of the Eval phase; moreover the expression neglects the contribution of C_{gdE2} .

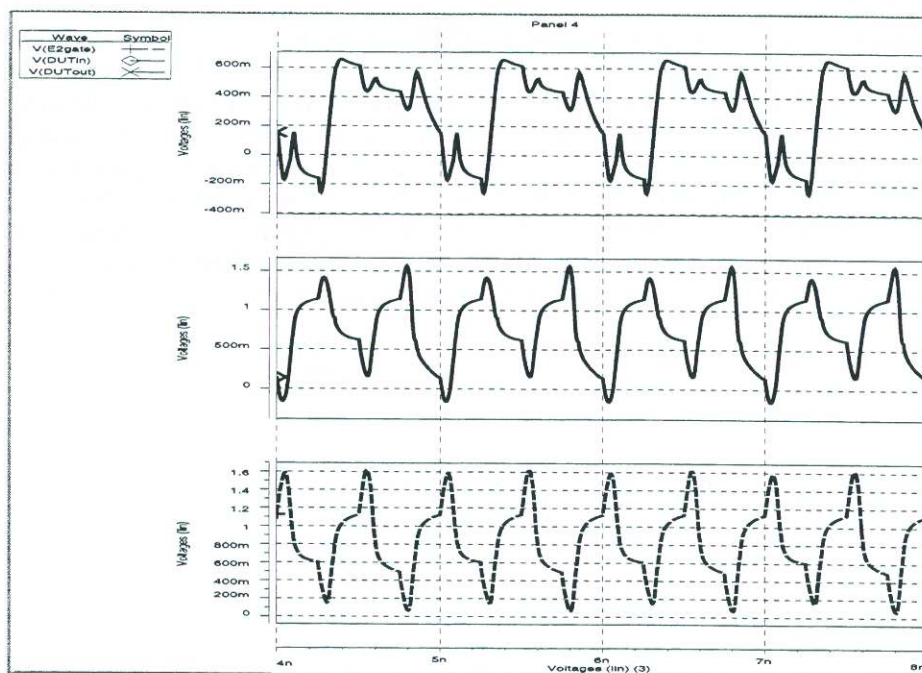


Figure 2: TDFL simulation with the voltage drop

The voltage drop problem can be partially solved by the charge injection mechanism from transistors D5 through E2. This compensation technique to be effective requires the increase of the width of E2 furtherly reducing the fan out of the gate.

MODIFIED TWO PHASED DYNAMIC LOGIC - MTDFL

The increasing of E1 in figure 1 is limited by the fan out reduction due to the charge partitioning of the output voltage on the C_{gs} of E1 transistor; on the other hand the voltage drop related to the *Eval* edge can represent a strong limitation to the reliability of the TDFL. One way to overcome this problem is to modify the input sampling mechanism: the input D transistor can be coupled with an enhancement device producing a compensating effect quite similar to the transmission gate (Charge Compensated Pass Transistor - CCPT), as shown in figure 3. Differently from the CMOS structure, the E MESFET never becomes conducting but acts only as a charge compensating device: since the *Eval* and *Pre* phases are complementary, during the rising edge of *Pre* there is a simultaneous falling edge of *Eval* signal therefore the charge injected through C_{gsD1} can be partially extracted by C_{gsE1} . In this way a large E2 is not necessary to minimize the voltage drop. To obtain the best results the two capacitances must be matched and for this reason the transistor D1 must be larger than E1 since its C_{gs} capacitance is lower for unit of width. During the hold phase it is mandatory that E1 never conduct; as a consequence, if V_{MAX} and V_{MIN} are the high and low input voltage to be sampled, the following equations must be verified:

$$\begin{aligned} V_{HI} &< V_{MIN} + V_{TE} \\ V_{HI} &> V_{MAX} - |V_{TD}| \\ V_{LO} &< V_{MIN} - |V_{TD}| \end{aligned}$$

where V_{HI} and V_{LO} are the levels of the phase signals and V_{TE} , V_{TD} are respectively the threshold voltages for the enhancement and depletion MESFETs. The first equation guarantees that the enhancement is always non conducting, the second one must be verified to transmit the V_{MAX} without any voltage degradation through the DFET; the last equation is required to isolate the load during the hold phase. In the E-D processes the values of V_{TD} and V_{TE} are spread so requiring that the previous equations must be verified in the worst case (minimum V_{TE} and maximum V_{TD}). These considerations led to select a V_{HI} equal to 0.2 V and V_{LO} equal to -1.2 V. E2, D2 and D3 act as a standard output TDFL stage, but with an increased fan out (5 gates) and this allows the logic synthesis of the most relevant VLSI structures. Figure 4 reports the test structure used for simulations. The D.U.T. is a latched inverter driven by another MTDFL device. The load circuit is a CCPT followed by a standard DCFL inverter. This solution has been adopted to prove the feasibility of a merged scheme (dynamic and static logic). The results of the simulations are shown in figure 5 where the Monte Carlo method has been used to verify the robustness of the scheme to the spreading of threshold voltages. In more details, $V(TP1)$ is the input of the DUT, $V(TP2)$ is the value stored in the transmission gate before the TDFL and $V(Pre)$ is one of the phase signals. It is possible to note that the differences in the threshold voltages do not affect significantly the waveforms, making the logic insensitive to technology parameters variation.

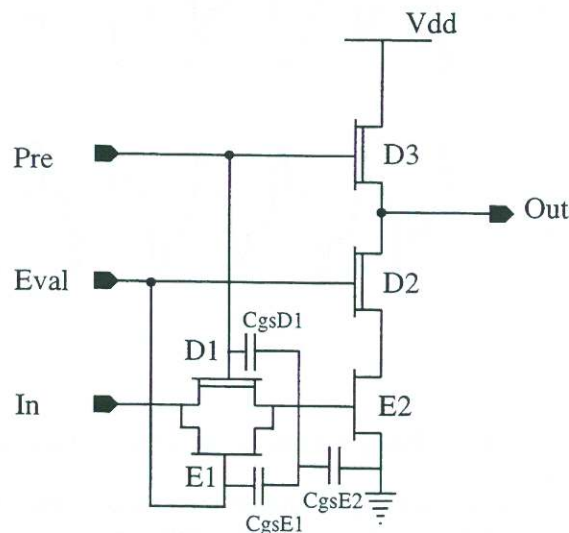


Figure 3: MTDFL: basic scheme

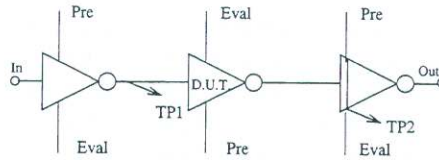


Figure 4: Basic test scheme of MTDFL: the driver and the DUT are MTDFL while the load is TDFL stage with a CCPT input stage

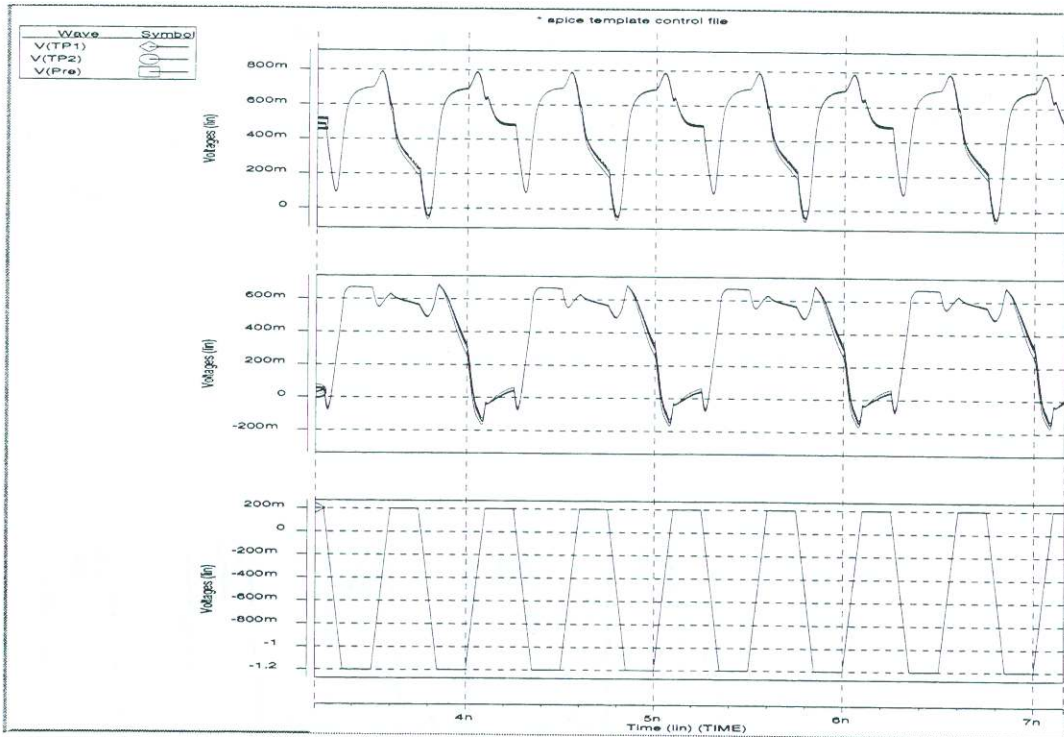


Figure 5: Simulation of MTDFL with Monte Carlo method; input to DUT gate, output of “transmission gate” before TDFL load stage and phase signals are reported

PSEUDO COMPLEMENTARY DYNAMIC LOGIC - PCDL

The intrinsic limitation of TDFL in terms of fan out logic levels and power dissipation can be overcome by introducing pseudo complementary schemes [4, 5]. The basic idea of the scheme in figure 6-a is to connect two TDFL gates (D3, D2, E1 and D5, D4, E2) active on the same phase in order to generate complementary signals (for more complex functions only the transistor E1 must be replaced with an appropriate network) to be used for driving the output totem pole structure that buffers the output. The transistors D6 and D7 decouple the output stage from the input: when the two input stages are in evaluation phase, E4 and E3 are driven by complementary signals. During the falling edge of the evaluation phase the gate of the output transistors (E3, E4) are completely discharged by the charge injection mechanism disconnecting the output node. The main advantage of this solution is the driving capability of the output: the totem pole structure can drive, during the evaluation phase, a larger number of loads depending only on the dimensions of E4 and E3, since the charge sharing mechanism that weakens the TDFL is overcome. The main drawback of this topology is the number of transistors, increased with respect to the TDFL, but some simplifications can be adopted in order to simplify the scheme maintaining the original properties. Moreover, the nodes A and B are both high at the end of the precharging phase and E3 and E4 are conducting at the same time so degrading the power dissipation figures. It can be noticed that when the gate comes out of the evaluation phase, the drain of the transistor E1 is discharged by the C_{gs} of D2; as a consequence the gate of E2 can be connected directly to the drain of E1

since, during the precharge phase, E2 will be always disconnected. A further advantage of this solution is that D4 is useless and can be dropped, since E2 grants to disconnect the node B from ground during the precharge phase. D6 and D7 have been inserted to disconnect the output totem pole during the precharge phase but the same behavior can be obtained connecting directly the gate of E3 to the drain of the transistor E1; also D6 can be therefore eliminated even if the output high level is slightly reduced with respect to the basic scheme where the rising edge of *Eval* injecting charge in the gate of E3 rises its voltage and therefore the output that is one V_T lower. Figure 6-b shows the resulting topology.

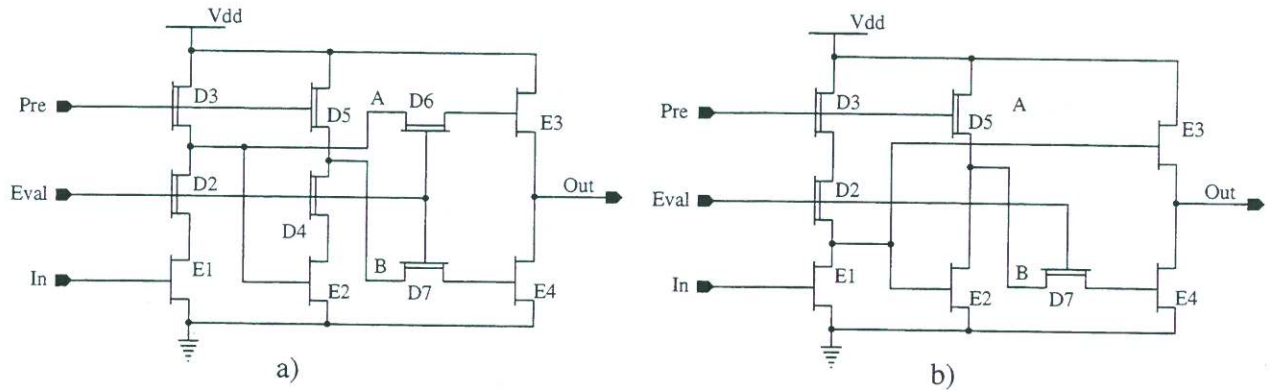


Figure 6: PCDL: basic scheme a) final scheme b)

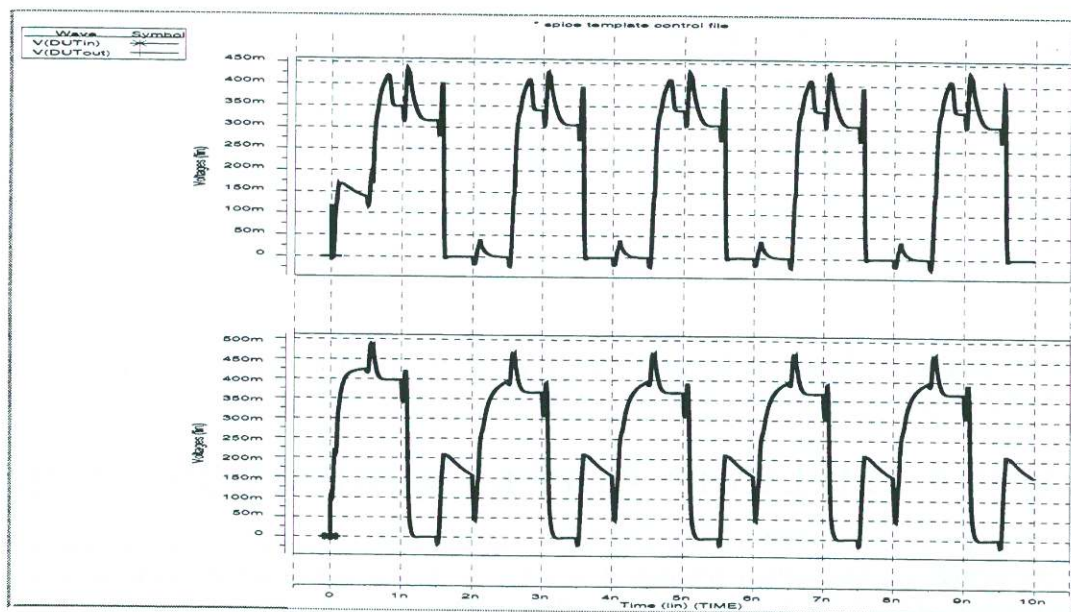


Figure 7: Simulation of PCDL logic: output of the driving device and output of the DUT circuit

From HSPICE simulations the PCDL shows the right behavior up to 2 GHz with a power supply voltage of 0.7 V with V_{OH} level of 450 mV and V_{OL} of roughly 100 mV when the fan-out is limited to two.

These conditions cannot be reached by standard TDFL. Power dissipation is reduced from 20 nW/MHz to 4 nW/MHz for a single gate, nonetheless the fan out increases up to 8 logic gates. In this case the output level range is reduced (170 mV - 340 mV). The simulations refer to a Vitesse E/D process where all the MESFET dimensions are $1 \times 0.8 \mu\text{m}$. The DUT is driven by another CPDL gate and is loaded by other 4 gates. The $V(\text{DUTin})$ is obtained by an input square wave at 1 GHz; it is possible to note the degradation of the output levels $V(\text{DUTout})$ due to the higher fan-out.

CONCLUSIONS

The basic cells of the new dynamic logics have been designed and simulated in order to demonstrate the feasibility of complex VLSI structures. A prototype test circuit with a 4-bit pipelined adder has been designed and it is now under fabrication. The same structure has been designed with a traditional DCFL logic in order to compare the main design parameters (table 1 shows the main parameters for the adder, without considering the preskew and deskew chains). It is worth noting that the power dissipation of the MTDFL logic is more than twenty times lower than the DCFL one.

The layout of the MTDFL block is reported in figure 8. The approach followed for the layout synthesis is standard cell based; the basic cells dimensions are $12.5 \times 20 \mu\text{m}$ and the total power dissipation is 151 nW/MHz/bit . The simulations show that the adder works properly up to 2 GHz.

PARAMETER	DCFL	MTDFL
V_{dd}	0,6 V	0,6 V
Gates	129	76
MOS	390	560
f_{MAX}	1,16 GHz	2 GHz
P_{MAX}	$3,73 \mu\text{W/MHz/bit}$	151 nW/MHz/bit

Table 1: Comparison of a 4 bit adder using TDFL and MTDFL (preskew and deskew chains are not considered)

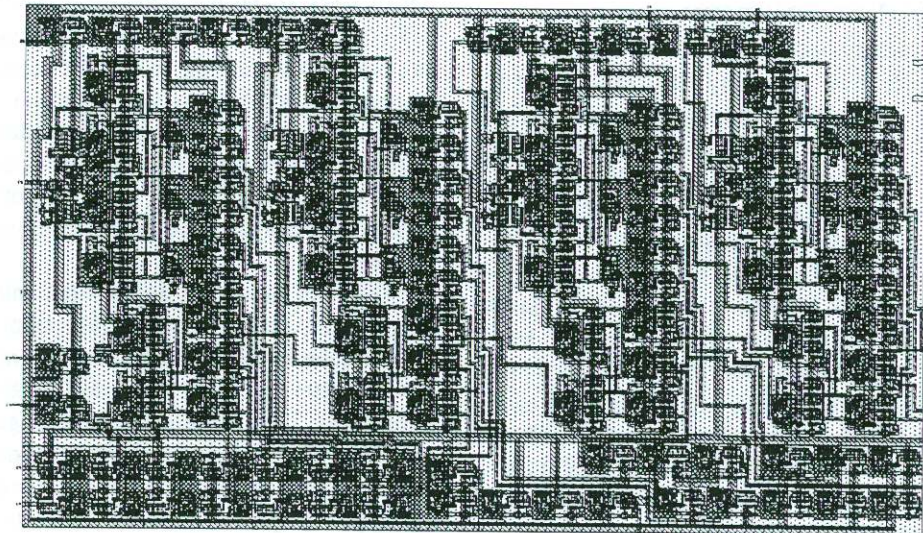


Figure 8: Layout of a 4-bit pipelined adder in MTDFL

References

- [1] P.S. Lassen, S. Long and K.R. Nary "Ultralow-Power GaAs MESFET MSI Circuits Using Two Phase Dynamic FET Logic" IEEE JOURNAL OF SOLID-STATE CIRCUITS VOL. 28, NO. 10 October 1993.
- [2] A. Guyot "Tradeoff in Arithmetic Operators" Gallium Arsenide VLSI 95 CIRCUITS and SYSTEMS, 10-12 May 1995 Maspalomas, Gran Canaria.
- [3] J. Jakobsen "Low-Power GaAs Multiplexer And Demultiplexer" IEEE GaAs94 European Gallium Arsenide Symposium Turin, April 1994 pp.199-203.
- [4] Riad Kanan and Bertrand Hochet and Michel Declercq, "Pseudo-Complementary FET Logic (PCFL) : A Low-Power Logic Family in GaAs" IEEE JOURNAL OF SOLID-STATE CIRCUITS, July 1996, Vol. 31.
- [5] Riad Kanan and Bertrand Hochet and F. Kaess and Michel Declercq, "A low power GaAs Flip Flop" '5th GaAs european symposium, Sept. 1997.