

# J-BAND 16 WATT HFET AMPLIFIER MODULE FOR VERY HIGH POWER APPLICATIONS

M. Calori, R. Graffitti, L. Marescialli, C. Proietti

Finmeccanica S.p.A. Alenia Settore Difesa Via Tiburtina Km. 12.400, 00131 Roma, Italy

Phone: +39-06-41973353 Fax: +39-06-41973701 E-mail: rapisarda@alenia.finmeccanica.it

## ABSTRACT

In this work we report on the design and construction of a three stage J-band (10÷10.5 GHz) high power amplifier based on 0.4  $\mu\text{m}$  gate-length HFET devices. In particular we will demonstrate that by means of a Micro Hybrid Integrated Circuits (MHIC) approach, power amplifier with  $P_{\text{out}}=16\text{ W}$ ,  $G_{\text{ass}}=19\text{ dB @ }1\text{dBc}$  and  $\eta=27\%$  can be routinely achieved.

## INTRODUCTION

The increasing demand of Microwave High Power Amplifiers with stringent dimension and weight specifications, requires continuous improvement in both active device performance and circuit design techniques in order to satisfy said requirements together with those of gain and power efficiency.

The availability of GaAs Heterostructure Field Effect Transistors (HFETs), superior to MESFETs in terms of gain and power added efficiency, is proving to be very interesting for the fabrication of compact high efficiency power amplifiers in a wide range of frequencies up to 25 GHz.

## ACTIVE DEVICE DESCRIPTION

The devices utilised in this work derive from Alenia's standard double-recess process for power HFET's (AL07EP), featuring an n-GaAs channel layer, on AlGaAs barrier layer and a 0.4  $\mu\text{m}$  gate-length Ti/Al "T-gate". In comparison with GaAs MESFET's, HFET's offer better performances in terms of device gain and bandwidth capability per output power [1], [2]. Figure 1 compares the associated gain vs. output r.f. power of a typical HFET with the one of a conventional implanted MESFET. Furthermore, over GaAs pseudomorphic HEMT's, HFET's offer improved linearity besides much easier epitaxial growth [2]; these advantages permit useful HFET's application in a wide class of products.

Alenia standard high power HFET uses an interdigital source-drain pattern, as shown in Figure 2; of course, fingers' length is a trade-off between operative frequency and active device transverse dimension. To ensure good thermal behaviour of the amplifier the GaAs substrate of the active devices are thinned down to approximately 50  $\mu\text{m}$  and subsequently attached to the metallic carrier by means of a Au:Sn eutectic alloy.

The active devices utilised in this work have variable gate widths in the range 4 to 12 mm.

## MICRO HYBRID INTEGRATED CIRCUIT TECHNOLOGY

In order to maintain reasonable impedance levels in restricted mechanic dimensions a Micro Hybrid technology was used. Said approach allows matching and feeding of very large gate peripheries by dividing the latter into an appropriate number of elementary cells. High dielectric constant substrates allowed to realise for every elementary cell either the lumped or distributed matching network elements in dimensions comparable to MMIC's size. A further advantage of this approach is that it allows to align and test single micro-hybrid elements as independent electrical functions. The

integration has been realised by means of different chip-carriers each one mounting the different amplifying stages and corresponding bias circuits. In order to obtain the high output power, standard combining techniques have been used on alumina substrates.

## POWER AMPLIFIER DESIGN, REALISATION AND PERFORMANCES

In order to achieve the specified 16 watt output power, preliminary design indicated the need of a 40 mm gate periphery for the output stage and as such the need to combine in parallel four 10 mm HFETs. Figure 3 is a photograph of the final stage of the amplifier illustrating the four HFETs in parallel combination with their respective input-output matching networks.

Detailed amplifier design was carried out with accurate equivalent circuit evaluation of 2 mm HFET elementary cell and source-pull/load-pull characterisation of 10 mm devices (fig. 4). The input and output matching networks utilised double step transformers in lumped and distributed form. As shown, by using elementary L-C lumped networks it is possible to feed said periphery and thus achieve 10% frequency bandwidth performance.

The second stage gate-width was chosen in such a way to properly drive the output stage, whilst the first stage design was optimised for the higher gain. Said stages included 4 mm and 12 mm HFET devices operating with 8V drain bias and 0.5A and 1.6A drain current respectively.

The output stage with 40 mm gate-width devices also operated with an 8V drain bias and a 5.3 A drain current.

In fig. 5 is presented the output power and  $G_{\text{ass}}$  performance of the three-stage amplifier operating in J-Band (10 ÷ 10.5 GHz). At central frequency 16 W output power corresponds to 19 dB of  $G_{\text{ass}}$  at 1 dB @ and, as shown in fig. 6, to a Power Added Efficiency (PAE) of 27%.

## CONCLUSIONS

We have designed and realised a three-stage micro hybrid amplifier operating in 10 ÷ 10.5 GHz bandwidth and performing 16 W  $P_{\text{OUT}}$  with 19 dB associated gain at 1 dB @ with 27% of PAE. It is expected that after the optimisation phase of said amplifier, activity currently in progress at both device (geometrical lay-out) and design (circuit and bias topology) levels, power added efficiencies of better than 30% can be achieved.

## REFERENCES

- [1] C. Lanzieri, M. Peroni, A. Cetronio, L. Costa, G. Meneghesso, C. Canali: "Performance and reliability of GaAs based power HFETs", GAAS 97 Proceedings of 5<sup>th</sup> European Gallium Arsenide and related III-V compounds Applications Symposium, pp.109-112, September 1997.
- [2] R. Menozzi, C. Lanzieri, D. Dieci, M. Peroni, A. Cetronio, C. Canali: "AlGaAs/GaAs HFET Power Devices for J-Band Applications: Performance Dependence on Gate/Recess Geometry", GAAS 98 Proceedings to be published.

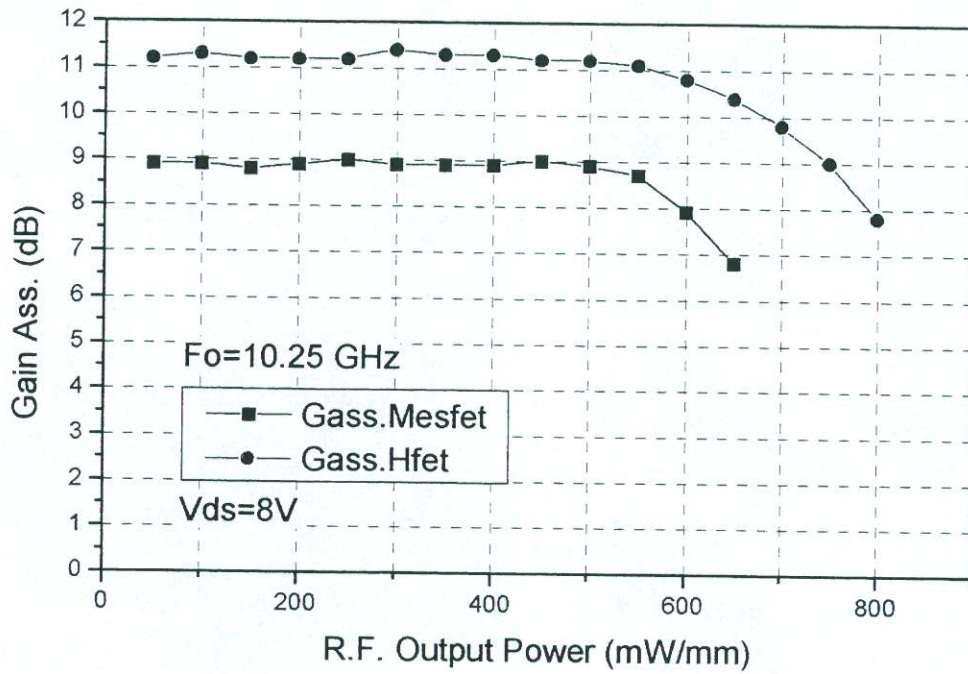


Fig. 1 - Alenia HFET Gain vs. Output Power (red) in comparison with Alenia MESFET (black)

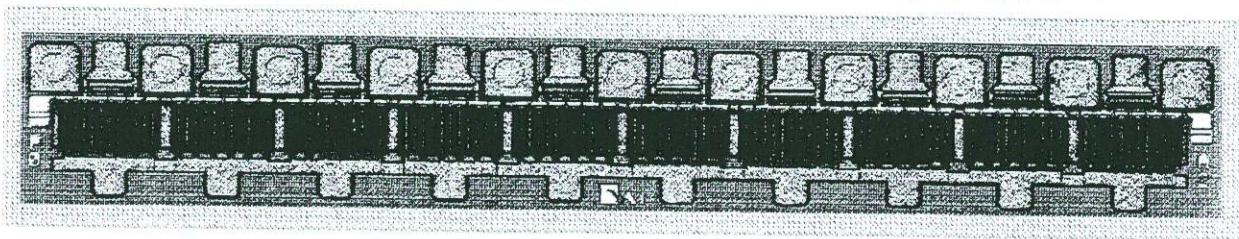


Fig. 2 - Alenia standard high power 10 mm gate width HFET photograph.

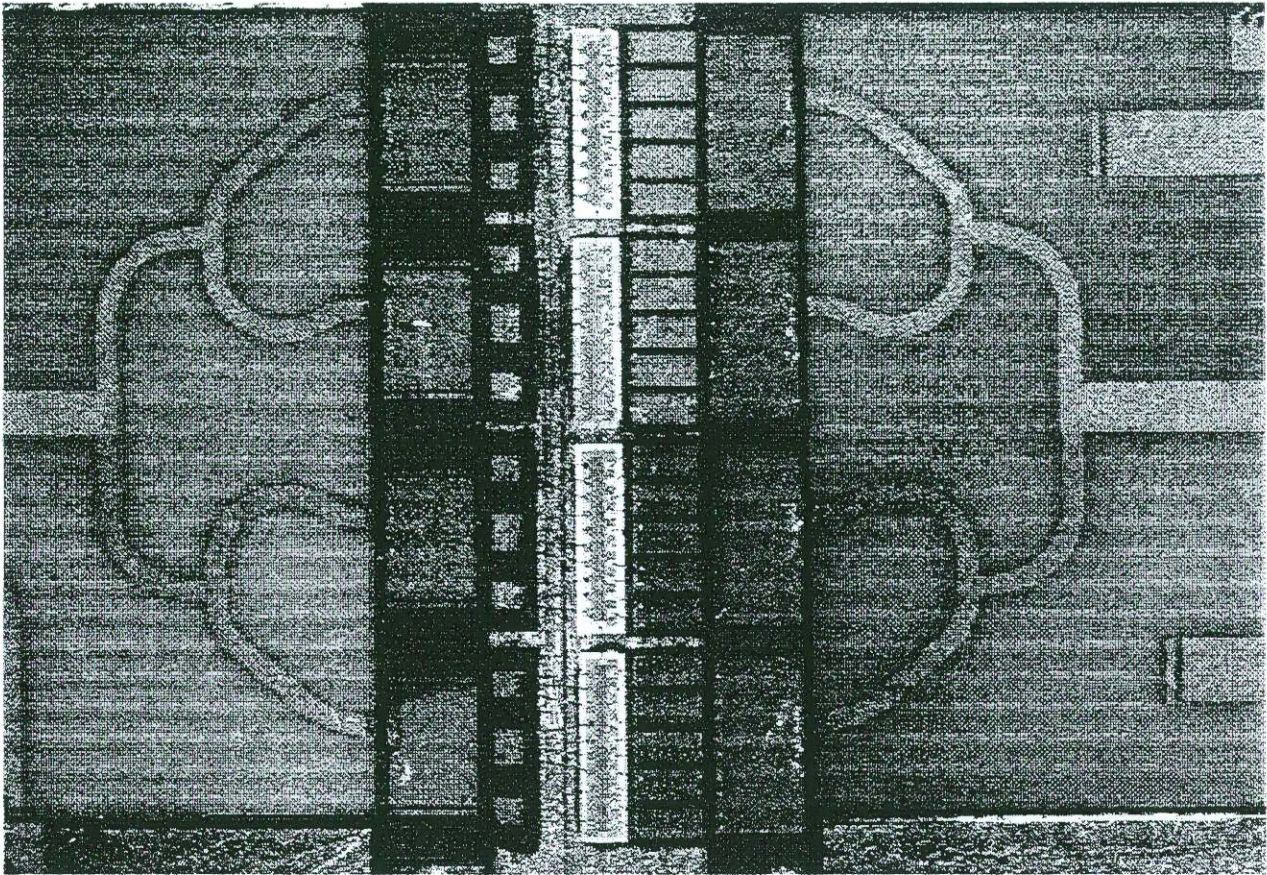


Fig. 3 - Amplifier output stage photograph.

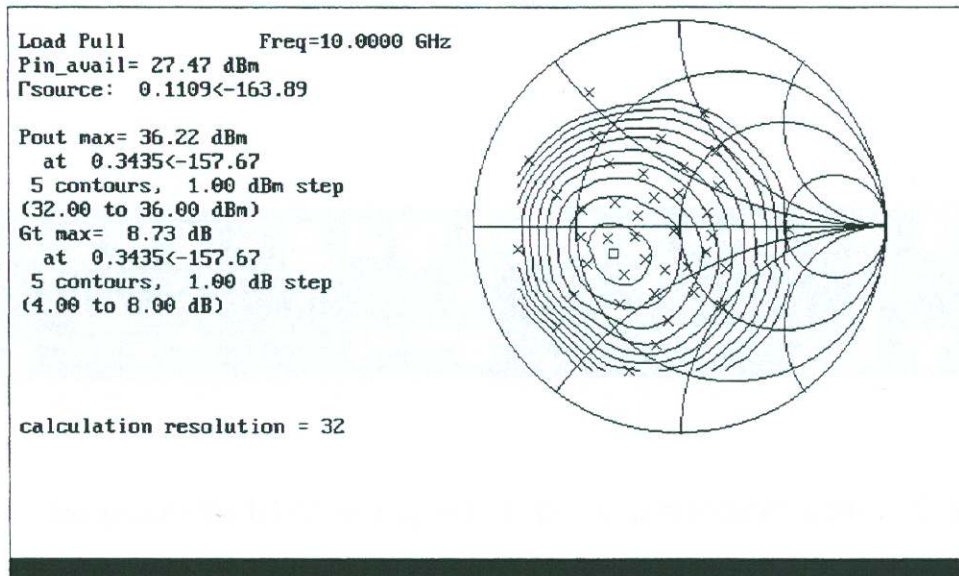


Fig. 4 - Load/pull characterisation of 10 mm Alenia HFET device.

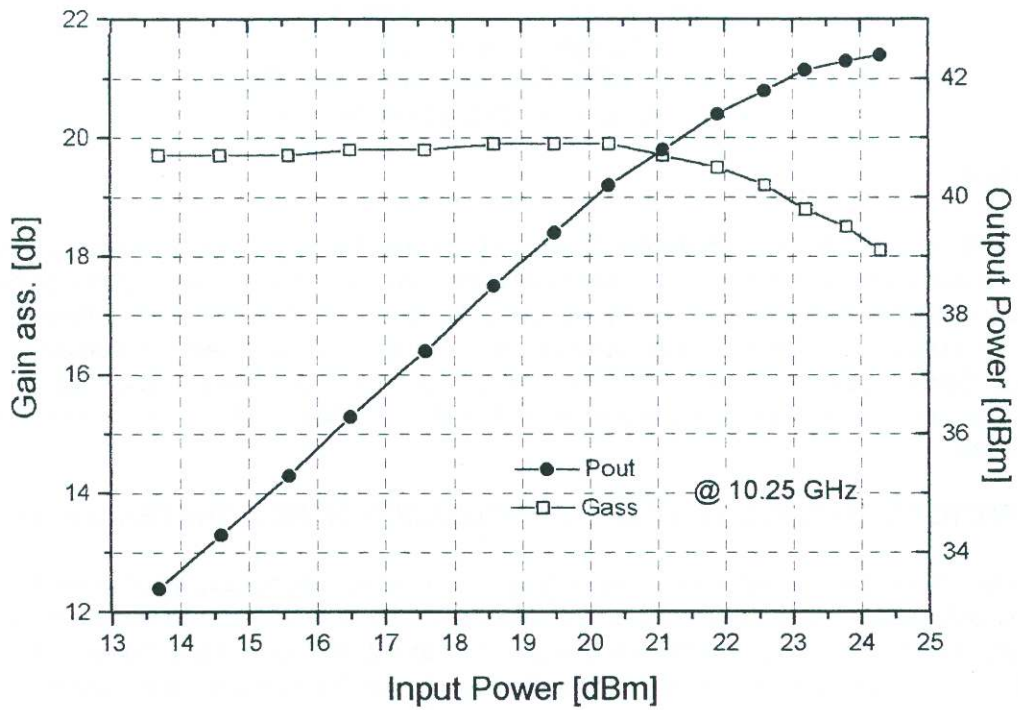


Fig. 5 - Output Power performance of three-stage amplifier.

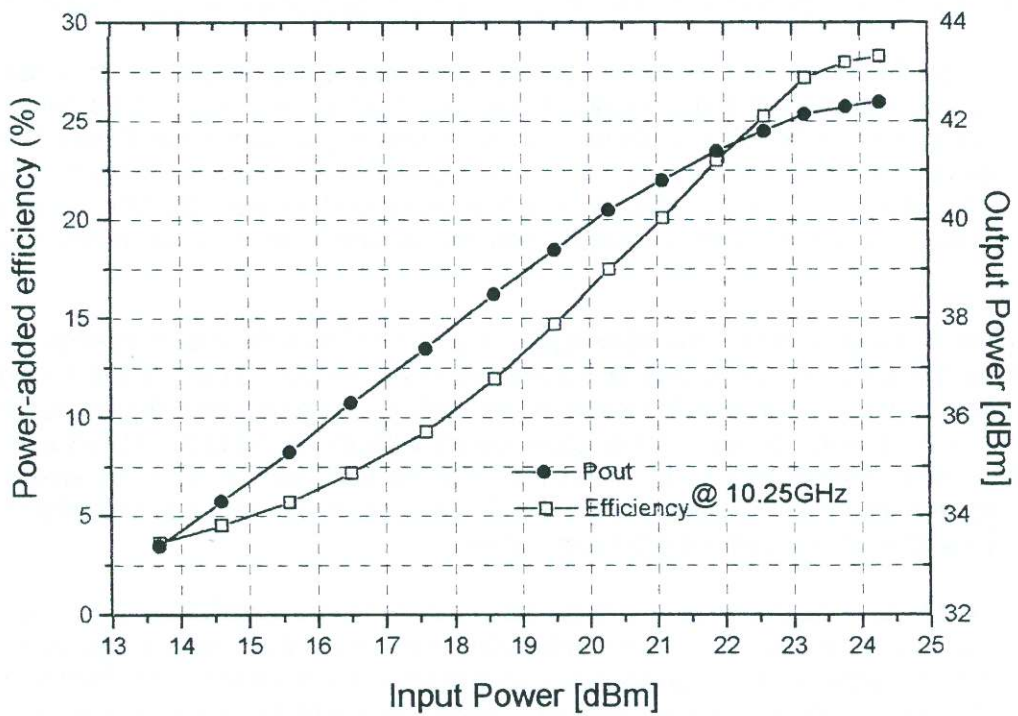


Fig. 6 - Power Added Efficiency performance of three-stage amplifier.